



# ***Reliability Report***

<b>Report Title:</b>	<b>GaAs PHEMT-J Process Cumulative Reliability</b>
<b>Report Number:</b>	<b>2013-00285</b>
<b>Revision:</b>	<b>10</b>
<b>Date:</b>	<b>11 March 2024</b>

## Summary

This report summarizes the process HTOL testing of the GaAs PHEMT-J process.

**Table 1: Process Characteristics**

### Fabrication Details

Wafer Fabrication Process	GaAs PHEMT-J
Passivation Layer	SiN
Bond Pad Metal Composition	Au

## Description / Results of Tests Performed

The following tables provide a description of the qualification tests conducted and the associated test results for products manufactured on the same technologies as described in Table 1. All devices were electrically tested before and after each stress. Any device that did not meet all electrical data sheet limits following stressing would be considered a valid (stress-attributable) failure unless there was conclusive evidence to indicate otherwise.

**Table 2: Process Qualification Test Results**

Test Name	Specification	Conditions	Device	Lot #	Sample Size	Qty. Failures
High Temperature Operating Life (HTOL)	JESD22-A108	T <sub>j-stress</sub> =125°C, Biased, 1,000 Hrs	HMC6488A	QTR2012-00017	80	0
			HMC6484	QTR2012-00042	80	0
			HMC1190A	Q11869	49	0
		T <sub>j-stress</sub> =150°C, Biased, 1,000 Hrs	HMC284A	QTR2012-00461	160	0
			HMC349A	QTR2014-00445	80	0
			HMC1190A	Q13411	148	0
			ADCA5191	Q18440	98	0
			ADCA5190	18440.1.2	82	0
		T <sub>j-stress</sub> =150°C, Biased, 168 Hrs	ADCS3280	18371.2.2	32	0
			HMC472A	QTR2013-00524	1134	0

Samples of the many devices manufactured with these package and process technologies are continuously undergoing reliability evaluation as part of the ADI Reliability Monitor Program. Additional qualification data is available on [Analog Devices' web site](#).

## **Approvals**

Reliability Engineer: Tom Wood

## **Additional Information**

Data sheets and other additional information are available on [Analog Devices' web site](#)

## Appendix

### GaAs PHEMT-J Failure Rate Estimate

The failure rate estimation was determined using the process HTOL test results and the parameters shown below:

- Die Use Junction Temperature,  $T_{j-use} = 85^{\circ}\text{C}$
- GaAs PHEMT-J Activation Energy = 1.46 eV

- Acceleration Factor (AF): 
$$AF = \exp\left[\left(\frac{E_A}{k}\right) \cdot \left(\left(\frac{1}{T_{USE}}\right) - \left(\frac{1}{T_{STRESS}}\right)\right)\right]$$

- Equivalent hours = Device hours x Acceleration Factor

Device	Qual Number	Equivalent Device Hours
HMC6488A	QTR2012-00017	9.4x10 <sup>6</sup> hours
HMC6484	QTR2012-00042	9.4x10 <sup>6</sup> hours
HMC1190A	Q11869	5.75x10 <sup>6</sup> hours
HMC284A	QTR2012-00461	2.34x10 <sup>8</sup> hours
HMC349A	QTR2014-00445	1.17x10 <sup>8</sup> hours
HMC1190A	Q13411	8.18x10 <sup>7</sup> hours
ADCA5191	Q18440	1.43x10 <sup>8</sup> hours
ADCA5190	18440.1.2	1.20x10 <sup>8</sup> hours
HMC472A	QTR2013-00524	2.78x10 <sup>8</sup> hours
ADCA3280	18371.2.2	4.09x10 <sup>8</sup> hours
Total Equivalent Device Hours =		1.41x10 <sup>9</sup> hours

The failure rate was calculated using Chi Square Statistic:

$$\lambda_{CL} = \frac{\chi^2_{\%CL, 2f+2} \cdot 10^9}{2 \cdot t \cdot SS \cdot AF}$$

at 60% and 90% Confidence Level (CL), with 0 units out of spec

and an 85°C die junction temperature;

#### Failure Rate

$$\lambda_{60} = [(\chi^2)_{60,2}] / (2 \times 1.41 \times 10^9) = 4.1 / 2.81 \times 10^9 = 6.50 \times 10^{-10} \text{ failures/hour or } 0.7 \text{ FIT or MTTF} = 1.54 \times 10^9 \text{ Hours}$$

$$\lambda_{90} = [(\chi^2)_{90,2}] / (2 \times 1.41 \times 10^9) = 7.8 / 2.81 \times 10^9 = 1.64 \times 10^{-9} \text{ failures/hour or } 21.6 \text{ FIT or MTTF} = 6.11 \times 10^8 \text{ Hours}$$