

Product Specification

NHD-2.23-12832UCY3

Graphic OLED Display Module

NHD-	Newhaven Display
2.23-	2.23" Diagonal Size
12832-	128 x 32 Pixel Resolution
UC-	Model
Y-	Emmitting Color: Yellow
3-	3V Power Supply

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Additional Resources

- **Support Forum:** <https://support.newhavendisplay.com/hc/en-us/community/topics>
- **GitHub:** <https://github.com/newhavendisplay>
- **Example Code:** <https://support.newhavendisplay.com/hc/en-us/categories/4409527834135-Example-Code/>
- **Knowledge Center:** https://www.newhavendisplay.com/knowledge_center.html
- **Quality Center:** https://www.newhavendisplay.com/quality_center.html
- **Precautions for using LCDs/LCMs:** <https://www.newhavendisplay.com/specs/precautions.pdf>
- **Warranty / Terms & Conditions:** <https://www.newhavendisplay.com/terms.html>

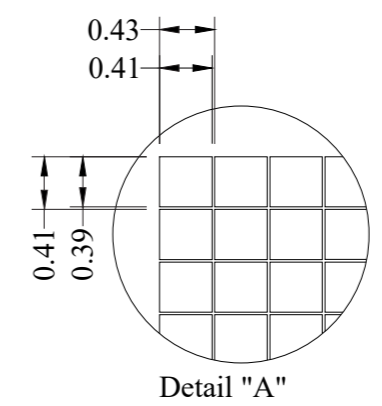
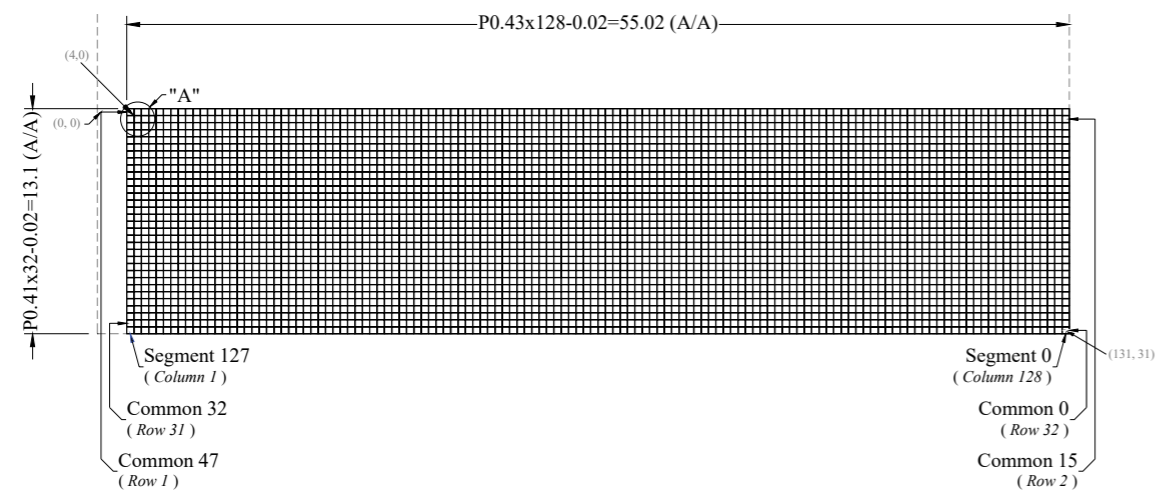
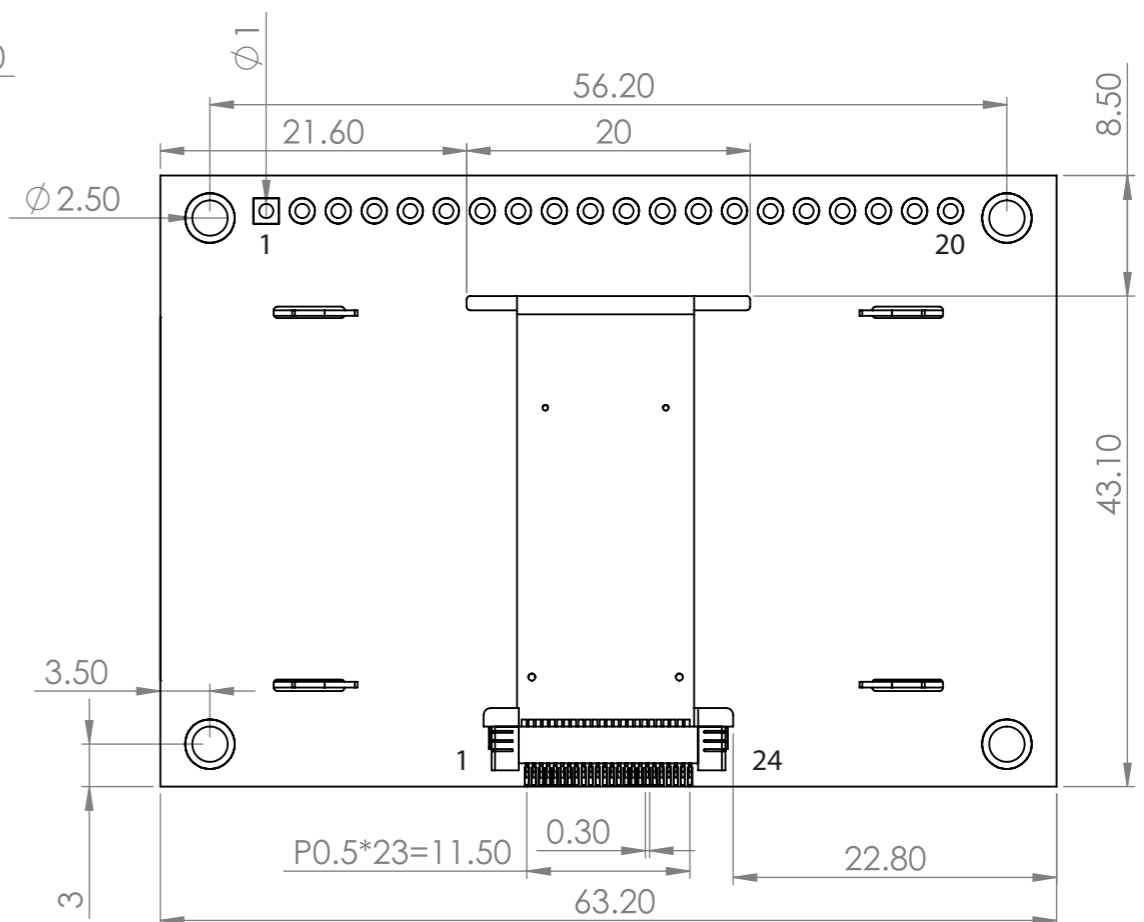
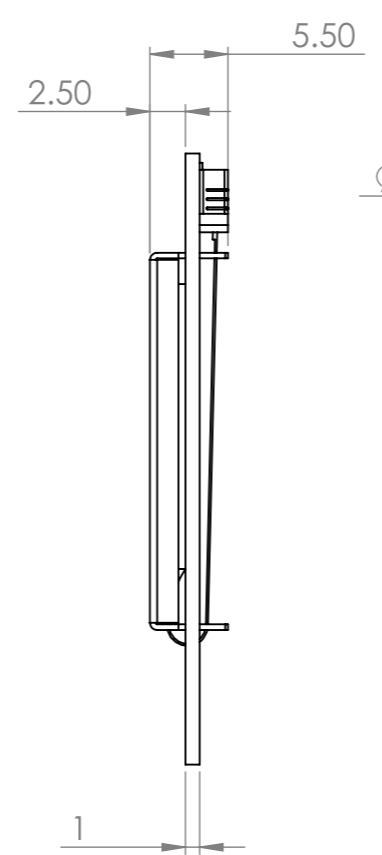
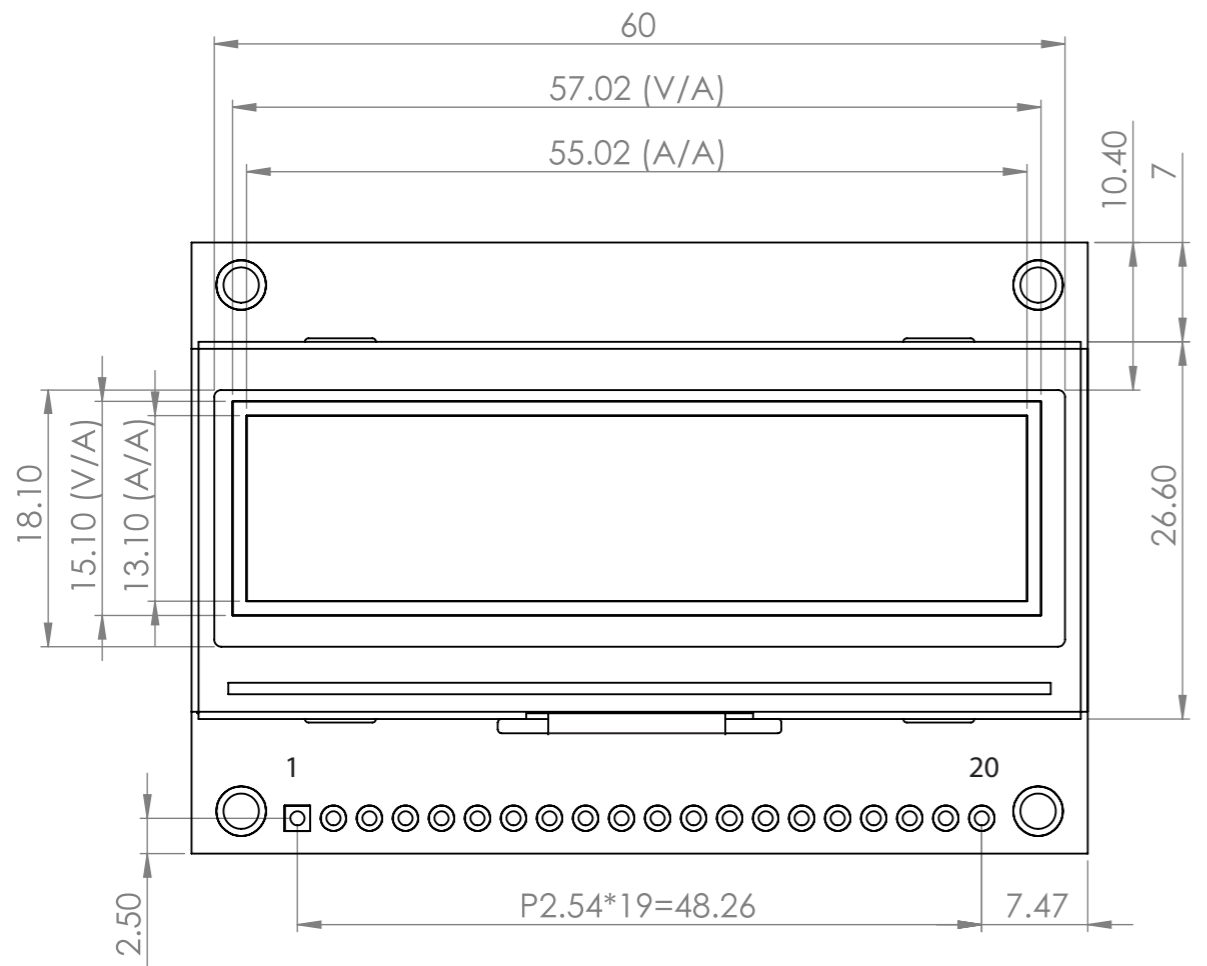
Document Revision History

Revision	Date	Description	Changed By
0	05/01/2011	Initial Product Release	-
1	02/22/2013	Electrical characteristics and mechanical drawing updated	JN
2	08/03/2020	Included MIN Supply Voltage & Reformatted 2D Mechanical Drawing	AS
3	09/01/2020	Updated 2D Mechanical Drawing	AS
4	02/23/2024	Contrast Ratio Updated	KL

Mechanical Drawing

Newhaven Display
NHD-2.23-12832UCY3
Date Code

Part Label (type/format may vary)



Product Description: 2.23" 128x32 Graphic OLED

1. Driver IC: SSD1305
2. Interface: 8-bit 6800/8080 Parallel, 3/4-wire SPI, I²C
3. Power Requirement: 3.3V OLED
4. Optical Features: Yellow Color, Anti-Glare, Full View
5. Recommended Pin Header: 1x20pin 2.54mm pitch

Standard Tolerance: (Unless otherwise specified) Linear: $\pm 0.3\text{mm}$		
	Drawing/Part Number: NHD-2.23-12832UCY3	Revision: -
Unless otherwise specified: • Dimensions are in Millimeters • Third Angle Projection	Drawn By: K. Lewis	Approved By: K. Lewis
	Drawn Date: 02/23/2024	Approved Date: 02/23/2024
This drawing is solely the property of Newhaven Display International, Inc. The information it contains is not to be disclosed, reproduced or copied in whole or part without written approval from Newhaven Display.		

Pin Description

Parallel Interface:

Pin No.	Symbol	External Connection	Function Description
1	VSS	Power Supply	Ground
2	VDD	Power Supply	Supply Voltage for OLED and logic.
3	NC	-	No Connect
4	D/C	MPU	Register select signal. D/C=0: Command, D/C=1: Data
5	R/W or /WR	MPU	6800-interface: Read/Write select signal, R/W=1: Read R/W: =0: Write 8080-interface: Active LOW Write signal.
6	E or /RD	MPU	6800-interface: Operation enable signal. Falling edge triggered. 8080-interface: Active LOW Read signal.
7-14	DB0 – DB7	MPU	8-bit Bi-directional data bus lines.
15	NC	-	No Connect
16	/RES	MPU	Active LOW Reset signal.
17	/CS	MPU	Active LOW Chip Select signal.
18	NC	-	No Connect
19	BS2	MPU	MPU Interface Select signal.
20	BS1	MPU	MPU Interface Select signal.

Serial Interface:

Pin No.	Symbol	External Connection	Function Description
1	VSS	Power Supply	Ground
2	VDD	Power Supply	Supply Voltage for OLED and logic.
3	NC	-	No Connect
4	D/C	MPU	Register select signal. D/C=0: Command, D/C=1: Data
5-6	VSS	Power Supply	Ground
7	SCLK	MPU	Serial Clock signal.
8	SDIN	MPU	Serial Data Input signal.
9	NC	-	No Connect
10-14	VSS	Power Supply	Ground
15	NC	-	No Connect
16	/RES	MPU	Active LOW Reset signal.
17	/CS	MPU	Active LOW Chip Select signal.
18	NC	-	No Connect
19	BS2	MPU	MPU Interface Select signal.
20	BS1	MPU	MPU Interface Select signal.

I2C Interface:

Pin No.	Symbol	External Connection	Function Description
1	VSS	Power Supply	Ground
2	VDD	Power Supply	Supply Voltage for OLED and logic.
3	NC	-	No Connect
4	SA0	MPU	Slave Address Selection signal.
5-6	VSS	Power Supply	Ground
7	SCL	MPU	Serial Clock signal.
8	SDA _{IN}	MPU	Serial Data input signal (pins 8 and 9 can be tied together).
9	SDA _{OUT}	MPU	Serial Data output signal (pin9 can be no connect).
10-14	VSS	Power Supply	Ground
15	NC	-	No Connect
16	/RES	MPU	Active LOW Reset signal.
17	VSS	Power Supply	Ground
18	NC	-	No Connect
19	BS2	MPU	MPU Interface Select signal.
20	BS1	MPU	MPU Interface Select signal.

Interface Selection

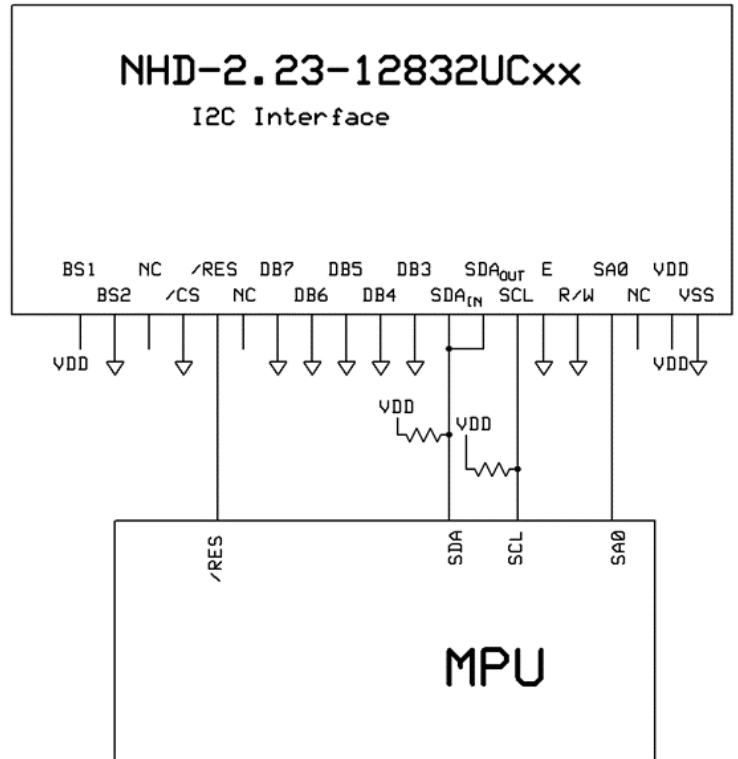
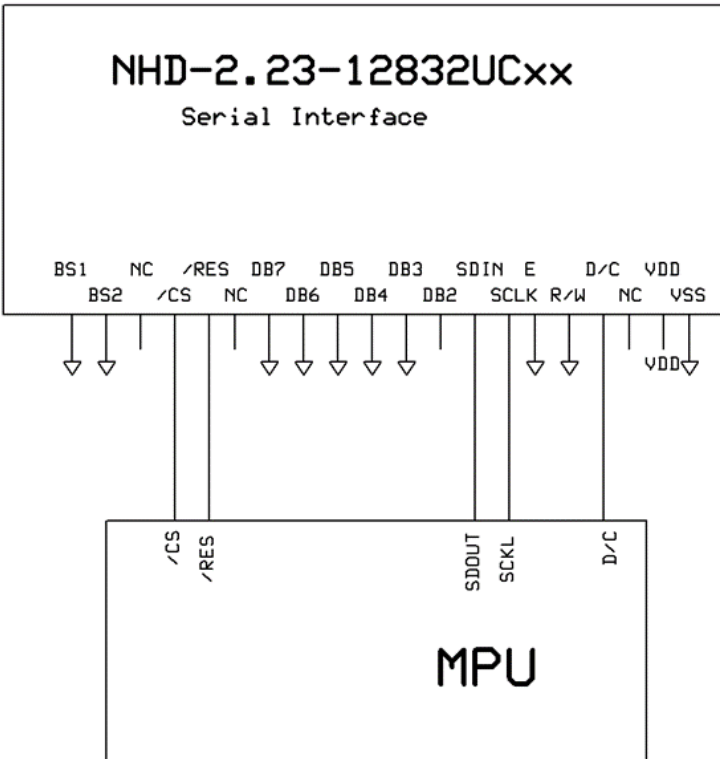
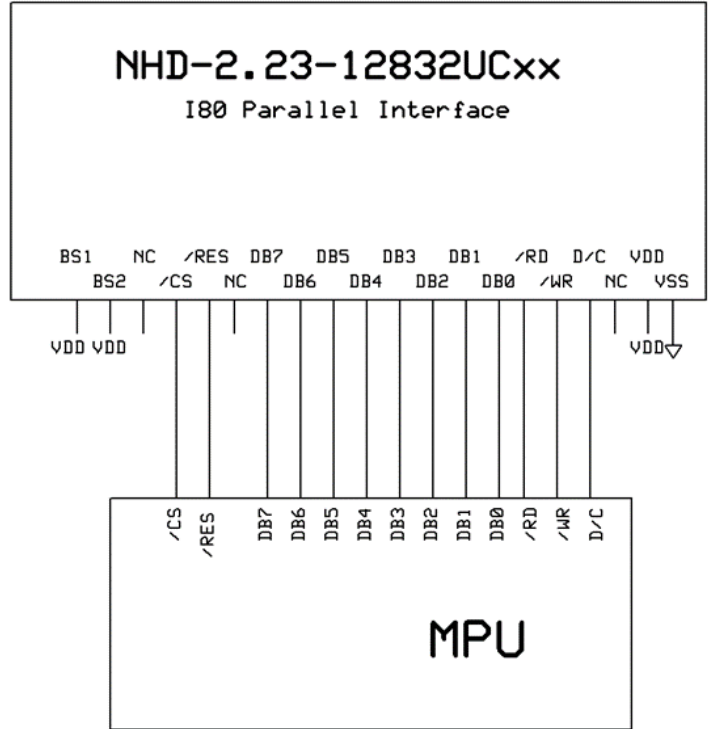
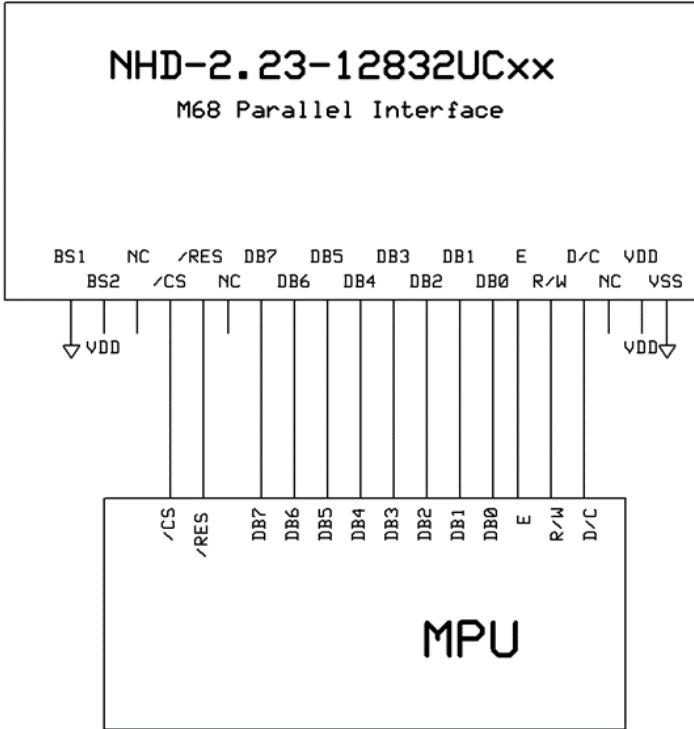
MPU Interface Pin Selections

Pin Name	6800 Parallel 8-bit interface	8080 Parallel 8-bit interface	Serial Interface	I2C Interface
BS2	1	1	0	0
BS1	0	1	0	1

MPU Interface Pin Assignment Summary

Bus Interface	Data/Command Interface								Control Signals				
	D7	D6	D5	D4	D3	D2	D1	D0	E	R/W	/CS	D/C	/RES
8-bit 6800	D[7:0]								E	R/W	/CS	D/C	/RES
8-bit 8080	D[7:0]								/RD	/WR	/CS	D/C	/RES
SPI	Tie LOW				NC	SDIN	SCLK	Tie LOW		/CS	D/C	/RES	
I2C	Tie LOW				SDA _{IN}	SDA _{OUT}	SCL	Tie LOW			SA0	/RES	

Wiring Diagrams



Electrical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating Temperature Range	Top	Absolute Max	-40	-	+85	°C
Storage Temperature Range	Tst	Absolute Max	-40	-	+90	°C
Supply Voltage	VDD		3.0	3.3	3.5	V
Supply Current (logic)	IDD	Ta=25°C, VDD=3.3V	-	180	300	µA
Supply Current (display)	ICC	50% ON, VDD=3.3V	-	60	70	mA
		100% ON, VDD=3.3V	-	108	120	mA
Sleep Mode Current	IDD+ICCSLEEP		-	3	15	µA
"H" Level input	Vih		0.8*VDD	-	VDD	V
"L" Level input	Vil		VSS	-	0.2*VDD	V
"H" Level output	Voh		0.9*VDD	-	VDD	V
"L" Level output	Vol		VSS	-	0.1*VDD	V

Optical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Viewing Angle – Top	AV		-	80	-	°
Viewing Angle – Bottom	AV		-	80	-	°
Viewing Angle – Left	AH		-	80	-	°
Viewing Angle – Right	AH		-	80	-	°
Contrast Ratio	Cr		10,000:1	-	-	-
Response Time (rise)	Tr	-	-	10	-	µs
Response Time (fall)	Tf	-	-	10	-	µs
Brightness		50% checkerboard	100	120	-	cd/m ²
Lifetime		Ta=25°C, 50% checkerboard	40,000	-	-	Hrs

Note: Lifetime at typical temperature is based on accelerated high-temperature operation. Lifetime is tested at average 50% pixels on and is rated as Hours until **Half-Brightness**. The Display OFF command can be used to extend the lifetime of the display.

Luminance of active pixels will degrade faster than inactive pixels. Residual (burn-in) images may occur. To avoid this, every pixel should be illuminated uniformly.

Controller Information

Built-in SSD1305 Controller: <https://support.newhavendisplay.com/hc/en-us/articles/4414488972695--SSD1305>

Table of Commands

Instruction	Code										Description	RESET value
	D/C	HEX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Set Lower Column Start Address	0	00~0F	0	0	0	0	X3	X2	X1	X0	Set the lower nibble of the column start address register for Page Addressing Mode.	0
Set Higher Column Start Address	0	10~1F	0	0	0	1	X3	X2	X1	X0	Set the higher nibble of the column start address register for Page Addressing Mode.	0
Set Memory Addressing Mode	0	20 A[1:0]	0 *	0 *	1 *	0 *	0 *	0 *	0 A1	0 A0	A[1:0] = 00b, Horizontal Addressing Mode A[1:0] = 01b, Vertical Addressing Mode A[1:0] = 10b, Page Addressing Mode A[1:0] = 11b, Invalid	10b
Set Column Address	0	21 A[7:0] B[7:0]	0 A7 B7	0 A6 B6	1 A5 B5	0 A4 B4	0 A3 B3	0 A2 B2	0 A1 B1	1 A0 B0	Setup column start and end address A[7:0]: Column start address. Range: 0-131d B[7:0]: Column end address. Range: 0-131d	0 131d
Set Page Address	0	22 A[2:0] B[2:0]	0 * *	0 * *	1 * *	0 * *	0 * *	0 A2 B2	1 A1 B1	0 A0 B0	Setup page start and end address A[2:0]: Page start address. Range: 0-7d B[2:0]: Page end address. Range: 0-7d	0 7d
Set Display Start Line	0	40~7F	0	1	X5	X4	X3	X2	X1	X0	Set display RAM display start line register from 0-63d.	0
Set Contrast Control	0	81 A[7:0]	1 A7	0 A6	0 A5	0 A4	0 A3	0 A2	0 A1	1 A0	Double byte command to select 1 out of 256 contrast steps. Contrast increases as the value increases.	0x80
Set Brightness	0	82 A[7:0]	1 A7	0 A6	0 A5	0 A4	0 A3	0 A2	1 A1	0 A0	Double byte command to select 1 out of 256 brightness steps. Brightness increases as the value increases.	0x80
Set Look-Up Table	0	91 X[5:0] A[5:0] B[5:0] C[5:0]	1 * * * *	0 * * * *	0 X5 A5 B5 C5	1 X4 A4 B4 C4	0 X3 A3 B3 C3	0 X2 A2 B2 C2	0 X1 A1 B1 C1	1 X0 A0 B0 C0	Set current drive pulse width of Bank 0, Color A, B and C. Bank 0: X[5:0] = 31 to 63. Pulse width set to 32 to 64 clocks. Color A: X[5:0] = 31 to 63. Pulse width set to 32 to 64 clocks. Color B: X[5:0] = 31 to 63. Pulse width set to 32 to 64 clocks. Color C: X[5:0] = 31 to 63. Pulse width set to 32 to 64 clocks. Note: Color D pulse width is fixed at 64 clocks.	0x31 0x3F 0x3F 0x3F
Set Bank Color of Bank1 to Bank16 (Page 0)	0	92 A[7:0] B[7:0] C[7:0] D[7:0]	1 A7 B7 C7 D7	0 A6 B6 C6 D6	0 A5 B5 C5 D5	1 A4 B4 C4 D4	0 A3 B3 C3 D3	0 A2 B2 C2 D2	1 A1 B1 C1 D1	0 A0 B0 C0 D0	Sets the bank color of Bank1~Bank16 to any one of the 4 colors A,B,C, and D. A[1:0] : 00b, 01b, 10b, or 11b for Color = A, B, C, or D of BANK1. A[3:2] : 00b, 01b, 10b, or 11b for Color = A, B, C, or D of BANK2. . . . D[5:4] : 00b, 01b, 10b, or 11b for Color = A, B, C, or D of BANK15. D[7:6] : 00b, 01b, 10b, or 11b for Color = A, B, C, or D of BANK16.	
Set Bank Color of Bank17 to Bank32 (Page 1)	0	93 A[7:0] B[7:0]	1 A7 B7	0 A6 B6	0 A5 B5	1 A4 B4	0 A3 B3	0 A2 B2	1 A1 B1	1 A0 B0	Sets the bank color of Bank17~Bank32 to any one of the 4 colors A,B,C, and D. A[1:0] : 00b, 01b, 10b, or 11b for Color = A, B, C, or D of BANK17.	

		C[7:0] D[7:0]	C7 D7	C6 D6	C5 D5	C4 D4	C3 D3	C2 D2	C1 D1	C0 D0	A[3:2] : 00b, 01b, 10b, or 11b for Color = A, B, C, or D of BANK18. . . . D[5:4] : 00b, 01b, 10b, or 11b for Color = A, B, C, or D of BANK31. D[7:6] : 00b, 01b, 10b, or 11b for Color = A, B, C, or D of BANK32.	
Set Segment Remap	0	A0/A1	1	0	1	0	0	0	0	X0	X[0] = 0; Column address 0 is mapped to SEG0 X[0] = 1; Column address 131 is mapped to SEG0	0
Entire Display ON	0	A4/A5	1	0	1	0	0	1	0	X0	X[0] = 0; Resume RAM content display. Output follows RAM content. X[0] = 1; Entire display ON. Output ignores RAM content.	0
Set Normal/ Inverse Display	0	A6/A7	1	0	1	0	0	1	1	X0	X[0] = 0; Normal display. X[0] = 1; Inverse display.	0
Set Multiplex Ratio	0	A8 A[5:0]	1 *	0 *	1 A5	0 A4	1 A3	0 A2	0 A1	0 A0	Set MUX ratio to N+1 MUX N=A[5:0]; from 16MUX to 64MUX (0 to 14 are invalid)	64
Dim mode setting	0	AB A[3:0] B[7:0] C[7:0]	1 * B7 C7	0 * B6 C6	1 * B5 C5	0 * B4 C4	1 A3 B3 C3	0 A2 B2 C2	1 A1 B1 C1	1 A0 B0 C0	A[3:0] = reserved. Set as 0000b B[7:0] = Set contrast for BANK0. Range 0-255d. Refer to command 81h. C[7:0] = Set brightness for color bank. Range 0-255d. Refer to command 82h.	
Master configuration	0	AD AE	1 1	0 0	1 0	0 0	1 1	1 1	0 1	1 0	Selects external VCC supply	AEh
Set Display ON/ OFF	0	AC/ AE/ AF	1	0	1	0	1	1	A1	A0	ACh = Display ON in dim mode AEh = Display OFF (sleep mode) AFh = Display ON in normal mode	AEh
Set Page Start Address	0	B0~B7	1	0	1	1	0	X2	X1	X0	Set GDRAM Page Start Address for Page Addressing Mode using X[2:0]. PAGE0~PAGE7	
Set COM Output Scan Direction	0	C0/C8	1	1	0	0	X3	0	0	0	X[3] = 0; Normal mode. Scan from COM0 to COM[N-1] X[3] = 1; Remapped mode. Scan from COM[N-1] to COM0	0
Set Display Offset	0	D3 A[5:0]	1 *	1 *	0 A5	1 A4	0 A3	0 A2	1 A1	1 A0	Set vertical shift by COM from 0~63.	0
Set Display Clock Divide Ratio / Oscillator Frequency	0	D5 A[7:0]	1 A7	1 A6	0 A5	1 A4	0 A3	1 A2	0 A1	1 A0	A[3:0] = Define the divide ratio of the display clocks. Divide ratio = A[3:0] +1 A[7:4] = Set the Oscillator Frequency. Frequency increases with the value of A[7:4]. Range 0000b~1111b.	0000b 0111b
Set Area Color Mode ON/OFF & Low Power Display Mode	0	D8 X[5:0]	1 0	1 0	0 X5	1 X4	1 0	0 X2	0 0	0 X0	X[5:4] = 00b; Monochrome mode X[5:4] = 11b; Area Color mode X[2] = 0 and X[0] = 0; Normal power mode X[2] = 1 and X[0] = 1; Set low power display mode	00 00
Set Pre-charge Period	0	D9 A[7:0]	1 A7	1 A6	0 A5	1 A4	1 A3	0 A2	0 A1	1 A0	A[3:0] = Phase 1 period of up to 15 DCLK clocks. 0 is invalid. A[7:4] = Phase 2 period of up to 15 DCLK clocks. 0 is invalid.	2h 2h

Set COM pins Hardware configuration	0	DA X[5:4]	1 0	1 0	0 X5	1 X4	1 0	0 0	1 1	0 0	X[4] = 0; Sequential COM pin configuration X[4] = 1; Alternative COM pin configuration X[5] = 0; Disable COM Left/Right remap X[5] = 1; Enable COM Left/Right remap	1 1
Set VCOMH Deselect Level	0	DB A[5:2]	1 0	1 0	0 A5	1 A4	1 A3	0 A2	1 0	1 0	A[5:2] = 0000b; VCOMH = ~0.43*VCC A[5:2] = 1101b; VCOMH = ~0.77*VCC A[5:2] = 1111b; VCOMH = ~0.83*VCC	1101
Enter Read Modify Write mode	0	E0	1	1	1	0	0	0	0	0	Enter the Read/Modify/Write mode.	
NOP	0	E3	1	1	1	0	0	0	1	1	Command for No Operation	
Exit Read Modify Write mode	0	EE	1	1	1	0	1	1	1	0	Exit the Read/Modify/Write mode.	

For detailed instruction information, see datasheet: http://www.newhavendisplay.com/app_notes/SSD1305.pdf

MPU Interface

For detailed timing information, see datasheet: http://www.newhavendisplay.com/app_notes/SSD1305.pdf

6800-MPU Parallel Interface

The parallel interface consists of 8 bi-directional data pins, R/W, D/C, E, and /CS.

A LOW on R/W indicates write operation, and HIGH on R/W indicates read operation.

A LOW on D/C indicates “Command” read or write, and HIGH on D/C indicates “Data” read or write.

The E input serves as data latch signal, while /CS is LOW. Data is latched at the falling edge of E signal.

Function	E	R/W	/CS	D/C
Write Command	↓	0	0	0
Read Status	↓	1	0	0
Write Data	↓	0	0	1
Read Data	↓	1	0	1

8080-MPU Parallel Interface

The parallel interface consists of 8 bi-directional data pins, /RD, /WR, D/C, and /CS.

A LOW on D/C indicates “Command” read or write, and HIGH on D/C indicates “Data” read or write.

A rising edge of /RS input serves as a data read latch signal while /CS is LOW.

A rising edge of /WR input serves as a data/command write latch signal while /CS is LOW.

Function	/RD	/WR	/CS	D/C
Write Command	1	↑	0	0
Read Status	↑	1	0	0
Write Data	1	↑	0	1
Read Data	↑	1	0	1

Alternatively, /RD and /WR can be kept stable while /CS serves as the data/command latch signal.

Function	/RD	/WR	/CS	D/C
Write Command	1	0	↑	0
Read Status	0	1	↑	0
Write Data	1	0	↑	1
Read Data	0	1	↑	1

Serial Interface

The serial interface consists of serial clock SCLK, serial data SDIN, D/C, and /CS.

D0 acts as SCLK and D1 acts as SDIN. D2 should be left open. D3~D7, E, and R/W should be connected to GND.

Function	/RD	/WR	/CS	D/C	D0
Write Command	0	0	0	0	↑
Write Data	0	0	0	1	↑

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6,...D0.

D/C is sampled on every eighth clock and the data byte in the shift register is written to the GDRAM or command register in the same clock.

Note: Read is not available in serial mode.

I²C Interface

The I2C interface consists of a slave address bit SA0, I2C-bus data signal SDA, and I2C-bus clock signal SCL. D1 and D2 can be tied together, and act as SDA. D0 acts as SCL. Both the data and clock signals must be connected to pull-up resistors. /RES is used to initialize the device.

Note: SA0 bit allows the device to have a slave address of either “0111100” or “0111101”.

Note: Data and acknowledgement are sent through the SDA. The ITO track resistance and the pull-up resistance at SDA becomes a voltage potential divider. As a result, it may not be possible to attain a valid logic “0” level on SDA for the ACK signal. SDA_{IN} must be connected, but SDA_{OUT} may be disconnected and the ACK signal will be ignored on the I2C bus.

For detailed protocol information, see datasheet: http://www.newhavendisplay.com/app_notes/SSD1305.pdf

Example Initialization Sequence:

```
Set_Display_On_Off(0x00); // Display Off (0x00/0x01)
Set_Display_Clock(0x10); // Set Clock as 160 Frames/Sec
Set_Multiplex_Ratio(0x1F); // 1/32 Duty (0x0F~0x3F)
Set_Display_Offset(0x00); // Shift Mapping RAM Counter (0x00~0x3F)
Set_Start_Line(0x00); // Set Mapping RAM Display Start Line (0x00~0x3F)
Set_Master_Config(0x00); // Disable Embedded DC/DC Converter (0x00/0x01)
Set_Area_Color(0x05); // Set Monochrome & Low Power Save Mode
Set_Addresssing_Mode(0x02); // Set Page Addressing Mode (0x00/0x01/0x02)
Set_Segment_Remap(0x01); // Set SEG/Column Mapping (0x00/0x01)
Set_Common_Remap(0x08); // Set COM/Row Scan Direction (0x00/0x08)
Set_Common_Config(0x10); // Set Alternative Configuration (0x00/0x10)
Set_LUT(0x3F,0x3F,0x3F,0x3F); // Define All Banks Pulse Width as 64 Clocks
Set_Contrast_Control(Brightness); // Set SEG Output Current
Set_Area_Brightness(Brightness); // Set Brightness for Area Color Banks
Set_Precharge_Period(0xD2); // Set Pre-Charge as 13 Clocks & Discharge as 2 Clock
Set_VCOMH(0x08); // Set VCOM Deselect Level
Set_Entire_Display(0x00); // Disable Entire Display On (0x00/0x01)
Set_Inverse_Display(0x00); // Disable Inverse Display On (0x00/0x01)
Fill_RAM(0x00); // Clear Screen
Set_Display_On_Off(0x01); // Display On (0x00/0x01)
```

Quality Information

Test Item	Content of Test	Test Condition	Note
High Temperature storage	Test the endurance of the display at high storage temperature.	+90°C , 240hrs	2
Low Temperature storage	Test the endurance of the display at low storage temperature.	-40°C , 240hrs	1,2
High Temperature Operation	Test the endurance of the display by applying electric stress (voltage & current) at high temperature.	+85°C 240hrs	2
Low Temperature Operation	Test the endurance of the display by applying electric stress (voltage & current) at low temperature.	-40°C , 240hrs	1,2
High Temperature / Humidity Operation	Test the endurance of the display by applying electric stress (voltage & current) at high temperature with high humidity.	+60°C , 90% RH , 240hrs	1,2
Thermal Shock resistance	Test the endurance of the display by applying electric stress (voltage & current) during a cycle of low and high temperatures.	-40°C,30min -> 25°C,5min -> 85°C,30min = 1 cycle 100 cycles	
Vibration test	Test the endurance of the display by applying vibration to simulate transportation and use.	10-22Hz , 15mm amplitude. 22-500Hz, 1.5G 30min in each of 3 directions X,Y,Z	3
Atmospheric Pressure test	Test the endurance of the display by applying atmospheric pressure to simulate transportation by air.	115mbar, 40hrs	3
Static electricity test	Test the endurance of the display by applying electric static discharge.	VS=800V, RS=1.5kΩ, CS=100pF One time	

Note 1: No condensation to be observed.

Note 2: Conducted after 2 hours of storage at 25°C, 0%RH.

Note 3: Test performed on product itself, not inside a container.

Evaluation Criteria:

- 1: Display is fully functional during operational tests and after all tests, at room temperature.
- 2: No observable defects.
- 3: Luminance >50% of initial value.
- 4: Current consumption within 50% of initial value