NCP1522B

Buck Converter - DC-DC

3 MHz, 600 mA

The NCP1522B step−down DC−DC converter is a monolithic integrated circuit optimized for portable applications powered from one cell Li−Ion or three cell Alkaline/NiCd/NiMH batteries. The part, available in adjustable output voltage versions ranging from 0.9 V to 3.3 V, is able to deliver up to 600 mA. It uses synchronous rectification to increase efficiency and reduce external part count. The device also has a built−in 3 MHz (nominal) oscillator which reduces component size by allowing smaller inductors and capacitors. Automatic switching PWM/PFM mode offers improved system efficiency.

Additional features include integrated soft−start, cycle−by−cycle current limiting and thermal shutdown protection. The NCP1522B is available in a space saving, low profile TSOP5 and UDFN6 packages.

Features

- Up to 93% Efficiency
- Allow Use of Small External Components
- Source up to 600 mA
- 3 MHz Switching Frequency
- Adjustable Output Voltage from 0.9 V to 3.3 V
- Synchronous Rectification for Higher Efficiency
- 2.7 V to 5.5 V Input Voltage Range
- Low Quiescent Current
- Shutdown Current Consumption of 0.3 μA
- Thermal Limit Protection
- Short Circuit Protection
- All Pins are Fully ESD Protected
- These are Pb−Free Devices

Typical Applications

- Cellular Phones, Smart Phones and PDAs
- Digital Still/Video Cameras
- MP3 Players and Portable Audio Systems
- Wireless and DSL Modems
- Portable Equipment
- USB Powered Devices

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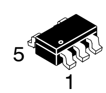
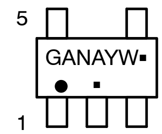
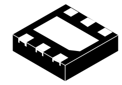
MARKING DIAGRAM



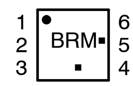
TSOP−5
SN SUFFIX
CASE 483



GAN = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)



UDFN6
MU SUFFIX
CASE 517AB



BR = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NCP1522BSNT1G	TSOP−5 (Pb−Free)	3000/Tape & Reel
NCP1522BMUTBG	UDFN6 (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

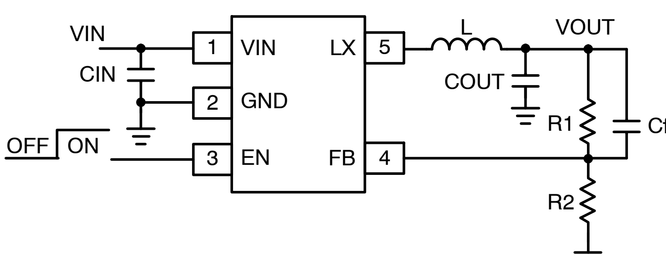


Figure 1. Typical Application − TSOP−5

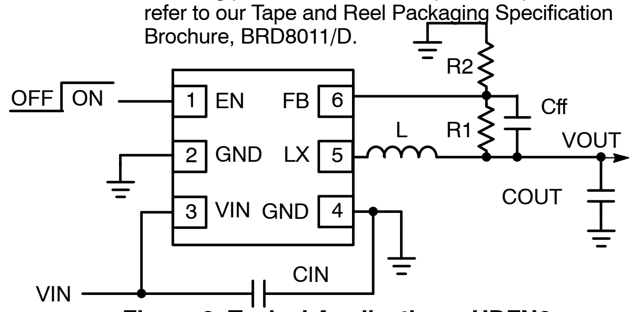


Figure 2. Typical Application − UDFN6

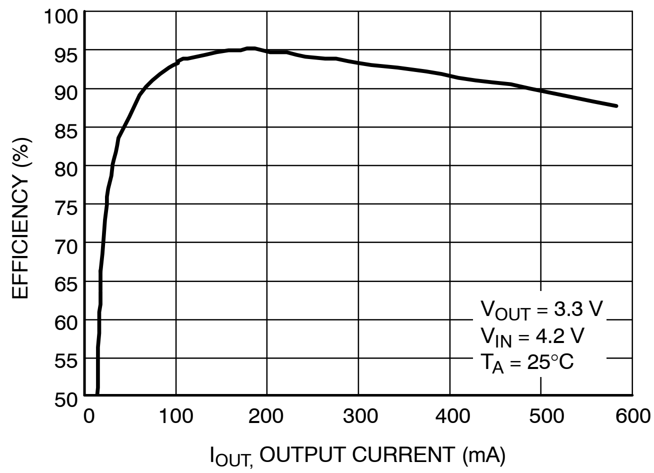


Figure 3. Efficiency vs. Output Current

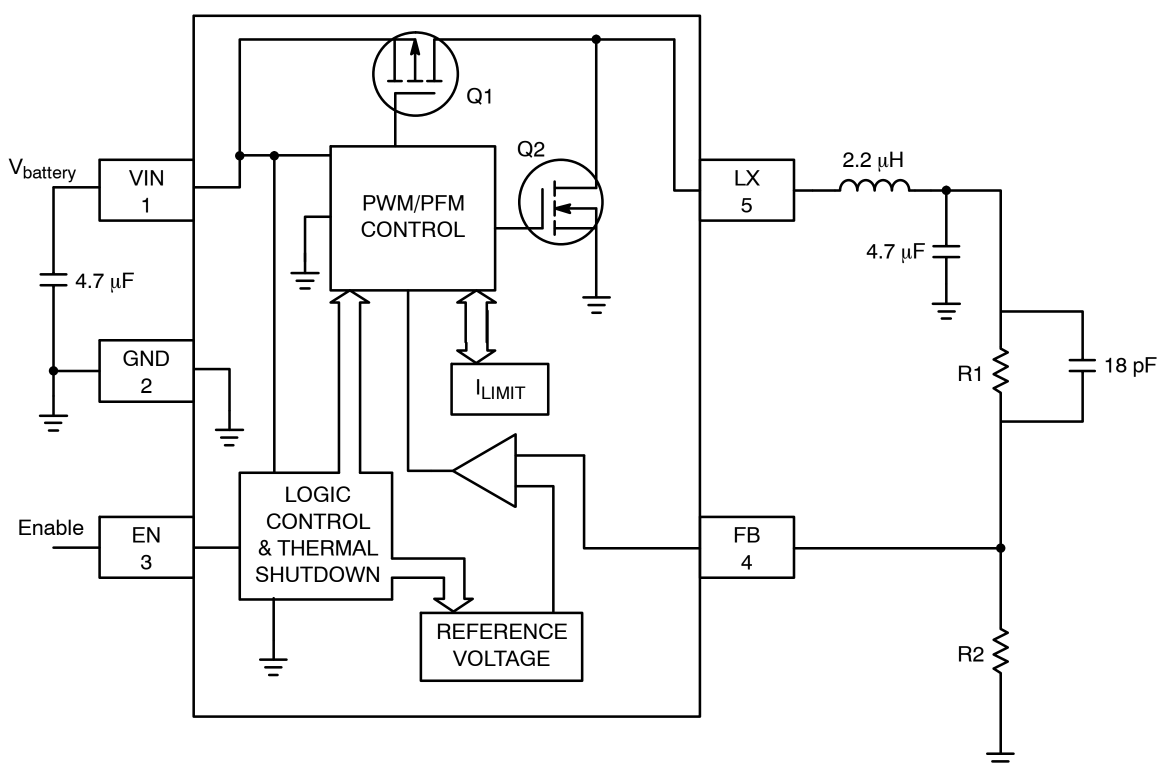
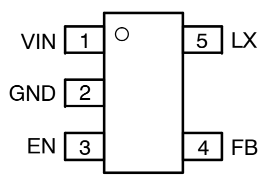


Figure 4. Simplified Block Diagram

PIN FUNCTION DESCRIPTION

Pin TSOP−5	Pin UDFN6	Pin Name	Type	Description
1	3	VIN	Analog / Power Input	Power supply input for the PFET power stage, analog and digital blocks. The pin must be decoupled to ground by a 10 μF ceramic capacitor.
2	2, 4	GND	Analog / Power Ground	This pin is the GND reference for the NFET power stage and the analog section of the IC. The pin must be connected to the system ground.
3	1	EN	Digital Input	Enable for switching regulators. This pin is active HIGH and is turned off by logic LOW on this pin.
4	6	FB	Analog Input	Feedback voltage from the output of the power supply. This is the input to the error amplifier.
5	5	LX	Analog Output	Connection from power MOSFETs to the Inductor.

PIN CONNECTIONS



(Top View)

Figure 5. Pin Connections − TSOP−5

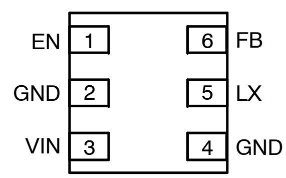


Figure 6. Pin Connections − UDFN6

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Minimum Voltage All Pins	V_{min}	−0.3	V
Maximum Voltage All Pins (Note 2)	V_{max}	7.0	V
Maximum Voltage EN, FB, LX	V_{max}	VIN + 0.3	V
Thermal Resistance, Junction−to−Air (with Recommended Soldering Footprint) TSOP−5 UDFN6	$R_{\theta JA}$	300 260	°C/W
Operating Ambient Temperature Range	T_A	−40 to 85	°C
Storage Temperature Range	T_{stg}	−55 to 150	°C
Junction Operating Temperature	T_j	−40 to 125	°C
Latchup Current Maximum Rating (T_A = 85°C) (Note 4) Other Pins	Lu	±100	mA
ESD Withstand Voltage (Note 3) Human Body Model Machine Model	V_{esd}	 2.0 200	 kV V
Moisture Sensitivity Level (Note 5)	MSL	1	per IPC

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Maximum electrical ratings are defined as those values beyond which damage to the device may occur at T_A = 25°C.
2. According to JEDEC standard JESD22−A108B.
3. This device series contains ESD protection and exceeds the following tests:
   Human Body Model (HBM) per JEDEC standard: JESD22−A114.
   Machine Model (MM) per JEDEC standard: JESD22−A115.
4. Latchup current maximum rating per JEDEC standard: JESD78.
5. JEDEC Standard: J−STD−020A.

ELECTRICAL CHARACTERISTICS (Typical values are referenced to T_A = +25°C, Min and Max values are referenced −40°C to +85°C ambient temperature, unless otherwise noted, operating conditions V_{IN} = 3.6 V, V_{OUT} = 1.2 V, unless otherwise noted.)

Rating	Pin		Symbol	Min	Typ	Max	Unit
	TSOP	UDFN					
VIN PIN							
Input Voltage Range	1	3	V_{IN}	2.7	–	5.5	V
Quiescent Current, PFM No Switching	1	3	$I_{q\ ON}$	–	50	90	μA
Standby Current, EN Low	1	3	$I_{q\ OFF}$	–	0.2	1.5	μA
Under Voltage Lockout (V_{IN} Falling)	1	3	V_{UVLO}	2.2	2.4	2.55	V
EN PIN							
Positive Going Input High Voltage Threshold, EN0 Signal	3	1	V_{IH}	1.2	–	–	V
Negative Going Input High Voltage Threshold, EN0 Signal	3	1	V_{IL}	–	–	0.4	V
EN High Input Current, EN = 3.6 V	3	1	I_{ENH}	–	2.0	–	μA
OUTPUT							
Output Voltage Accuracy (Note 6) Ambient Temperature Overtemperature Range			ΔV_{OUT}	 – –3.0	 ±1.0 ±2.0	 – ±3.0	%
Minimum Output Voltage (Note 7)			V_{OUT}	–	0.9	–	V
Maximum Output Voltage			V_{OUT}	–	3.3	–	V
Output Voltage Load Regulation Overtemperature I_{OUT} = 100 mA to 600 mA			V_{OUT}	 –	 0.0008	 –	%/mA
Load Transient Response, Rise/Falltime 1 μs 10 mA to 100 mA Load Step 200 mA to 600 mA Load Step			V_{OUT}	 – –	 50 54	 – –	mV
Output Voltage Line Regulation, I_{OUT} = 100 mA, V_{IN} = 2.7 V to 5.5 V			V_{OUT}	 –	 0.08	 –	%
Line Transient Response, I_{OUT} = 100 mA, 3.6 V to 3.0 V Line Step (Falltime=50 μs)			V_{OUT}	 –	 2.0	 –	mV_{PP}
Output Voltage Ripple, I_{OUT} = 300 mA (PWM Mode)			V_{OUT}	–	1.0	–	mV
Output Voltage Ripple, I_{OUT} = 0 mA (PFM Mode)			V_{OUT}	–	8.0	–	mV
Peak Inductor Current	5	5	I_{LIM}	–	1200	–	mA
Oscillator Frequency	5	5	F_{OSC}	2.4	3.0	3.6	MHz
Duty Cycle	5	5	–	–	–	100	%
Soft−Start Time			T_{START}	–	320	500	μs
Thermal Shutdown Threshold			T_{SD}	–	160	–	°C
Thermal Shutdown Hysteresis			T_{SDH}	–	25	–	°C
POWER SWITCHES							
P−Channel On−Resistance			RLxH	–	400	–	mΩ
N−Channel On−Resistance			RLxL	–	400	–	mΩ
P−Channel Leakage Current			I_{LeakH}	–	0.05	–	μA
N−Channel Leakage Current			I_{LeakL}	–	0.01	–	μA

6. The overall output voltage tolerance depends upon the accuracy of the external resistor (R1, R2).
7. For V_{OUT} = 0.9 V, maximum input voltage do not exceed 5.2 V.

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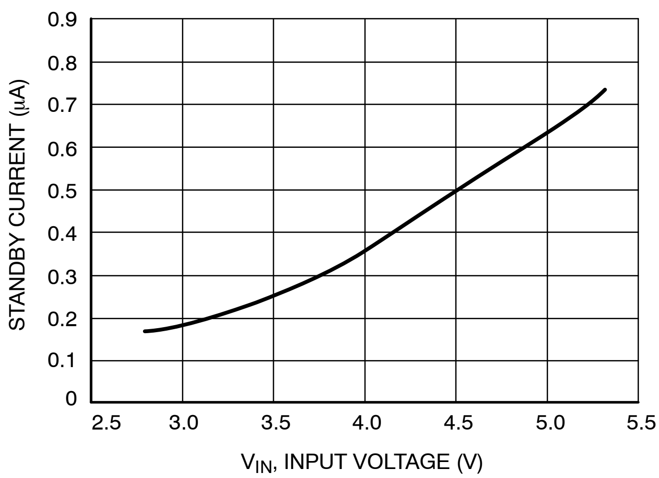


Figure 7. Shutdown Current vs. Supply Voltage

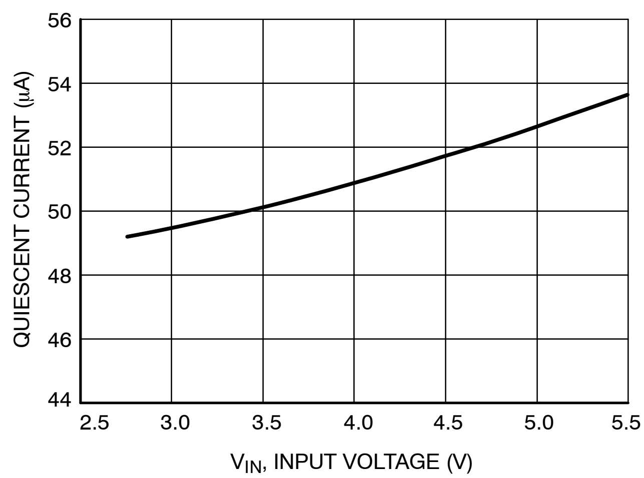


Figure 8. Quiescent Current PFM No Switching vs. Supply Voltage

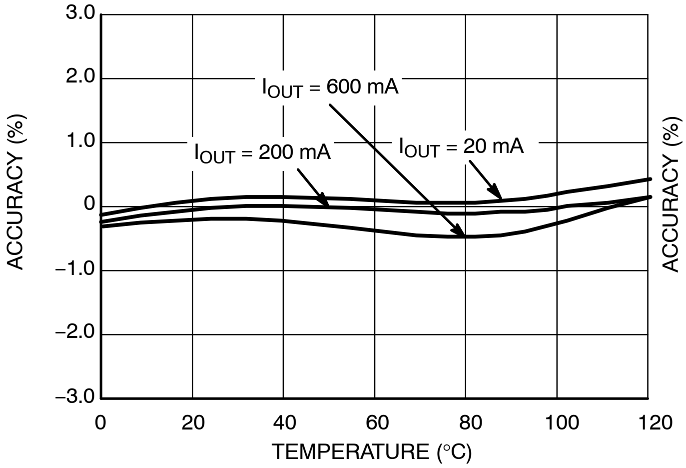


Figure 9. Output Voltage Accuracy vs. Temperature (V_{IN} = 3.6 V, V_{OUT} = 1.2 V)

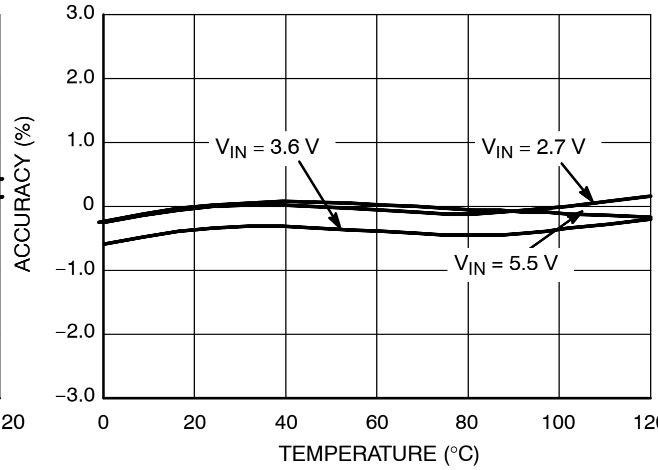


Figure 10. Output Voltage Accuracy vs. Temperature (V_{OUT} = 1.2 V, I_{OUT} = 200 mA)

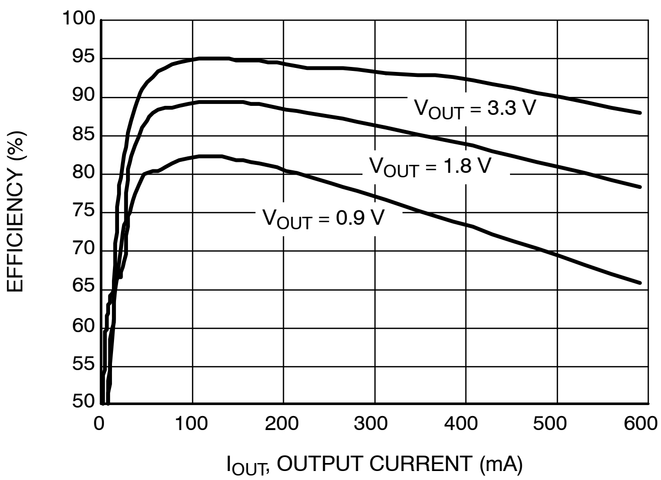


Figure 11. Efficiency vs. Output Current (V_{IN} = 3.6 V, T_A = 25°C)

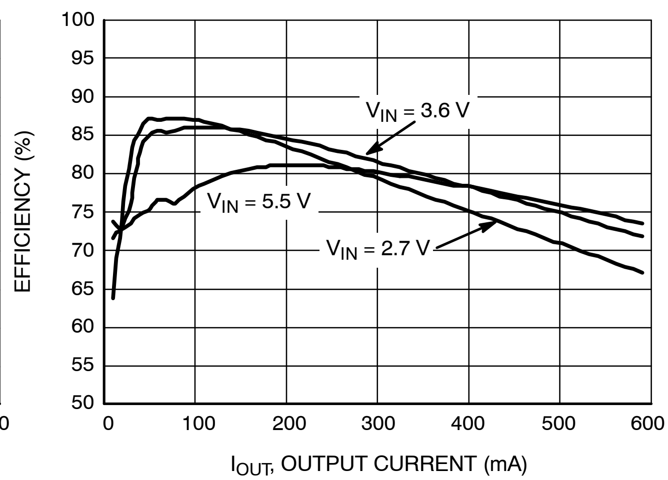


Figure 12. Efficiency vs. Output Current (V_{OUT} = 1.2 V, T_A = 25°C)

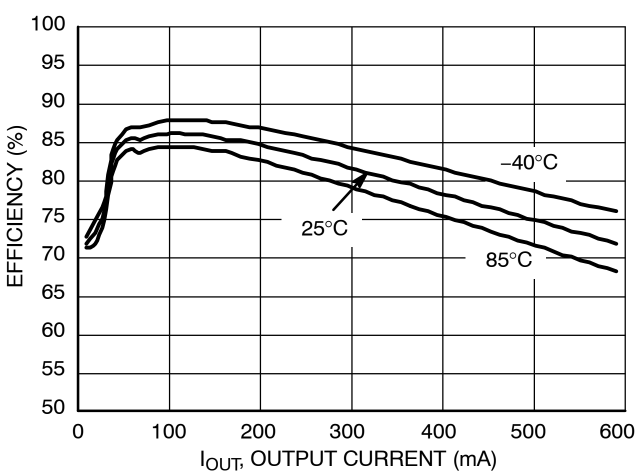


Figure 13. Efficiency vs. Output Current (V_{IN} = 3.6 V, V_{OUT} = 1.2 V)

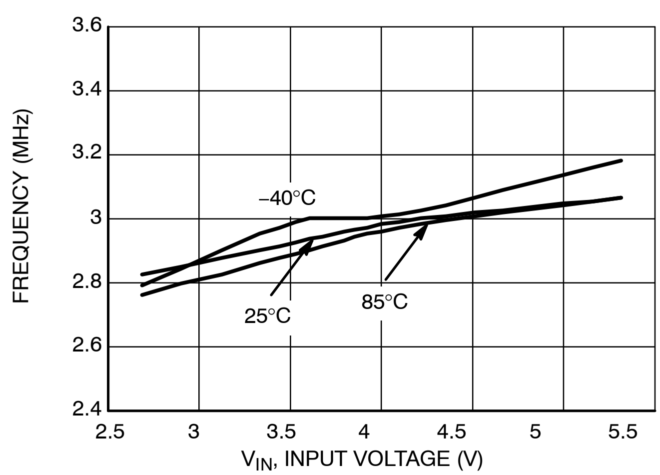


Figure 14. Switching Frequency vs. Input Voltage (V_{OUT} = 1.2 V, I_{OUT} = 300 mA)

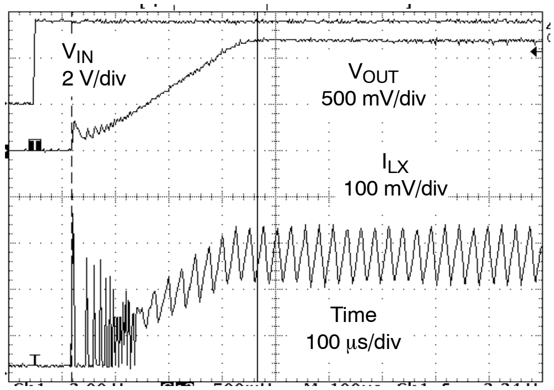


Figure 15. Typical Soft−Start (V_{OUT} = 1.2 V, I_{OUT} = 250 mA)

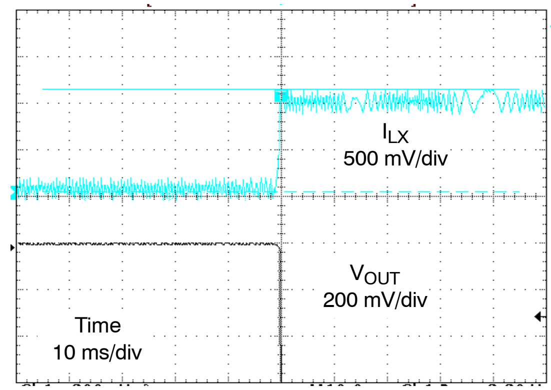


Figure 16. Short−Circuit Protection (V_{IN} = 3.6 V, V_{OUT} = 1.2 V)

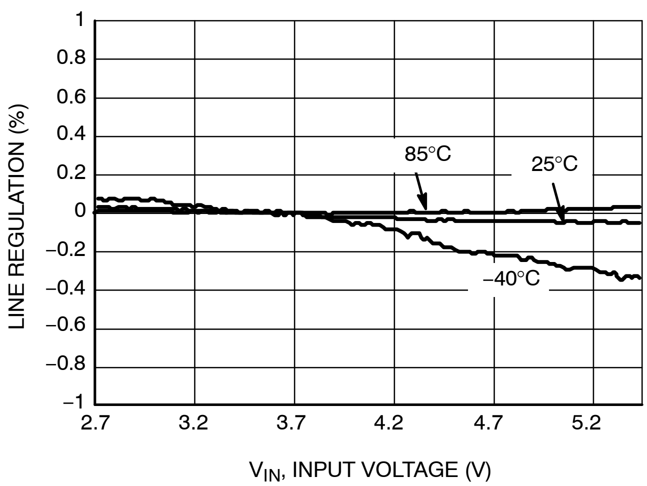


Figure 17. Line Regulation (V_{OUT} = 1.2 V, I_{OUT} = 300 mA)

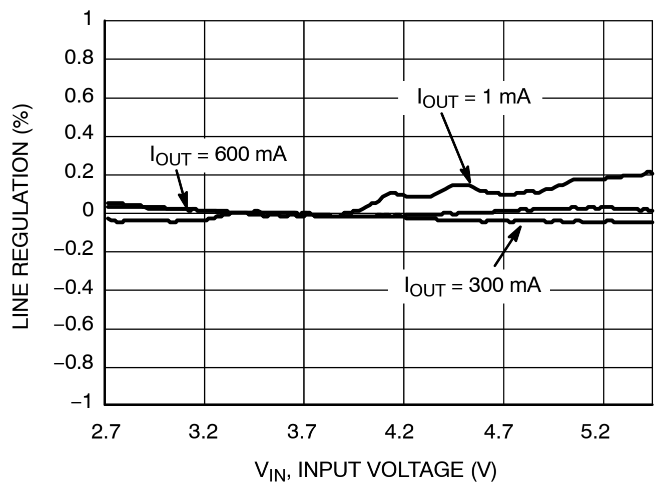


Figure 18. Line Regulation (V_{OUT} = 1.2 V, T_A = 25°C)

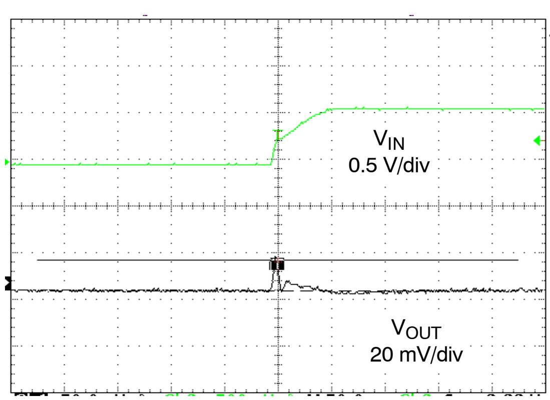


Figure 19. 3.0 V to 3.6 V Line Transient (Risetime = 50 μs, V_{OUT} = 1.2 V, I_{OUT} = 100 mA, T_A = 25°C)

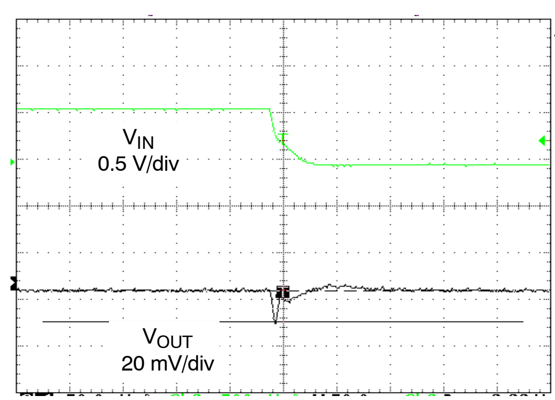


Figure 20. 3.6 V to 3.0 V Line Transient (Risetime = 50 μs, V_{OUT} = 1.2 V, I_{OUT} = 100 mA, T_A = 25°C)

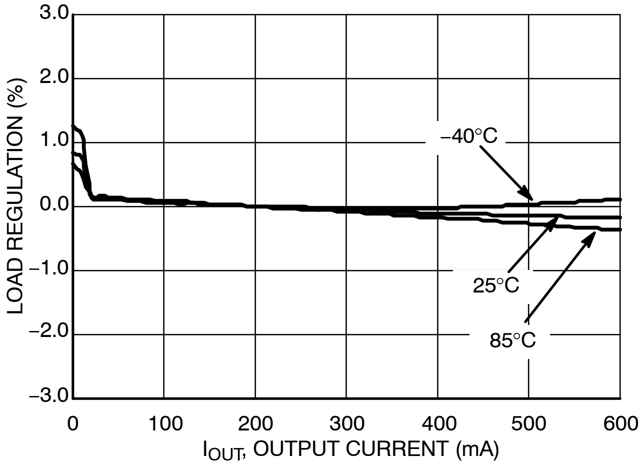


Figure 21. Load Regulation
(V_{IN} = 3.6 V, V_{OUT} = 1.2 V)

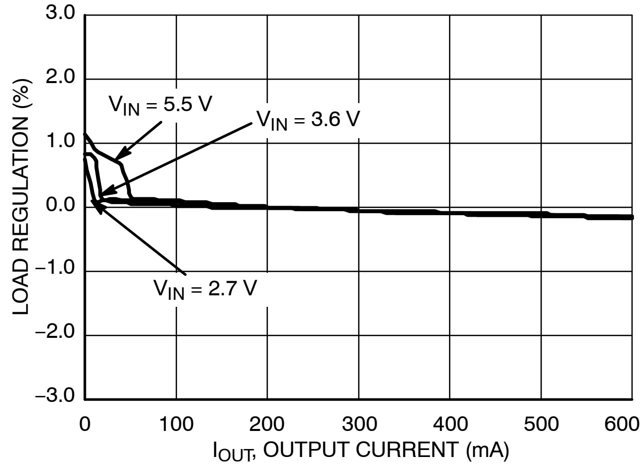


Figure 22. Load Regulation
(V_{OUT} = 1.2 V, T_A = 25°C)

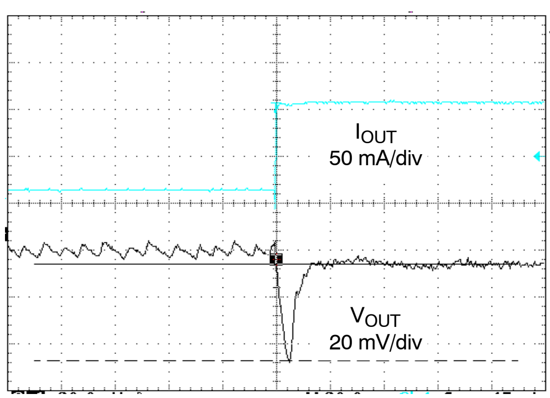


Figure 23. 10 mA to 100 mA Load Transient
(V_{IN} = 3.6 V, V_{OUT} = 1.2 V, T_A = 25°C)

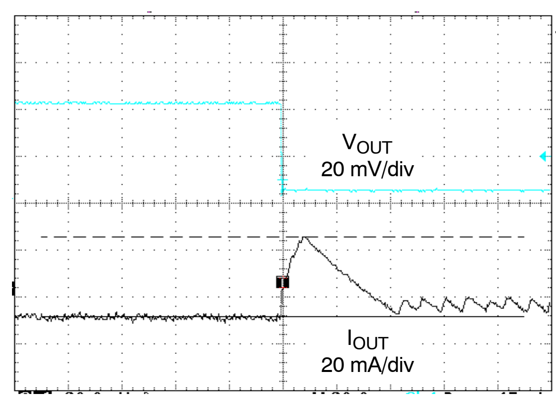


Figure 24. 100 mA to 10 mA Load Transient
(V_{IN} = 3.6 V, V_{OUT} = 1.2 V, T_A = 25°C)

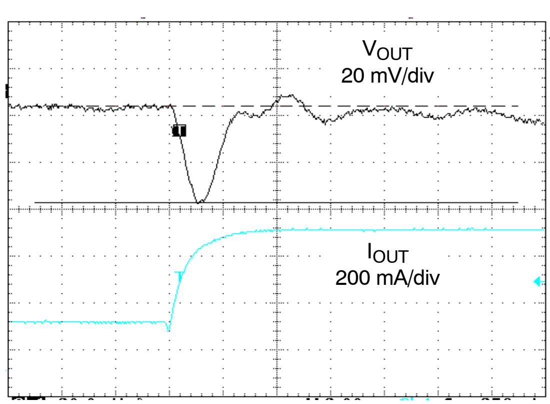


Figure 25. 200 mA to 600 mA Load Transient
(V_{IN} = 3.6 V, V_{OUT} = 1.2 V, T_A = 25°C)

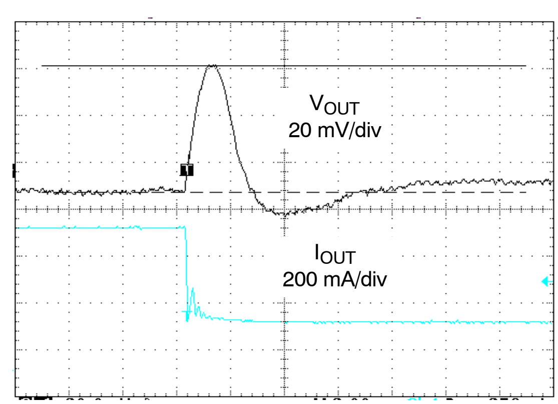


Figure 26. 600 mA to 200 mA Load Transient
(V_{IN} = 3.6 V, V_{OUT} = 1.2 V, T_A = 25°C)

DC/DC OPERATION DESCRIPTION

Detailed Description

The NCP1522B uses a constant frequency, voltage mode step−down architecture. Both the main (P−Channel MOSFET) and synchronous (N−Channel MOSFET) switches are internal.

The output voltage is set by an external resistor divider in the range of 0.9 V to 3.3 V and can source at least 600 mA.

The NCP1522B works with two modes of operation; PWM/PFM depending on the current required. In PWM mode, the device can supply voltage with a tolerance of ±3% and 90% efficiency or better. Lighter load currents cause the device to automatically switch into PFM mode to reduce current consumption and extended battery life.

Additional features include soft−start, undervoltage protection, current overload protection, and thermal shutdown protection. As shown in Figure 1, only six external components are required. The part uses an internal reference voltage of 0.6 V. It is recommended to keep NCP1522B in shutdown mode until the input voltage is 2.7 V or higher.

PWM Operating Mode

In this mode, the output voltage of the device is regulated by modulating the on−time pulse width of the main switch Q1 at a fixed 3 MHz frequency.

The switching of the PMOS Q1 is controlled by a flip−flop driven by the internal oscillator and a comparator that compares the error signal from an error amplifier with the sum of the sensed current signal and compensation ramp.

The driver switches ON and OFF the upper side transistor (Q1) and switches the lower side transistor in either ON state or in current source mode.

At the beginning of each cycle, the main switch Q1 is turned ON by the rising edge of the internal oscillator clock. The inductor current ramps up until the sum of the current sense signal and compensation ramp becomes higher than the error amplifier's voltage. Once this has occurred, the PWM comparator resets the flip−flop, Q1 is turned OFF while the synchronous switch Q2 is turned in its current source mode. Q2 replaces the external Schottky diode to reduce the conduction loss and improve the efficiency. To avoid overall power loss, a certain amount of dead time is introduced to ensure Q1 is completely turned OFF before Q2 is being turned ON.

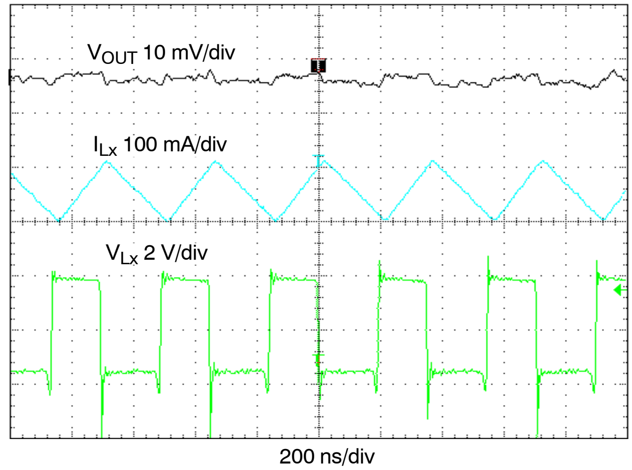


Figure 27. PWM Switching Waveform (V_{IN} = 3.6 V, V_{OUT} = 1.2 V, I_{OUT} = 600 mA)

PFM Operating Mode

Under light load conditions, the NCP1522B enters in low current PFM mode operation to reduce power consumption. The output regulation is implemented by pulse frequency modulation. If the output voltage drops below the threshold of PFM comparator, a new cycle will be initiated by the PFM comparator to turn on the switch Q1. Q1 remains ON during the minimum on time of the structure while Q2 is in its current source mode. The peak inductor current depends upon the drop between input and output voltage. After a short dead time delay where Q1 is switched OFF, Q2 is turned in its ON state. The negative current detector will detect when the inductor current drops below zero and sends the signal to turn Q2 to current source mode to prevent a too large deregulation of the output voltage. When the output voltage falls below the threshold of the PFM comparator, a new cycle starts immediately.

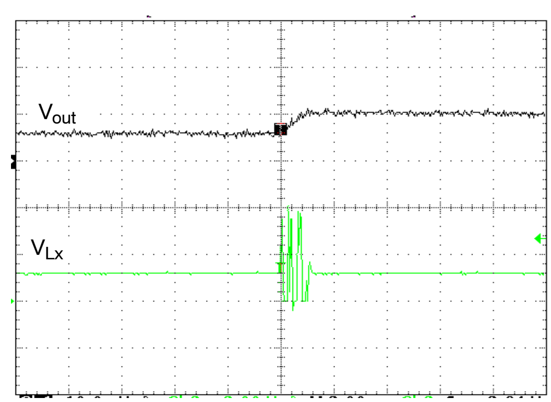


Figure 28. PFM Switching Waveforms (V_{IN} = 3.6 V, V_{OUT} = 1.2 V, I_{OUT} = 0 mA, Temp = 25°C)

Soft−Start

The NCP1522B uses soft−start to limit the inrush current when the device is initially powered up or enabled. Soft−start is implemented by gradually increasing the reference voltage until it reaches the full reference voltage. During startup, a pulsed current source charges the internal soft−start capacitor to provide gradually increasing reference voltage. When the voltage across the capacitor ramps up to the nominal reference voltage, the pulsed current source will be switched off and the reference voltage will switch to the regular reference voltage.

Cycle−by−Cycle Current Limitation

From the block diagram, an I_{LIM} comparator is used to realize cycle−by−cycle current limit protection. The comparator compares the LX pin voltage with the reference voltage, which is biased by a constant current. If the inductor current reaches the limit, the I_{LIM} comparator detects the LX voltage falling below the reference voltage and releases the signal to turn off the switch Q1. The cycle−by−cycle current limit is set at 1200 mA (nom).

Low Dropout Operation

The NCP1522B offers a low input to output voltage difference. The NCP1522B can operate at 100% duty cycle. In this mode the PMOS (Q1) remains completely on.

The minimum input voltage to maintain regulation can be calculated as:

$$V_{IN(min)} = V_{OUT(max)} + (I_{OUT} \times (R_{DS(ON)} + R_{INDUCTOR})) \quad \text{(eq. 1)}$$

- V_{OUT}: Output Voltage (Volts)
- I_{OUT}: Max Output Current
- $R_{DS(ON)}$ = P−Channel Switch $R_{DS(ON)}$
- $R_{INDUCTOR}$: Inductor Resistance (DCR)

Undervoltage Lockout

The input voltage V_{IN} must reach 2.4 V (typ) before the NCP1522B enables the DC/DC converter output to begin the start up sequence (see Soft−Start section). The UVLO threshold hysteresis is typically 100 mV.

Shutdown Mode

Forcing this pin to a voltage below 0.4 V will shut down the IC. In shutdown mode, the internal reference, oscillator and most of the control circuitries are turned off. Therefore, the typical current consumption will be 0.3 μA (typical value). Applying a voltage above 1.2 V to EN pin will enable the device for normal operation. The typical threshold is around 0.7 V. The device will go through soft−start to normal operation.

Thermal Shutdown

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. If the junction temperature exceeds 160°C, the device shuts down. In this mode switch Q1 and Q2 and the control circuits are all turned off. The device restarts in soft−start after the temperature drops below 135°C. This feature is provided to prevent catastrophic failures from accidental device overheating, and it is not intended as a substitute for proper heatsinking.

Short Circuit Protection

When the output is shorted to ground, the device limits the inductor current. The duty−cycle is minimum and the consumption on the input line is 300 mA (Typ). When the short circuit condition is removed, the device returns to the normal mode of operation.

APPLICATION INFORMATION

Output Voltage Selection

The output voltage is programmed through an external resistor divider connected from V_{OUT} to FB then to GND. For low power consumption and noise immunity, the resistor from FB to GND (R2) should be in the [100 k−600 k] range. If R2 is 200 k given the V_{FB} is 0.6 V, the current through the divider will be 3.0 μA.

The formula below gives the value of V_{OUT}, given the desired R1 and the R1 value:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) \quad \text{(eq. 2)}$$

- V_{OUT}: Output Voltage (Volts)
- V_{FB}: Feedback Voltage = 0.6 V
- R1: Feedback Resistor from V_{OUT} to FB
- R2: Feedback Resistor from FB to GND

Input Capacitor Selection

In PWM operating mode, the input current is pulsating with a large switching noise. Using an input bypass capacitor can reduce the peak current transients drawn from the input supply source, thereby reducing switching noise significantly. The capacitance needed for the input bypass capacitor depends on the source impedance of the input supply.

The maximum RMS current occurs at 50% duty cycle with maximum output current, which is $I_{out\_max}/2$.

For NCP1522B, a low profile ceramic capacitor of 4.7 μF should be used for most of the cases. For effective bypass results, the input capacitor should be placed as close as possible to the V_{IN} pin.

Table 1. List of Input Capacitors

Murata	GRM188R60J475KE	4.7 μF
	GRM21BR71C475KA	
Taiyo Yuden	JMK212BY475MG	4.7 μF
TDK	C2012X5ROJ475KB	4.7 μF
	C1632X5ROJ475KT	

Output L−C Filter Design Considerations

The NCP1522B operates at 3 MHz frequency and uses voltage mode architecture. The correct selection of the output filter ensures good stability and fast transient response.

Due to the nature of the buck converter, the output L−C filter must be selected to work with internal compensation. For NCP1522B, the internal compensation is internally fixed and it is optimized for an output filter of L = 2.2 μH and C_{OUT} = 4.7 μF.

The corner frequency is given by:

$$f_C = \frac{1}{2\pi\sqrt{L \times C_{OUT}}} = \frac{1}{2\pi\sqrt{2.2\ \mu H \times 4.7\ \mu F}} = 49\ kHz \quad \text{(eq. 3)}$$

The device is intended to operate with inductance value of 2.2 μH.

If the corner frequency is moved, it is recommended to check the loop stability depending on the accepted output ripple voltage and the required output curret. Take care to check the loop stability. The phase margin is usually higher than 45°.

Table 2. L−C Filter Example

Inductance (L)	Output Capacitor (C_{OUT})
1.0 μH	10 μF
2.2 μH	4.7 μF

Inductor Selection

The inductor parameters directly related to device performances are saturation current and DC resistance and inductance value. The inductor ripple current (ΔI_L) decreases with higher inductance:

$$\Delta I_L = \frac{V_{OUT}}{L \times f_{SW}}\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad \text{(eq. 4)}$$

- $\Delta I_{L:}$ Peak to Peak Inductor Ripple Current
- L: Inductor Value
- $f_{SW:}$ Switching Frequency

The saturation current of the inductor should be rated higher than the maximum load current plus half the ripple current:

$$I_{L(MAX)} = I_{O(MAX)} + \frac{\Delta I_L}{2} \quad \text{(eq. 5)}$$

- $\Delta I_{L(MAX):}$ Maximum Inductor Current
- $\Delta I_{O(MAX):}$ Maximum Output Current

The inductor's resistance will factor into the overall efficiency of the converter. For best performance, the DC resistance should be less than 0.3 Ω for good efficiency.

Table 3. LIST OFINDUCTORS

Coilcraft	DO1605−T Series
	LPO3010 Series
FDK	MIPW3226 Series
TDK	VLF3010AT Series
Taiyo Yuden	LQ CBL2012 Series

Output Capacitor Selection

Selecting the proper output capacitor is based on the desired output ripple voltage. Ceramic capacitors with low ESR values will have the lowest output ripple voltage and are strongly recommended. The output capacitor requires an X7R dielectric.

The output ripple voltage in PWM mode is given by:

$$\Delta V_{OUT} = \Delta I_L \times \left(\frac{1}{4 \times f_{SW} \times C_{OUT}} + ESR \right) \quad \text{(eq. 6)}$$

- ΔV_{OUT}: Output Voltage Ripple in PWM Mode
- ΔI_L: Peak to Peak Inductor Ripple Current
- f_{SW}: Switching Frequency
- C_{OUT}: Output Capacitor
- ESR: Output Capacitor Serial Resistor

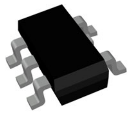
Table 4. LIST OF OUTPUT CAPACITORS

Murata	GRM188R60J475KE	4.7 μF
	GRM21BR71C475KA	
	GRM188R60OJ106ME	10 μF
	GRM21BR60J106ME19L	
Taiyo Yuden	JMK212BY475MG	4.7 μF
	JMK212BJ106MG	10 μF
TDK	C2012X5ROJ475KB	4.7 μF
	C1632X5ROJR75KT	
	C2012X5ROJ106K	10 μF

Feed−Forward Capacitor Selection

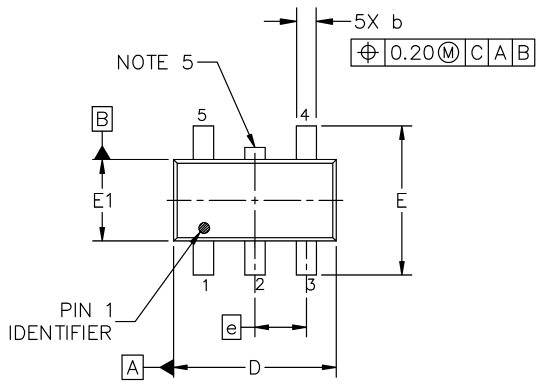
The feed−forward capacitor sets the feedback loop response and is critical to obtain good loop stability.

Given that the compensation is internally fixed, an 18 pF or higher ceramic capacitor is needed. Choose a small ceramic capacitor X7R dielectric.



TSOP−5 3.00x1.50x0.95, 0.95P
CASE 483
ISSUE P

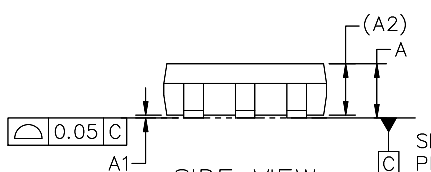
DATE 01 APR 2024



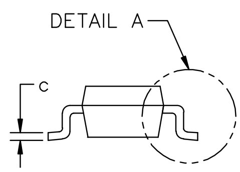
TOP VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS (ANGLES IN DEGREES).
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OF GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

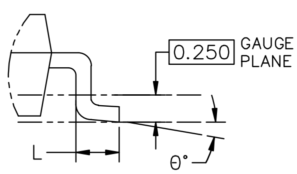


SIDE VIEW

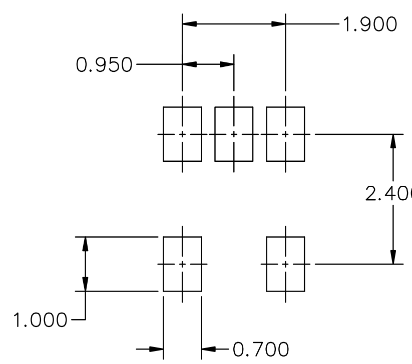


END VIEW

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.900	1.000	1.100
A1	0.010	0.055	0.100
A2	0.950 REF.		
b	0.250	0.375	0.500
c	0.100	0.180	0.260
D	2.850	3.000	3.150
E	2.500	2.750	3.000
E1	1.350	1.500	1.650
e	0.950 BSC		
L	0.200	0.400	0.600
θ	0°	5°	10°



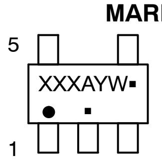
DETAIL "A"
SCALE 2:1



RECOMMENDED MOUNTING FOOTPRINT*

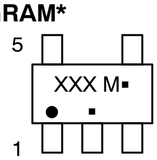
* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



Analog

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package



Discrete/Logic

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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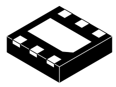
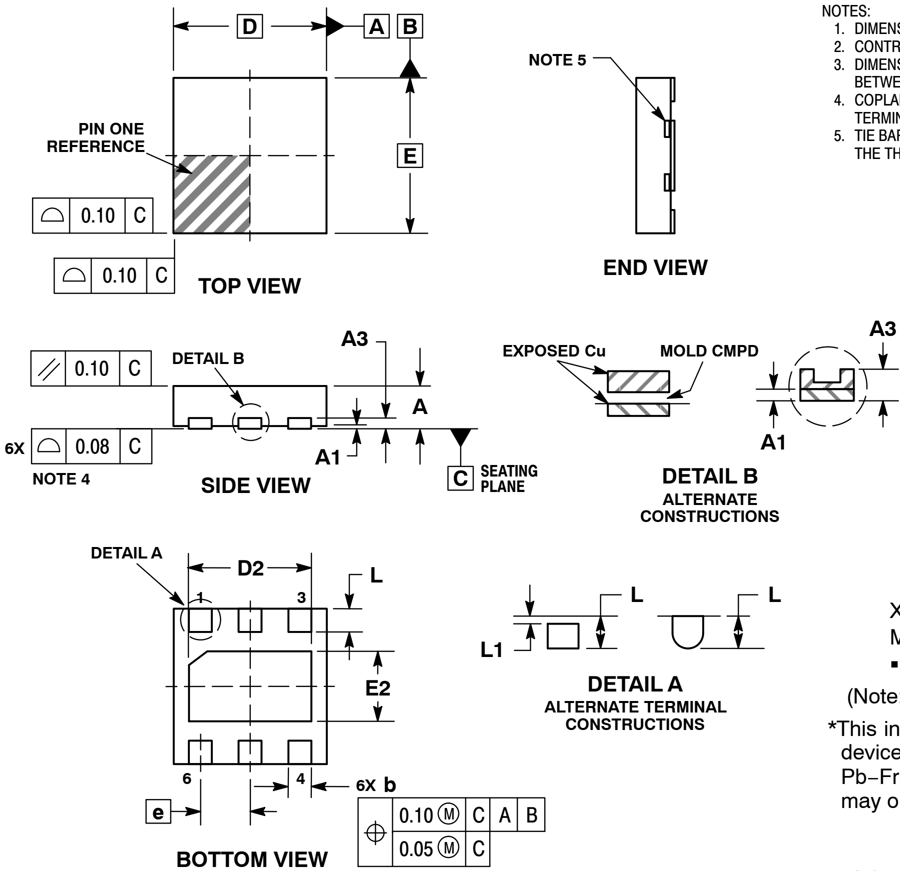
DESCRIPTION:	**TSOP−5 3.00x1.50x0.95, 0.95P**	**PAGE 1 OF 1**



SCALE 4:1

UDFN6 2x2, 0.65P
CASE 517AB
ISSUE C

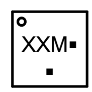
DATE 10 APR 2013



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. TIE BARS MAY BE VISIBLE IN THIS VIEW AND ARE CONNECTED TO THE THERMAL PAD.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.127 REF	
b	0.25	0.35
D	2.00 BSC	
D2	1.50	1.70
E	2.00 BSC	
E2	0.80	1.00
e	0.65 BSC	
L	0.25	0.35
L1	---	0.15

GENERIC MARKING DIAGRAM*

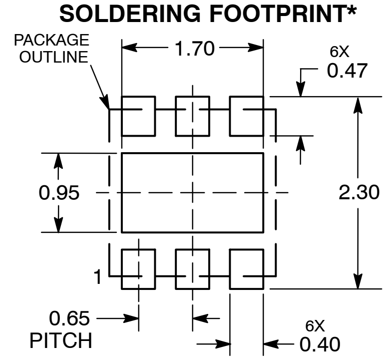


XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	UDFN6 2X2, 0.65P	PAGE 1 OF 1

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