LM4120 Precision Micropower Low Dropout Voltage Reference

1 Features

- Small SOT23-5 Package
- Low Dropout Voltage: 120 mV Typical at 1 mA
- High Output Voltage Accuracy: 0.2%
- Source and Sink Current Output: ±5 mA
- Supply Current: 160 µA Typical
- Low Temperature Coefficient: 50 ppm/°C
- Enable Pin
- Fixed Output Voltages: 1.8, 2.048, 2.5, 3, 3.3, 4.096, and 5 V
- Industrial Temperature Range: −40°C to 85°C
- (For Extended Temperature Range, −40°C to 125°C, Contact TI)

2 Applications

- Portable, Battery-Powered Equipment
- Instrumentation and Process Control
- Automotive and Industrial
- Test Equipment
- Data Acquisition Systems
- Precision Regulators
- Battery Chargers
- Base Stations
- Communications
- Medical Equipment

3 Description

The LM4120 device is a precision low-power, low dropout bandgap voltage reference with up to 5-mA output current source and sink capability.

This series reference operates with input voltages as low as 2 V and up to 12 V, consuming 160-µA (typical) supply current. In power-down mode, device current drops to less than 2 µA.

The LM4120 comes in two grades (A and Standard) and seven voltage options for greater flexibility. The best grade devices (A) have an initial accuracy of 0.2%, while the standard have an initial accuracy of 0.5%, both with a temperature coefficient of 50 ppm/°C ensured from −40°C to 125°C.

The very low dropout voltage, low supply current, and power-down capability of the LM4120 make this product an ideal choice for battery-powered and portable applications.

The device performance is ensured over the industrial temperature range (−40°C to 85°C), while certain specifications are ensured over the extended temperature range (−40°C to 125°C). Contact TI for full specifications over the extended temperature range. The LM4120 is available in a standard 5-pin SOT-23 package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM4120	SOT-23 (5)	1.60 mm × 2.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Functional Block Diagram

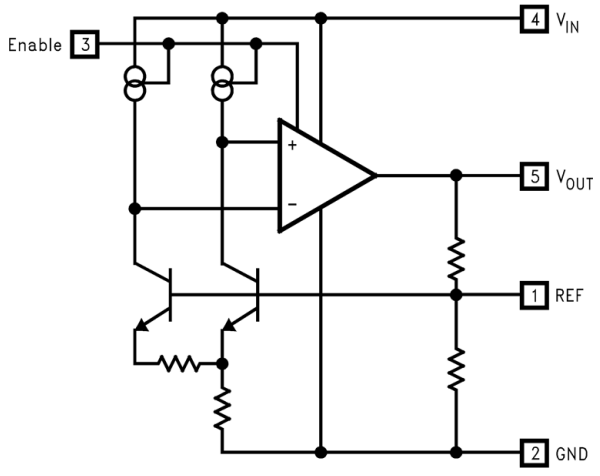


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (February 2016) to Revision F — **Page**

- Added updated *Layout Example* ... 16

Changes from Revision D (July 2015) to Revision E — **Page**

- Added updated *Layout Example* ... 16

Changes from Revision C (April 2013) to Revision D — **Page**

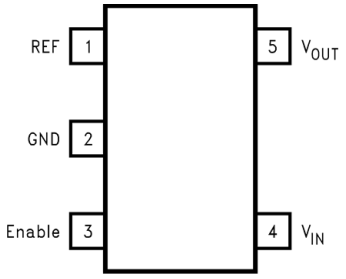
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1

Changes from Revision B (April 2013) to Revision C — **Page**

- Changed layout of National Data Sheet to TI format ... 14

5 Pin Configuration and Functions

DBV Package
5-Pin SOT-23
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
Enable	3	I	Pulled to input for normal operation. Forcing this pin to ground will turn off the output.
GND	2	—	Negative supply or ground connection
REF	1	—	REF pin. This pin must be left unconnected.
V_{IN}	4	I	Positive supply
V_{OUT}	5	O	Reference output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Maximum voltage on input or enable pins		–0.3	14	V
Output short-circuit duraion			Indefinite	
Power dissipation (T_A = 25°C) (2)			350	mW
Lead temperature	Soldering, (10 sec.)		260	°C
	Vapor Phase (60 sec.)		215	°C
	Infrared (15 sec.)		220	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Without PCB copper enhancements. The maximum power dissipation must be derated at elevated temperatures and is limited by T_{JMAX} (maximum junction temperature), $R_{\theta JA}$ (junction-to-ambient thermal resistance) and T_A (ambient temperature). The maximum power dissipation at any temperature is: $PDiss_{MAX} = (T_{JMAX} – T_A) / R_{\theta JA}$ up to the value listed in the *Absolute Maximum Ratings*.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 (2)	±750	
		Machine Model	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Ambient temperature	–40		85	°C
Junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC[1]		LM4120 DBV [SOT-23] 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	170.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	123.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	30.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	17.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	29.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

unless otherwise specified, V_{IN} = 3.3 V, I_{LOAD} = 0, C_{OUT} = 0.01 µF, $T_A = T_j$ = 25°C.

PARAMETER		TEST CONDITIONS		MIN [1]	TYP [2]	MAX [1]	UNIT
1.8 V, 2.048 V, AND 2.5 V							
V_{OUT}	Output voltage initial accuracy LM4120A-1.800 LM4120A-2.048 LM4120A-2.500					±0.2%	
	LM4120-1.800 LM4120-2.048 LM4120-2.500					±0.5%	
TCV_{OUT}/°C	Temperature coefficient	–40°C ≤ T_A ≤ +125°C			14	50	ppm/°c
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation	3.3 V ≤ V_{IN} ≤ 12 V			0.0007	0.008	%/V
			–40°C ≤ T_A ≤ 85°C			0.01	
$\Delta V_{OUT}/\Delta I_{LOAD}$	Load regulation	0 mA ≤ I_{LOAD} ≤ 1 mA			0.03	0.08	%/mA
			–40°C ≤ T_A ≤ 85°C			0.17	
		1 mA ≤ I_{LOAD} ≤ 5 mA			0.01	0.04	
			–40°C ≤ T_A ≤ 85°C			0.1	
		–1 mA ≤ I_{LOAD} ≤ 0 mA			0.04	0.12	
		–5 mA ≤ I_{LOAD} ≤ −1 mA			0.01		
$V_{IN}-V_{OUT}$	Dropout voltage [3]	I_{LOAD} = 0 mA			45	65	mV
			–40°C ≤ T_A ≤ 85°C			80	
		I_{LOAD} = 1 mA			120	150	
			–40°C ≤ T_A ≤ 85°C			180	
		I_{LOAD} = 5 mA			180	210	
			–40°C ≤ T_A ≤ 85°C			250	

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate TI's Averaging Outgoing Quality Level (AOQL).
(2) Typical numbers are at 25°C and represent the most likely parametric norm.
(3) Dropout voltage is the differential voltage between V_{OUT} and V_{IN} at which V_{OUT} changes ≤ 1% from V_{OUT} at V_{IN} = 3.3 V for 1.8 V, 2 V, 2.5 V, and V_{OUT} + 1 V for others. For 1.8-V option, dropout voltage is not ensured over temperature. A parasitic diode exists between input and output pins; it will conduct if V_{OUT} is pulled to a higher voltage than V_{IN}.

Electrical Characteristics (continued)

unless otherwise specified, V_{IN} = 3.3 V, I_{LOAD} = 0, C_{OUT} = 0.01 µF, $T_A = T_j$ = 25°C.

PARAMETER		TEST CONDITIONS		MIN (1)	TYP (2)	MAX (1)	UNIT
V_N	Output (4)	0.1 Hz to 10 Hz			20		μV_{PP}
		10 Hz to 10 kHz			36		
I_S	Supply current				160	250	µA
			–40°C ≤ T_A ≤ 85°C			275	
I_{SS}	Power-down supply current	Enable = 0.4 V –40°C ≤ T_J ≤ 85°C Enable = 0.2 V				1	µA
			–40°C ≤ T_A ≤ 85°C			2	
V_H	Logic high input voltage				2.4		V
		–40°C ≤ T_A ≤ 85°C		2.4			
V_L	Logic low input voltage				0.4		V
		–40°C ≤ T_A ≤ 85°C				0.2	
I_H	Logic high input current				7		µA
		–40°C ≤ T_A ≤ 85°C				15	
I_L	Logic low input current				0.1		µA
I_{SC}	Short circuit current	V_{IN} = 3.3 V, V_{OUT} = 0			15		mA
			–40°C ≤ T_A ≤ 85°C	6		30	
		V_{IN} = 12 V, V_{OUT} = 0			17		
			–40°C ≤ T_A ≤ 85°C	6		30	
Hyst	Thermal hysteresis (5)	–40°C ≤ T_A ≤ 125°C			0.5		mV/V
ΔV_{OUT}	Long term stability (6)	1000 hrs @ 25°C			100		ppm
3 V, 3.3 V, 4.096 V, AND 5 V							
V_{OUT}	Output voltage initial accuracy LM4120A-3.000 LM4120A-3.300 LM4120A-4.096 LM4120A-5.000					±0.2%	
	LM4120-3.000 LM4120-3.300 LM4120-4.096 LM4120-5.000					±0.5%	
TCV_{OUT}/°C	Temperature coefficient	–40°C ≤ T_A ≤ 125°C			14	50	ppm/°c
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation	(V_{OUT} + 1 V) ≤ V_{IN} ≤ 12 V			0.0007	0.008	%/V
			–40°C ≤ T_A ≤ 85°C			0.01	
$\Delta V_{OUT}/\Delta I_{LOAD}$	Load regulation	0 mA ≤ I_{LOAD} ≤ 1 mA			0.03	0.08	%/mA
			–40°C ≤ T_A ≤ 85°C			0.17	
		1 mA ≤ I_{LOAD} ≤ 5 mA			0.01	0.04	
			–40°C ≤ T_A ≤ 85°C			0.1	
		–1 mA ≤ I_{LOAD} ≤ 0 mA			0.04	0.12	
		–5 mA ≤ I_{LOAD} ≤ –1 mA			0.01		
$V_{IN}-V_{OUT}$	Dropout voltage (3)	I_{LOAD} = 0 mA			45	65	mV
			–40°C ≤ T_A ≤ 85°C			80	
		I_{LOAD} = 1 mA			120	150	
			–40°C ≤ T_A ≤ 85°C			180	
		I_{LOAD} = 5 mA			180	210	
			–40°C ≤ T_A ≤ 85°C			250	

(4) Output noise voltage is proportional to V_{OUT}. V_N for other voltage option is calculated using (V_N(1.8 V) / 1.8) × V_{OUT}.
V_N (2.5 V) = (36 μV_{PP} / 1.8) × 2.5 = 46 μV_{PP}.
(5) Thermal hysteresis is defined as the change in 25°C output voltage before and after exposing the device to temperature extremes.
(6) Long term stability is change in V_{REF} at 25°C measured continuously during 1000 hours.

Electrical Characteristics (continued)

unless otherwise specified, V_{IN} = 3.3 V, I_{LOAD} = 0, C_{OUT} = 0.01 µF, $T_A = T_j$ = 25°C.

PARAMETER		TEST CONDITIONS		MIN (1)	TYP (2)	MAX (1)	UNIT
3 V, 3.3 V, 4.096 V, AND 5 V (continued)							
V_N	Output noise voltage (4)	0.1 Hz to 10 Hz			20		μV_{PP}
		10 Hz to 10 kHz			36		
I_S	Supply current				160	250	µA
		–40°C ≤ T_A ≤ 85°C				275	
I_{SS}	Power-down supply current	Enable = 0.4 V –40°C ≤ T_J ≤ 85°C Enable = 0.2 V				1	µA
			–40°C ≤ T_A ≤ 85°C			2	
V_H	Logic high input voltage				2.4		V
		–40°C ≤ T_A ≤ 85°C		2.4			
V_L	Logic low input voltage				0.4		V
		–40°C ≤ T_A ≤ 85°C				0.2	
I_H	Logic high input current				7		µA
		–40°C ≤ T_A ≤ 85°C				15	
I_L	Logic low input current				0.1		µA
I_{SC}	Short circuit current	V_{OUT} = 0			15		mA
			–40°C ≤ T_A ≤ 85°C	6		30	
		V_{IN} = 12 V, V_{OUT} = 0			17		
			–40°C ≤ T_A ≤ 85°C	6		30	
Hyst	Thermal hysteresis (5)	–40°C ≤ T_A ≤ 125°C			0.5		mV/V
ΔV_{OUT}	Long term stability (6)	1000 hours @ 25°C			100		ppm

6.6 Typical Characteristics

unless otherwise specified, V_{IN} = 3.3 V, V_{OUT} = 2.5 V, I_{LOAD} = 0, C_{OUT} = 0.022 µF, T_A = 25°C, and V_{EN} = V_{IN}

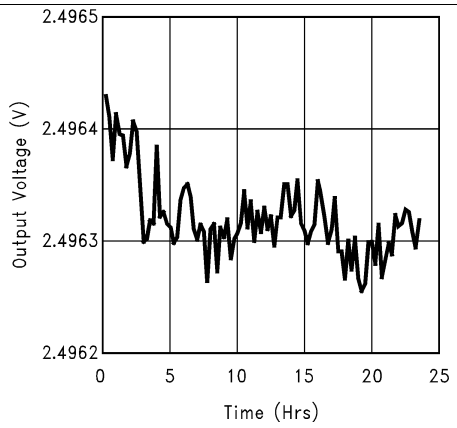


Figure 1. Long Term Drift

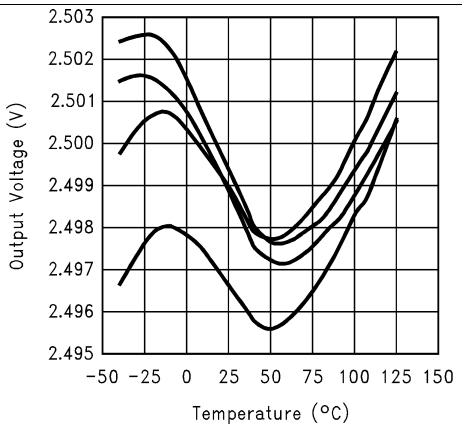


Figure 2. Typical Temperature Drift

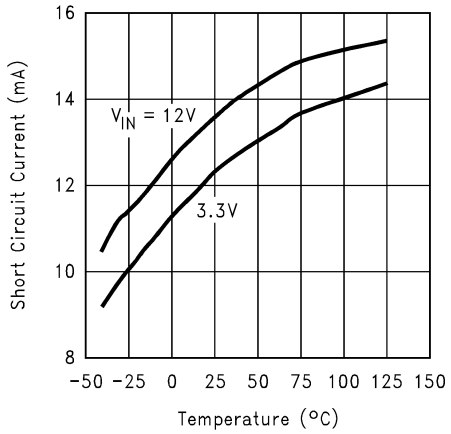


Figure 3. Short Circuit Current vs Temperature

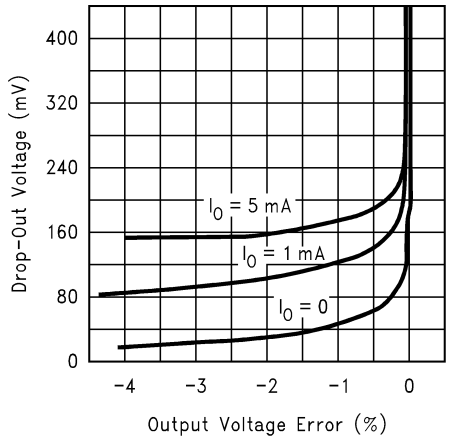


Figure 4. Dropout Voltage vs Output Error

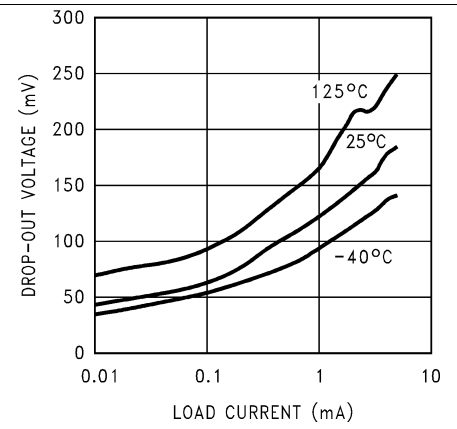


Figure 5. Dropout Voltage vs Load Current

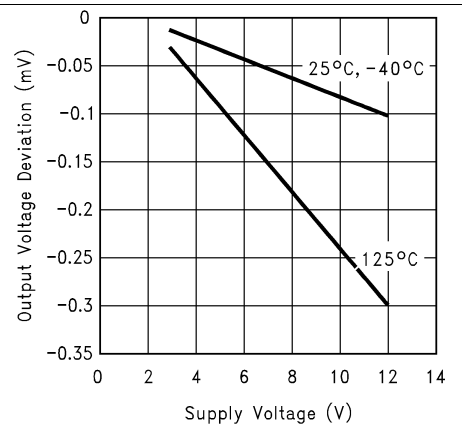


Figure 6. Line Regulation

Typical Characteristics (continued)

unless otherwise specified, V_{IN} = 3.3 V, V_{OUT} = 2.5 V, I_{LOAD} = 0, C_{OUT} = 0.022 µF, T_A = 25°C, and V_{EN} = V_{IN}

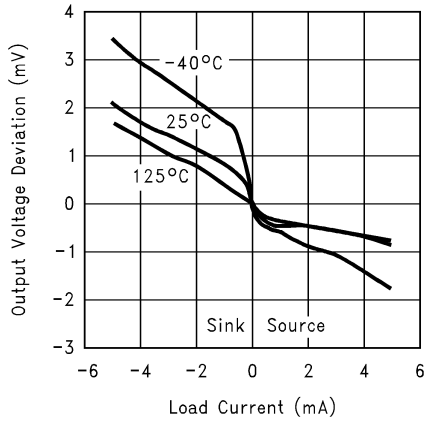


Figure 7. Load Regulation

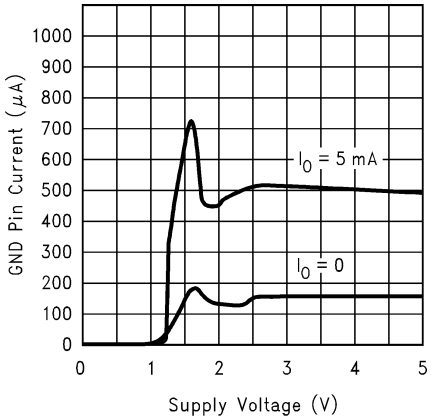


Figure 8. GND Pin Current

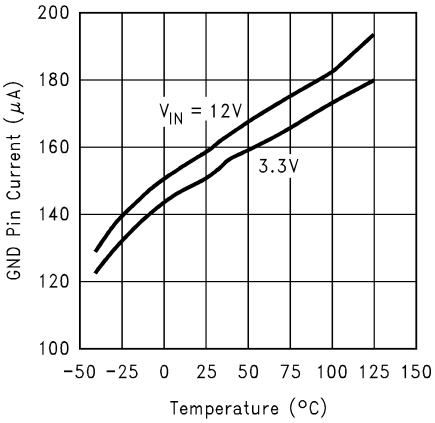


Figure 9. GND Pin Current at No Load vs Temperature

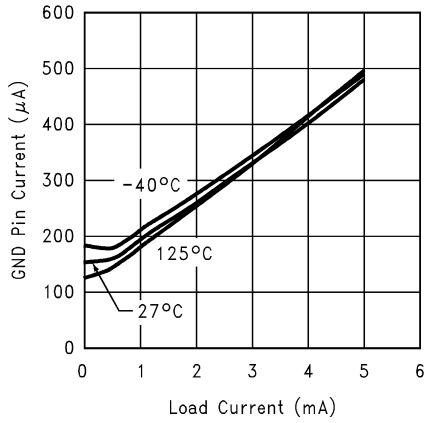


Figure 10. GND Pin Current vs Load

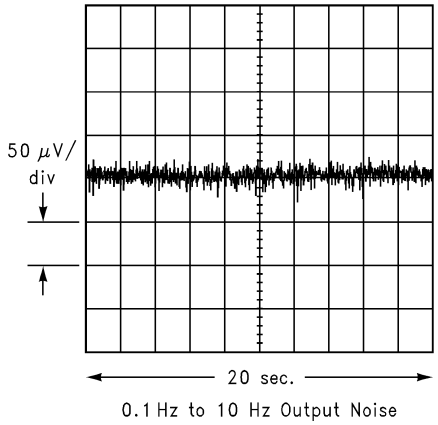


Figure 11. 0.1-Hz to 10-Hz Output Noise

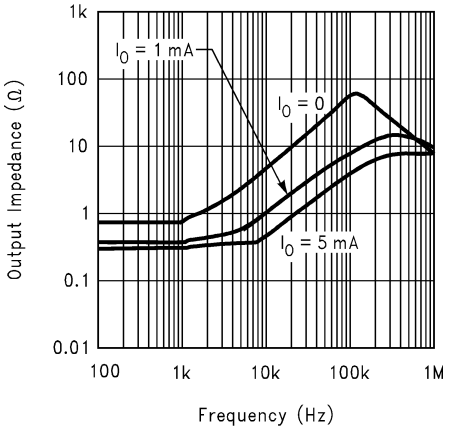


Figure 12. Output Impedance vs Frequency

Typical Characteristics (continued)

unless otherwise specified, V_{IN} = 3.3 V, V_{OUT} = 2.5 V, I_{LOAD} = 0, C_{OUT} = 0.022 µF, T_A = 25°C, and V_{EN} = V_{IN}

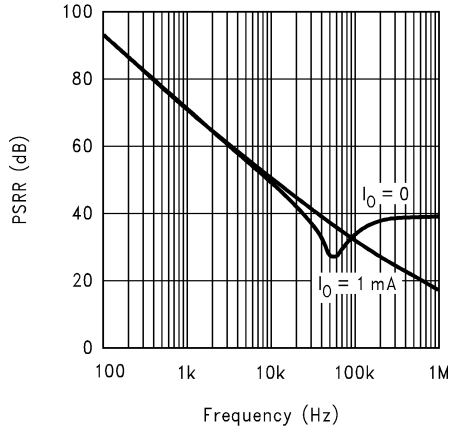


Figure 13. PSRR vs Frequency

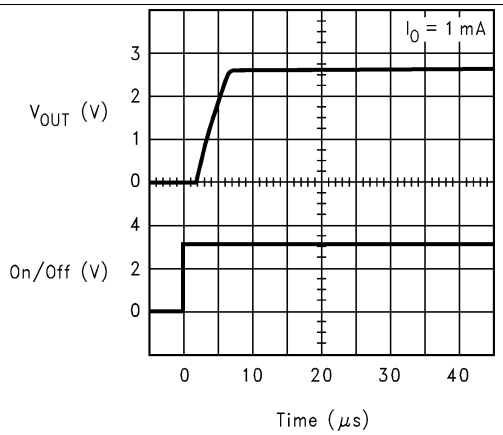


Figure 14. Enable Response

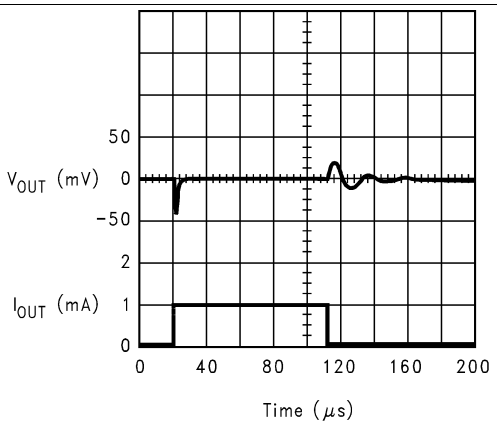


Figure 15. Load Step Response

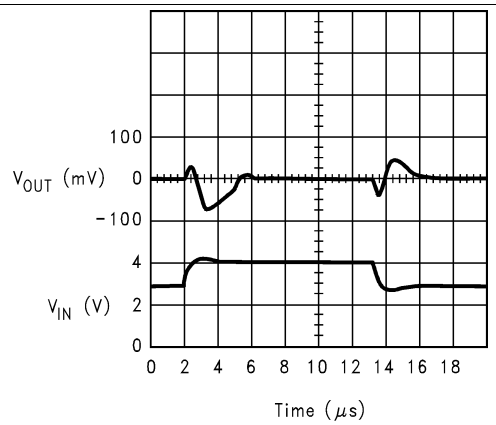


Figure 16. Line Step Response

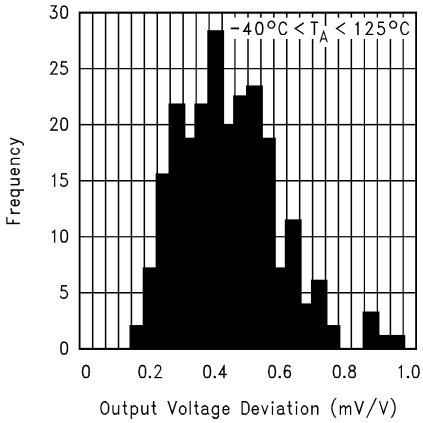


Figure 17. Thermal Hysteresis

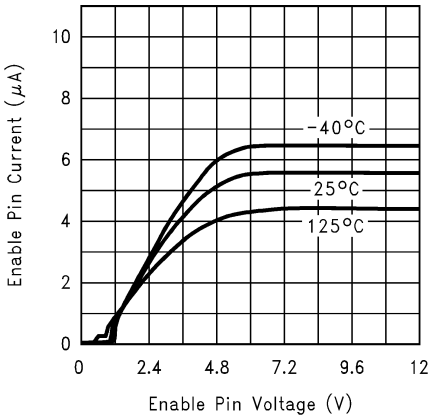


Figure 18. Enable Pin Current

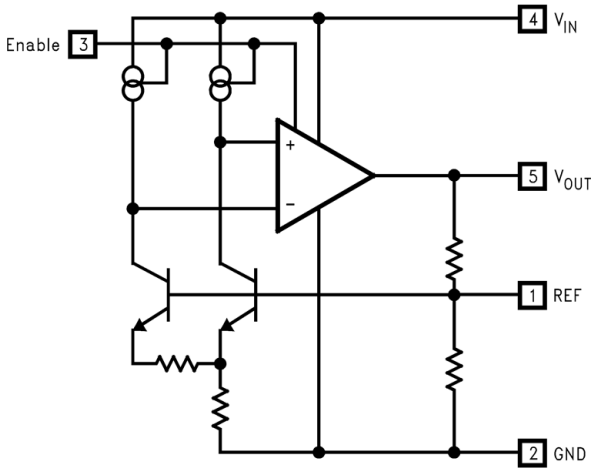
7 Detailed Description

7.1 Overview

The LM4120 device is a precision bandgap voltage reference available in seven different voltage options with up to 5-mA current source and sink capability. This series reference can operate with input voltages from 2 V to 12 V while consuming 160-µA (typical) supply current. In power-down mode, device current drops to less than 2 µA. The LM4120 is available in two grades, A and Standard.

The best grade devices (A) have an initial accuracy of 0.2% with a TEMPCO of 50 ppm/°C ensured from −40°C to 125°C.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Enable

The ENABLE analog input pin with limited hysteresis generally requires 6 µA (typical) of current to start up the part. During normal operation, the Enable pin must be connected to the VIN pin. There is a minimum slew rate on this pin of about 0.003 V/µs to prevent glitches on the output. All of these conditions can easily be met with ordinary CMOS or TTL logic. The Enable pin can also be used to remotely operate the LM4120 by pulling up the Enable pin voltage to the input voltage level.

When remotely shutting down the LM4120, the Enable pin must be pulled down to the ground. Floating this pin is not recommended.

7.3.2 Reference

The REF pin must remain unconnected in all cases. The reference pin is sensitive to noise, and capacitive loading. Therefore, during the PCB layout care must be taken to keep this pin isolated as much as possible.

7.4 Device Functional Modes

Table 1 describes the functional modes of the LM4120.

Table 1. Enable Pin Mode Summary

ENABLE PIN CONNECTION	LOGIC STATE	DESCRIPTION
EN = VIN	1	Normal Operation. LM4120 starts up.
EN = GND	0	LM4120 in shutdown mode

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The standard application circuit for the LM4120 is shown in Figure 29. The device is designed to be stable with ceramic output capacitors in the range of 0.022 µF to 0.047 µF. The minimum required output capacitor is 0.022 µF. These capacitors typically have an ESR of about 0.1 Ω to 0.5 Ω. Smaller ESR can be tolerated, but larger ESR cannot be tolerated. The output capacitor can be increased to improve load transient response, up to about 1 µF. However, values above 0.047 µF must be tantalum. With tantalum capacitors in the 1-µF range, a small capacitor between the output and the reference pin is required. This capacitor will typically be in the 50-pF range. Care must be taken when using output capacitors of 1 µF or larger. These applications must be thoroughly tested over temperature, line, and load.

An input capacitor is typically not required. However, a 0.1-µF ceramic can be used to help prevent line transients from entering the LM4120. Larger input capacitors must be tantalum or aluminum.

The reference pin is sensitive to noise, and capacitive loading. Therefore, the PCB layout must isolate this pin as much as possible.

The enable pin is an analog input with very little hysteresis. About 6 µA into this pin is required to turn the part on, and it must be taken close to GND to turn the part off (see *Electrical Characteristics* for thresholds). If the shutdown feature is not required, then this pin can safely be connected directly to the input supply.

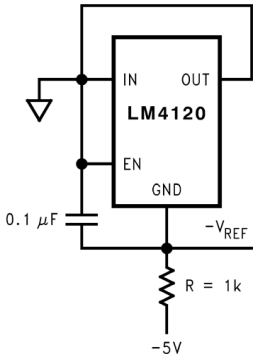


Figure 19. Voltage Reference With Negative Output Circuit

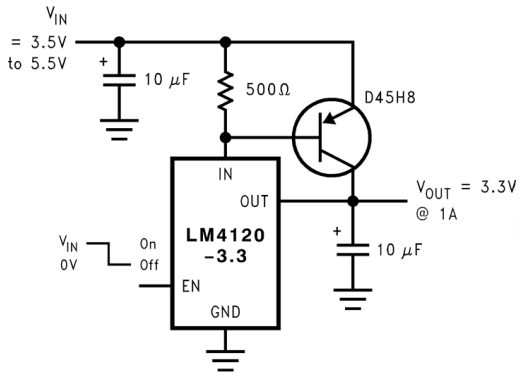


Figure 20. Precision High-Current Low-Dropout Regulator Circuit

Application Information (continued)

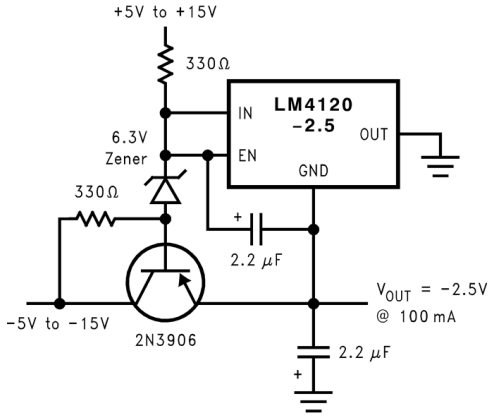


Figure 21. Precision High-Current Negative Voltage Regulator Circuit

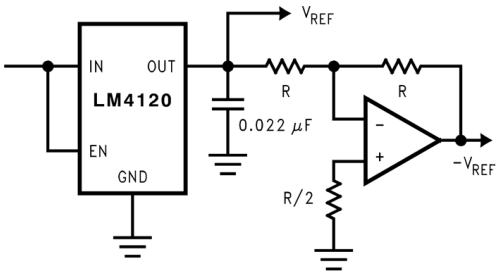


Figure 22. Voltage Reference With Complimentary Output Circuit

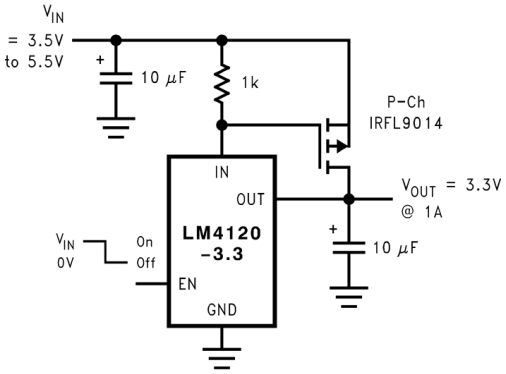


Figure 23. Precision High-Current Low-Dropout Regulator Circuit

Application Information (continued)

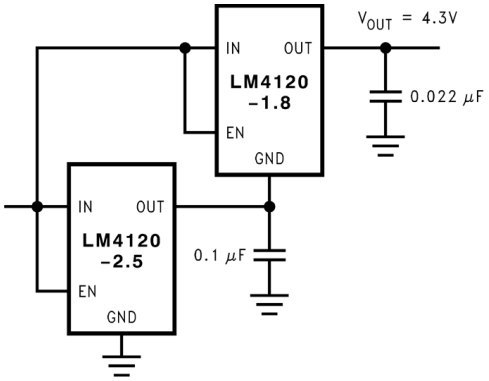


Figure 24. Stacking Voltage References Circuit

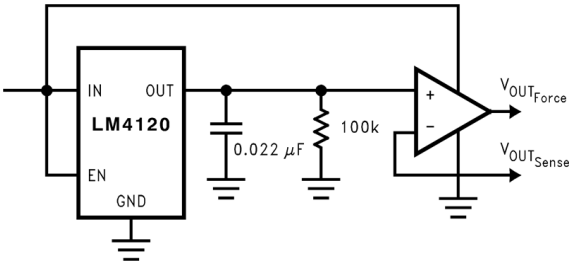


Figure 25. Precision Voltage Reference With Force and Sense Output Circuit

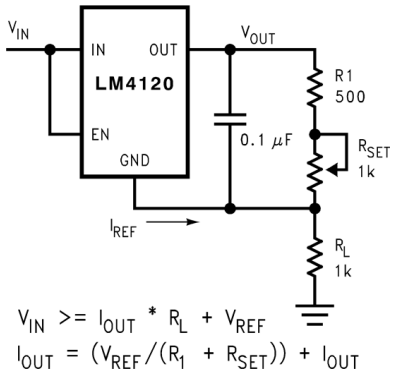


Figure 26. Programmable Current Source Circuit

Application Information (continued)

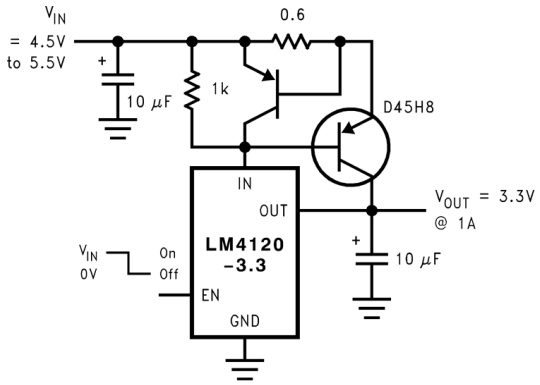


Figure 27. Precision Regulator With Current Limiting Circuit

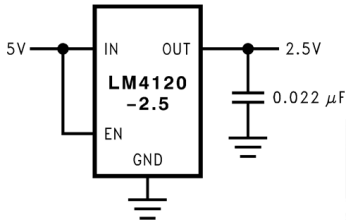


Figure 28. Power Supply Splitter Circuit

8.2 Typical Application

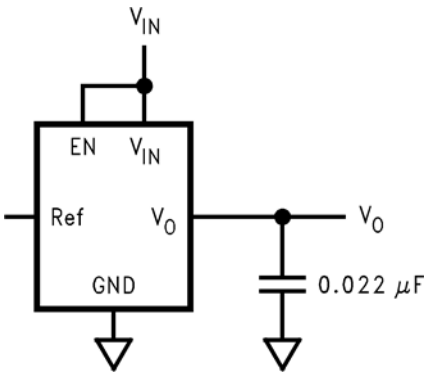


Figure 29. Standard Application Circuit

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 2 as the input parameters.

Table 2. Design Parameters

PARAMETER	EXAMPLE VALUE
Output Voltage VOUT	1.8 V, 2.048 V, 2.5 V, 3 V, 3.3 V, 4.096 V, 5 V
Input Voltage Range VIN	VOUT 120 mV to 12 V
Load Current	1 mA (typical)

8.2.2 Detailed Design Procedure

8.2.2.1 Input Capacitors

Although not always required, an input capacitor is recommended. A supply bypass capacitor on the input assures that the reference is working from a source with low impedance, which improves stability. A bypass capacitor can also improve transient response by providing a reservoir of stored energy that the reference can utilize in case where the load current demand suddenly increases. The value used for CIN may be used without limit.

8.2.2.2 Output Capacitors

The LM4120 may require a 0.022-µF to 1-µF output capacitor for loop stability (compensation) as well as transient response. During the sudden changes in load current demand, the output capacitor must source or sink current during the time it takes the control loop of the LM4120 to respond.

8.2.3 Application Curves

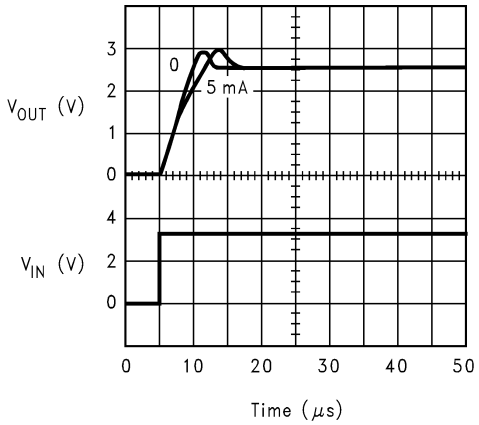


Figure 30. Start-Up Response

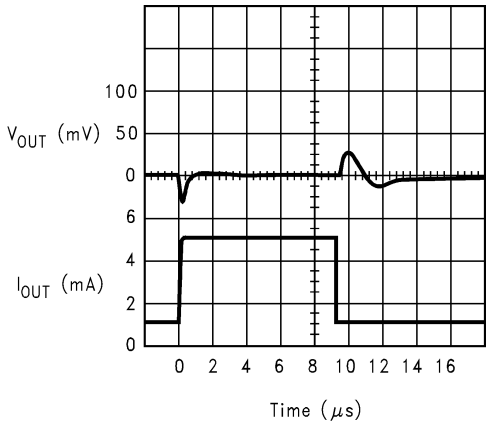


Figure 31. Load Step Response

9 Power Supply Recommendations

Noise on the power-supply input can effect the output noise, but can be reduced by using an optional bypass capacitor between the input pin and the ground. A ceramic input capacitor more than 0.1 µF or higher can be used for that purpose.

10 Layout

10.1 Layout Guidelines

The mechanical stress due to PC board mounting can cause the output voltage to shift from its initial value. The center of a PC board generally has the highest mechanical and thermal expansion stress. Mounting the device near the edges or the corners of the board where mechanical stress is at its minimum. References in SOT packages are generally less prone to assembly stress than devices in Small Outline (SOIC) package.

A mechanical isolation of the device by creating an island by cutting a U shape slot (U - SLOT) on the PCB while mounting the device helps in reducing the impact of the PC board stresses on the output voltage of the reference. This approach would also provide some thermal isolation from the rest of the circuit.

Figure 32 shows a recommended printed board layout for LM4120 along with an in-set diagram. The in-set diagram exhibits a slot cut on three sides of the reference IC, which provides a relief to the IC from external PCB stress.

10.2 Layout Example

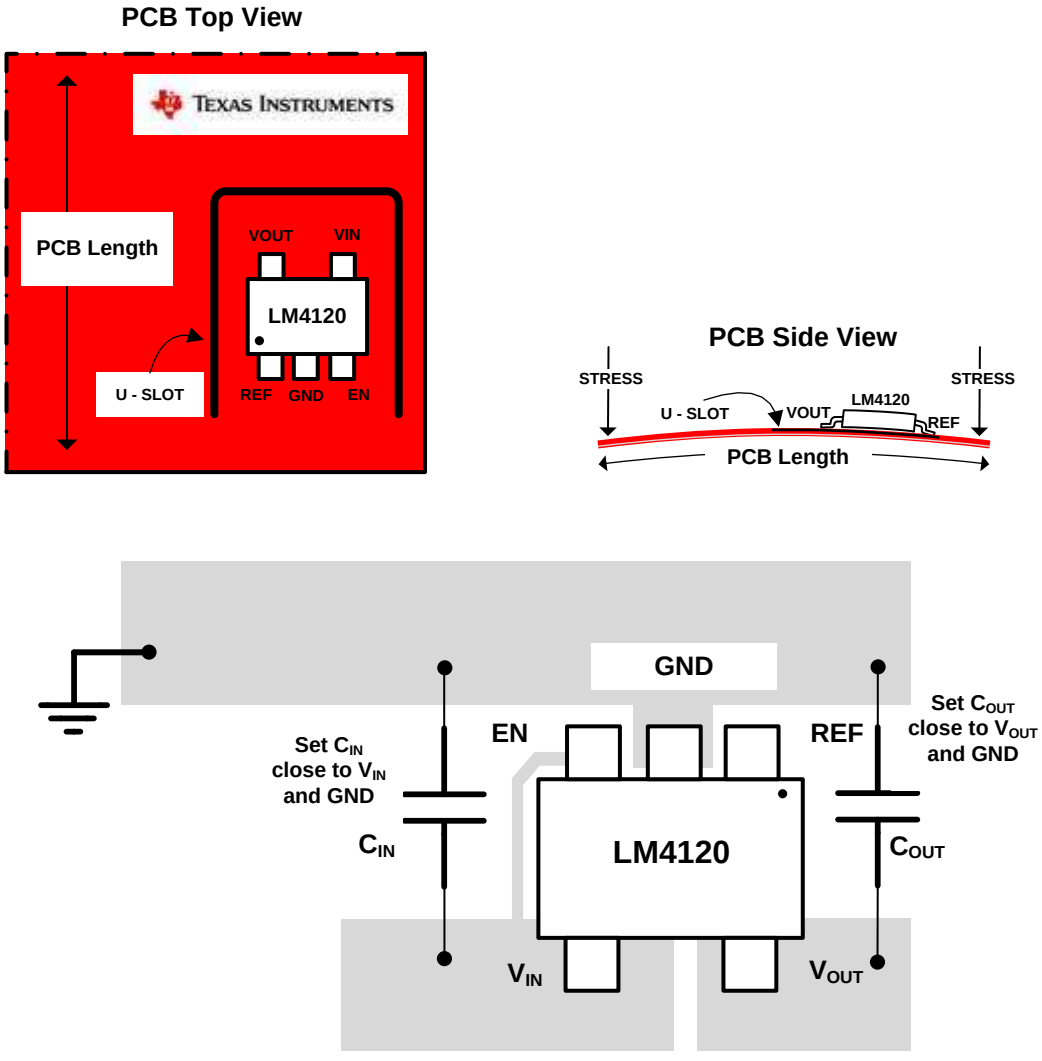


Figure 32. Typical Layout Example With LM4120

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM4120AIM5-1.8/NOPB	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 85	R21A	
LM4120AIM5-2.0/NOPB	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 85	R14A	
LM4120AIM5-2.5/NOPB	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 85	R08A	
LM4120AIM5-3.3/NOPB	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 85	R16A	
LM4120AIM5-4.1/NOPB	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 85	R17A	
LM4120AIM5X-1.8/NOPB	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 85	R21A	
LM4120AIM5X-2.5/NOPB	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 85	R08A	
LM4120AIM5X-3.3/NOPB	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 85	R16A	
LM4120AIM5X-4.1/NOPB	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 85	R17A	
LM4120IM5-1.8/NOPB	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 85	R21B	
LM4120IM5-2.0/NOPB	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 85	R14B	
LM4120IM5-2.5/NOPB	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 85	R08B	
LM4120IM5-3.0/NOPB	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 85	R15B	
LM4120IM5-3.3/NOPB	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 85	R16B	
LM4120IM5-4.1/NOPB	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 85	R17B	
LM4120IM5-5.0/NOPB	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 85	R18B	
LM4120IM5X-1.8/NOPB	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 85	R21B	
LM4120IM5X-2.0/NOPB	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 85	R14B	
LM4120IM5X-2.5/NOPB	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 85	R08B	
LM4120IM5X-3.0/NOPB	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 85	R15B	
LM4120IM5X-3.3/NOPB	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 85	R16B	
LM4120IM5X-4.1/NOPB	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 85	R17B	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

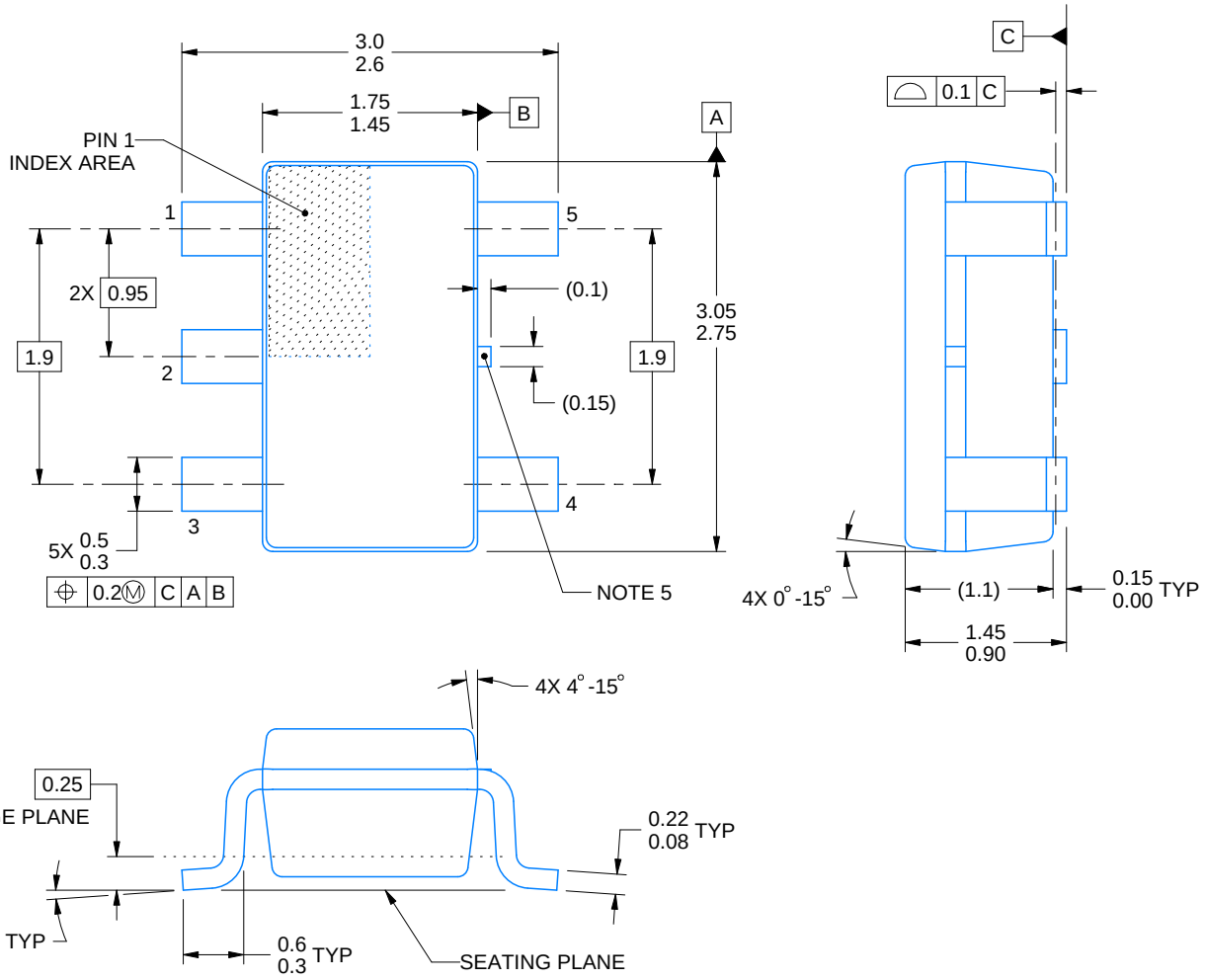
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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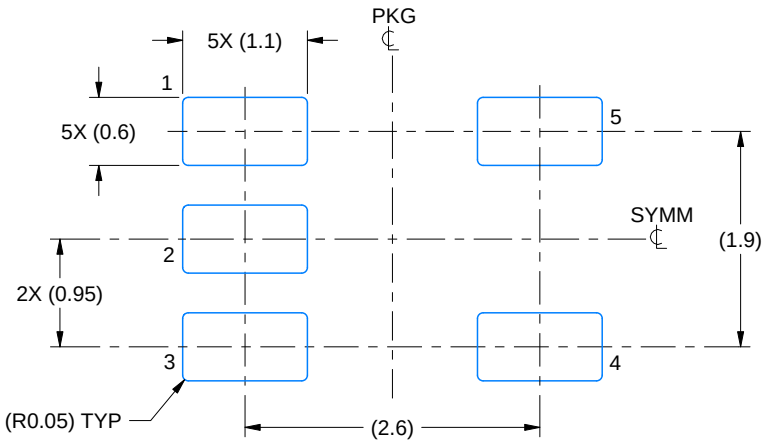
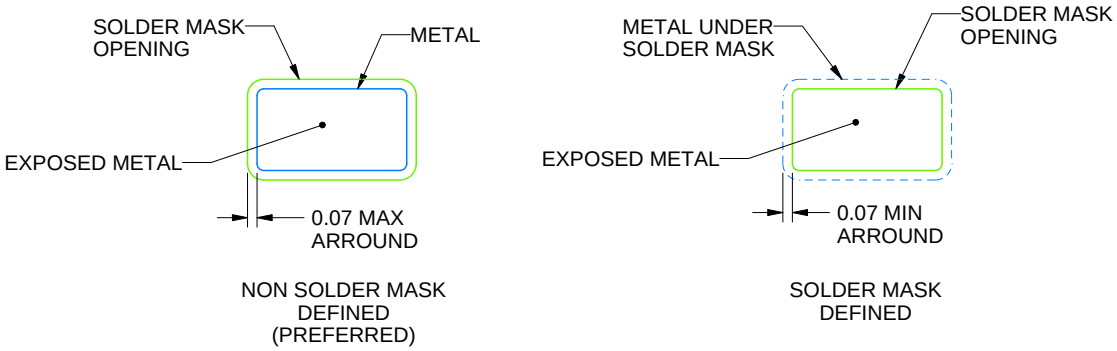
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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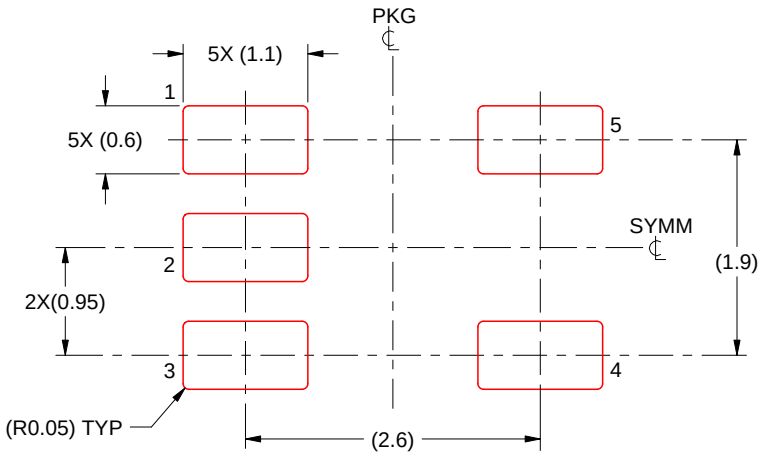
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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