

## LMS33460 3-V Undervoltage Detector

### 1 Features

- Ultra-Low Power
- 3-V Detection
- Input Voltage From 0.8 V to 7 V
- Open-Drain Output
- Ultra-Small 5-Pin SC70 Package
- Extended Temperature Range (–40°C to 85°C)
- Ultra-Low Quiescent Current (1  $\mu$ A Typical)

### 2 Applications

- Low Battery Voltage Detectors
- Power Fail Indicators
- Processor Reset Generators
- Battery Backup Controls
- Battery-Operated Equipment
- Hand-Held Instruments
- Undervoltage Detectors

### 3 Description

The LMS33460 device is an undervoltage detector with a 3-V threshold and extremely low power consumption. The LMS33460 is specifically designed to accurately monitor power supplies. It is especially suited to battery-powered systems where low quiescent current and small size are required. This IC generates an active output whenever the input voltage drops below 3 V.

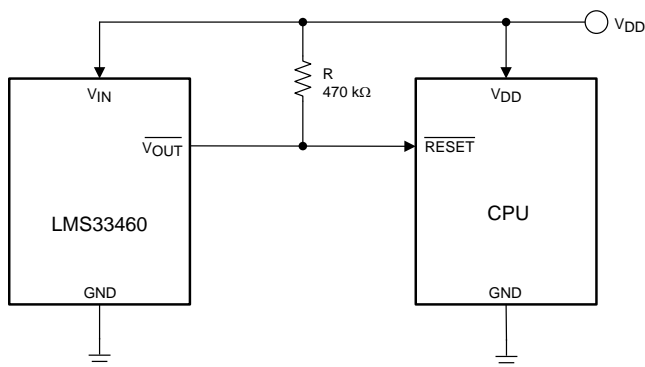
This part uses a precision on-chip voltage reference and a comparator to measure the input voltage. Built-in hysteresis helps to prevent erratic operation in the presence of noise. The UVD is available in the ultra-miniature 5-pin SC70 package.

#### Device Information<sup>(1)</sup>

| PART NUMBER | PACKAGE  | BODY SIZE (NOM)   |
|-------------|----------|-------------------|
| LMS33460    | SC70 (5) | 2.00 mm x 1.25 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Typical Application



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#### SC70 Package



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

### Changes from Revision D (April 2013) to Revision E

**Page**

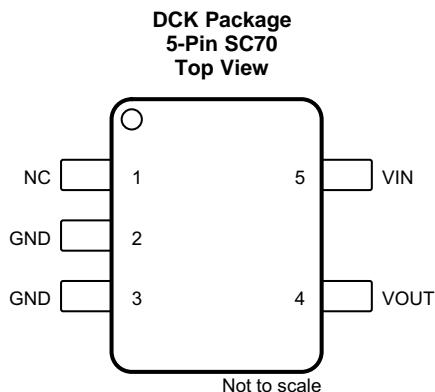
|   |                                     |
|---|-------------------------------------|
| <ul style="list-style-type: none"> <li>• Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i>, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section. .... 1</li> <li>• Deleted <i>Ordering Information</i> table; see POA at the end of the data sheet..... 1</li> <li>• Added <i>Thermal Information</i> table ..... 4</li> <li>• Changed <math>R_{\theta JA}</math> value From: 478 To: 275.5 ..... 4</li> </ul> | <p>1</p> <p>1</p> <p>4</p> <p>4</p> |
|---|-------------------------------------|

### Changes from Revision C (April 2013) to Revision D

**Page**

|  |          |
|--|----------|
| <ul style="list-style-type: none"> <li>• Changed layout of National Semiconductor Data Sheet to TI format ..... 1</li> </ul> | <p>1</p> |
|--|----------|

## 5 Pin Configuration and Functions



### Pin Functions

| PIN  |     | I/O | DESCRIPTION   |
|------|-----|-----|---|
| NAME | NO. |     |   |
| GND  | 2   | —   | Internally connected to ground. Can be left floating or connected to GND (pin 3). |
| GND  | 3   | —   | Ground  |
| NC   | 1   | —   | No connection   |
| VIN  | 5   | I   | Input supply  |
| VOUT | 4   | O   | Voltage output  |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                                  | MIN | MAX | UNIT |
|----------------------------------|-----|-----|------|
| Input voltage to GND             |     | 8   | V    |
| Output voltage to GND            |     | 8   | V    |
| Output continuous output current |     | 30  | mA   |
| Vapor phase IR convection reflow |     | 240 | °C   |
| Junction temperature, $T_J$      |     | 150 | °C   |
| Storage temperature, $T_{stg}$   | -65 | 150 | °C   |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

|             |                         | VALUE   | UNIT  |
|-------------|-------------------------|---|-------|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup> | ±2500 |
|             |                         | Machine model   | ±200  |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

|       | MIN | MAX | UNIT |
|-------|-----|-----|------|
| $T_J$ | -40 | 85  | °C   |

## 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |  | LMS33460   |      |
|-------------------------------|--|------------|------|
|                               |  | DCK (SC70) |      |
|                               |  | 5 PINS     |      |
|                               |  |            | UNIT |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance       | 275.5      | °C/W |
| $R_{\theta JC(top)}$          | Junction-to-case (top) thermal resistance    | 102.5      | °C/W |
| $R_{\theta JB}$               | Junction-to-board thermal resistance         | 54         | °C/W |
| $\psi_{JT}$                   | Junction-to-top characterization parameter   | 2.7        | °C/W |
| $\psi_{JB}$                   | Junction-to-board characterization parameter | 53.3       | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

$T_J = 25^\circ\text{C}$  (unless otherwise noted)

| PARAMETER                 |  | TEST CONDITIONS                                     | MIN   | TYP       | MAX   | UNIT          |
|---------------------------|--|---|-------|-----------|-------|---------------|
| $V_{DET}$                 | Detector threshold                                 | $V_{IN}$ falling                                    | 2.85  | 3         | 3.15  | V             |
| $V_{HYS}$                 | Detector voltage hysteresis                        | $V_{IN}$ rising                                     | 0.095 | 0.155     | 0.215 | V             |
| $I_{IN}$                  | Input supply current                               | $V_{IN} = 2.87\text{ V}$                            |       | 1         | 2.2   | $\mu\text{A}$ |
|                           |  | $V_{IN} = 4.7\text{ V}$                             |       | 1.2       | 3.6   | $\mu\text{A}$ |
|                           |  | $V_{IN} = 7\text{ V}^{(1)}$                         |       | 25        | 200   | $\mu\text{A}$ |
| $V_{IN(MAX)}$             | Maximum operating voltage                          |   |       |           | 7     | V             |
| $V_{IN(MIN)}$             | Minimum operating voltage                          |   |       | 0.7       | 1.1   | V             |
|                           |  | $T_J = -40^\circ\text{C}$ to $85^\circ\text{C}$     |       | 1         | 1.3   |               |
| $I_{OUT(LOW)}$            | Output current low                                 | $V_{OUT} = 0.05\text{ V}$ , $V_{IN} = 1.1\text{ V}$ | 0.01  | 0.6       |       | mA            |
|                           |  | $V_{OUT} = 0.5\text{ V}$ , $V_{IN} = 1.5\text{ V}$  | 2     | 11        |       |               |
| $t_{PDHL}$                | Output delay time (output transition high to low ) | $C_L = 10\text{ pF}$ , $R_L = 470\text{ k}\Omega$   |       | 130       | 200   | $\mu\text{s}$ |
| $\Delta V_{DET}/\Delta T$ | Detect voltage temperature coefficient             | $T_J = -40^\circ\text{C}$ to $85^\circ\text{C}$     |       | $\pm 120$ |       | PPM/°C        |

(1) Quiescent current increases substantially above 5.5 V, but is very low in the normal range below 5.5 V.

## 6.6 Typical Characteristics

$T_A = 25^\circ\text{C}$ ,  $R_L = 470\text{ k}\Omega$ , and  $C_L = 10\text{ pF}$  (unless otherwise noted)

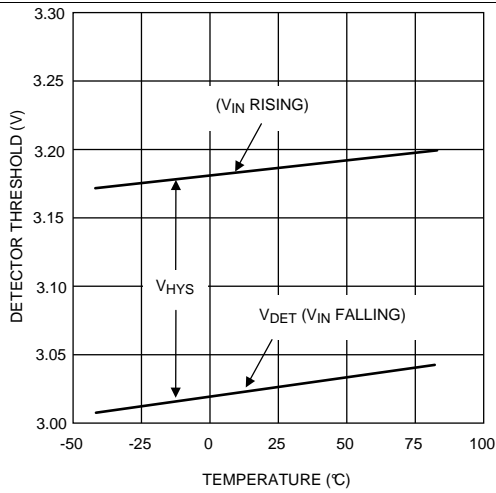


Figure 1. Detector Threshold vs Temperature

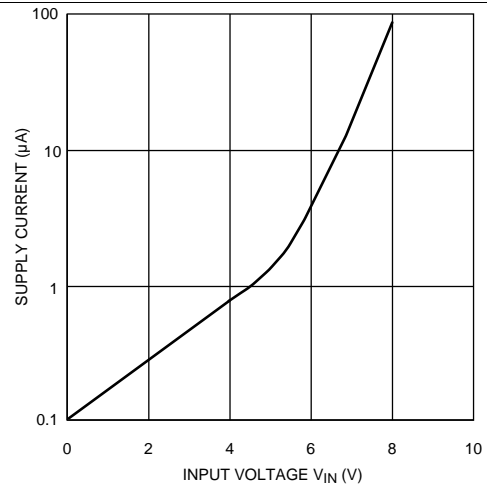


Figure 2. Supply Current vs Input Voltage

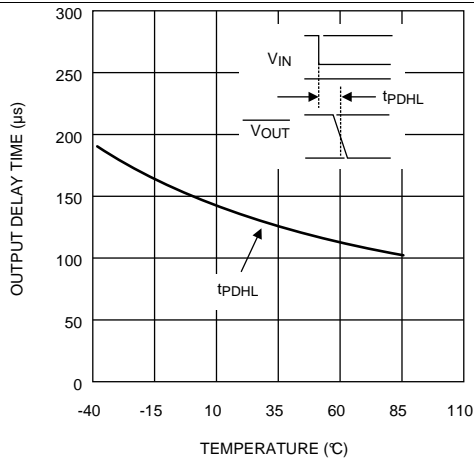


Figure 3. Propagation Delay Time ( $t_{PDHL}$ ) vs Temperature

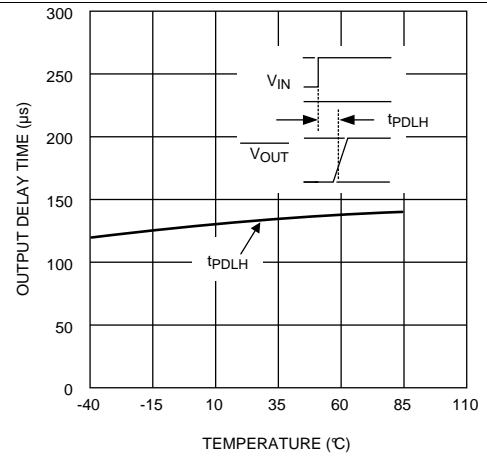


Figure 4. Propagation Delay Time ( $t_{PDLH}$ ) vs Temperature

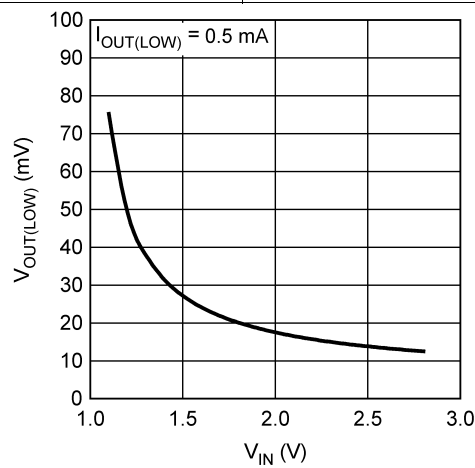


Figure 5.  $V_{OUT(LOW)}$  vs  $V_{IN}$

## 7 Detailed Description

### 7.1 Overview

The LMS33460 is a micropower undervoltage-sensing circuit with an open-drain output configuration, which requires a pull resistor.

The LMS33460 features a voltage reference, a comparator with precise thresholds and built-in hysteresis to prevent erratic reset operation.

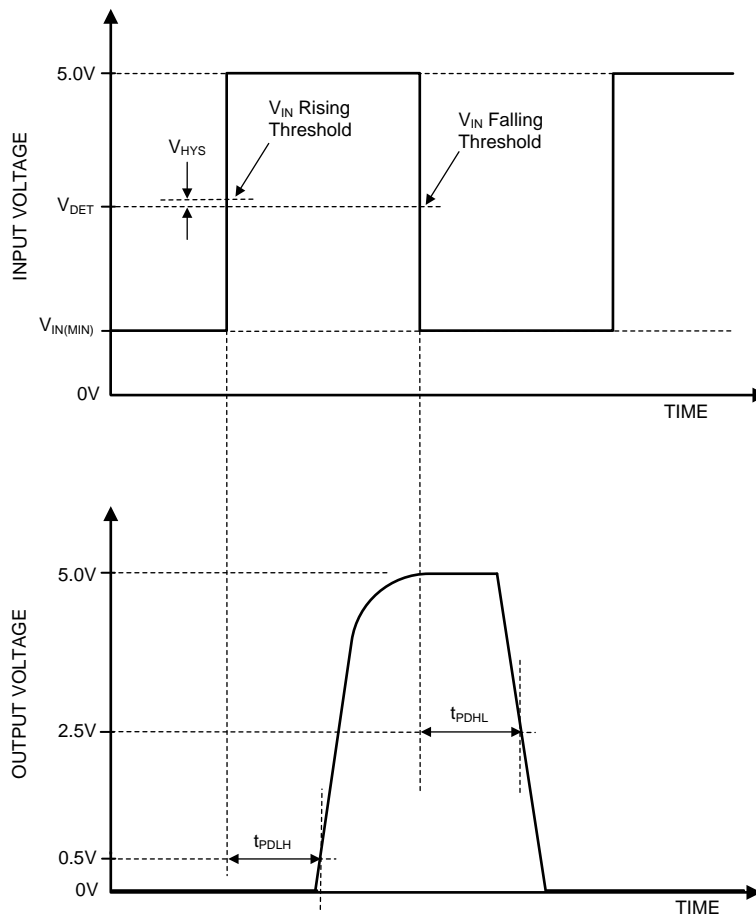
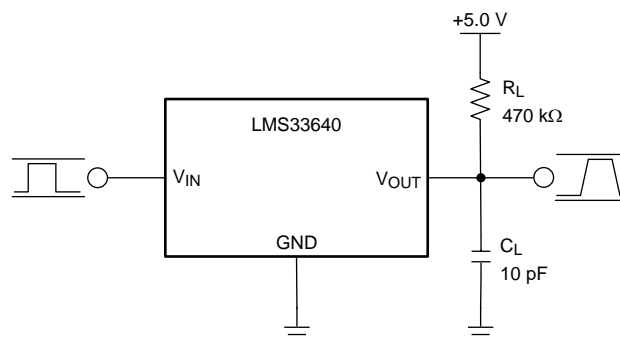


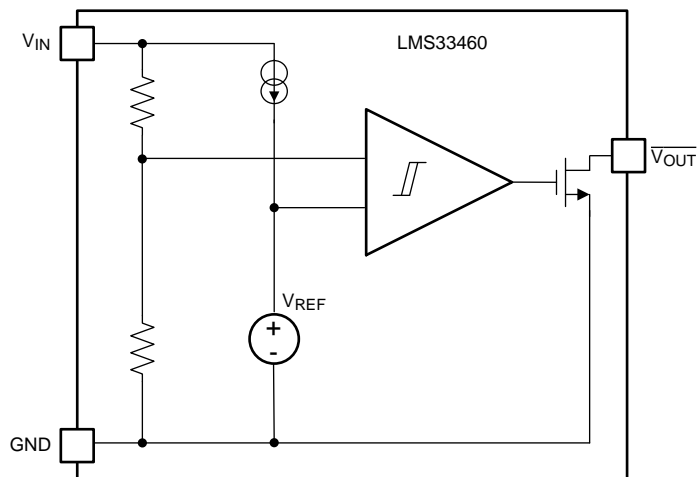
Figure 6. Propagation Delay Timing Diagram



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Figure 7. Propagation Delay Test Circuit

## 7.2 Functional Block Diagram



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## 7.3 Feature Description

The input supply ( $V_{IN}$ ) is the voltage that is being monitored and as it decreases past 3 V, the active-low output ( $V_{OUT}$ ) transitions to a logic low state. When  $V_{IN}$  rises above 3 V plus the built-in hysteresis,  $V_{OUT}$  returns to its original state of logic high. The LMS33460 has built-in hysteresis when the input supply is coming back up to help prevent erratic output operation when the input voltage crosses the threshold.

The LMS33460 is useful in a variety of applications that require low voltage detection and is suited for battery-powered systems where low quiescent current and small package size is required. It can also be used as a precision reset circuit for microcontroller applications.

## 7.4 Device Functional Modes

### 7.4.1 Start Up

As the input voltage ( $V_{IN}$ ) ramps up, the output ( $V_{OUT}$ ) remains logic low until  $V_{IN}$  reaches 3.15 V due to the built-in hysteresis (nominally 150 mV). After  $V_{IN}$  crosses that threshold,  $V_{OUT}$  remains logic high until  $V_{IN}$  drops below the 3-V threshold. The hysteresis only applies to the  $V_{IN}$  rising threshold.

## 8 Application and Implementation

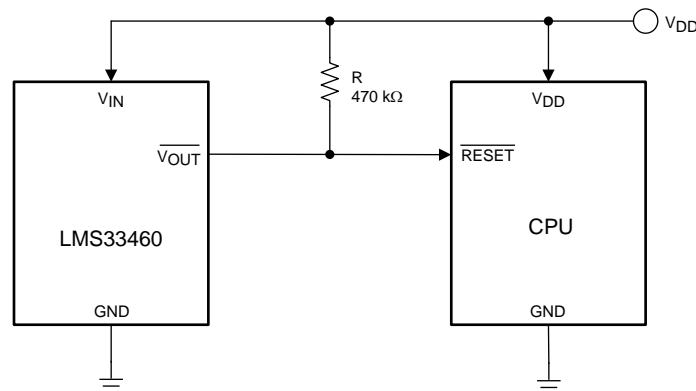
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

This device is ideal to use in battery-powered or microprocessor based systems and can be used as a low voltage indicator or reset circuit.

### 8.2 Typical Application



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**Figure 8. Typical Application Schematic**

#### 8.2.1 Design Requirements

For this design example, use the parameters listed in [Table 1](#) as the input parameters.

**Table 1. Design Parameters**

| PARAMETER                    | EXAMPLE VALUE |
|------------------------------|---------------|
| Input supply voltage maximum | 7 V           |
| V <sub>OUT</sub> maximum     | 7 V           |
| V <sub>OUT</sub> minimum     | 0 V           |
| Pullup resistor              | 470 kΩ        |

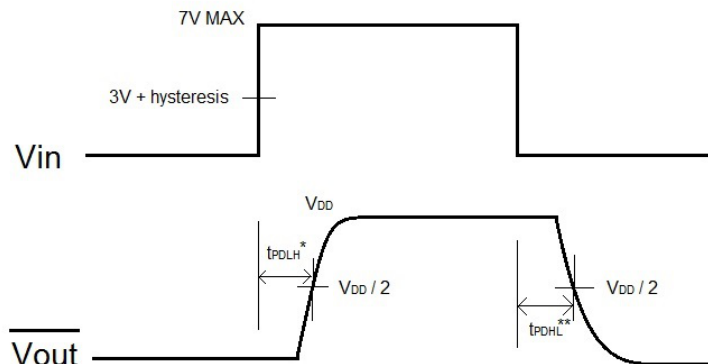
#### 8.2.2 Detailed Design Procedure

The LMS33460 is a very easy to use low voltage detector. All that required is the input supply voltage and a pullup resistor at the output. TI recommends 470 kΩ for the pullup resistor.



### 8.2.3 Application Curve

$R_L = 475\text{ k}\Omega$



\* See Figure 4 for tPDLH values

\*\* See Figure 3 for tPDHL values

**Figure 9. LMS33460 Turnon**

## 9 Power Supply Recommendations

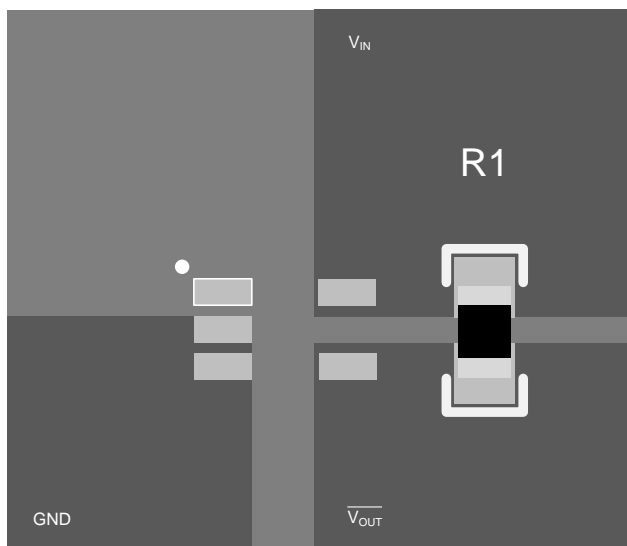
The input of the LMS33460 is designed to handle up to the recommended supply voltage of 7 V and remain in the recommended input voltage range during operation. No input capacitor is required.

## 10 Layout

### 10.1 Layout Guidelines

Place the output pullup resistor, and delay capacitor if used, as close as possible to the IC. Keep traces short between the IC and the components used at the output to ensure the timing delay is as accurate as possible.

### 10.2 Layout Example



**Figure 10. Layout Example Diagram**

## 11 Device and Documentation Support

### 11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

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### 11.3 Trademarks

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### 11.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 11.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---------|
| LMS33460MG/NOPB  | ACTIVE        | SC70         | DCK             | 5    | 1000        | RoHS & Green    | SN                                   | Level-1-260C-UNLIM   | -40 to 85    | C33                     | Samples |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LMS33460MG/NOPB | SC70         | DCK             | 5    | 1000 | 178.0              | 8.4                | 2.25    | 2.45    | 1.2     | 4.0     | 8.0    | Q3            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LMS33460MG/NOPB | SC70         | DCK             | 5    | 1000 | 208.0       | 191.0      | 35.0        |

# DCK0005A



## PACKAGE OUTLINE

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



4214834/E 06/2024

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

# EXAMPLE BOARD LAYOUT

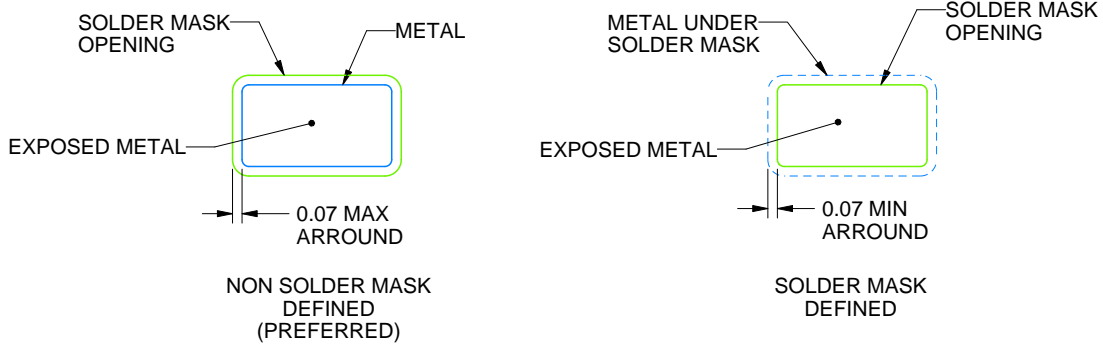
DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X



SOLDER MASK DETAILS

4214834/E 06/2024

NOTES: (continued)

- 7. Publication IPC-7351 may have alternate designs.
- 8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE: 18X

4214834/E 06/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.



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