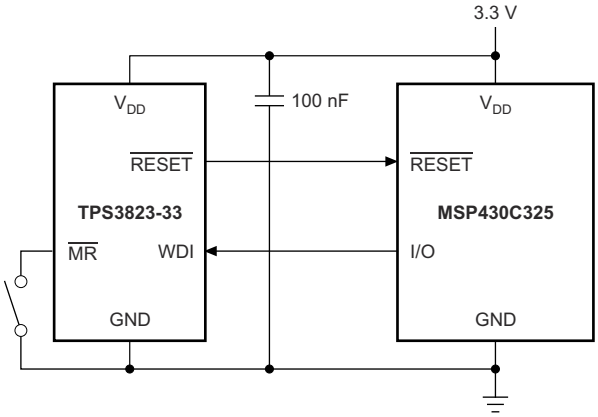
TPS382x Voltage Monitor With Watchdog Timer

1 Features

- Power-on reset generator with a fixed delay time of 200 ms (TPS3823, TPS3824, TPS3825, and TPS3828) or 25 ms (TPS3820)
- Manual reset input (TPS3820, TPS3823, TPS3825, and TPS3828)
- Reset output available in active-low (TPS3820, TPS3823, TPS3824, and TPS3825), active-high (TPS3824 and TPS3825), and open drain (TPS3828)
- Supply voltage supervision range: 2.5 V, 3 V, 3.3 V, 5 V
- Watchdog timer (TPS3820, TPS3823, TPS3824, and TPS3828)
- Supply current of 15 µA (typical)
- 5-pin SOT-23 package
- Temperature range: −40°C to 85°C (−40°C to 125°C for TPS3823A-33)

2 Applications

- DSPs, microcontrollers, or microprocessors
- Industrial equipment
- Programmable controls
- Automotive systems
- Portable and battery-powered equipment
- Intelligent instruments
- Wireless communications systems
- Notebook and desktop computers



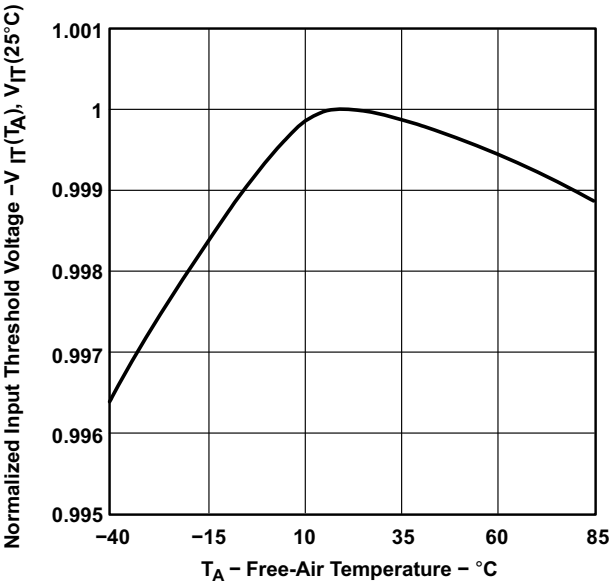
Typical Application Schematic

3 Description

The TPS382x family of supervisors provide circuit initialization and timing supervision, primarily for DSP and processor-based systems. During power on, $\overline{\text{RESET}}$ asserts when the supply voltage V_{DD} becomes greater than 1.1 V. Thereafter, the supply voltage supervisor monitors V_{DD} and keeps $\overline{\text{RESET}}$ active low as long as V_{DD} remains less than the threshold voltage, V_{IT-}. An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. The delay time, t_d, starts after V_{DD} has risen above the threshold voltage (V_{IT-} + V_{HYS}). When the supply voltage drops below the threshold voltage V_{IT-}, the output becomes active (low) again. No external components are required. All the devices of this family have a fixed-sense threshold voltage, V_{IT-}, set by an internal voltage divider. The TPS382x family also offers watchdog time out options of 200 ms (TPS3820) and 1.6 s (TPS3823, TPS3824, and TPS3828).

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TPS382x	SOT-23 (5)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Normalized Input Threshold Voltage vs Free-Air Temperature

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision M (July 2020) to Revision N (July 2022)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1

Changes from Revision L (January 2018) to Revision M (July 2020)	Page
• Added Operating free-air, TA for TPS3823A-33 only	5
• Added Electrical Characteristics for TPS3823A-33 only Table	7
• Added new typical performance curves Figure 7-9 through Figure 7-26	9

5 Device Comparison Table

DEVICE	RESET	$\overline{\text{RESET}}$	WDI	$\overline{\text{MR}}$
TPS3820		Push-pull	X	X
TPS3823		Push-pull	X	X
TPS3823A		Push-pull	X	X
TPS3824	Push-pull	Push-pull	X	
TPS3825	Push-pull	Push-pull		X
TPS3828		Open-drain	X	X

6 Pin Configuration and Functions

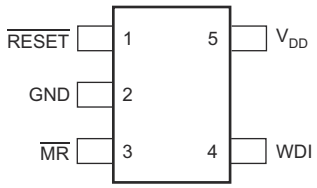


Figure 6-1. 5-Pin SOT-23 TPS3820, TPS3823, TPS3823A, TPS3828: DBV Package (Top View)

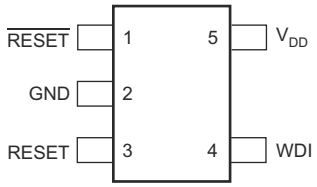


Figure 6-2. 5-Pin SOT-23 TPS3824: DBV Package (Top View)

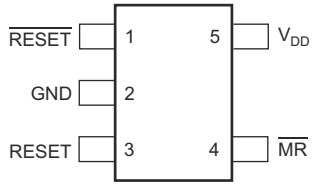


Figure 6-3. 5-Pin SOT-23 TPS3825: DBV Package (Top View)

Table 6-1. Pin Functions

PIN				I/O	DESCRIPTION
NAME	TPS3820, TPS3823, TPS3823A, TPS3828	TPS3824	TPS3825		
GND	2	2	2	—	Ground connection
$\overline{MR}$	3	—	4	I	Manual-reset input. Pull low to force a reset. $\overline{RESET}$ remains low as long as $\overline{MR}$ is low and for the time-out period after $\overline{MR}$ goes high. Leave unconnected or connect to V_{DD} when unused.
RESET	—	3	3	O	Active-high reset output. Either push-pull or open-drain output stage.
$\overline{RESET}$	1	1	1	O	Active-low reset output. Either push-pull or open-drain output stage.
V_{DD}	5	5	5	I	Supply voltage. Powers the device and monitors its own voltage.
WDI	4	4	—	I	Watchdog timer input. If WDI remains high or low longer than the time-out period, then reset is triggered. The timer clears when reset is asserted or when WDI sees a rising edge or a falling edge. If unused, the WDI connection must be high impedance to prevent it from causing a reset event.

7 Specifications

7.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
Voltage	V_{DD}	–0.3	6	V
	RESET, $\overline{\text{RESET}}$, MR, WDI	–0.3	(V_{DD} + 0.3)	
Current	Maximum low output, I_{OL}	–5	5	mA
	Maximum high output, I_{OH}	–5	5	
	Output range (V_O < 0 or V_O > V_{DD}), I_{OK}	–10	10	
	Continuous total power dissipation	See *Thermal Information*		
Temperature	Operating free-air, T_A	–40	85	°C
	Operating free-air, T_A for TPS3823A-33 only	–40	125	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted).

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	1.1		5.5	V
V_{IH}	High-level input voltage at $\overline{\text{MR}}$ and WDI	0.7 × V_{DD}			V
V_{IL}	Low-level input voltage			0.3 × V_{DD}	V
Δt/ΔV	Input transition rise and fall rate at $\overline{\text{MR}}$ or WDI			100	ns/V
T_A	Operating free-air temperature	–40		85	°C
T_A	Operating free-air temperature for TPS3823A-33 only	–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS382x DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	209.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	72.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	36.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.1	°C/W

7.4 Thermal Information (continued)

THERMAL METRIC(1)		TPS382x DBV (SOT-23) 5 PINS	UNIT
ψ_{JB}	Junction-to-board characterization parameter	35.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

over operating junction temperature range -40°C to 85°C (unless otherwise noted)

7.5 Electrical Characteristics

PARAMETER				TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$\overline{RESET}$	TPS382x-25	$V_{DD} = V_{IT-} + 0.2$ V, $I_{OH} = -20$ µA	0.8 × V_{DD}			V
			TPS382x-30 TPS382x-33 TPS382xA-33	$V_{DD} = V_{IT-} + 0.2$ V, $I_{OH} = -30$ µA				
			TPS382x-50	$V_{DD} = V_{IT-} + 0.2$ V $I_{OH} = -120$ µA	V_{DD} – 1.5 V			
		RESET	TPS3824-25 TPS3825-25	$V_{DD} \geq 1.8$ V, $I_{OH} = -100$ µA	0.8 × V_{DD}			
			TPS3824-30 TPS3825-30	$V_{DD} \geq 1.8$ V, $I_{OH} = -150$ µA				
			TPS3824-33 TPS3825-33					
			TPS3824-50 TPS3825-50					
V_{OL}	Low-level output voltage	RESET	TPS3824-25 TPS3825-25	$V_{DD} = V_{IT-} + 0.2$ V, $I_{OL} = 1$ mA			0.4	V
			TPS3824-30 TPS3825-30	$V_{DD} = V_{IT-} + 0.2$ V, $I_{OL} = 1.2$ mA				
			TPS3824-33 TPS3825-33					
			TPS3824-50 TPS3825-50	$V_{DD} = V_{IT-} + 0.2$ V, $I_{OL} = 3$ mA				
		$\overline{RESET}$	TPS382x-25	$V_{DD} = V_{IT-} - 0.2$ V, $I_{OL} = 1$ mA			0.4	
			TPS382x-30	$V_{DD} = V_{IT-} - 0.2$ V, $I_{OL} = 1.2$ mA				
			TPS382x-33 TPS382xA-33					
			TPS382x-50	$V_{DD} = V_{IT-} - 0.2$ V, $I_{OL} = 3$ mA			0.4	
	Power-up reset voltage(1)			$V_{DD} \geq 1.1$ V, $I_{OL} = 20$ µA			0.4	V
V_{IT-}	Negative-going input threshold voltage (2)		TPS382x-25	T_A = 0°C to 85°C	2.21	2.25	2.30	V
			TPS382x-30		2.59	2.63	2.69	
			TPS382x-33 TPS382xA-33		2.88	2.93	3	
			TPS382x-50		4.49	4.55	4.64	
			TPS382x-25	T_A = –40°C to 85°C	2.20	2.25	2.30	
			TPS382x-30		2.57	2.63	2.69	
			TPS382x-33 TPS382xA-33		2.86	2.93	3	
			TPS382x-50	T_A = –40°C to 85°C	4.46	4.55	4.64	
V_{hys}	Hysteresis at V_{DD} input		TPS382x-25			30		mV
			TPS382x-30					
			TPS382x-33 TPS382xA-33					
			TPS382x-50			50		
$I_{IH(AV)}$	Average high-level input current	WDI		WDI = V_{DD}, time average (DC = 88%)		120		µA
$I_{IL(AV)}$	Average low-level input current			WDI = 0.3 V, V_{DD} = 5.5 V time average (DC = 12%)		–15		

7.5 Electrical Characteristics (continued)

PARAMETER				TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	High-level input current		WDI	WDI = V_{DD}		140	190	µA
			$\overline{MR}$	$\overline{MR}$ = V_{DD} × 0.7, V_{DD} = 5.5 V		–40	–60	
I_{IL}	Low-level input current		WDI	WDI = 0.3 V, V_{DD} = 5.5 V		140	190	µA
			$\overline{MR}$	$\overline{MR}$ = 0.3 V, V_{DD} = 5.5 V		–110	–160	
I_{OS}	Output short-circuit current(3)	$\overline{RESET}$	TPS382x-25	V_{DD} = $V_{IT, max}$ + 0.2 V, V_O = 0 V			–400	µA
			TPS382x-30					
			TPS382x-33 TPS382xA-33					
			TPS382x-50				–800	
I_{DD}	Supply current			WDI, $\overline{MR}$, and outputs unconnected		15	25	µA
	Internal pullup resistor at $\overline{MR}$					52		kΩ
C_i	Input capacitance at $\overline{MR}$, WDI			V_I = 0 V to 5.5 V		5		pF

(1) The lowest supply voltage at which $\overline{RESET}$ becomes active. t_r, V_{DD} ≥ 15 µs/V.
(2) To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 µF) must be placed near the supply terminals.
(3) The $\overline{RESET}$ short-circuit current is the maximum pullup current when $\overline{RESET}$ is driven low by a microprocessor bidirectional reset pin.

over operating junction temperature range -40°C to 125°C (unless otherwise noted) for TPS3823A-33 only

7.6 Electrical Characteristics for TPS3823A-33 only

PARAMETER				TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$\overline{RESET}$		V_{DD} = V_{IT-} + 0.2 V, I_{OH} = –30 µA	0.8 × V_{DD}			V
V_{OL}	Low-level output voltage	$\overline{RESET}$		V_{DD} = V_{IT-} – 0.2 V, I_{OL} = 1.2 mA			0.45	V
	Power-up reset voltage(1)			V_{DD} ≥ 1.1 V, I_{OL} = 20 µA			0.4	V
V_{IT-}	Negative-going input threshold voltage (2)				2.83	2.93	3	V
V_{hys}	Hysteresis at V_{DD} input					30		mV
$I_{IH(AV)}$	Average high-level input current		WDI	WDI = V_{DD}, time average (DC = 88%)		120		µA
$I_{IL(AV)}$	Average low-level input current			WDI = 0.3 V, V_{DD} = 5.5 V time average (DC = 12%)		–15		
I_{IH}	High-level input current		WDI	WDI = V_{DD}		140	190	µA
			$\overline{MR}$	$\overline{MR}$ = V_{DD} × 0.7, V_{DD} = 5.5 V		–40	–60	
I_{IL}	Low-level input current		WDI	WDI = 0.3 V, V_{DD} = 5.5 V		140	190	µA
			$\overline{MR}$	$\overline{MR}$ = 0.3 V, V_{DD} = 5.5 V		–110	–160	
I_{OS}	Output short-circuit current(3)	$\overline{RESET}$		V_{DD} = $V_{IT, max}$ + 0.2 V, V_O = 0 V			–400	µA
I_{DD}	Supply current			WDI, $\overline{MR}$, and outputs unconnected		15	25	µA
	Internal pullup resistor at $\overline{MR}$					52		kΩ
C_i	Input capacitance at $\overline{MR}$, WDI			V_I = 0 V to 5.5 V		5		pF

(1) The lowest supply voltage at which $\overline{RESET}$ becomes active. t_r, V_{DD} ≥ 15 µs/V.
(2) To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 µF) must be placed near the supply terminals.
(3) The $\overline{RESET}$ short-circuit current is the maximum pullup current when $\overline{RESET}$ is driven low by a microprocessor bidirectional reset pin.

7.7 Timing Requirements

At R_L = 1 MΩ, C_L = 50 pF, and T_J = 25°C, unless otherwise noted.

				MIN	TYP	MAX	UNIT
t_w	Pulse width	at V_{DD}	V_{DD} = V_{IT-} + 0.2 V, V_{DD} = V_{IT-} – 0.2 V	6			µs
		at $\overline{MR}$	V_{DD} ≥ V_{IT-} + 0.2 V, V_{IL} = 0.3 × V_{DD}, V_{IH} = 0.7 × V_{DD}	1			µs
		at WDI	V_{DD} ≥ V_{IT-} + 0.2 V, V_{IL} = 0.3 × V_{DD}, V_{IH} = 0.7 × V_{DD}	100			ns

7.8 Switching Characteristics

At R_L = 1 MΩ, C_L = 50 pF, and T_J = 25°C, unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{tout}	Watchdog time out	TPS3820	$V_{DD} \geq V_{IT-} + 0.2$ V See Figure 7-1	112	200	300	ms
		TPS3823/4/8, TPS3823A		0.9	1.6	2.5	s
t_d	Delay time	TPS3820	$V_{DD} \geq V_{IT-} + 0.2$ V See Figure 7-1	15	25	37	ms
		TPS3823/4/5/8, TPS3823A		120	200	300	
t_{PHL}	Propagation (delay) time, high-to-low-level output	$\overline{MR}$ to $\overline{RESET}$ delay (TPS3820/3/5/8, TPS3823A)	$V_{DD} \geq V_{IT-} + 0.2$ V, $V_{IL} = 0.3 \times V_{DD}$, $V_{IH} = 0.7 \times V_{DD}$			0.1	µs
		V_{DD} to $\overline{RESET}$ delay	$V_{IL} = V_{IT-} - 0.2$ V, $V_{IH} = V_{IT-} + 0.2$ V			25	
t_{PLH}	Propagation (delay) time, low-to-high-level output	$\overline{MR}$ to RESET delay (TPS3824/5)	$V_{DD} \geq V_{IT-} + 0.2$ V, $V_{IL} = 0.3 \times V_{DD}$, $V_{IH} = 0.7 \times V_{DD}$			0.1	µs
		V_{DD} to RESET delay (TPS3824/5)	$V_{IL} = V_{IT-} - 0.2$ V, $V_{IH} = V_{IT-} + 0.2$ V			25	

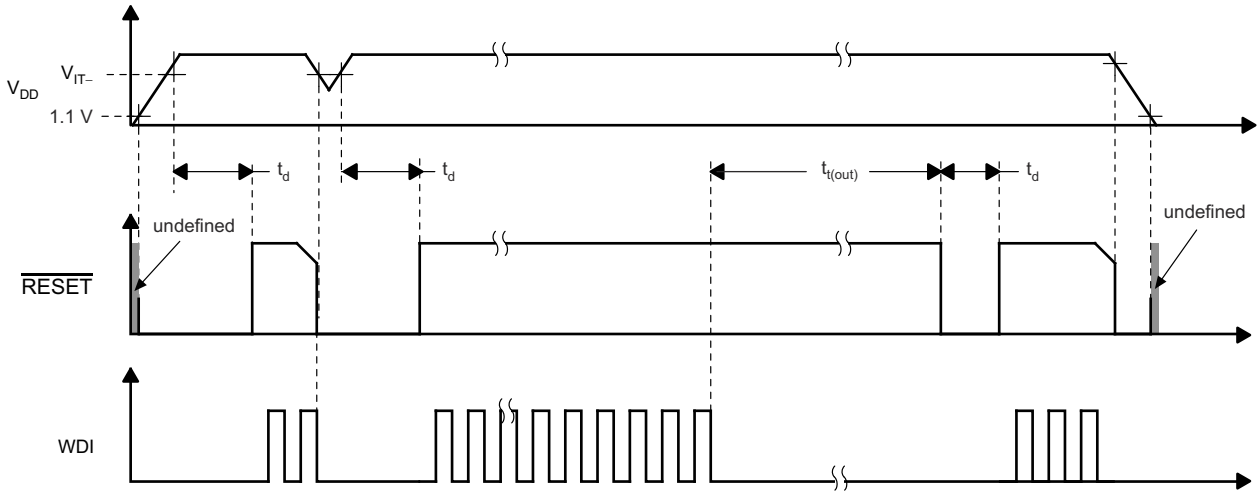


Figure 7-1. Timing Diagram

7.9 Typical Characteristics

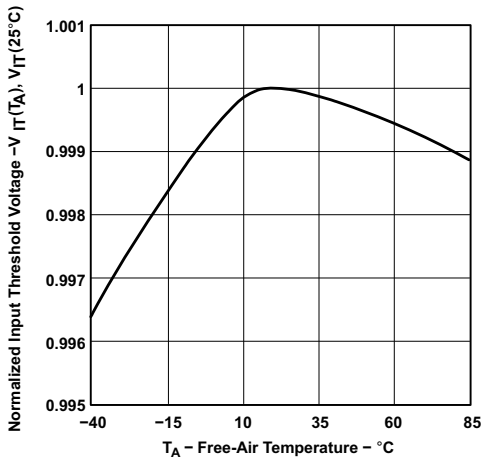


Figure 7-2. Normalized Input Threshold Voltage vs Free-Air Temperature at V_{DD}

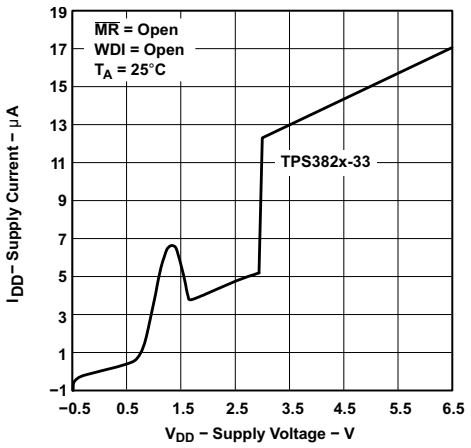


Figure 7-3. Supply Current vs Supply Voltage

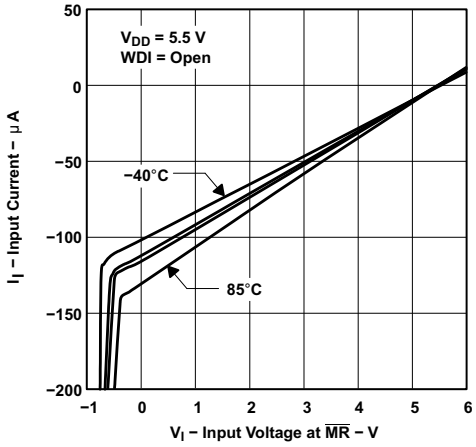


Figure 7-4. Input Current vs Input Voltage at $\overline{MR}$

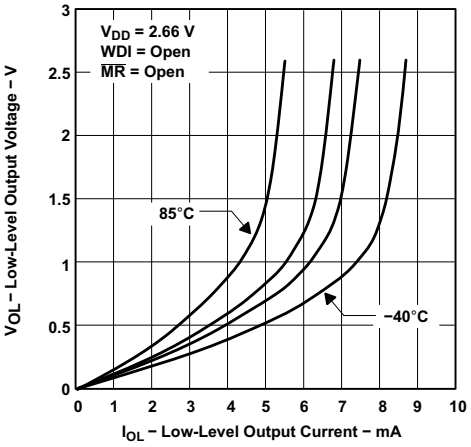


Figure 7-5. Low-Level Output Voltage vs Low-Level Output Current

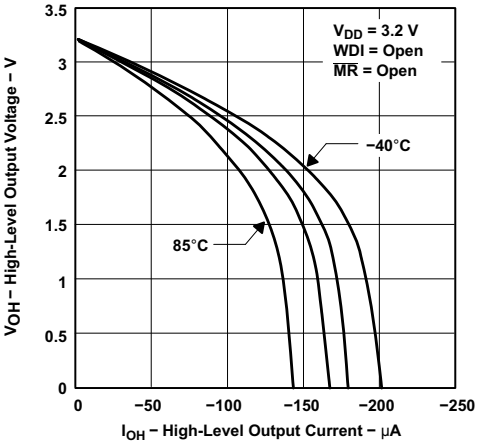


Figure 7-6. High-Level Output Voltage vs High-Level Output Current

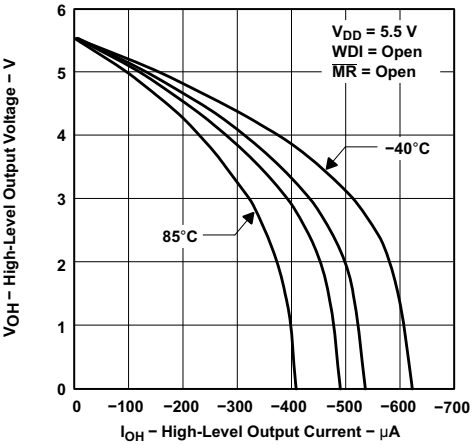


Figure 7-7. High-Level Output Voltage vs High-Level Output Current

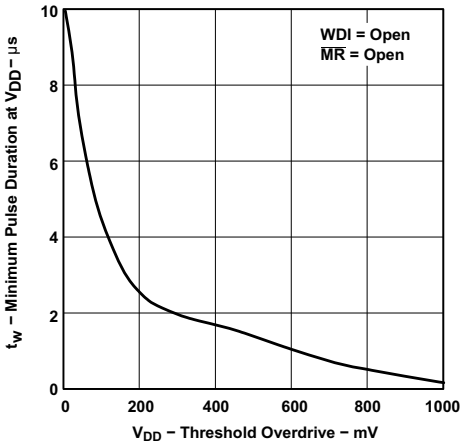


Figure 7-8. Minimum Pulse Duration at V_{DD} vs V_{DD} Threshold Overdrive

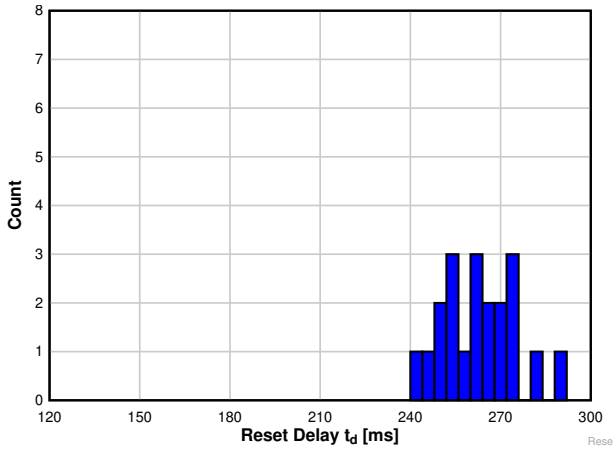


Figure 7-9. Reset Delay Histogram for TPS3823A-33 Devices at -40°C (Unit Count = 20)

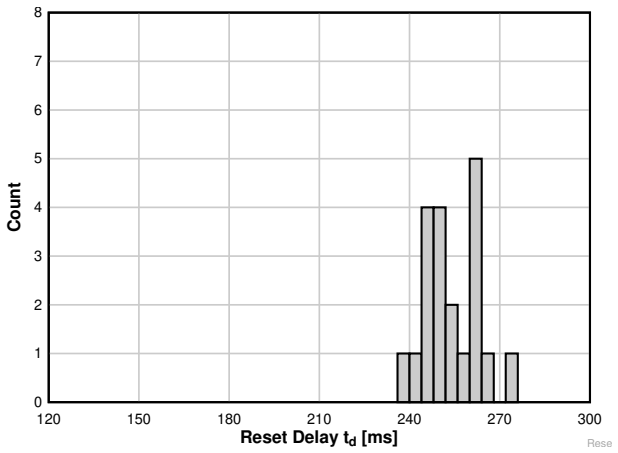


Figure 7-10. Reset Delay Histogram for TPS3823A-33 Devices at 25°C (Unit Count = 20)

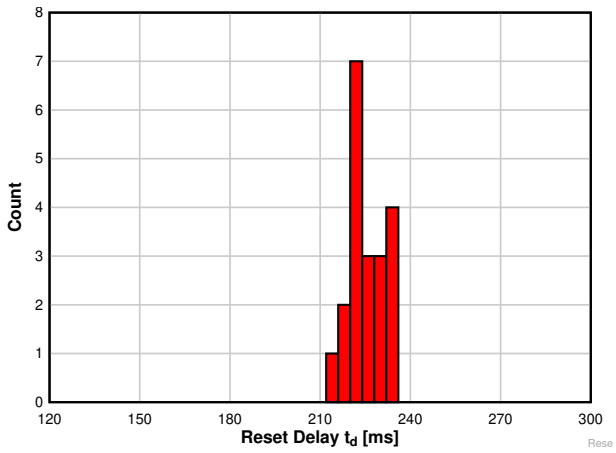


Figure 7-11. Reset Delay Histogram for TPS3823A-33 Devices at 125°C (Unit Count = 20)

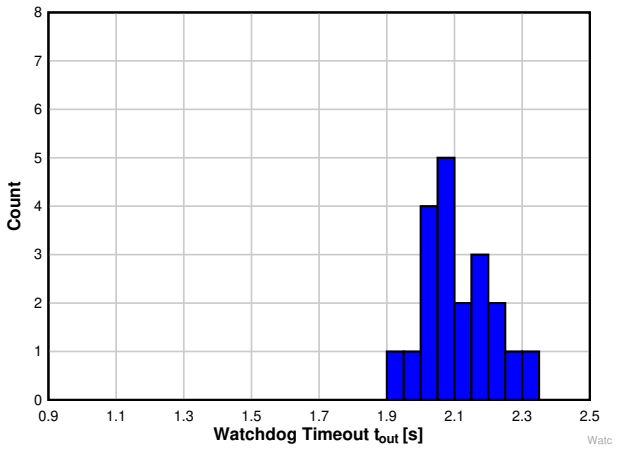


Figure 7-12. Watchdog Timeout Histogram for TPS3823A-33 Devices at -40°C (Unit Count = 20)

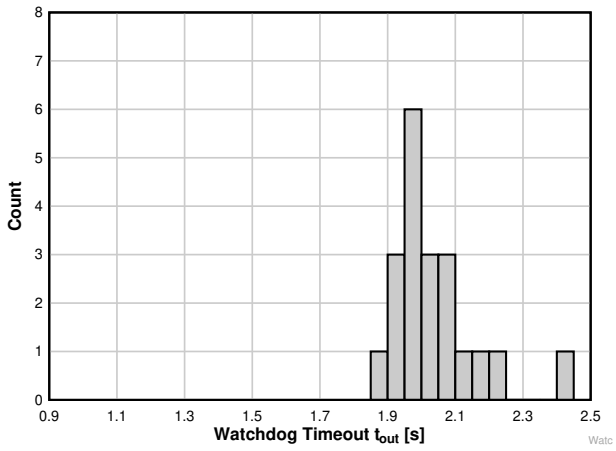


Figure 7-13. Watchdog Timeout Histogram for TPS3823A-33 Devices at 25°C (Unit Count = 20)

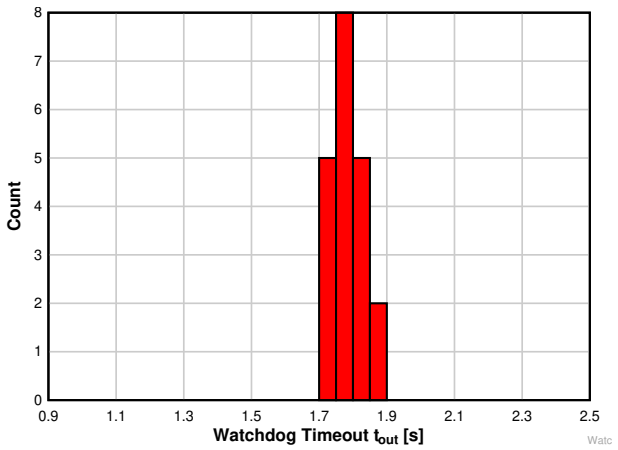


Figure 7-14. Watchdog Timeout Histogram for TPS3823A-33 Devices at 125°C (Unit Count = 20)

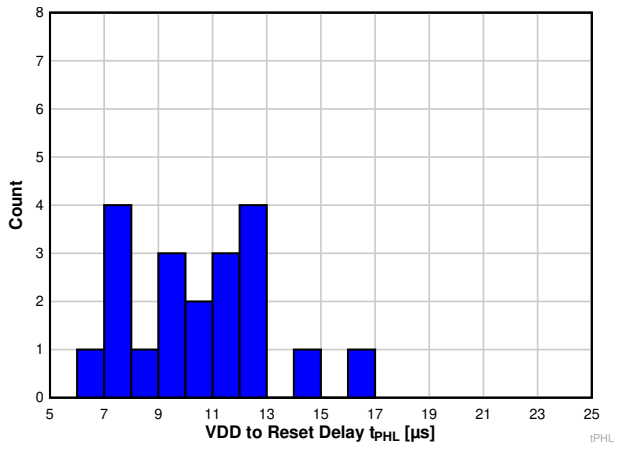


Figure 7-15. VDD to Reset Delay Histogram for TPS3823A-33 Devices at -40°C (Unit Count = 20)

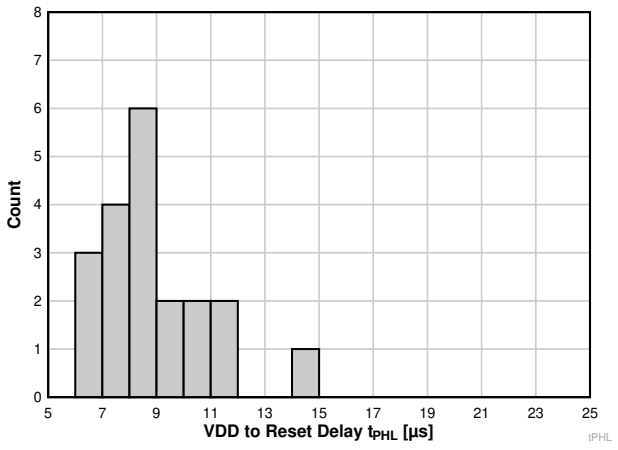


Figure 7-16. VDD to Reset Delay Histogram for TPS3823A-33 Devices at 25°C (Unit Count = 20)

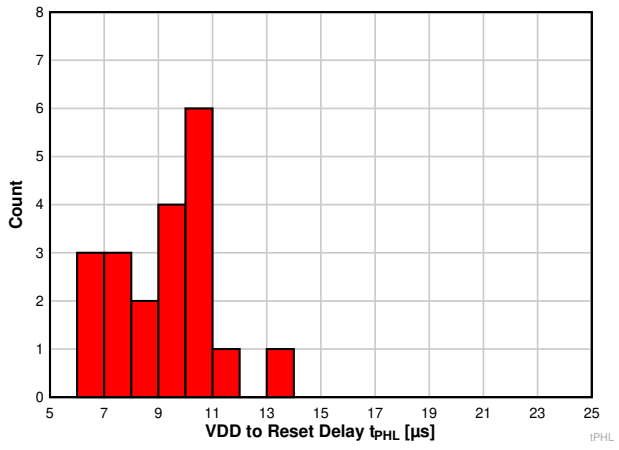


Figure 7-17. VDD to Reset Delay Histogram for TPS3823A-33 Devices at 125°C (Unit Count = 20)

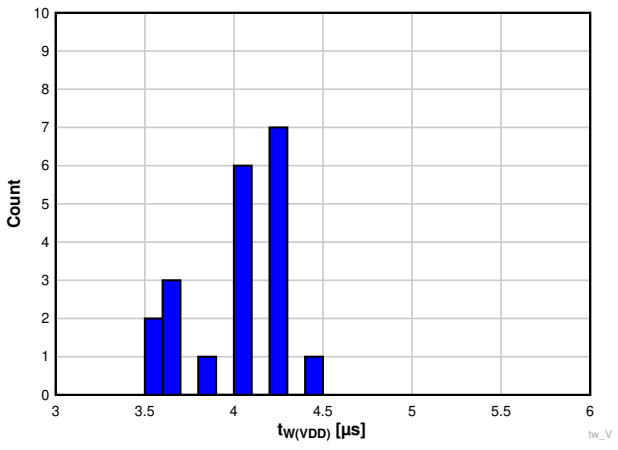


Figure 7-18. VDD Pulse Width Histogram for TPS3823A-33 Devices at -40°C (Unit Count = 20)

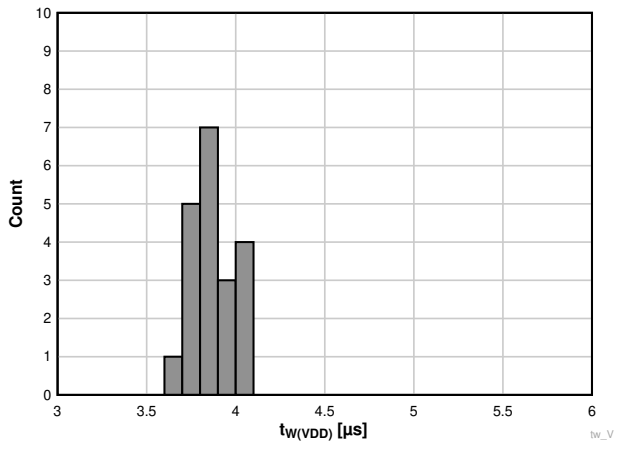


Figure 7-19. VDD Pulse Width Histogram for TPS3823A-33 Devices at 25°C (Unit Count = 20)

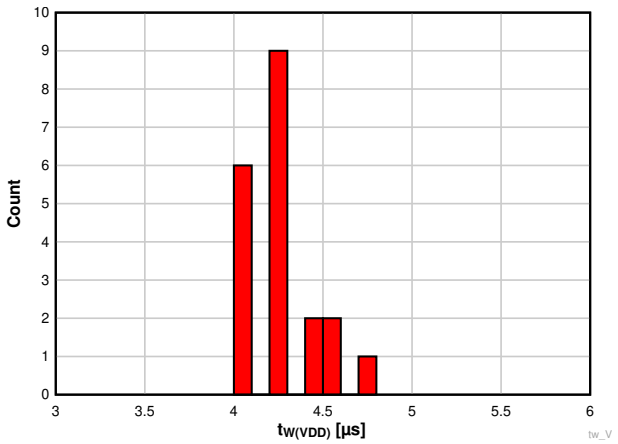


Figure 7-20. VDD Pulse Width Histogram for TPS3823A-33 Devices at 125°C (Unit Count = 20)

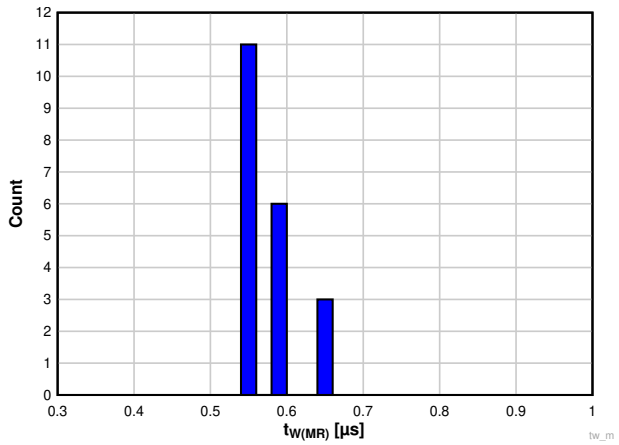


Figure 7-21. Manual Reset Pulse Width Histogram for TPS3823A-33 Devices at -40°C (Unit Count = 20)

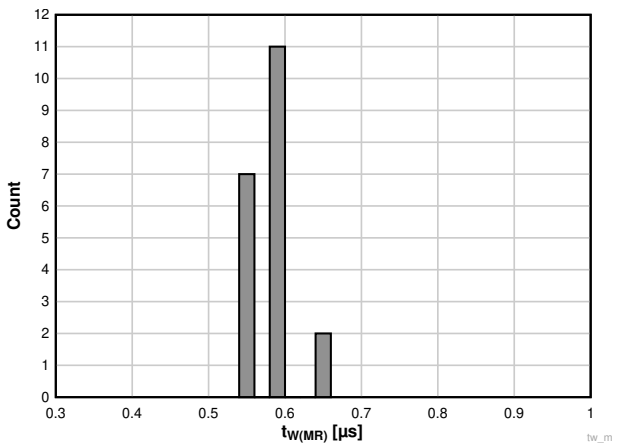


Figure 7-22. Manual Reset Pulse Width Histogram for TPS3823A-33 Devices at 25°C (Unit Count = 20)

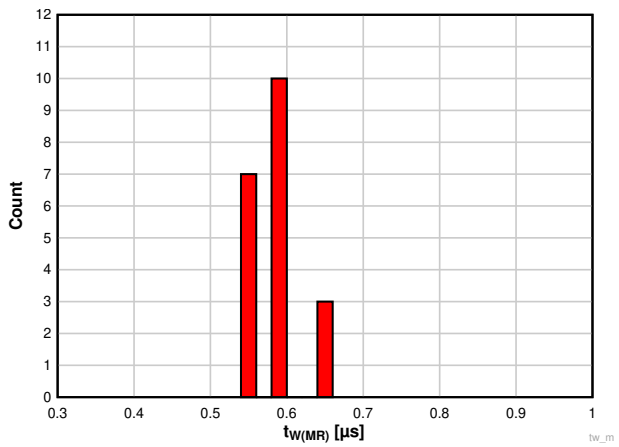


Figure 7-23. Manual Reset Pulse Width Histogram for TPS3823A-33 Devices at 125°C (Unit Count = 20)

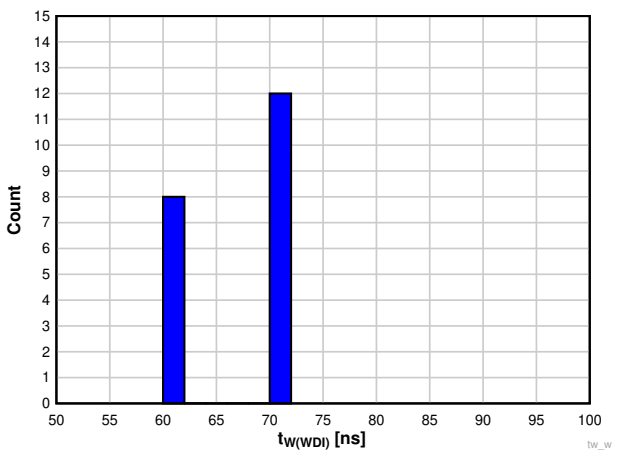


Figure 7-24. WDI Pulse Width Histogram for TPS3823A-33 Devices at -40°C (Unit Count = 20)

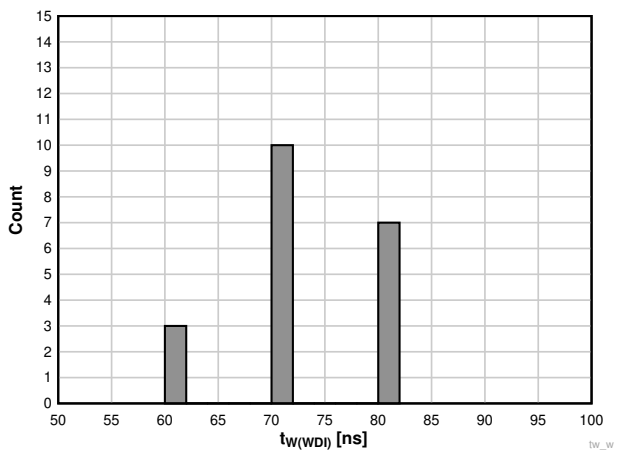


Figure 7-25. WDI Pulse Width Histogram for TPS3823A-33 Devices at 25°C (Unit Count = 20)

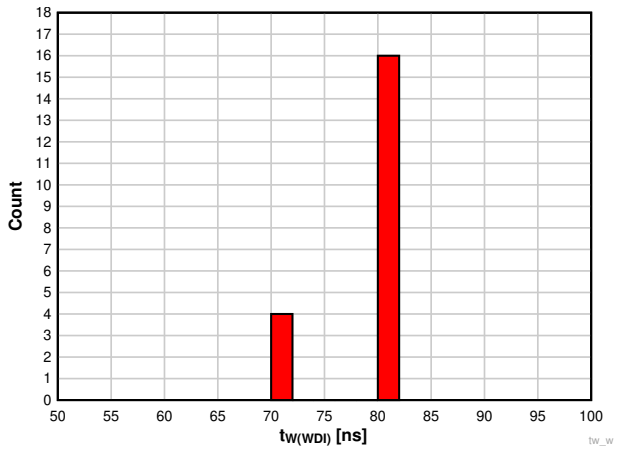


Figure 7-26. WDI Pulse Width Histogram for TPS3823A-33 Devices at 125°C (Unit Count = 20)

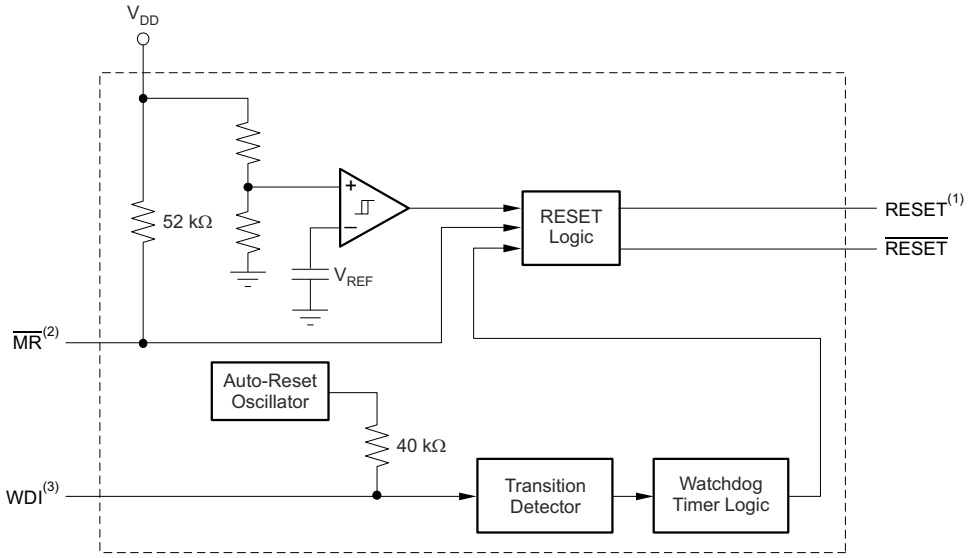
8 Detailed Description

8.1 Overview

The TPS382x family of supervisors provide circuit initialization and timing supervision. Optional configurations include devices with active-high and active-low output signals (TPS3824/5), devices with a watchdog timer (TPS3820/3/4/8), and devices with manual reset ($\overline{MR}$) pins (TPS3820/3/5/8). $\overline{RESET}$ asserts when the supply voltage, V_{DD}, rises above 1.1 V. For devices with active-low output logic, the device monitors V_{DD} and keeps $\overline{RESET}$ low as long as V_{DD} remains below the negative threshold voltage, V_{IT-}. For devices with active-high output logic, RESET remains high as long as V_{DD} remains below V_{IT-}. An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. The delay time, t_d, starts after V_{DD} rises above the positive threshold voltage (V_{IT-} + V_{HYS}). When the supply voltage drops below V_{IT-}, the output becomes active (low) again. All the devices of this family have a fixed-sense threshold voltage, V_{IT-}, set by an internal voltage divider, so no external components are required.

The TPS382x family is designed to monitor supply voltages of 2.5 V, 3 V, 3.3 V, and 5 V. The devices are available in a 5-pin SOT-23 package and are characterized for operation over a temperature range of −40°C to 85°C. Only TPS3823A-33 is characterized for operation over a temperature range −40°C to 125°C.

8.2 Functional Block Diagram



A. TPS3824/5
B. TPS3820/3/5/8
C. TPS3820/3/4/8

8.3 Feature Description

8.3.1 Manual Reset ($\overline{MR}$)

The $\overline{MR}$ input allows an external logic signal from processors, logic circuits, and/or discrete sensors to force a reset signal regardless of V_{DD} with respect to V_{IT-} or the state of the watchdog timer. A low level at $\overline{MR}$ causes the reset signals to become active.

8.3.2 Active-High or Active-Low Output

All TPS382x devices have an active-low logic output ($\overline{RESET}$), while the TPS3824/5 devices also include an active-high logic output (RESET).

8.3.3 Push-Pull or Open-Drain Output

All TPS382x devices, except for TPS3828, have push-pull outputs. TPS3828 devices have an open-drain output.

8.3.4 Watchdog Timer (WDI)

The TPS3820, TPS3823, TPS3824, and TPS3828 devices have a watchdog timer that must be periodically triggered by either a positive or negative transition at WDI to avoid a reset signal being issued. When the supervising system fails to retrigger the watchdog circuit within the time-out interval, t_{tout}, $\overline{\text{RESET}}$ becomes active for the time period t_d. This event also reinitializes the watchdog timer.

The watchdog timer can be disabled by disconnecting the WDI pin from the system. If the WDI pin detects that it is in a high-impedance state, the TPS3820, TPS3823, TPS3824, or TPS3828 will generate its own WDI pulse to ensure that $\overline{\text{RESET}}$ does not assert. If this behavior is not desired, place a 1-kΩ resistor from WDI to ground. This resistor will help ensure that the TPS3820, TPS3823, TPS3824, or TPS3828 detects that WDI is not in a high-impedance state.

In applications where the input to the WDI pin is active (transitioning high and low) and the TPS3820, TPS3823, TPS3824, or TPS3828 is asserting $\overline{\text{RESET}}$, $\overline{\text{RESET}}$ is stuck at a logic low after the input voltage returns above V_{IT-}. If the application requires that input to WDI be active when the reset signal is asserted, then either the **A** version of the device or a FET should be used to decouple the WDI signal. The **A** version does not latch the reset signal to the asserted state if a WDI pulse is received while RESET is asserted. An external FET decouples the WDI signal by disconnecting the WDI input when $\overline{\text{RESET}}$ is asserted. For more details on this, see *Decoupling WDI During Reset Event*. The **A** version of the device does not require this FET, but it does operate in circuits that have it. Therefore, the **A** version is backwards-compatible with the non-**A** versions.

8.4 Device Functional Modes

Table 8-1 lists the functional modes of the TPS382x devices.

Table 8-1. Function Table

INPUTS		OUTPUTS	
$\overline{\text{MR}}$ (1)	$V_{DD} > V_{IT}$	$\overline{\text{RESET}}$	RESET(2)
L	0	L	H
L	1	L	H
H	0	L	H
H	1	H	L

(1) TPS3820/3/5/8
(2) TPS3824/5

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPS382x family of devices are very small supervisory circuits that monitor fixed supply voltages of 2.5 V, 3 V, 3.3 V, and 5 V. The TPS382x family operates from 1.1 V to 5.5 V. Orderable options include versions with either push-pull or open-drain outputs, versions that use active-high or active-low logic for output signals, versions with a manual reset pin, and versions with a watchdog timer. See the *Device Comparison Table* for an overview of device options.

9.2 Typical Applications

9.2.1 Supply Rail Monitoring With Watchdog Time-Out and 200-ms Delay

The TPS3823A can be used to monitor the supply rail for devices such as microcontrollers. The downstream device is enabled by the TPS3823A once the voltage on the supply pin (V_{DD}) is above the internal threshold voltage (V_{IT-} + V_{HYS}). The downstream device is disabled by the TPS3823A when V_{DD} falls below the threshold voltage minus the hysteresis voltage (V_{IT-}). The TPS3823A also issues a reset signal if the WDI input is not periodically triggered by a positive or negative transition at WDI. When the supervising system fails to retrigger the watchdog circuit within the time-out interval, t_{tout}, $\overline{\text{RESET}}$ becomes active for the time period t_d.

Some applications require a shorter reset signal than the 200 ms that most of the TPS382x family provide. In these cases, the TPS3820 is a good choice because it has a delay time of only 25 ms. If an open-drain output is required, replace the TPS3823A with the TPS3828 (if the WDI input must be active while $\overline{\text{RESET}}$ is low, see *Decoupling WDI During Reset Event*). Figure 9-1 shows the TPS3823A in a typical application.

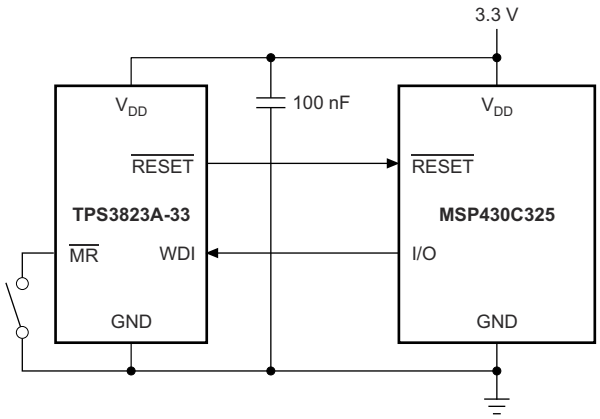


Figure 9-1. Supply Rail Monitoring With Watchdog Time-Out

9.2.1.1 Design Requirements

The TPS3823A must drive the enable pin of a MSP430C325 using a logic-high signal to signify that the supply voltage is above the minimum operating voltage of the device and monitor the I/O pin to determine if the microcontroller is operating correctly.

9.2.1.2 Detailed Design Procedure

Determine which version of the TPS382x family best suits the functional performance required.

If the input supply is noisy, include an input capacitor to help avoid unwanted changes to the reset signal.

9.2.1.3 Application Curve

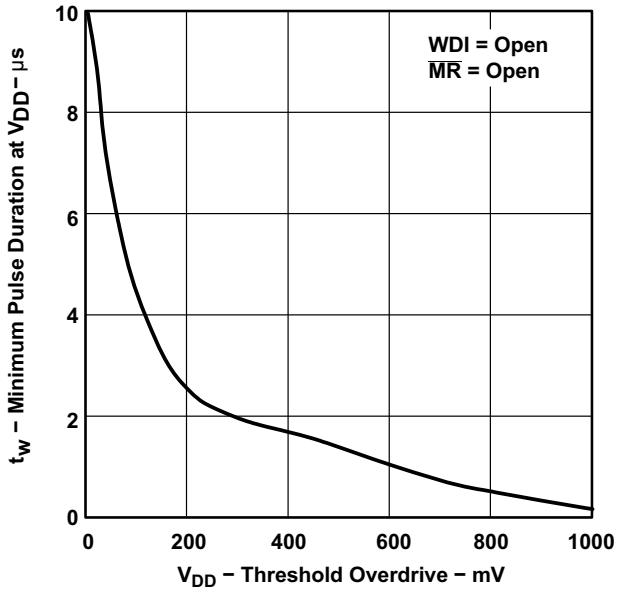


Figure 9-2. Minimum Pulse Duration at V_{DD} vs V_{DD} Threshold Overdrive

9.2.2 Decoupling WDI During Reset Event

If the application requires that the input to WDI is active when the reset signal is asserted and the **A** version of the device cannot be used, Figure 9-3 shows how to decouple WDI from the active signal using an N-channel FET. The N-channel FET is placed in series with the WDI pin, with the gate of the FET connected to the $\overline{\text{RESET}}$ output.

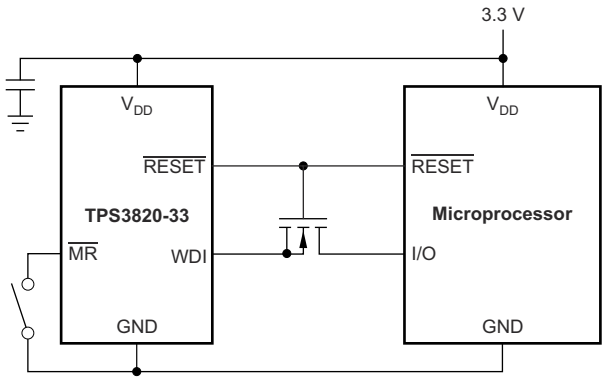


Figure 9-3. WDI Example

9.2.2.1 Design Requirements

The TPS3820 must drive the enable pin of a microprocessor using a logic-high signal to signify that the supply voltage is above the minimum operating voltage of the device and monitor the I/O pin to determine if the microcontroller is operating correctly. The reset signal delay time should be greater than 10 ms but less than 50 ms to achieve the desired behavior.

9.2.2.2 Detailed Design Procedure

Determine which version of the TPS3820 is best suited for monitoring the supply voltage.

If the input supply is noisy, include an input capacitor to help avoid unwanted changes to the reset signal.

9.2.2.3 Application Curve

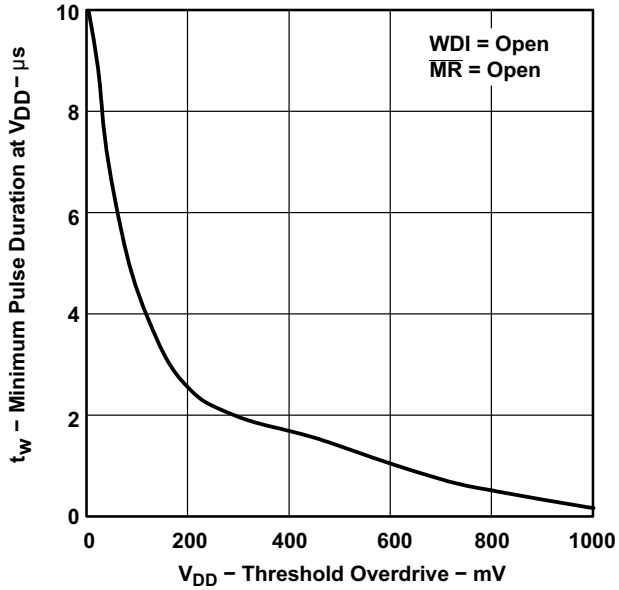


Figure 9-4. Minimum Pulse Duration at V_{DD} vs V_{DD} Threshold Overdrive

10 Power Supply Recommendations

These devices are designed to operate from an input supply with a voltage range from 1.1 V to 5.5 V. Though not required, it is good analog design practice to place a 0.1-µF ceramic capacitor close to the V_{DD} pin if the input supply is noisy.

11 Layout

11.1 Layout Guidelines

Follow these guidelines to lay out the printed-circuit board (PCB) that is used for the TPS382x family of devices.

- Place the V_{DD} decoupling capacitor (C_{VDD}) close to the device.
- Avoid using long traces for the V_{DD} supply node. The V_{DD} capacitor (C_{VDD}), along with parasitic inductance from the supply to the capacitor, can form an LC tank and create ringing with peak voltages above the maximum V_{DD} voltage.

11.2 Layout Example

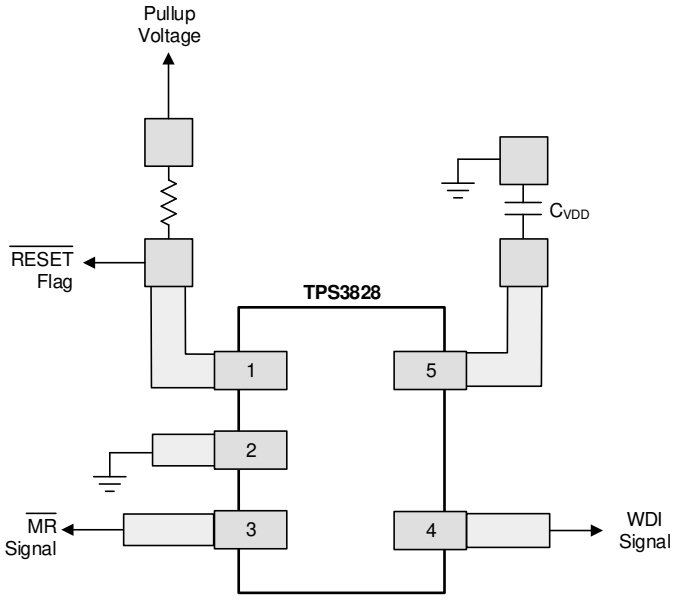


Figure 11-1. Example Layout (DBV Package)

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

12.1.1.1 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS382x is available through the product folders under *Tools & Software*.

12.1.2 Device Nomenclature

Table 12-1. Ordering Information

ORDERABLE DEVICE NAME(1) (2) (3)		THRESHOLD VOLTAGE(4)	MARKING
TPS3820-33DBVT	TPS3820-33DBVR	2.93 V	PDEI
TPS3820-50DBVT	TPS3820-50DBVR	4.55 V	PDDI
TPS3823-25DBVT	TPS3823-25DBVR	2.25 V	PAPI
TPS3823-30DBVT	TPS3823-30DBVR	2.63 V	PAQI
TPS3823-33DBVT	TPS3823-33DBVR	2.93 V	PARI
TPS3823-50DBVT	TPS3823-50DBVR	4.55 V	PASI
TPS3824-25DBVT	TPS3824-25DBVR	2.25 V	PATI
TPS3824-30DBVT	TPS3824-30DBVR	2.63 V	PAUI
TPS3824-33DBVT	TPS3824-33DBVR	2.93 V	PAVI
TPS3824-50DBVT	TPS3824-50DBVR	4.55 V	PAWI
TPS3825-33DBVT	TPS3825-33DBVR	2.93 V	PDGI
TPS3825-50DBVT	TPS3825-50DBVR	4.55 V	PDFI
TPS3828-33DBVT	TPS3828-33DBVR	2.93 V	PDII
TPS3828-50DBVT	TPS3828-50DBVR	4.55 V	PDHI
TPS3823A-33DBVT	TPS3823A-33DBVR	2.93 V	PYPI

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) The DBVT package indicates tape and reel of 250 parts.
(3) The DBVR package indicates tape and reel of 3000 parts.
(4) For other threshold voltage versions, contact the local TI sales office.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation, see the following:

Disabling the Watchdog Timer for TI's Family of Supervisors (SLVA145)

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3820-33DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDEI	Samples
TPS3820-33DBVT	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 85	PDEI	
TPS3820-33DBVTG4	NRND	SOT-23	DBV	5	250	TBD	Call TI	Call TI	-40 to 85		
TPS3820-50DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDDI	Samples
TPS3820-50DBVT	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 85	PDDI	
TPS3823-25DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PAPI	Samples
TPS3823-25DBVT	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI		PAPI	
TPS3823-30DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PAQI	Samples
TPS3823-30DBVT	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI		PAQI	
TPS3823-33DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PARI	Samples
TPS3823-33DBVT	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI		PARI	
TPS3823-33DBVTG4	NRND	SOT-23	DBV	5	250	TBD	Call TI	Call TI			
TPS3823-50DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PASI	Samples
TPS3823-50DBVT	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI		PASI	
TPS3823-50DBVTG4	NRND	SOT-23	DBV	5	250	TBD	Call TI	Call TI			
TPS3823A-33DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PYPI	Samples
TPS3823A-33DBVT	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 125	PYPI	
TPS3824-25DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PATI	Samples
TPS3824-25DBVT	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI		PATI	
TPS3824-30DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PAUI	Samples
TPS3824-30DBVRG4	ACTIVE	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 85		Samples
TPS3824-30DBVT	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI		PAUI	
TPS3824-33DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PAVI	Samples
TPS3824-33DBVT	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI		PAVI	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3824-50DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PAWI	Samples
TPS3824-50DBVT	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI		PAWI	
TPS3825-33DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDGI	Samples
TPS3825-33DBVT	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 85	PDGI	
TPS3825-33DBVTG4	NRND	SOT-23	DBV	5	250	TBD	Call TI	Call TI	-40 to 85		
TPS3825-50DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDFI	Samples
TPS3825-50DBVT	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 85	PDFI	
TPS3825-50DBVTG4	NRND	SOT-23	DBV	5	250	TBD	Call TI	Call TI	-40 to 85		
TPS3828-33DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDII	Samples
TPS3828-33DBVT	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 85	PDII	
TPS3828-33DBVTG4	NRND	SOT-23	DBV	5	250	TBD	Call TI	Call TI	-40 to 85		
TPS3828-50DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDHI	Samples
TPS3828-50DBVT	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 85	PDHI	
TPS3828-50DBVTG4	NRND	SOT-23	DBV	5	250	TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS3820, TPS3823, TPS3824, TPS3825, TPS3828 :

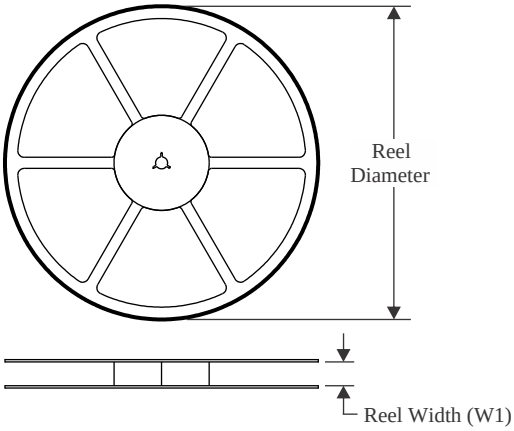
- Automotive : TPS3820-Q1, TPS3823-Q1, TPS3824-Q1, TPS3825-Q1, TPS3828-Q1

NOTE: Qualified Version Definitions:

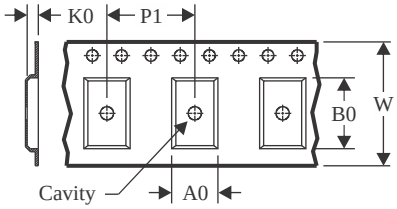
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

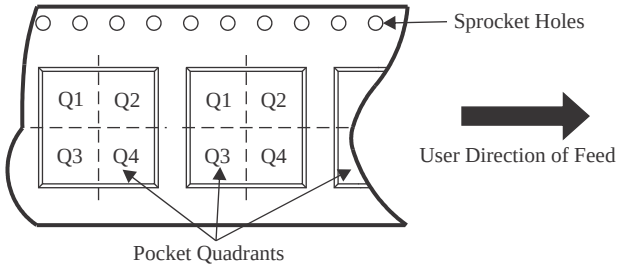


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

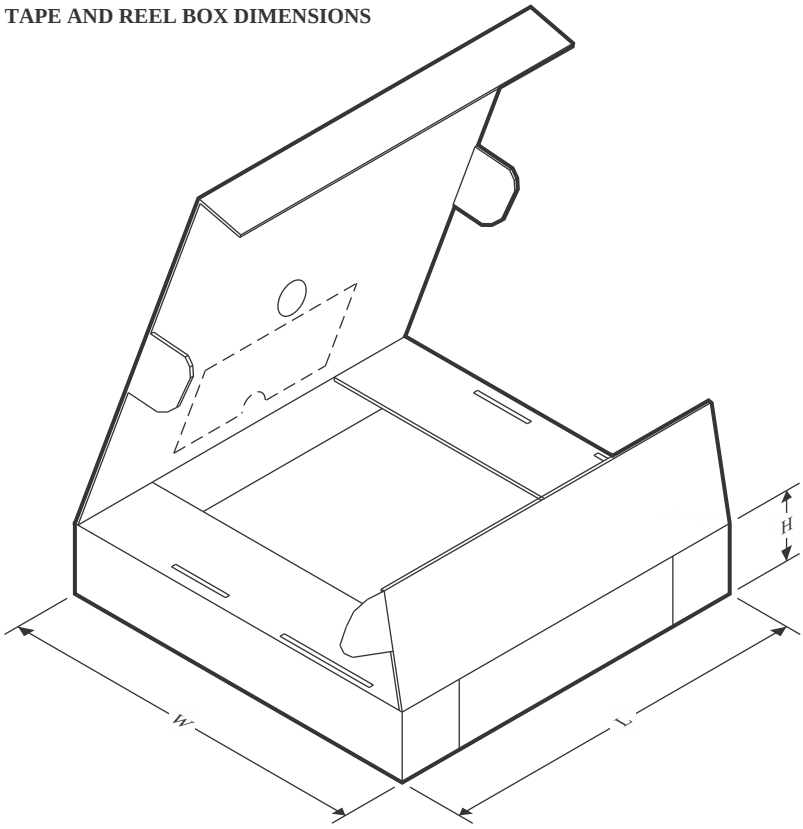


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3820-33DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS3820-50DBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3820-50DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3823-25DBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3823-25DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3823-30DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3823-33DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3823-50DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3823A-33DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS3824-25DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3824-25DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3824-30DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3824-30DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3824-33DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3824-50DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3825-33DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3825-50DBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3825-50DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3828-33DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3828-50DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3820-33DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS3820-50DBVR	SOT-23	DBV	5	3000	200.0	183.0	25.0
TPS3820-50DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS3823-25DBVR	SOT-23	DBV	5	3000	203.0	203.0	35.0
TPS3823-25DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS3823-30DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS3823-33DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS3823-50DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS3823A-33DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS3824-25DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS3824-25DBVR	SOT-23	DBV	5	3000	200.0	183.0	25.0
TPS3824-30DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS3824-30DBVR	SOT-23	DBV	5	3000	200.0	183.0	25.0
TPS3824-33DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS3824-50DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS3825-33DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS3825-50DBVR	SOT-23	DBV	5	3000	203.0	203.0	35.0
TPS3825-50DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0

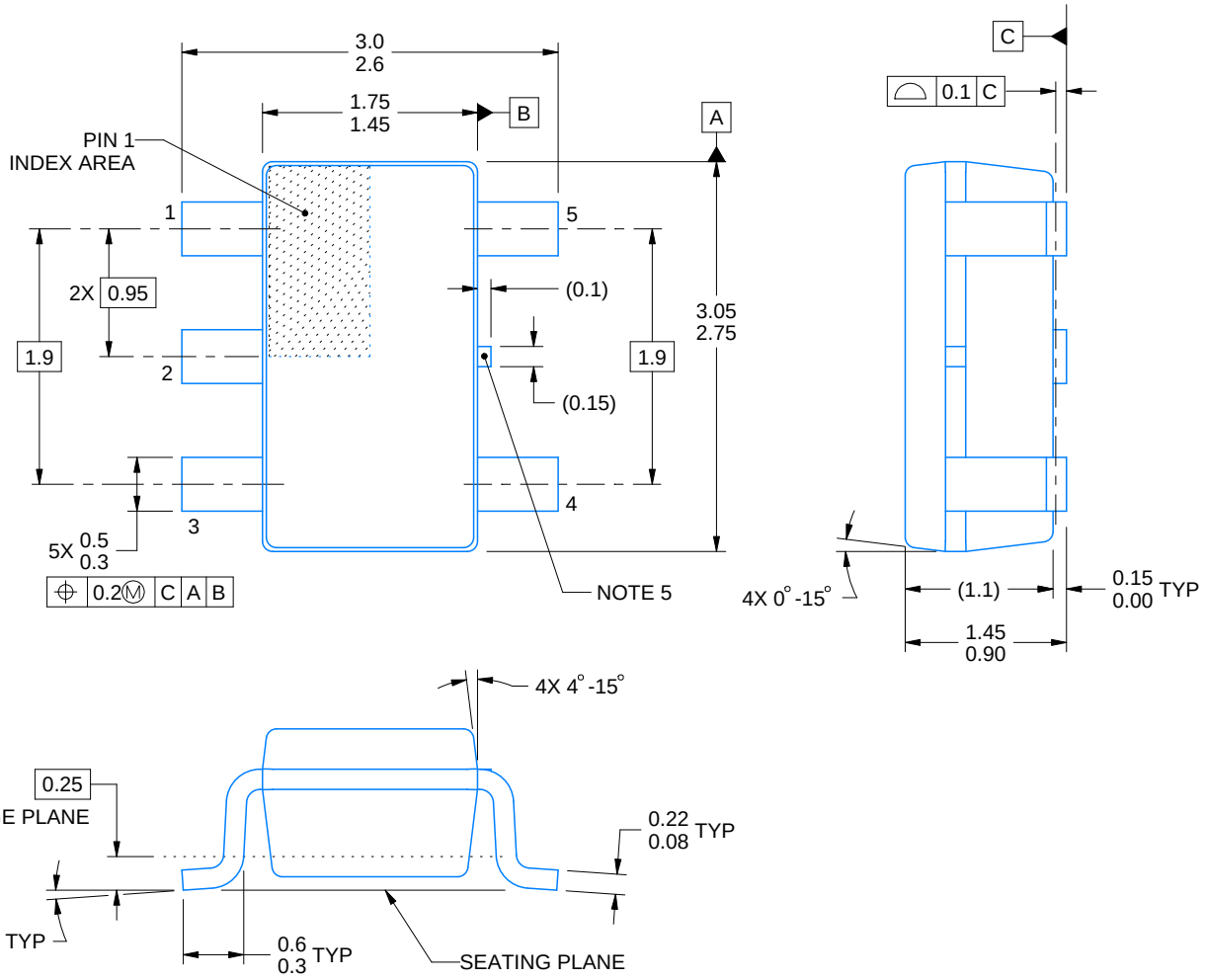
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3828-33DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS3828-50DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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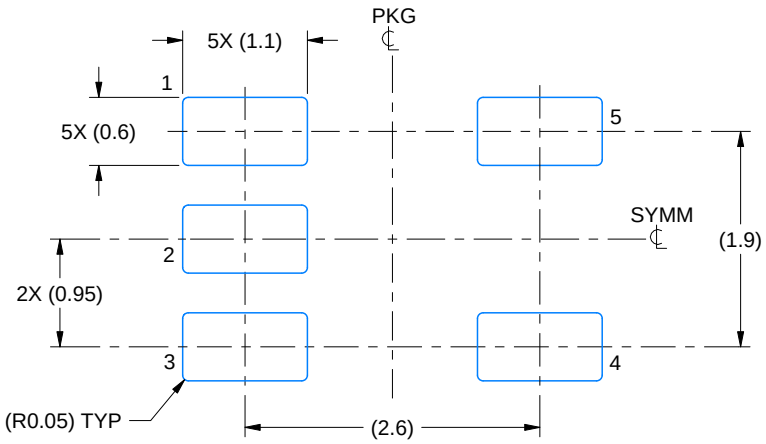
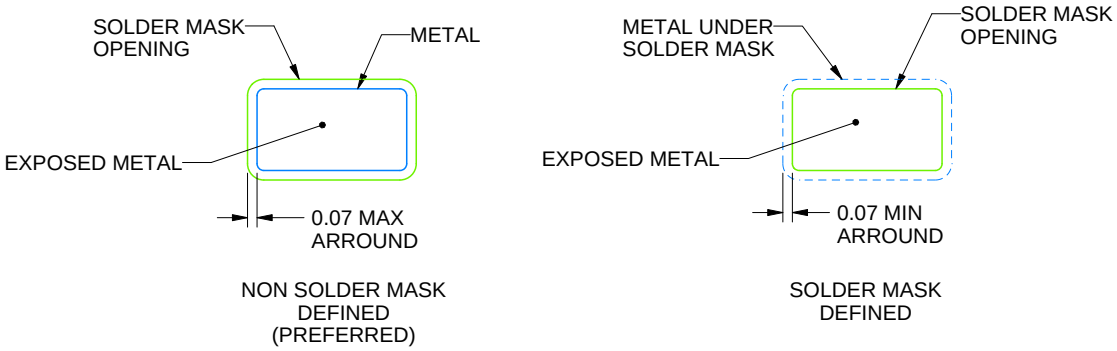
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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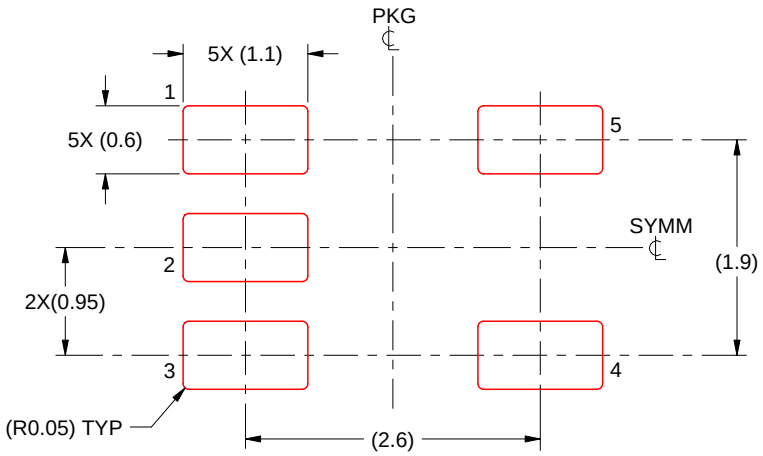
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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