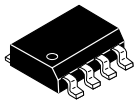
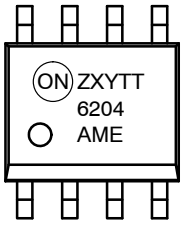
mWSaver® Synchronous Rectification Controller for Flyback and Forward Freewheeling Rectification

FAN6204A



SOIC8
CASE 751EB

MARKING DIAGRAM



Z = Plant Code
X = Year Code
Y = Week Code
TT = Die Run Code
6204AME = Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 11 of this data sheet.

Description

FAN6204A is a secondary−side synchronous rectification (SR) controller to drive SR MOSFET for improving efficiency. The IC is suitable for flyback converters and forward free−wheeling rectification.

FAN6204A can be applied in continuous or discontinuous conduction mode (CCM and DCM) and quasi−resonant (QR) flyback converters based on the proprietary innovative linear−predict timing−control technique. The benefits of this technique include a simple control method without current−sense circuitry to accomplish noise immunity.

With PWM frequency tracking and secondary−side winding voltage detection, FAN6204A can operate in both fixed− and variable−frequency systems.

In Green Mode, the SR controller stops all SR switching operation to reduce the operating current. Power consumption is maintained at minimum level in light− load condition.

Features

- mWSaver Technology:
  - Internal Green Mode to Stop SR Switching for Lower No−Load Power Consumption
  - 1.1 mA Ultra−Low Green Mode Operating Current
- SR Controller
- Suited for Flyback Converter in QR, DCM, and CCM Operation
- Suited for Forward Freewheeling Rectification
- PWM Frequency Tracking with Secondary−Side Winding Voltage Detection
- Ultra−Low V_{DD} Operating Voltage for Various Output Voltage Applications (5 V~24 V)
- V_{DD} Pin Over−Voltage Protection (OVP)
- 12 V (Typical) Gate Driver Clamp
- 8−Pin SOP Package
- This is a Pb−Free Device

Applications

- AC/DC NB Adapters
- Open−Frame SMPS
- Battery Charger

APPLICATION DIAGRAMS

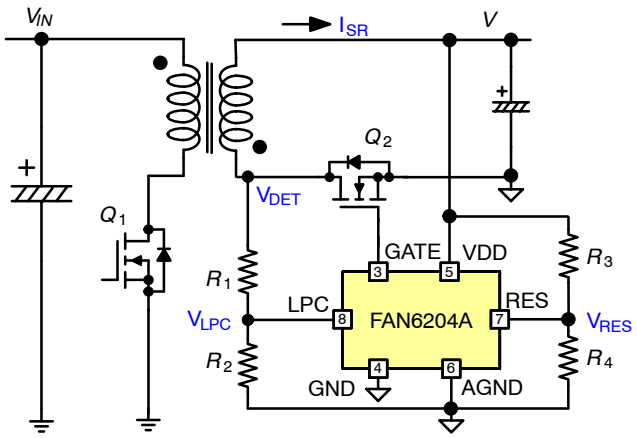


Figure 1. Typical Application Circuit for Flyback Converter

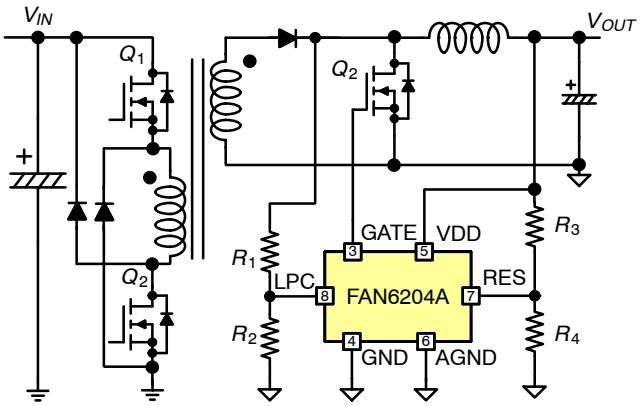


Figure 2. Typical Application Circuit for Forward Freewheeling Rectification

INTERNAL BLOCK DIAGRAM

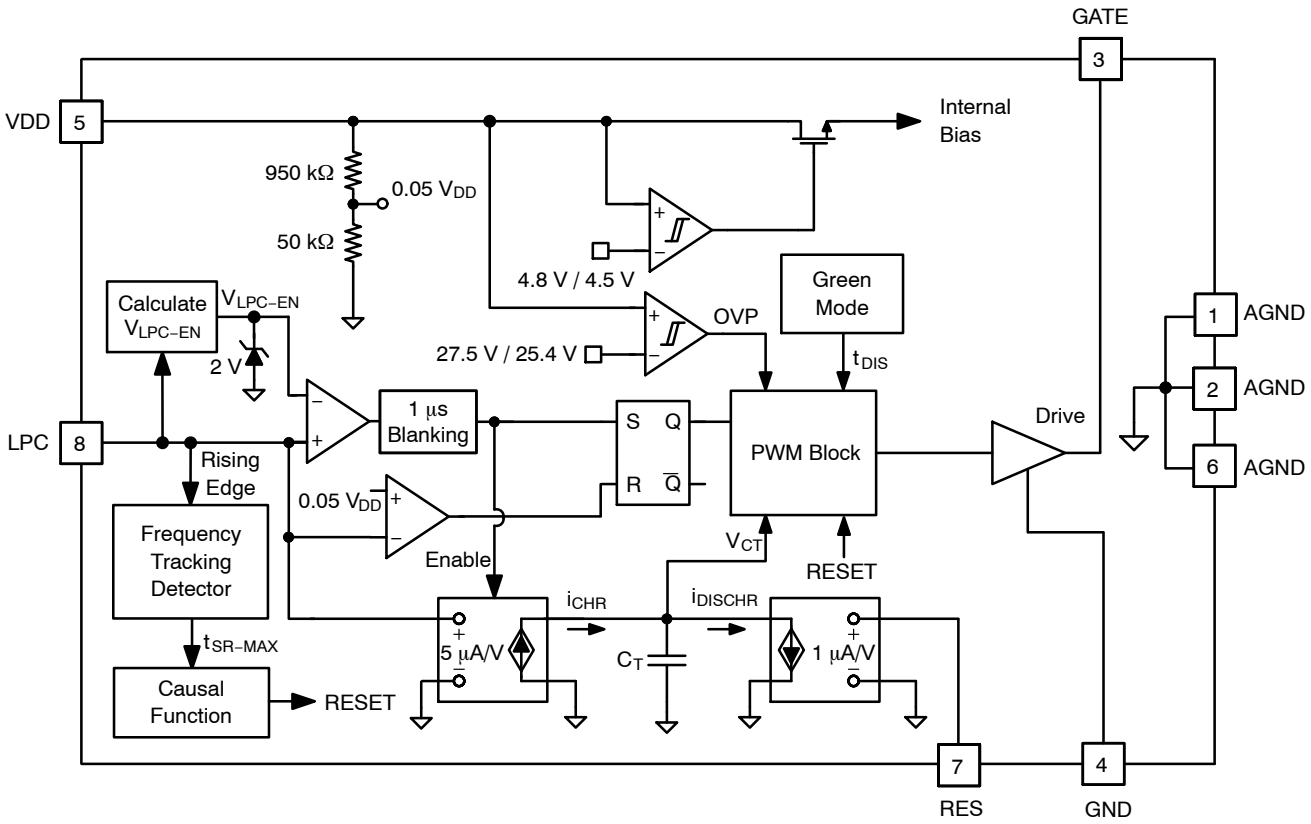


Figure 3. Functional Block Diagram

PIN CONFIGURATION

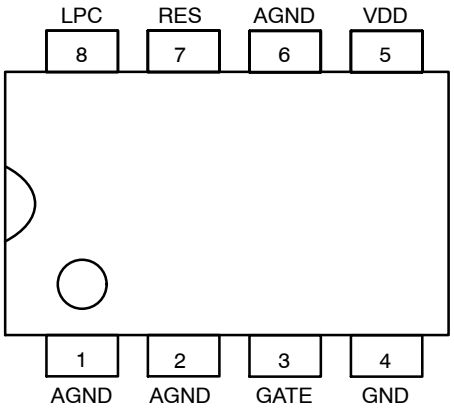


Figure 4. Pin Assignments

PIN DESCRIPTION

Pin No.	Name	Description
1	AGND	Signal Ground.
2	AGND	Signal Ground.
3	GATE	Driver Output. The totem−pole output driver for driving the power MOSFET.
4	GND	Ground. MOSFET source connection.
5	VDD	Power Supply. The threshold voltages for startup and turn−off are 4.8 V and 4.5 V, respectively.
6	AGND	Signal Ground.
7	RES	Reset Control of Linear Predict. The RES pin is used to detect the output voltage level through a voltage divider. An internal current source, I_{DISCHR}, is modulated by the voltage level on the RES pin.
8	LPC	Winding Detection. This pin is used to detect the voltage on the winding during the on−time period of the primary GATE.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
V_{DD}	DC Supply Voltage	−	30	V
V_L	LPC, RES	−0.3	7.0	V
P_D	Power Dissipation (T_A = 25°C)	−	0.8	W
Θ_{JA}	Thermal Resistance (Junction−to−Air)	−	151	°C/W
Θ_{JC}	Thermal Resistance (Junction−to−Case)	−	58	°C/W
T_{STG}	Storage Temperature Range	−55	+150	°C
T_J	Junction Temperature	−40	+150	°C
T_L	Lead Temperature (Soldering 10 Seconds)	−	+260	°C
ESD	Human Body Model	−	5	kV
	Charged Device Model	−	2	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
2. All voltage values, except differential voltages, are given with respect to GND pin.

ELECTRICAL CHARACTERISTICS (V_{DD} = 15 V and T_A = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OP}	Continuously Operating Voltage		V_{DD-OFF}	–	28.5	V
V_{DD-ON}	Turn−On Threshold Voltage		4.3	4.8	5.3	V
V_{DD-OFF}	Turn−Off Threshold Voltage		4.0	4.5	5.0	V
$V_{DD-HYST}$	$V_{DD-ON} - V_{DD-OFF}$		0.1	0.3	0.5	V
I_{DD-OP}	Operating Current	V_{DD} = 15 V, L_{PC} = 50 kHz, MOSFET C_{ISS} = 6000 pF	–	7	8	mA
$I_{DD-GREEN}$	Operating Current in Green Mode	V_{DD} = 15 V	–	1.1	1.3	mA
I_{DD-ST}	Startup Current	$V_{DD} < V_{DD-ON}$	–	150	200	μA
V_{DD-OVP}	V_{DD} Over−Voltage Protection		26.0	27.5	28.5	V
$V_{DD-OVP-HYST}$	Hysteresis Voltage for V_{DD} OVP		1.8	2.1	2.4	V
$t_{VDD-OVP}$	V_{DD} OVP Debounce Time		40	70	100	μs
OUTPUT DRIVER SECTION						
V_Z	Gate Output Clamp Voltage		10	12	14	V
V_{OL}	Output Voltage Low	V_{DD} = 6 V, I_O = 50 mA	–	–	0.5	V
V_{OH}	Output Voltage High	V_{DD} = 6 V, I_O = 50 mA	4	–	–	V
t_R	Rising Time	V_{DD} = 12 V, C_L = 6 nF, OUT = 2 V~9 V	30	70	120	ns
		V_{DD} = 6 V, C_L = 6 nF, OUT = 0.4 V~4 V	70	120	170	ns
t_F	Falling Time	V_{DD} = 12 V, C_L = 6 nF, OUT = 9 V~2 V	20	50	100	ns
		V_{DD} = 6 V, C_L = 6 nF, OUT = 4 V~0.4 V	20	90	130	ns
$t_{PD\_HIGH\_LPC}$	Propagation Delay to Turn−on Gate (LPC Trigger)	t_R: 0 V~2 V, V_{DD} = 12 V	–	250	–	ns
$t_{PD\_LOW\_LPC}$	Propagation Delay to Turn−off Gate (LPC Trigger) (Note 3)	t_F: 100%~90%, V_{DD} = 12 V	–	180	–	ns
$t_{MAX-PERIOD}$	Limitation between LPC Rising Edge to Gate Falling Edge		22.5	25.0	28.0	μs
$V_{PMOS-ON}$	Internal PMOS Turn−On to Pull−HIGH Gate (Note 3)		–	8.3	–	V
$V_{PMOS-ON-HYS}$	Hysteresis Voltage On (Note 3)		–	0.9	–	V
$t_{INHIBIT}$	Gate Inhibit Time	M2 Option (Enable)	1.6	2.2	2.8	μs
$V_{GATE-PULL-HIGH}$	Gate Pull−HIGH Voltage	V_{DD} = 5 V	4.5	–	–	V
LPC SECTION						
t_{BNK}	Blanking Time for Charging C_T		400	500	600	ns
$t_{DELAY-COMP}$	Sampling Continuous Time for t_{BNK} Compensation (Note 3)		–	1	–	μs
$V_{LPC-SOURCE}$	LPC Lower Clamp Voltage	Source I_{LPC} = 5 μA	0.1	0.2	0.3	V
$I_{LPC-SOURCE}$	LPC Source Current	V_{LPC} = 0 V	40	80	120	μA
V_{LPC-EN}	Threshold Voltage to Enabled SR Switching	$V_{LPC-EN} = V_{LPC-HIGH}$ x 0.83 at $V_{LPC-HIGH}$ x 0.83 < 2 V, V_O = 15 V, $V_O = V_{DD}$, $V_{LPC-HIGH}$ = 1.2 V	0.85	1.00	1.15	V
$V_{EN-CLAMP}$	Threshold Clamp Voltage to Enable SR Switching	V_{LPC-EN} = 2 V at $V_{LPC-HIGH}$ x 0.83 > 2 V	–	2	–	V
$V_{LPC-TH-HIGH}$	Threshold Voltage on LPC Rising Edge	Decrease VLPC from 0.05 Vo + 0.05, V_O = 15 V, $V_O = V_{DD}$	0.7	0.8	0.9	V
$t_{BNK-DIS}$	Blanking Time at the Falling Edge of V_{LPC}	Prevent LPC Spike to Turn−Off Gate	–	350	–	ns
$V_{LPC-CLAMP-H}$	Higher Clamp Voltage (Note 3)		–	6	–	V
$V_{LPC-DIS}$	LPC Voltage to Disable SR Gate		4.0	4.2	4.4	V
$t_{LPC-HIGH}$	Debounce Time for Disable SR Gate		–	1	–	μs

ELECTRICAL CHARACTERISTICS (V_{DD} = 15 V and T_A = 25°C unless otherwise noted) (continued)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
RES SECTION						
V_{RES-EN}	Threshold Voltage of V_{RES} to Enable SR MOSFET		0.60	0.75	0.90	V
$t_{RES-LOW}$	Debounce Time to Disable RES Function		–	1	2	μs
$V_{RES-CLAMP-H}$	Higher Clamp Voltage (Note 3)		–	6	–	V
$K_{RES-DROP}$	RES Dropping Protection Ratio within One Cycle		–	90	–	%
$t_{RES-DROP}$	Debounce Time for RES Voltage−Drop Protection		–	1.5	–	μs
INTERNAL TIMING SECTION						
t_{CT}	Linear Operation Range of C_T	V_{LPC} = 1.5 V	27	30	33	μs
V_{LPC-OP}	Linear Operation Range of LPC to Charge C_T	V_{DD} < 5 V	0.8	–	3.4	V
		V_{DD} > 5 V	0.8	–	4.0	V
V_{RES-OP}	Linear Operation Range of RES to Discharge C_T	V_{DD} < 5 V	0.8	–	3.4	V
		V_{DD} > 5 V	0.8	–	4.0	V
$Ratio_{LPC-RES}$	Ratio Between LPC and RES		4.65	5.00	5.35	
t_{LPC-EN}	Minimum LPC Time to Enable SR Switching, $V_{LPC-HIGH}$ > V_{LPC-EN}		0.9	1.1	1.3	μs
$t_{gate-limit}$	t_{on-SR} (n + 1) < $t_{gate-limit}$ x t_{on-SR} (n)		105	–	120	%
GREEN SECTION						
$t_{GREEN-OFF}$	C_T Capacitor t_{DIS} Time to Leave Green Mode	f_S = 65 kHz	4.60	5.35	6.10	μs
$t_{GREEN-ON}$	C_T Capacitor t_{DIS} Time to Enter Green Mode	f_S = 65 kHz	4.25	4.80	5.35	μs
$t_{GREEN-TIME-enter}$	Cycle Time to Enter Green Mode	C_T Discharge Time < $t_{GREEN-ON}$	–	3	–	Times
$t_{GREEN-TIME-leave}$	Cycle Time to Leave Green Mode	C_T Discharge Time > $t_{GREEN-OFF}$	–	7	–	Times
$t_{GREEN-ENTER}$	No Gate Signal to Enter Green Mode (Note 3)		–	75	–	μs
CAUSAL FUNCTION SECTION						
t_{CAUSAL}	Once t_{S-PWM} (n + 1) > t_{CAUSAL} x t_{S-PWM} (n), SR Stops Switching and Enter Green Mode	f_S = 65 kHz → 40 kHz	–	120	–	%
tDEAD−CAUSAL	SR Turn−off Dead Time by Causal Function	f_S = 65 kHz	380	580	780	ns
$t_{DEAD-CFR}$	Dead Time to Shrink SR ON Time	CFR (Causal Function Regulator)	–	150	–	ns
$t_{DEAD-RE-CFR}$	SR ON Time Narrowed Down Width when $t_{DEAD-CFR}$ Triggered		–	1.5	–	μs
INTERNAL OVER−TEMPERATURE PROTECTION SECTION						
T_{OTP}	Internal Threshold Temperature for OTP (Note 3)		–	140	–	°C
$T_{OTP-HYST}$	Hysteresis Temperature for Internal OTP (Note 3)		–	20	–	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

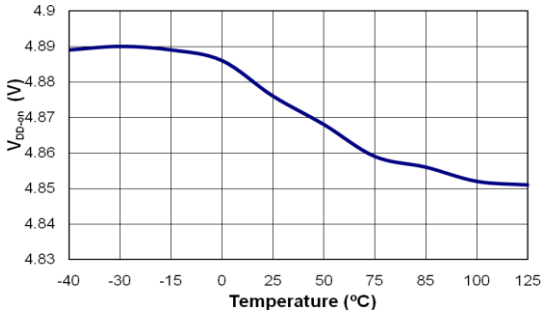


Figure 5. Turn−On Threshold Voltage

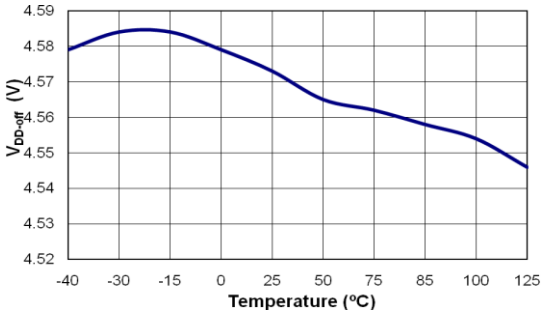


Figure 6. Turn−Off Threshold Voltage

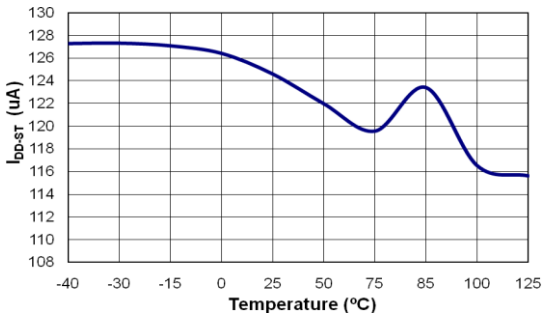


Figure 7. Startup Current

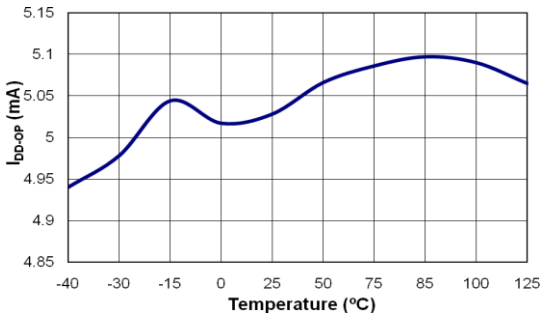


Figure 8. Operating Current

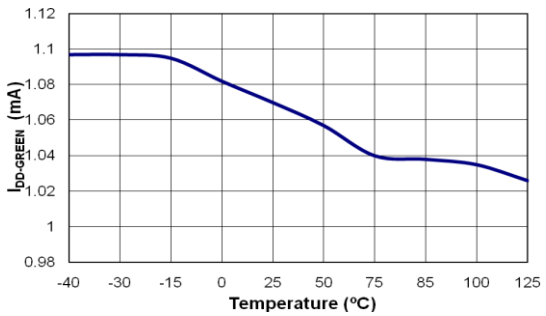


Figure 9. Operating Current in Green Mode

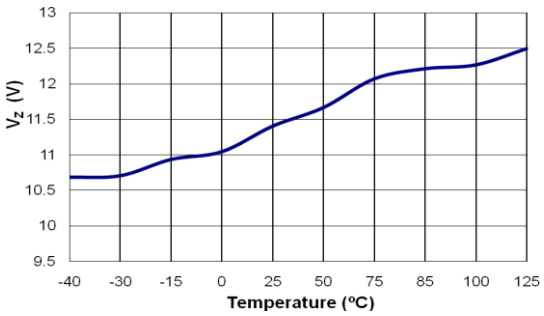


Figure 10. Gate Output Clamping Voltage

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

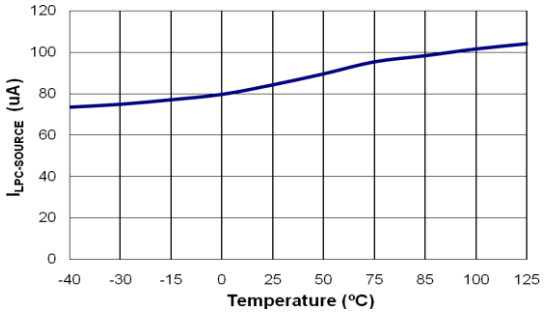


Figure 11. LPC Source Current

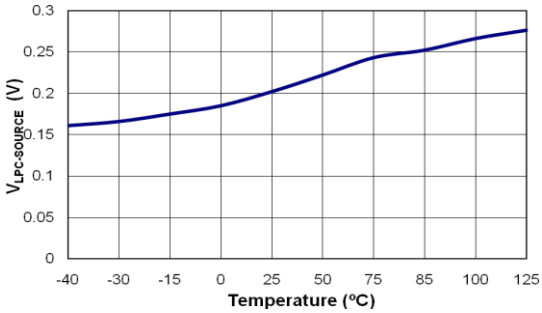


Figure 12. LPC Lower Clamp Voltage

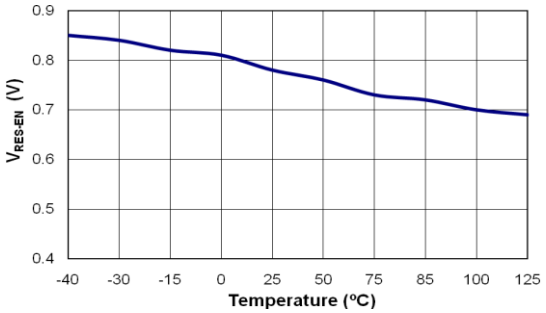


Figure 13. Threshold Voltage of V_{RES}

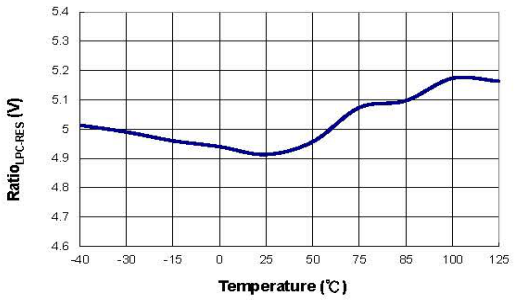


Figure 14. Ratio between LPC and RES

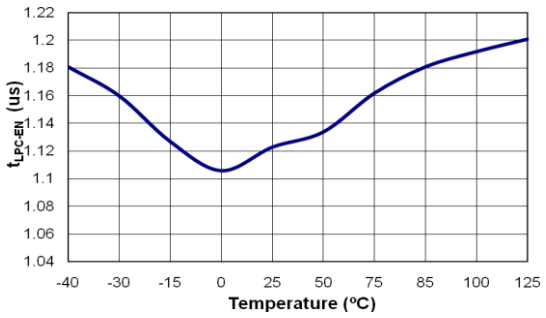


Figure 15. Minimum LPC Enable Time

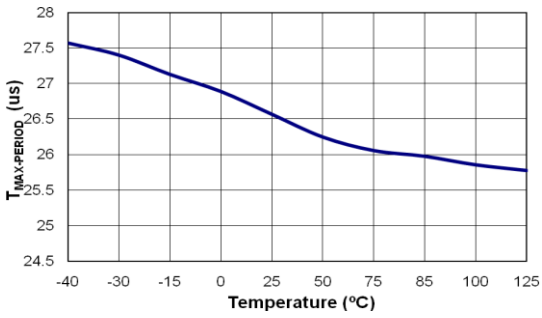


Figure 16. Maximum Period between LPC Rising Edge to Gate Falling Edge

FUNCTIONAL DESCRIPTION

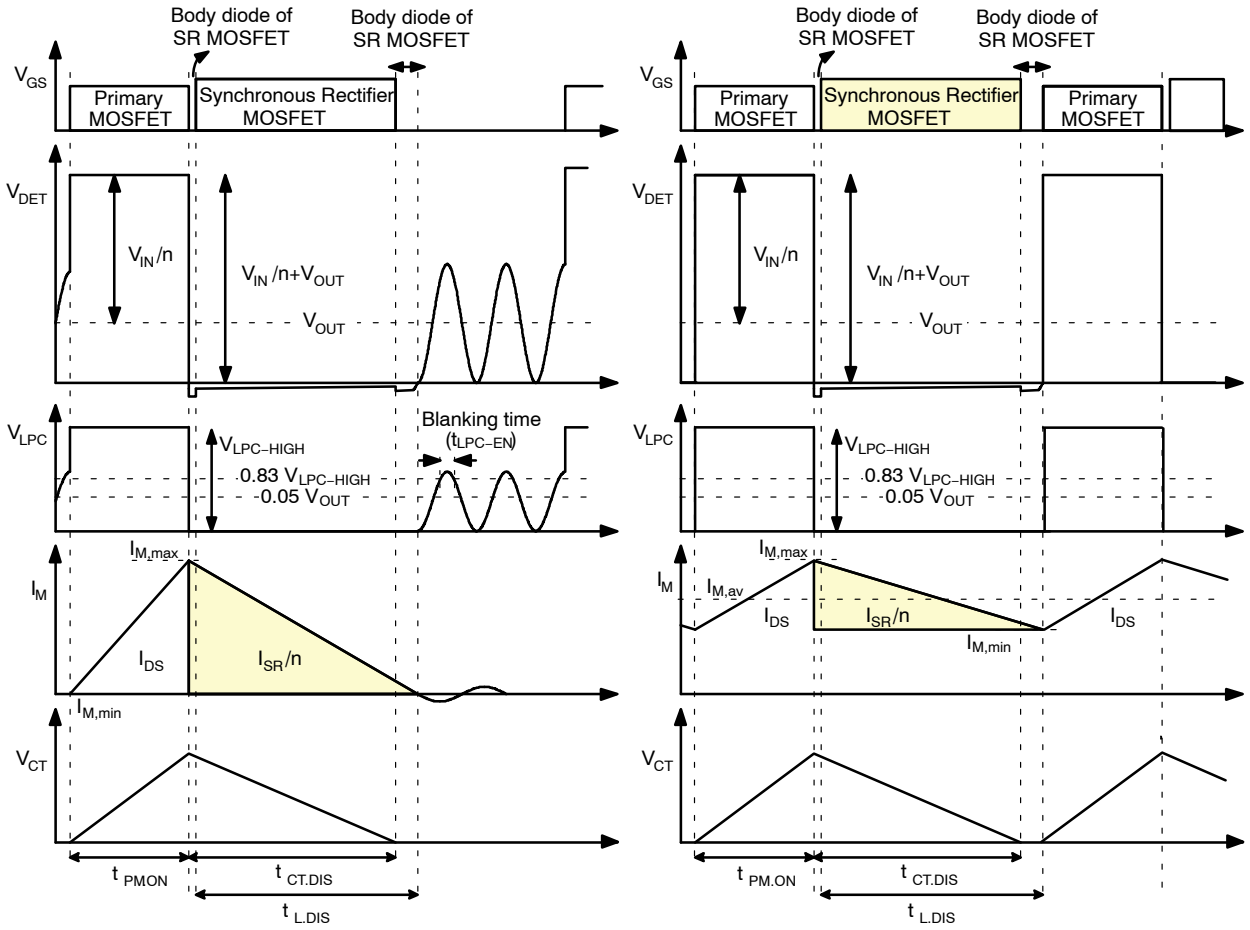


Figure 17. Typical Waveforms of Linear−Predict Timing Control in CCM and DCM/QR Flyback

Linear Predict Timing Control

The SR MOSFET turn−off timing is determined by linear−predict timing control and the operation principle is based on the volt−second balance theorem. The volt− second balance theorem states that the inductor average voltage is zero during a switching period in steady state, so the charge voltage and charge time product is equal to the discharge voltage and discharge time product. In flyback converters, the charge voltage on the magnetizing inductor is input voltage (V_{IN}), while the discharge voltage is nV_{OUT}, as the typical waveforms show in Figure 17. The following equation can be drawn:

$$V_{IN} \cdot t_{PM.ON} = n \cdot V_{OUT} \cdot t_{L.DIS} \quad \text{(eq. 1)}$$

where $t_{PM,ON}$ is inductor charge time and $t_{L,DIS}$ is inductor discharge time.

FAN6204A uses the LPC and RES pins with two sets of voltage dividers to sense DET voltage (V_{DET}) and output voltage (V_{OUT}), respectively; so V_{IN}/n, $t_{PM.ON}$, and V_{OUT} can be obtained. As a result, $t_{L,DIS}$, which is the on−time of SR MOSFET, can be predicted by Equation 1. As shown in Figure 17, the SR MOSFET is turned on when the SR MOSFET body diode starts conducting and DET voltage drops to zero. The SR MOSFET is turned off by linear−predict timing control.

Circuit Realization

The linear−predict timing−control circuit generates a replica (V_{CT}) of magnetizing current of flyback transformer using internal timing capacitor (C_T), as shown in Figure 18. Using the internal capacitor voltage, the inductor discharge time ($t_{L.DIS}$) can be detected indirectly, as shown in Figure 17. When CT is discharged to zero, the SR controller turns off the SR MOSFET.

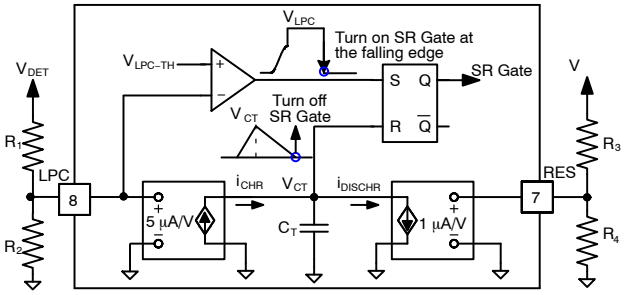


Figure 18. Simplified Linear−Predict Block

The voltage−second balance equation for the primary−side inductance of the flyback converter is given in Equation 1. Inductor current discharge time is given as:

$$t_{L.DIS} = \frac{V_{IN} \cdot t_{PM.ON}}{n \cdot V_{OUT}} \quad \text{(eq. 2)}$$

The voltage scale−down ratio between RES and LPC is defined as K below:

$$K = \frac{R_4 / (R_3 + R_4)}{R_2 / (R_1 + R_2)} \quad \text{(eq. 3)}$$

During $t_{PM.ON}$, the charge current of C_T is $i_{CHR} - i_{DICHR}$, while during $t_{L.DIS}$, the discharge current is i_{DICHR}. As a result, the current−second balance equation for internal timing capacitor (C_T) can be derived from:

$$\left(\frac{5}{K} \cdot \left(\frac{V_{IN}}{n} + V_{OUT}\right) - V_{OUT}\right) \cdot t_{PM.ON} = V_{OUT} \cdot t_{CT.DIS} \quad \text{(eq. 4)}$$

Therefore, the discharge time of C_T is given as:

$$t_{CT.DIS} = \frac{\left(\frac{5}{K} \cdot \left(\frac{V_{IN}}{n} + V_{OUT}\right) - V_{OUT}\right) \cdot t_{PM.ON}}{V_{OUT}} \quad \text{(eq. 5)}$$

When the voltage scale−down ratio between RES and LPC (K) is five (5), the discharge time of C_T ($t_{CT.DIS}$) is the same as inductor current discharge time ($t_{L.DIS}$). However, considering the tolerance of voltage divider resistors and internal circuit, the scale−down ratio (K) should be larger than five (5) to guarantee that $t_{CT.DIS}$ is shorter than $t_{L.DIS}$. It is typical to set K around 5~5.5.

Referring to Figure 17; when LPC voltage is higher than V_{LPC-EN} over a blanking time (t_{LPC-EN}) and lower than $V_{LPC-TH-HIGH}$ (0.05 V_{OUT}), then SR MOSFET can be triggered. Therefore, V_{LPC-EN} must be lager than $V_{LPC-TH-}$HIGH or the SR MOSFET cannot be turned on. When designing the voltage divider of LPC, R_1 and R_2 should be considered as:

$$0.83 \cdot \frac{R_2}{R_1 + R_2} \cdot \left(\frac{V_{IN.MIN}}{n} + V_{OUT}\right) > 0.05\, V_{OUT} + 0.3 \quad \text{(eq. 6)}$$

On the other hand, the linear operation ranges of LPC and RES (1~4 V) should be considered as:

$$\frac{R_2}{R_1 + R_2} \cdot \left(\frac{V_{IN.MAX}}{n} + V_{OUT}\right) < 4 \quad \text{(eq. 7)}$$

$$\frac{R_4}{R_3 + R_4} \cdot V_{OUT} < 4 \quad \text{(eq. 8)}$$

CCM Operation

The typical waveforms of CCM operation in steady state are shown as Figure 17. When the primary−side MOSFET is turned on, the energy is stored in L_m. During the on−time of the primary−side MOSFET ($t_{PM.ON}$), the magnetizing current (I_M) increases linearly from $I_{M,min}$ to $I_{M,max}$. Meanwhile, internal timing capacitor (C_T) is charged by current source ($i_{CHR} - i_{DICHR}$) proportional to V_{IN}, so V_{CT} also increases linearly.

When the primary−side MOSFET is turned off, the energy stored in L_m is released to the output. During the inductor discharge time ($t_{L.DIS}$), the magnetizing current (I_M) decreases linearly from $I_{M,max}$ to $I_{M,min}$. At the same time, the internal timing capacitor (C_T) is discharged by current source (i_{DISCHR}) proportional to V_{OUT}, so V_{CT} also decreases linearly. To guarantee the proper operation of SR, it is important to turn off SR MOSFET just before SR current reaches $I_{M,min}$ so that the body diode of SR MOSFET conducts naturally during the dead time.

DCM / QR Operation

In DCM / QR operation, when primary−side MOSFET is turned off, the energy stored in L_m is fully released to the output at the turn−off timing of primary−side MOSFET. Therefore, the DET voltage continues resonating until the primary−side MOSFET is turned on, as depicted in Figure 17. While DET voltage is resonating, DET voltage and LPC voltage drop to zero by resonance, which can trigger the turn−on of the SR MOSFET. To prevent fault triggering of the SR MOSFET in DCM operation, blanking time is introduced to LPC voltage. The SR MOSFET is not turned on even when LPC voltage drops below 0.05 V_{OUT} unless LPC voltage stays above 0.83 $V_{LPC-HIGH}$ longer than the blanking time (t_{LPC-EN}). The turn−on timing of the SR MOFET is inhibited by gate inhibit time ($t_{INHIBIT}$), once the SR MOSFET turns off, to prevent fault triggering.

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Green−Mode Operation

To minimize the power consumption at light−load condition, the SR circuit is disabled when the load decreases. As illustrated in Figure 19, the discharge times of inductor and internal timing capacitor decrease as load decreases. If the discharge time of the internal timing capacitor is shorter than $t_{GREEN-ON}$ (around 4.8 µs) for more than three cycles, the SR circuit enters Green Mode. Once FAN6204A enters Green Mode, the SR MOSFET stops switching and the major internal block is shut down to further reduce operating current of the SR controller. In Green Mode, the operating current reduces to 1.1 mA. This allows power supplies to meet the most stringent power conservation requirements.

When the discharge time of the internal capacitor is longer than $t_{GREEN-OFF}$ (around 5.35 μs) for more than seven cycles, the SR circuit is enabled and resumes the normal operation, as shown in Figure 20.

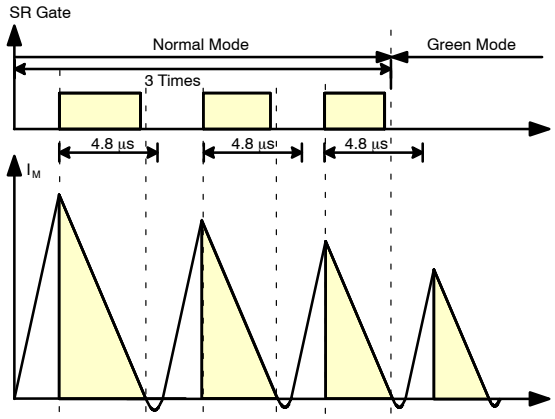

Figure 19. Entering Green Mode

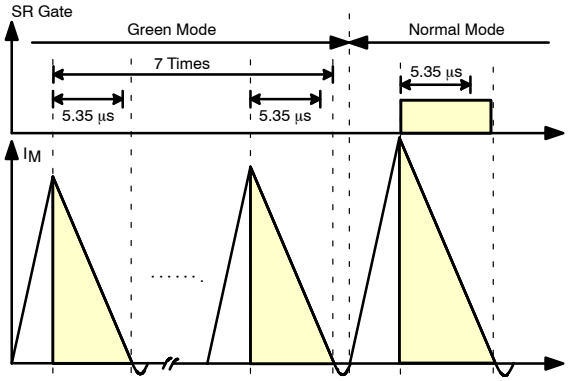

Figure 20. Resuming Normal Operation

Causal Function

Causal function is utilized to limit the time interval (t_{SR-MAX}) from the rising edge of V_{LPC} to the falling edge of the SR gate. t_{SR-MAX} is limited to 97% of previous switching period, as shown in Figure 21. When the system operates at fixed frequency, whether voltage−second balance theorem can be applied or not, causal function can guarantee reliable operation.

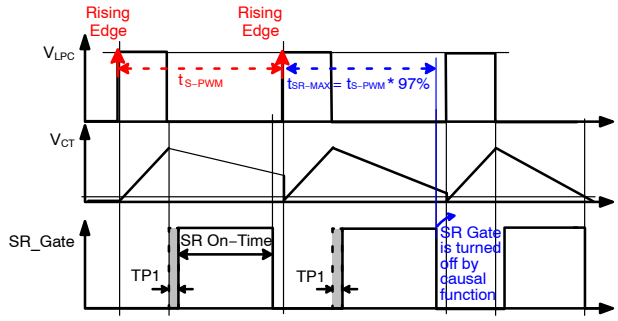

Figure 21. Causal Function Operation

Fault Causal Timing Protection

Fault causal timing protection is utilized to disable the SR gate under some abnormal conditions. Once the switching period (t_{S-PWM} (n)) is longer than 120% of previous switching period (t_{S-PWM} (n−1)), SR gate is disabled and enters Green Mode, as shown in Figure 22. Since the rising edge of V_{LPC} among switching periods (t_{S-PWM}) is tracked for causal function, the accuracy of switching period is important. Therefore, if the detected switching period has a serious variation under some abnormal conditions, the SR gate should be terminated to prevent fault trigger.

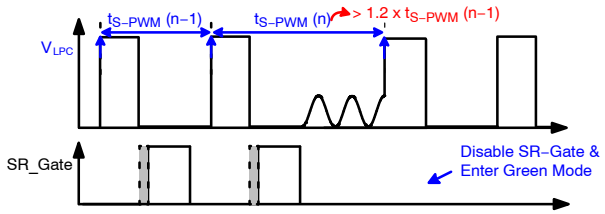

Figure 22. Fault Causal Timing Protection

Gate Expand Limit Protection

Gate expand limit protection controls on−time expansion of the SR MOSFET. Once the discharge time of the internal timing capacitor ($t_{DIS.CT}$) is longer than 115% of previous on time of the SR MOSFET (t_{on-SR} (n−1)); t_{on-SR} (n) is limited to 115% of t_{on-SR} (n−1), as shown in Figure 23. When output load changes rapidly from light load to heavy load, voltage−second balance theorem may not be applied. In this transient state, gate expand limit protection is activated to prevent overlap between SR gate and PWM gate.

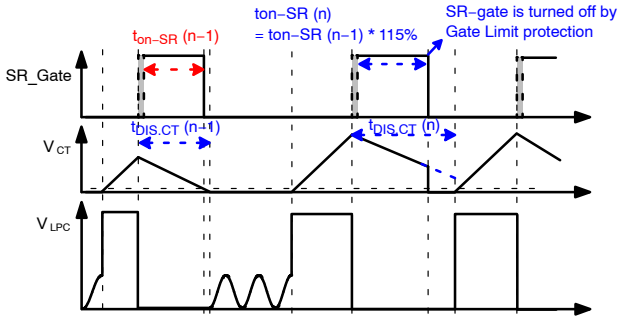

Figure 23. Gate Expand Limit Protection

RES Voltage Drop Protection

RES voltage drop protection prevents V_{RES} dropping too much within a cycle. The V_{RES} is sampled as a reference voltage, V_{RES}', on V_{LPC} rising edge. Once V_{RES} drops below 90% of V_{RES}' for longer than a debounce time ($t_{RES-DROP}$), the SR gate is turned off immediately, as shown in Figure 24. When output voltage drops rapidly within a switching cycle, voltage−second balance may not be applied, RES dropping protection is activated to prevent overlap.

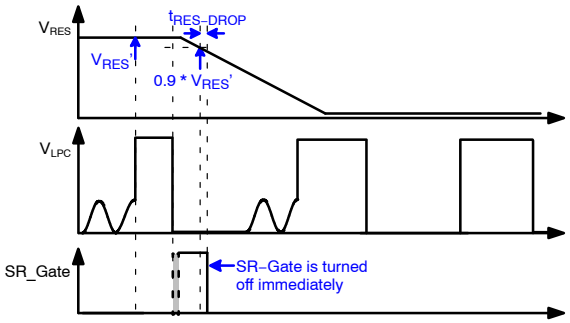

Figure 24. V_{RES} Dropping Protection

LPC Pin Open / Short Protection

LPC−Open Protection: If V_{LPC} is higher than $V_{LPC-DIS}$ (4.2 V) for longer than debounce time $t_{LPC-HIGH}$, FAN6204A stops switching immediately and enters Green Mode. V_{LPC} is clamped at 6 V to avoid LPC pin damage.

LPC−Short Protection: If V_{LPC} is pulled to ground and the charging current of timing capacitor (C_T) is near zero, so that SR gate is not output.

RES Pin Open / Short Protection

RES−Open Protection: If V_{RES} is pulled to HIGH level, the gate signal is extremely small and FAN6204A enters Green Mode. In addition, V_{RES} is clamped at 6 V to avoid RES pin damage.

RES−Short Protection: If V_{RES} is lower than V_{RES-EN} (0.7 V) for longer than debounce time $t_{RES-LOW}$, FAN6204A stops switching immediately and enters Green Mode.

Under−Voltage Lockout (UVLO)

The power ON and OFF V_{DD} threshold voltages are fixed at 4.8 V and 4.5 V, respectively. With an ultra−low V_{DD} threshold voltage, FAN6204A can be used in various output voltage applications.

V_{DD} Pin Over−Voltage Protection (OVP)

Over−voltage conditions are usually caused by an open feedback loop. V_{DD} over−voltage protection prevents damage on the SR MOSFET. When the voltage on VDD pin exceeds 27.5 V, the SR controller stops switching the SR MOSFET.

Over−Temperature Protection (OTP)

To prevent SR gate from fault triggering in high temperatures, internal over−temperature protection is integrated in FAN6204A. Once the temperature is over 140°C, SR gate is disabled until the temperature drops below 120°C.

ORDERING INFORMATION

Part Number	Package	Operating Temperature Range	Shipping†
FAN6204AMX	8−Pin, Small Outline Package (SOP) (Pb−Free)	−40°C to +105°C	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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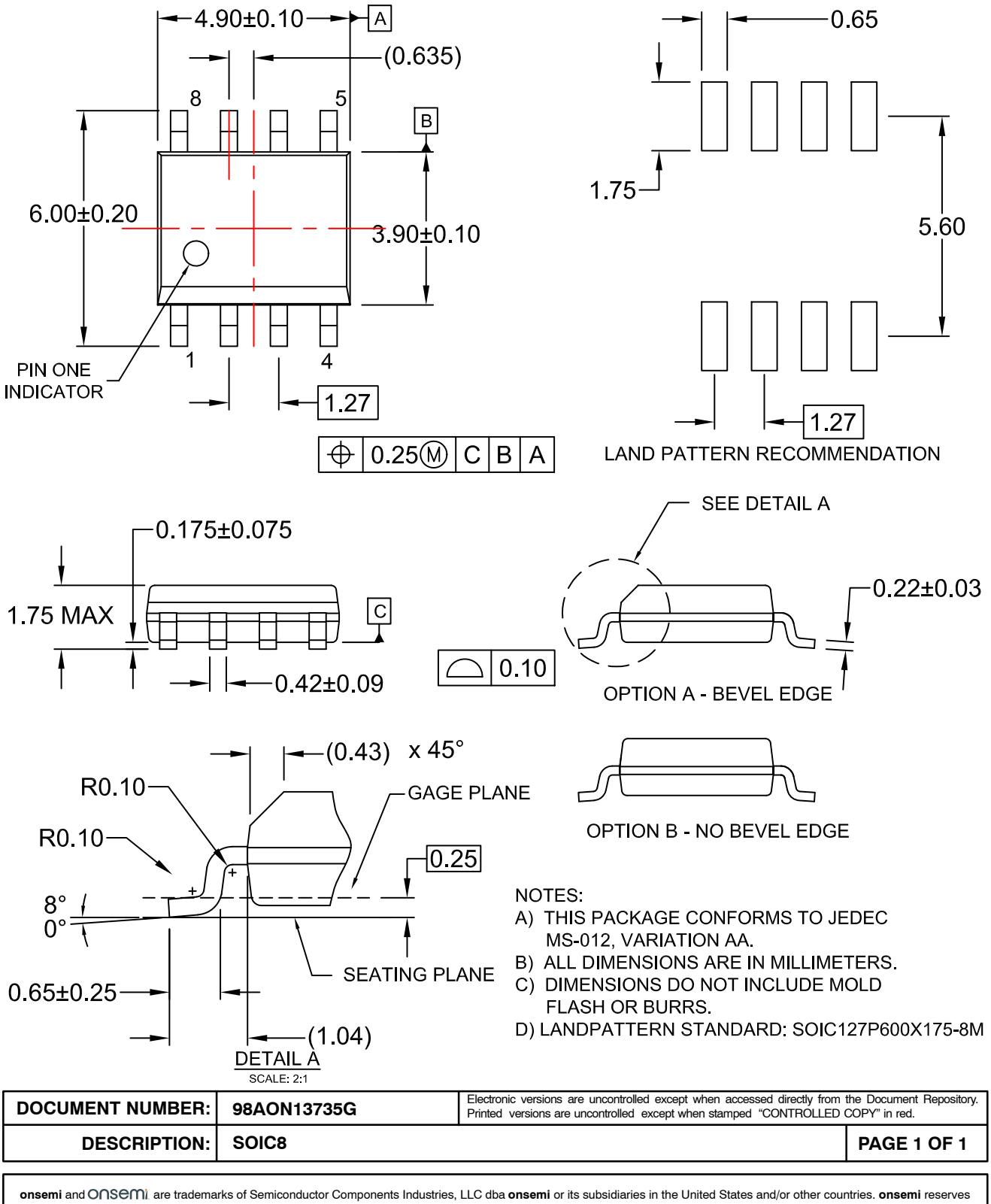

NOTES:
A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M

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