TPS65951 Silicon Errata

This document describes the TPS65951 bugs, limitations, and enhancements with suggested workarounds.

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1 In master mode, an increase to 32-kHz jitter occurs when voice path is on

Impact:

32-kHz oscillator: 32-kHz clock jitter increases.

Description:

In all I/O buffers, analog ground was shorted with digital ground through CDM (charge device model).

Workaround:

No workaround.

2 Pop noise on headset output occurs while using 5-wire connection

Impact:

Audio: Pop noise occurs on headset output in 5-wire connection.

Description:

Because switching on of amplifier HSO and amplifier HSOVMID cannot be simultaneous, as their enables are in different registers, a pop noise is heard on the headset in 5-wires connection.

Workaround:

Software: In 5-wire configuration, the pop noise is attenuated by changing the register setting sequencing:

Power Up:

- VMID_EN = 1
- RAMP_EN = 1
- HS amplifier enabled
- HSOVMID amplifier enabled

Power Down:

- HSOVMID amplifier disabled
- HS amplifier disabled
- RAMP_EN = 0
- VMID_EN = 0

3 VIO cannot be disabled in slave mode

Impact:

Disabling VIO in slave mode is not supported.

Description:

In slave mode, even if the IO_1P8 device power is provided by an external supply instead of VIO, it is not possible to turn off the VIO regulator. This is because the internal clocking of the device uses the RC oscillator of the VIO regulator and disabling the regulator also disables the clock preventing the device from functioning correctly.

Workaround:

VIO can be placed in sleep mode instead of off. The VIO current in sleep mode is 20 µA typical and 50 µA maximum.

4 Inband tone occurs in ADC path when Fs = 32 kHz, and when MCLK = 19.2 or 38.4 MHz

Impact:

No functional impact.

Description:

~ 5 kHz to 9 kHz tone at approximately –80 dBFs in uplink path when the sampling rate is 32 kHz and when the master clock is 19.2 MHz or 38.4 MHz. There is no issue when the master clock is 26 MHz.

Workaround:

No workaround.

5 Leakage exists between the 32KXIN input pad and ground path

Impact:

There will be some leakage between the 32KXIN pad and the ground path based on the input voltage applied.

Description:

When the crystal oscillator is in bypass mode, the 32KXIN input pad should be in high-impedance mode. However, this is not the case. This allows a leakage path between this pad and ground. The following table shows the relation between the input voltage and the leakage.

Input Voltage (V)	Input Impedance kΩ (From Ground)		Input Leakage, µA (To Ground)	
	Minimum	Maximum	Minimum	Maximum
< 0.4	> 10 MΩ	> 10 MΩ	0.0	0.0
0.6	2960	> 10 MΩ	0.0	0.2
0.8	700	3550	0.1	1.2
1.0	350	530	1.8	2.9
1.2	180	330	3.7	6.3
1.4	120	240	6.1	10.8
1.6	90	190	8.8	15.8
1.8	70	160	12.1	21.5

Workaround:

No workaround.

6 Soft volume control feature limitation

Impact:

Soft volume limitation.

Description:

The soft volume control feature cannot be used under specific register settings. When SOFTVOL_CTL = 0x2F (bit0 = 1) and OPT_MODE = 1, there is an issue related to the digital fine gain control.

Workaround:

Soft volume can be used in the setting as shown in the following table.

Register OPTION = 0x02				Register RX_PATH_SEL		Can Soft Volume Work?
ARXR2_EN	ARXL2_EN	ARXR1_EN	ARXL1_VRX_EN	RXL1_SEL	RXR1_SEL	
1	1	0	0	0X0 or 0x1	0x0 or 0x1	No
1	1	0	0	0x2 or 0x3	0x2 or 0x3	Yes

7 An automatic error defect occurs

Impact:

This is different than charger error detection. A normal charger error differs from this behavior and is working as expected. This does not block any functionality.

Description:

Specification description:

When a charger is enabled (USBCHRG_ENZ asserted to low), a timer of 2.5 seconds minimum starts. Until the time-out, all errors are masked. At the end of the time-out, if charging has not started yet (USBCHRG_STATZ = 1), an automatic error is asserted and USBCHRG_ENZ is released high during 100 ms.

According to design specification this behavior should loop until the USBCHRG_STATZ pin is asserted low by the charger.

Observed behavior:

If the charger never acknowledges the charge (by setting the USBCHRG_STATZ pin low within 2.5 seconds after the USBCHRG_ENZ pin is asserted by the TPS65951), the automatic error is generated only once and USBCHRG_ENZ is reasserted high only once.

A normal charger error differs from this behavior and is working as expected.

Workaround:

No workaround.

8 After error detection, the BCI FSM (state-machine) can go from IDLE to CHARGE state in 61 µs (Typ) while a delay of 135.8 ms (Typ) is expected

Impact:

When the BQ is in error, the TPS65951 BCI FSM (in hardware/precharge mode) enables charge (setting USBCHRG_ENZ signal low) every 2 ms instead of every CHG_ERROR100MS (= 135.8 ms typ). This causes the BQ error pulse to be sent more frequently, but it has no functional impact (charge not starting), nor does it have a reliability impact on the BQ.

Description:

Expected behavior:

When in hardware/precharge mode and an error is detected in the external charger (for example, the BQ watchdog expires):

1. The BCI FSM should go back to IDLE state (disabling charge by setting the USBCHRG_ENZ signal high), and wait for CHG_ERROR100MS (= 135.8 ms typ).
2. The BCI FSM should then return to CHARGE state (USBCHRG_ENZ signal low) to see if the BQ recovers.
3. Here error should be masked for CHG_ERROR2S5 (= 3.4 seconds typ). If after CHG_ERROR2S5 error is detected, then USBCHRG_ENZ should go back to 1).

The FSM should loop between IDLE and CHARGE states this way: CHG_ERROR100MS (= 135.8 ms typ) in IDLE state (USBCHRG_ENZ signal high), CHG_ERROR2S5 (= 3.4 seconds typ) in CHARGE state (USBCHRG_ENZ signal low).

Behavior seen:

1. The BCI FSM goes back to IDLE state (disabling charge by setting the USBCHRG_ENZ signal high) and waits for CHG_ERROR100MS (= 135.8 ms typ).
2. The BCI FSM returns to CHARGE state (USBCHRG_ENZ signal low) to see if the BQ recovers.
3. Here a new error is detected as soon as sent by the BQ (masking for CHG_ERROR2S5 [= 3.4 seconds typ] not working for this particular BQ error, and the delay signal [delayed for CHG_ERROR100MS] is not asserted).
4. The BCI returns to IDLE state and waits only for two clock cycles (= 61 µs typ).
5. The BCI returns to CHARGE state (sets USBCHRG_ENZ signal low) until the next error from the BQ (coming after 2 ms when BQ in error and charge enabled).

6. Looping between steps 4 and 5.

   The FSM loops between IDLE and CHARGE states this way: 61 µs in IDLE state, 2 ms in CHARGE state.

When the charging watchdog in the TPS65951 expires, the BCI sets the USBCHRG_ENZ signal high (signal stays high), and the BQ stops sending error pulses.

Workaround:

No workaround.

9 Spikes occur on HFCLKOUT during switch on following an asynchronous switch off

Impact:

After an asynchronous switch off (that is, PWRON_8s or WD-event), spikes occur on HFCLKOUT during the next switch on. The spikes occur after CLKEN is asserted, but before NRESPWRON is asserted. Because they occur before NRESPWRON, there should be no system impact.

Description:

Expected behavior:

Globally, HFCLKOUT is gated by the clkout signal resync on mclk, which is present only when clken is available (and hfclkin is present). See Figure 1.

- Normal/controlled switch off:
  - clkout is switched off before clken → the mclk clock is available after clkout goes low and the resynchronized enable of hfclkout GCM is properly disabled.
- PWRON_8s and any “async” switch-off events like watchdog:
  - clkout and clken are reset together → the resynchronized enable stays high until the next mclk clock cycle, which comes during the next switch on (when clken and hfclkin are present), so the hfclkout will be gated after one or two hfclkin clock cycles only. Due to this, spikes are seen on HFCLKOUT during the switch on following an asynchronous switch off.

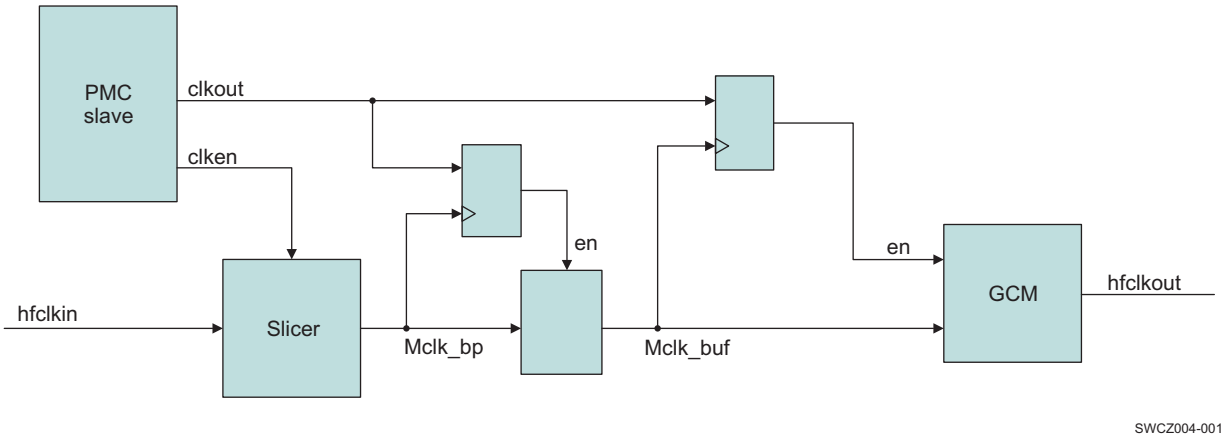

Figure 1. Block Diagram of HFCLKOUT Gating

Workaround:

No workaround.

10 DC load regulation of some external LDO regulators is higher than the maximum value specified

Impact:

The DC load is out of specification for some LDOs.

Description:

Due to important package parasitics, the DC load regulation of the VAUX1, VAUX3, VMMC1, and VPLL1 regulators is out of specification.

The following table presents the current specification and the new specification.

Regulator	Parameter	Test Conditions	Current Specification	New Specification	Unit
			Maximum	Maximum	
VAUX1	DC load regulation	On mode: 0 < IO < IMAX	20	40	mV
VAUX3	DC load regulation	On mode: 0 < IO < IMAX	20	40	mV
VMMC1	DC load regulation	On mode: 0 < IO < IMAX	20	35	mV
VPLL1	DC load regulation	On mode: 0 < IO < IMAX	20	25	mV

Workaround:

No workaround.

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