# TPS255x Adjustable Current-Limited Power-Distribution Switches

## 1 Features

- Adjustable current-limit, 100 mA–1100 mA
- Fast overcurrent response - 2 µS typical
- 94-mΩ high-side MOSFET (DBV package)
- Reverse input-output voltage protection
- Operating range: 2.5 V to 6.5 V
- Deglitched fault report
- 1-µA maximum standby supply current
- Junction temperature range: –40°C to 125°C
- Built-in soft-start
- 15 kV ESD protection (with external capacitance)
- UL listed – file No. E169910
- Current-limit resistor calculator – SLVC163

## 2 Applications

- USB Ports/Hubs
- Cell phones
- Laptops
- Heavy Capacitive Loads
- Reverse-Voltage Protection

## 3 Description

The TPS2550/51 power-distribution switch is intended for applications where heavy capacitive loads and short-circuits are likely to be encountered, incorporating a 100-mΩ, N-channel MOSFET in a single package. The current-limit threshold is user adjustable between 100 mA and 1.1 A via an external resistor. The power-switch rise and fall times are controlled to minimize current surges during switching.

The device limits the output current to a desired level by switching into a constant-current mode when the output load exceeds the current-limit threshold or a short is present. An internal reverse-voltage detection comparator disables the power-switch in the event that the output voltage is driven higher than the input to protect devices on the input side of the switch. The $\overline{\text{FAULT}}$ logic output asserts low during both overcurrent and reverse-voltage conditions.

**Package Information**

| PART NUMBER | PACKAGE(1) | BODY SIZE (NOM) |
|---|---|---|
| TPS255x | SOT-23 (6) | 2.90 mm × 1.60 mm |
| | WSON (6) | 2.00 mm × 2.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

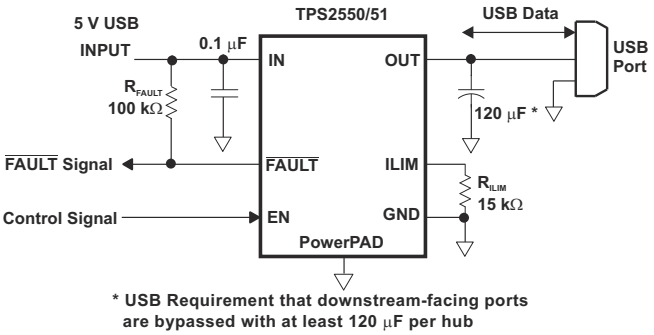



**Figure 3-1. Typical Application as USB Power Switch**

# Table of Contents



## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

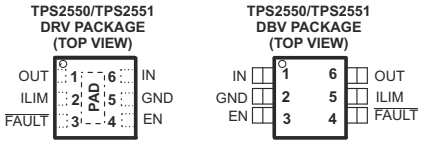
| Changes from Revision B (November 2008) to Revision C (October 2023) | Page |
|---|---|
| • Added GPN to beginning of title | 0 |
| • Updated the numbering format for tables, figures, and cross-references throughout the document | 1 |
| • Changed the high-side MOSFET resistance to 94-mΩ | 1 |
| • Moved the Device Comparison table | 1 |
| • Added a Package Information table, and removed the General Switch Catalog table | 1 |
| • Changed this section title to "Device Comparison Table" and reorganized so that it follows the Revision History section | 3 |
| • Changed this section title to "Pin Configuration and Functions", and added a pinout drawing before the Pin Functions table | 4 |
| • Updated the "ESD content" and the mark message | 5 |
| • Added "ESD Ratings" section | 5 |
| • Moved topic to follow the ESD Ratings section | 6 |
| • Changed this section title to "Thermal Information" | 6 |
| • Moved topic to follow the "Thermal Metrics" section | 6 |
| • Added "Functional Block Diagram" section | 12 |
| • Added "Device Functional Modes" section | 13 |
| • Added the "Design Requirements" section | 15 |
| • Added "Power Supply Recommendations" section | 19 |
| • Added "Layout" section | 20 |

## 5 Device Comparison Table

| DEVICE | AMBIENT TEMPERATURE(1) | ENABLE | SON (2) (DRV) | SOT23(2) (DBV) | RECOMMENDED MAXIMUM CONTINUOUS LOAD CURRENT |
|---|---|---|---|---|---|
| TPS2550 | –40°C to 85°C | Active low | TPS2550DRV | TPS2550DBV | 1.1 A |
| TPS2551 | | Active high | TPS2551DRV | TPS2551DBV | 1.1 A |

(1) Maximum ambient temperature is a function of device junction temperature and system level considerations, such as power dissipation and board layout. See *dissipation rating table* and *recommended operating conditions* for specific information related to these devices.
(2) Add an R suffix to the device type for tape and reel.

# 6 Pin Configuration and Functions




**EN = Active Low for the TPS2550**
**EN = Active High for the TPS2551**

**Table 6-1. Pin Functions**

| PIN | | | | | I/O | DESCRIPTION |
|---|---|---|---|---|---|---|
| NAME | TPS2550DBV | TPS2551DBV | TPS2550DRV | TPS2551DRV | | |
| $\overline{EN}$ | 3 | – | 4 | – | I | Enable input, logic low turns on power switch |
| EN | – | 3 | – | 4 | I | Enable input, logic high turns on power switch |
| GND | 2 | 2 | 5 | 5 | | Connect ground connection externally to POWER PAD |
| IN | 1 | 1 | 6 | 6 | I | Input voltage; connect a 0.1 µF or greater ceramic capacitor from IN to GND as close to the IC as possible. |
| $\overline{FAULT}$ | 4 | 4 | 3 | 3 | O | Active-low open-drain output, asserted during overcurrent, overtemperature, or reverse-voltage conditions. |
| OUT | 6 | 6 | 1 | 1 | O | Power-switch output |
| ILIM | 5 | 5 | 2 | 2 | I | External resistor used to set current-limit threshold; recommended 14.3 kΩ ≤ $R_{ILIM}$ ≤ 80.6 kΩ. |
| PowerPAD™ | – | – | PAD | PAD | | Internally connected to GND; used to heat-sink the part to the circuit board traces, connect to GND pin. |

# 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating free-air temperature range unless otherwise noted(1) (2)

| | | VALUE | UNIT |
|---|---|---|---|
| | Voltage range on IN, OUT, EN or $\overline{EN}$, ILIM, $\overline{FAULT}$ | –0.3 to 7 | V |
| | Voltage range from IN to OUT | –7 to 7 | V |
| $I_{OUT}$ | Continuous output current | Internally limited | |
| | Continuous total power dissipation | See "Thermal Information Table" | |
| | $\overline{FAULT}$ sink current | 25 | mA |
| | ILIM source current | 1 | mA |
| $T_J$ | Maximum junction temperature | –40 to 150 | °C |
| $T_{Sgt}$ | Storage temperature | –65 to 150 | °C |
| | Lead temperature 1,6 mm (1/16-inch) from case for 10 seconds | 300 | °C |

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Voltages are referenced to GND unless otherwise noted.

## 7.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101(2) | ±500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IN}$ | Input voltage, IN | | 2.5 | 6.5 | V |
| $V_{EN}$ | Enable voltage | TPS2550 | 0 | 6.5 | V |
| $V_{/EN}$ | | TPS2551 | 0 | 6.5 | |
| $I_{OUT}$ | Continuous output current, OUT | | 0 | 1.1 | A |
| $R_{ILIM}$ | Current-limit set resistor from ILIM to GND | | 14.3 | 80.6 | kΩ |
| $I_{/FAULT}$ | $\overline{FAULT}$ sink current | | 0 | 10 | mA |
| $T_J$ | Operating virtual junction temperature | DRV & DBV | –40 | 125 | °C |

## 7.4 Thermal Information

| BOARD | PACKAGE | THERMAL RESISTANCE $\theta_{JA}$ | THERMAL RESISTANCE $\theta_{JC}$ | $T_A \le 25°C$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25°C$ | $T_A = 70°C$ POWER RATING | $T_A = 85°C$ POWER RATING | $T_A = 110°C$ POWER RATING |
|---|---|---|---|---|---|---|---|---|
| Low-K(1) | DBV | 350°C/W | 55°C/W | 285 mW | 2.85 mW/°C | 155 mW | 114 mW | 42 mW |
| High-K(2) | DBV | 160°C/W | 55°C/W | 625 mW | 6.25 mW/°C | 340 mW | 250 mW | 93 mW |
| Low-K(1) | DRV | 140°C/W | 20°C/W | 715 mW | 7.1 mW/°C | 395 mW | 285 mW | 107 mW |
| High-K(2) | DRV | 75°C/W | 20°C/W | 1330 mW | 13.3 mW/°C | 730 mW | 530 mW | 200 mW |

(1) The JEDEC low-K (1s) board used to derive this data was a 3in × 3in, two-layer board with 2-ounce copper traces on top of the board.
(2) The JEDEC high-K (2s2p) board used to derive this data was a 3in × 3in, multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on top and bottom of the board.

## 7.5 Electrical Characteristics

over recommended operating junction temperature range, 2.5 V ≤ $V_{IN}$ ≤ 6.5 V, $R_{ILIM}$ = 14.3 kΩ, $V_{/EN}$ = 0 V, or $V_{EN}$ = 5.0 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS(1) | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **POWER SWITCH** | | | | | | | |
| $r_{DS(on)}$ | Static drain-source on-state resistance | DBV package, $T_J$ = 25 °C | | | 94 | 100 | mΩ |
| | | DBV package, –40 °C ≤$T_J$ ≤125 °C | | | | 140 | |
| | | DRV package, $T_J$ = 25 °C | | | 100 | 115 | |
| | | DRV package, –40 °C ≤$T_J$ ≤105 °C | | | | 145 | |
| | | DRV package, –40 °C ≤$T_J$ ≤125 °C | | | | 150 | |
| $t_r$ | Rise time, output | $V_{IN}$ = 6.5 V | $C_L$ = 1 µF, $R_L$ = 100 Ω, (see Figure 8-1) | | 1.0 | 1.5 | ms |
| | | $V_{IN}$ = 2.5 V | | | 0.65 | 1.0 | |
| $t_f$ | Fall time, output | $V_{IN}$ = 6.5 V | | 0.2 | | 0.5 | |
| | | $V_{IN}$ = 2.5 V | | 0.2 | | 0.5 | |
| **ENABLE INPUT EN OR $\overline{EN}$** | | | | | | | |
| $V_{IH}$ | High-level input voltage | | | 1.1 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | 0.66 | |
| $I_{EN}$ | Input current | $V_{EN}$ = 0 V or 6.5 V, $V_{/EN}$ = 0 V or 6.5 V | | –0.5 | | 0.5 | µA |
| $t_{on}$ | Turnon time | $C_L$ = 1 µF, $R_L$ = 100 Ω, (see Figure 8-1) | | | | 3 | ms |
| $t_{off}$ | Turnoff time | | | | | 3 | ms |
| **CURRENT LIMIT** | | | | | | | |
| $I_{OS}$ | Short-circuit current, OUT connected to GND | | $R_{ILIM}$ = 80.6 kΩ | 160 | 265 | 350 | mA |
| | | | $R_{ILIM}$ = 38.3 kΩ | 350 | 550 | 700 | |
| | | | $R_{ILIM}$ = 15 kΩ | 1100 | 1450 | 1700 | |
| $I_{OC}$ | Current-limit threshold (Maximum DC output current $I_{OUT}$ delivered to load) | | $R_{ILIM}$ = 80.6 kΩ | 340 | 365 | 390 | |
| | | | $R_{ILIM}$ = 38.3 kΩ | 670 | 715 | 755 | |
| | | | $R_{ILIM}$ = 15 kΩ | 1600 | 1700 | 1800 | |

## 7.5 Electrical Characteristics (continued)

over recommended operating junction temperature range, 2.5 V ≤ $V_{IN}$ ≤ 6.5 V, $R_{ILIM}$ = 14.3 kΩ, $V_{/EN}$ = 0 V, or $V_{EN}$ = 5.0 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS[1] | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{IOS}$ | Response time to short circuit | $V_{IN}$ = 5.0 V (see Figure 8-2) | | | 2 | | µs |
| **REVERSE-VOLTAGE PROTECTION** | | | | | | | |
| | Reverse-voltage comparator trip point ($V_{OUT}$ – $V_{IN}$) | | | 95 | 135 | 190 | mV |
| | Time from reverse-voltage condition to MOSFET turn off | $V_{IN}$ = 5.0 V | | 3 | 5 | 7 | ms |
| **SUPPLY CURRENT** | | | | | | | |
| $I_{IN\_off}$ | Supply current, low-level output | $V_{IN}$ = 6.5 V, No load on OUT, V $\overline{EN}$ = 6.5 V or $V_{EN}$ = 0 V, 14.3 kΩ ≤ $R_{ILIM}$ ≤ 80.6 kΩ | | | 0.1 | 1 | µA |
| $I_{IN\_on}$ | Supply current, high-level output | $V_{IN}$ = 6.5 V, No load on OUT, V $\overline{EN}$ = 0 V or $V_{EN}$ = 6.5 V | $R_{ILIM}$ = 15 kΩ | | | 150 | µA |
| | | | $R_{ILIM}$ = 80.6 kΩ | | | 130 | µA |
| $I_{REV}$ | Reverse leakage current | $V_{OUT}$ = 6.5 V, $V_{IN}$ = 0 V | $T_J$ = 25 °C | | 0.01 | 1 | µA |
| **UNDERVOLTAGE LOCKOUT** | | | | | | | |
| $V_{UVLO}$ | Low-level input voltage, IN | $V_{IN}$ rising | | | 2.35 | 2.45 | V |
| | Hysteresis, IN | $T_J$ = 25 °C | | | 25 | | mV |
| **$\overline{FAULT}$ FLAG** | | | | | | | |
| $V_{OL}$ | Output low voltage, $\overline{FAULT}$ | $I_{/FAULT}$ = 1 mA | | | | 180 | mV |
| | Off-state leakage | $V_{/FAULT}$ = 6.5 V | | | | 1 | µA |
| | $\overline{FAULT}$ deglitch | $\overline{FAULT}$ assertion or de-assertion due to overcurrent condition | | 5 | 7.5 | 10 | ms |
| | | $\overline{FAULT}$ assertion or de-assertion due to reverse-voltage condition | | 2 | 4 | 6 | ms |
| **THERMAL SHUTDOWN** | | | | | | | |
| | Thermal shutdown threshold | | | 155 | | | °C |
| | Thermal shutdown threshold in current-limit | | | 135 | | | °C |
| | Hysteresis | | | | 15 | | °C |

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

## 7.6 Typical Characteristics

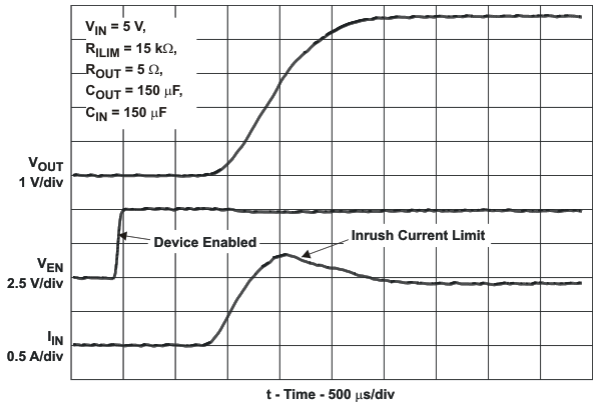



**Figure 7-1. Turnon Delay and Rise Time**

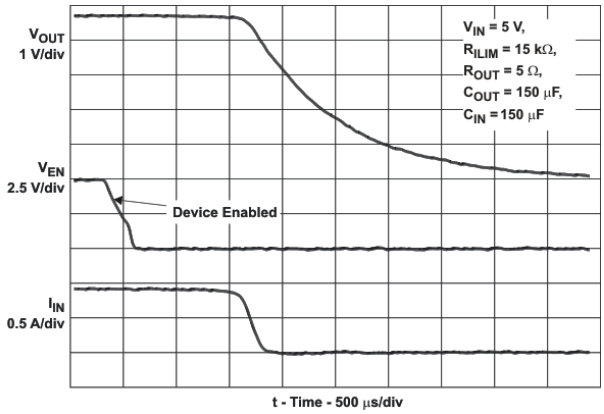



**Figure 7-2. Turnoff Delay and Fall Time**

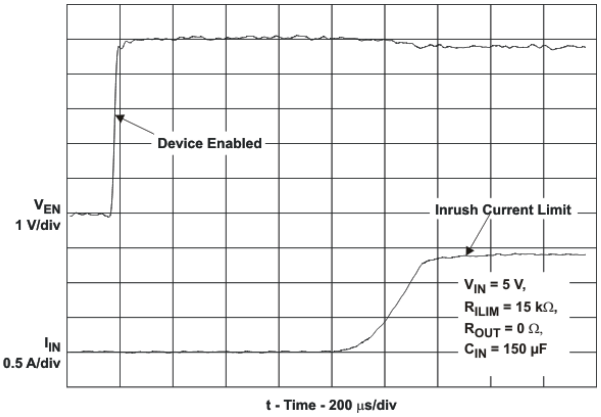



**Figure 7-3. Device Enabled into Short-Circuit**

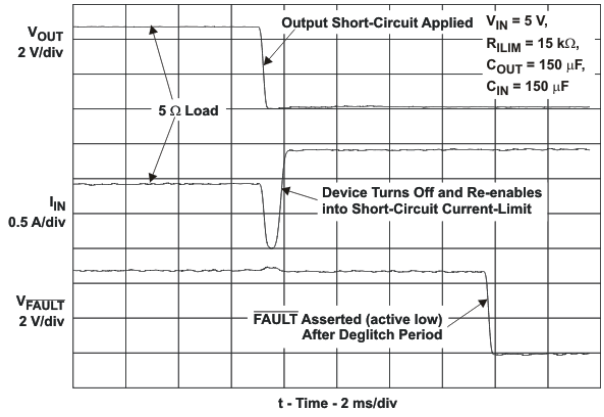



**Figure 7-4. Full-Load to Short-Circuit Transient Response**

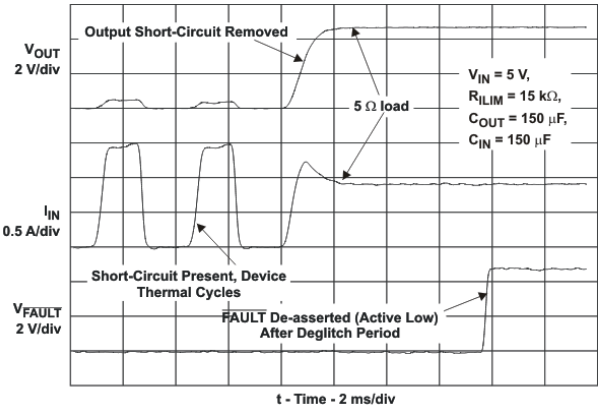



**Figure 7-5. Short-Circuit to Full-Load Recovery Response**

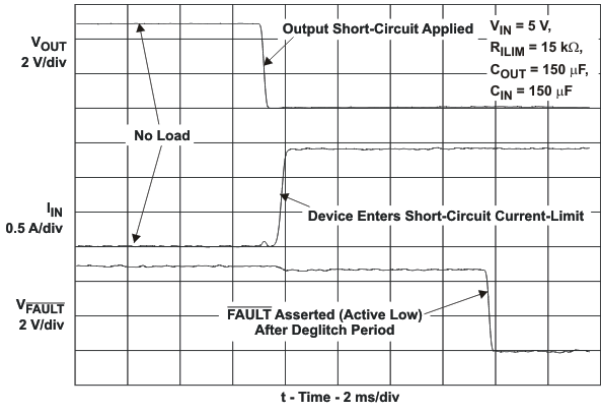



**Figure 7-6. No-Load to Short-Circuit Transient Response**

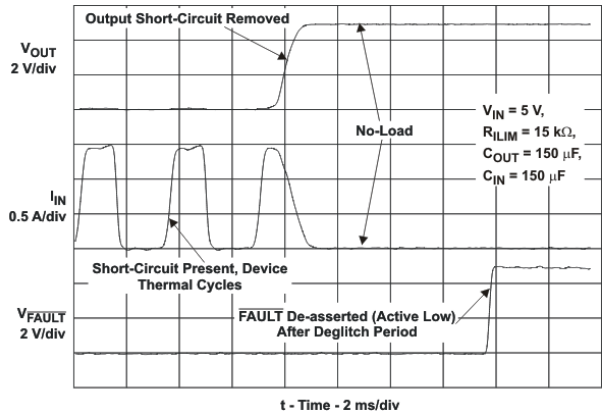



**Figure 7-7. Short-Circuit to No-Load Recovery Response**

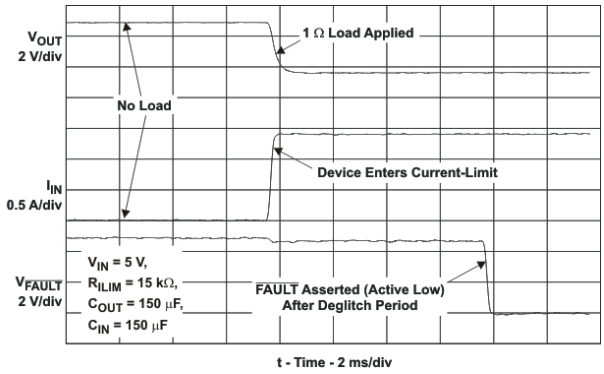



**Figure 7-8. No Load to 1Ω Transient Response**

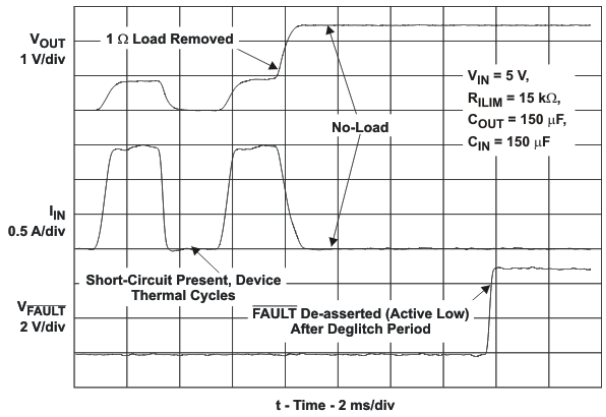



**Figure 7-9. 1Ω to No Load Transient Response**

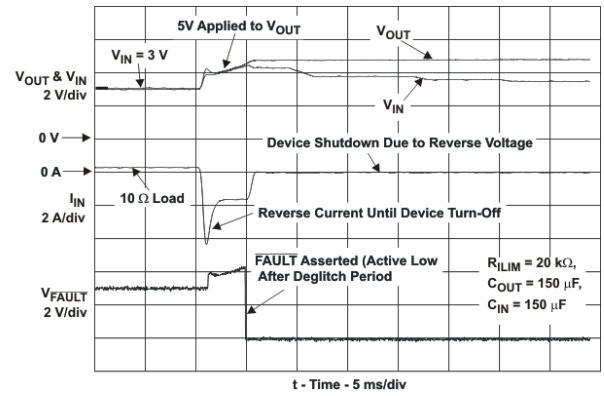



**Figure 7-10. Reverse-Voltage Protection Response**

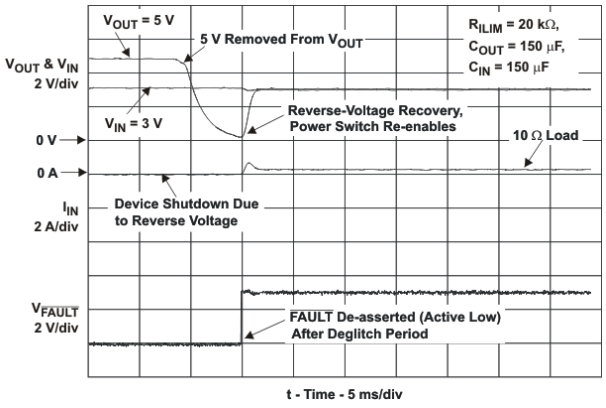



**Figure 7-11. Reverse-Voltage Protection Recovery**

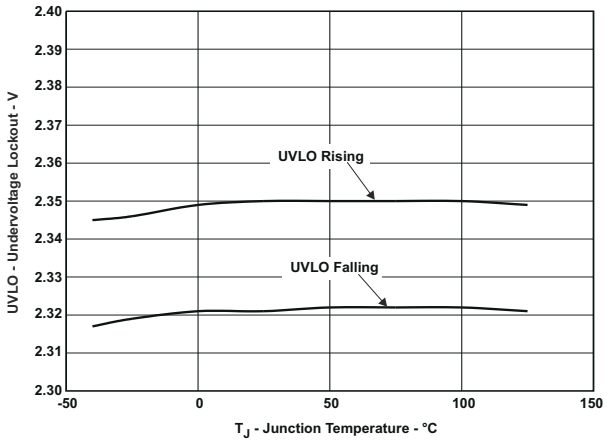



**Figure 7-12. UVLO – Undervoltage Lockout – V**

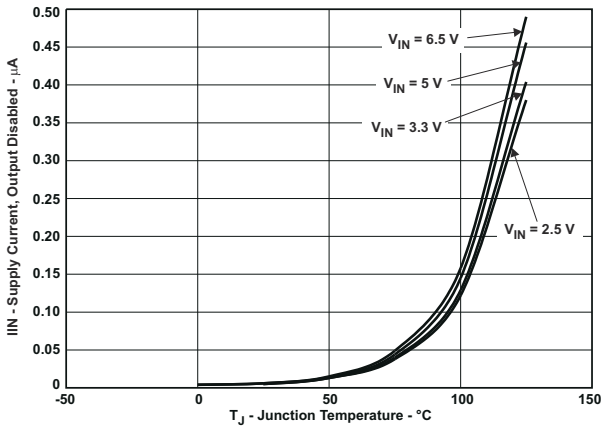



**Figure 7-13. $I_{IN}$ – Supply Current, Output Disabled – µA**

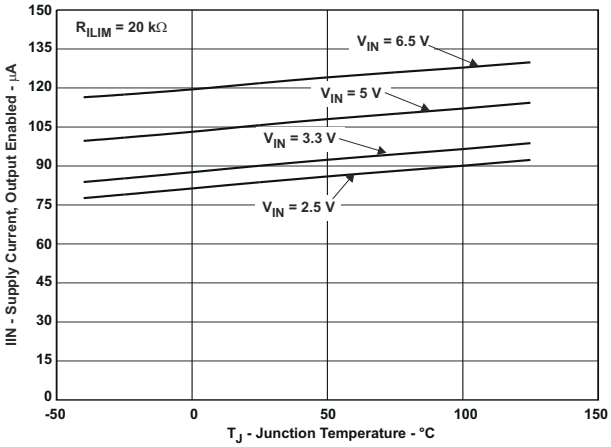



**Figure 7-14. $I_{IN}$ – Supply Current, Output Enabled – µA**

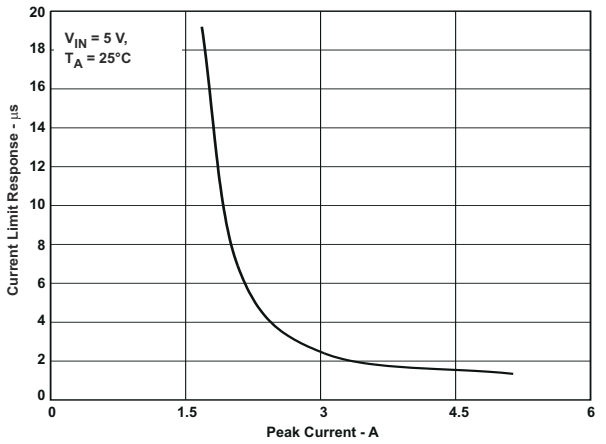



**Figure 7-15. Current Limit Response – µs**

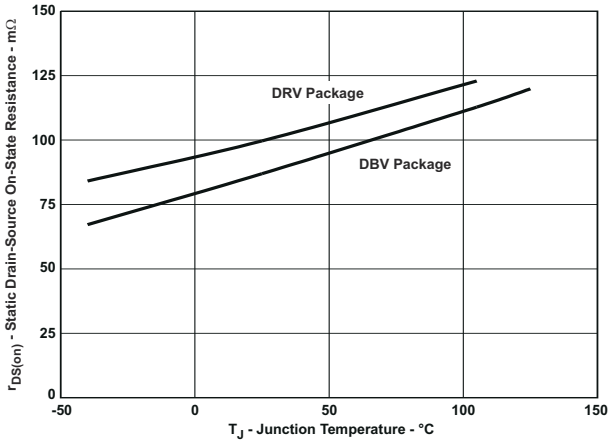



**Figure 7-16. MOSFET $r_{DS(on)}$ Vs. Junction Temperature**

## 8 Parameter Measurement Information

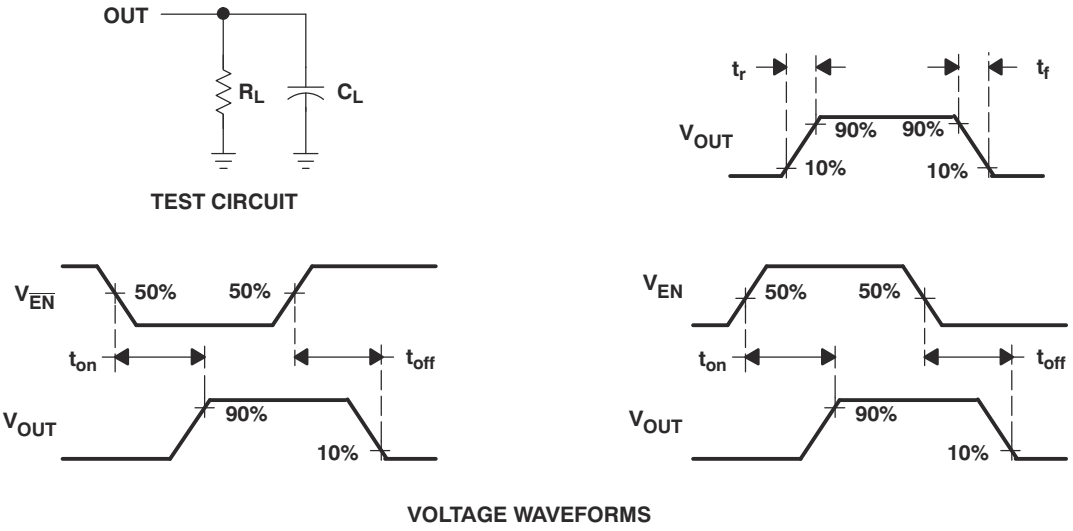



**Figure 8-1. Test Circuit and Voltage Waveforms**

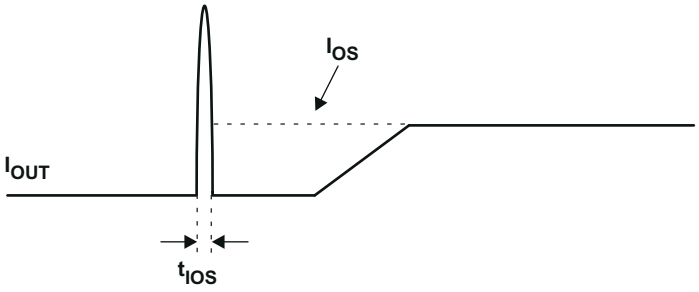



**Figure 8-2. Response Time to Short-Circuit Waveform**

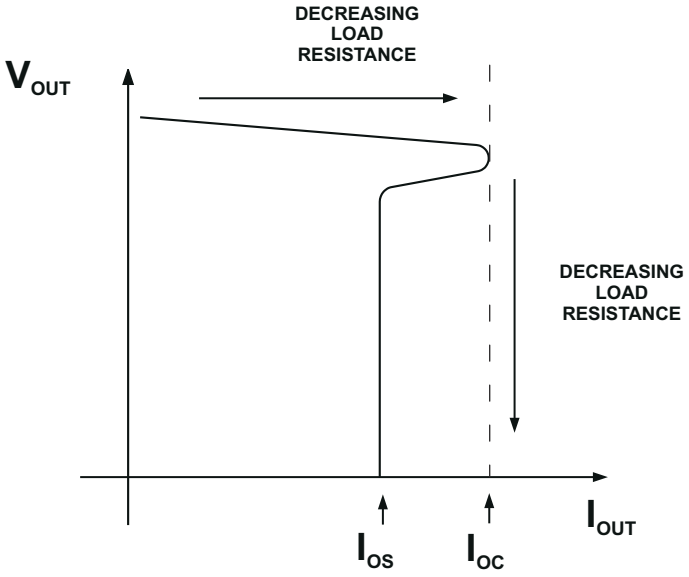


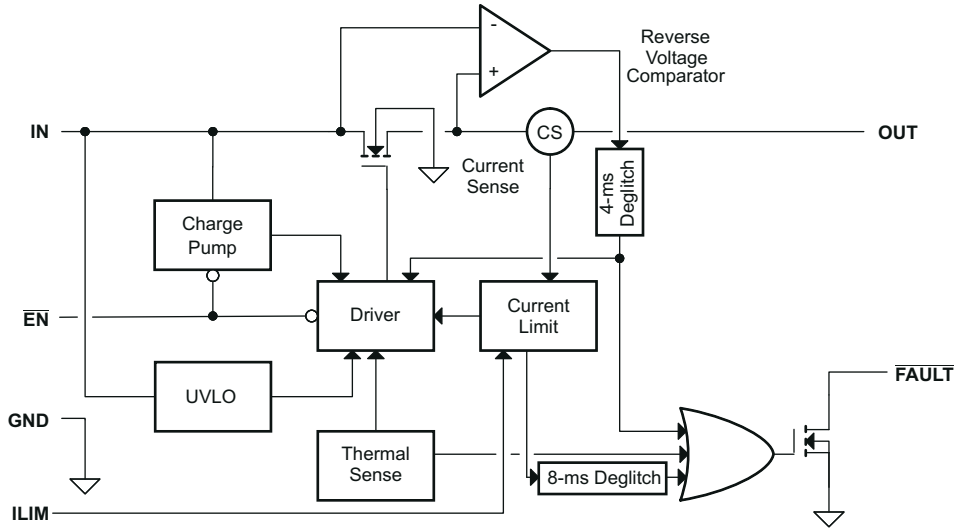

**Figure 8-3. Output Voltage vs. Current-Limit Threshold**

# 9 Detailed Description

## 9.1 Overview

The TPS2550/51 are current-limited, power distribution switches using N-channel MOSFETs for applications where short-circuits or heavy capacitive loads are encountered. These devices allow the user to program the current-limit threshold between 100 mA and 1.1 A via an external resistor. Additional device shutdown features include overtemperature protection and reverse-voltage protection. The device incorporates an internal charge pump and gate drive circuitry necessary to drive the N-channel MOSFET. The charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.5 V and requires little supply current. The driver controls the gate voltage of the power switch. The driver incorporates circuitry that controls the rise and fall times of the output voltage to limit large current and voltage surges and provide built-in soft-start functionality.

## 9.2 Functional Block Diagram




## 9.3 Feature Description

### 9.3.1 Overcurrent

The TPS2550/51 responds to an overcurrent condition by limiting its output current to the $I_{OC}$ and $I_{OS}$ levels shown in Figure 9-1. Three response profiles are possible depending on the loading conditions and are summarized in Figure 8-3.

One response profile occurs if the TPS2550/51 is enabled into a short-circuit. The output voltage is held near zero potential with respect to ground and the TPS2550/51 ramps the output current to $I_{OS}$ (see Figure 7-3).

A second response profile occurs if a short is applied to the output after the TPS2550/51 is enabled. The device responds to the overcurrent condition within time $t_{IOS}$ (see Figure 8-2). The current-sense amplifier is over-driven during this time and momentarily disables the internal current-limit MOSFET. The current-sense amplifier gradually recovers and limits the output current to $I_{OS}$.

A third response profile occurs if the load current gradually increases. The device first limits the load current to $I_{OC}$. If the load demands a current greater than $I_{OC}$, the TPS2550/51 folds back the current to $I_{OS}$ and the output voltage decreases to $I_{OS}$ x $R_{LOAD}$ for a resistive load, which is shown in Figure 8-3.

The TPS2550/51 thermal cycles if an overload condition is present long enough to activate thermal limiting in any of the above cases. The device turns off when the junction temperature exceeds 135°C (typ). The device remains off until the junction temperature cools 15°C (typ) and then restarts. The TPS2550/51 cycles on/off until the overload is removed (see Figure 7-5 and Figure 7-7) .

### 9.3.2 Reverse-Voltage Protection

The reverse-voltage protection feature turns off the N-channel MOSFET whenever the output voltage exceeds the input voltage by 135 mV (typical) for 4-ms. This feature prevents damage to devices on the input side of the TPS2550/51 by preventing significant current from sinking into the input capacitance. The N-channel MOSFET is allowed to turn-on once the output voltage goes below the input voltage for the same 4-ms deglitch time. The reverse-voltage comparator also asserts the $\overline{\text{FAULT}}$ output (active-low) after 4-ms.

### 9.3.3 $\overline{\text{FAULT}}$ Response

The $\overline{\text{FAULT}}$ open-drain output is asserted (active low) during an overcurrent, overtemperature or reverse-voltage condition. The output remains asserted until the fault condition is removed. The TPS2550/51 is designed to eliminate false $\overline{\text{FAULT}}$ reporting by using an internal delay "deglitch" circuit for overcurrent (7.5-ms) and reverse-voltage (4-ms) conditions without the need for external circuitry. This "deglitch" circuit ensures that $\overline{\text{FAULT}}$ is not accidentally asserted due to normal operation such as starting into a heavy capacitive load. The deglitch circuitry delays entering and leaving fault conditions. Overtemperature conditions are not deglitched and assert the $\overline{\text{FAULT}}$ signal immediately.

### 9.3.4 Undervoltage Lockout (UVLO)

The undervoltage lockout (UVLO) circuit disables the power switch until the input voltage reaches the UVLO turn-on threshold. Built-in hysteresis prevents unwanted on/off cycling due to input voltage drop from large current surges.

### 9.3.5 ENABLE ( $\overline{\text{EN}}$ or EN)

The logic enable controls the power switch, bias for the charge pump, driver, and other circuits to reduce the supply current. The supply current is reduced to less than 1-µA when a logic high is present on $\overline{\text{EN}}$ or when a logic low is present on EN. A logic low input on $\overline{\text{EN}}$ or a logic high input on EN enables the driver, control circuits, and power switch. The enable input is compatible with both TTL and CMOS logic levels.

### 9.3.6 Thermal Sense

The TPS2550/51 protects itself with two independent thermal sensing circuits that monitor the operating temperature of the power-switch and disables operation if the temperature exceeds recommended operating conditions. The device operates in constant-current mode during an overcurrent conditions, which increases the voltage drop across power-switch. The power dissipation in the package is proportional to the voltage drop across the power-switch, so the junction temperature rises during an overcurrent condition. The first thermal sensor turns off the power-switch when the die temperature exceeds 135°C and the part is in current limit. The second thermal sensor turns off the power-switch when the die temperature exceeds 155°C regardless of whether the power-switch is in current limit. Hysteresis is built into both thermal sensors, and the switch turns on after the device has cooled approximately 15°C. The switch continues to cycle off and on until the fault is removed. The open-drain false reporting output $\overline{\text{FAULT}}$ is asserted (active low) immediately during an overtemperature shutdown condition.

### 9.3.7 Device Functional Modes

There are no other functional modes.

## 9.4 Programming

### 9.4.1 Programming the Current-Limit Threshold

The overcurrent threshold is user programmable via an external resistor. Many applications require that the minimum current-limit is above a certain current level or that the maximum current-limit is below a certain current level, so it is important to consider the tolerance of the overcurrent threshold when selecting a value for $R_{ILIM}$. The following equations and Figure 9-1 can be used to calculate the resulting overcurrent threshold for a given external resistor value ®$_{ILIM}$). Figure 9-1 includes current-limit tolerance due to variations caused by temperature and process. To reduce parasitic effects on the current-limit accuracy, make the traces routing the $R_{ILIM}$ resistor to the TPS2550/51 as short as possible.

There are two important current-limit thresholds for the device and are related by Figure 8-3. The first threshold is the short-circuit current threshold $I_{OS}$. $I_{OS}$ is the current delivered to the load if the part is enabled into a short-circuit or a short-circuit is applied during normal operation. The second threshold is the overcurrent threshold $I_{OC}$. $I_{OC}$ is the peak DC current that can be delivered to the load before the device begins to limit current. $I_{OC}$ is important if ramped loads or slow transients are common to the application. It is important to consider both $I_{OS}$ and $I_{OC}$ when choosing $R_{ILIM}$. $R_{ILIM}$ can be selected to provide a current-limit threshold that occurs 1) above a minimum load current or 2) below a maximum load current.

To design above a minimum current-limit threshold, find the intersection of $R_{ILIM}$ and the maximum desired load current on the $I_{OS(min)}$ curve and choose a value of $R_{ILIM}$ below this value. Programming the current-limit above a minimum threshold is important to ensure start-up into full-load or heavy capacitive loads. The resulting maximum DC load current is the intersection of the selected value of $R_{ILIM}$ and the $I_{OC(max)}$ curve.

To design below a maximum DC current level, find the intersection of $R_{ILIM}$ and the maximum desired load current on the $I_{OC(max)}$ curve and choose a value of $R_{ILIM}$ above this value. Programming the current-limit below a maximum threshold is important to avoid current-limiting upstream power supplies causing the input voltage bus to droop. The resulting minimum short-circuit current is the intersection of the selected value of $R_{ILIM}$ and the $I_{OS(min)}$ curve.

Overcurrent Threshold Equations ($I_{OC}$):

- $I_{OC(max)}$ (mA) = (24500 V) / ($R_{ILIM}$ kΩ) $^{0.975}$ + 50
- $I_{OC(typ)}$ (mA) = (23800 V) / ($R_{ILIM}$ kΩ) $^{0.985}$ + 50
- $I_{OC(min)}$ (mA) = (23100 V) / ($R_{ILIM}$ kΩ) $^{0.996}$ + 50

Short-Circuit Current Equations ($I_{OS}$):

- $I_{OS(max)}$ (mA) = (25500 V) / ($R_{ILIM}$ kΩ) $^{1.013}$ + 50
- $I_{OS(typ)}$ (mA) = (28700 V) / ($R_{ILIM}$ kΩ) $^{1.114}$ + 50
- $I_{OS(min)}$ (mA) = (39700 V) / ($R_{ILIM}$ kΩ) $^{1.342}$ + 50

where 14.3 kΩ ≤ $R_{ILIM}$ ≤ 80.6 kΩ. $I_{OS(typ)}$ and $I_{OS(max)}$ are not plotted to improve graph clarity.

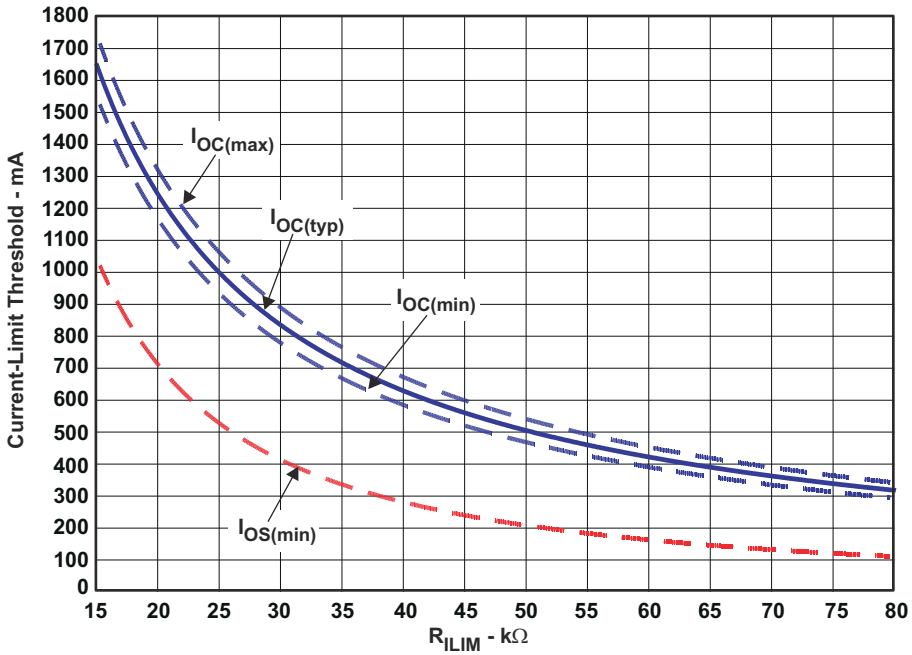



**Figure 9-1. Current-Limit Threshold Vs.$R_{ILIM}$**

# 10 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 10.1 Application Information

The TPS255x current-limited power switch uses N-channel MOSFETs in applications requiring continuous load current. The device enters constant-current mode when the load exceeds the current limit threshold.

## 10.2 Typical Applications

### 10.2.1 Two-Level Current-Limit Circuit

Some applications require different current-limit thresholds depending on external system conditions. Figure 10-1 shows an implementation for an externally controlled, two-level current-limit circuit. The current-limit threshold is set by the total resistance from ILIM to GND (see previously discussed "Programming the Current-Limit Threshold" section). A logic-level input enables/disables MOSFET Q1 and changes the current-limit threshold by modifying the total resistance from ILIM to GND. Additional MOSFETs/resistor combinations can be used in parallel to Q1/R2 to increase the number of additional current-limit levels.

**Note**

Do not drive the ILIM directly with an external signal.

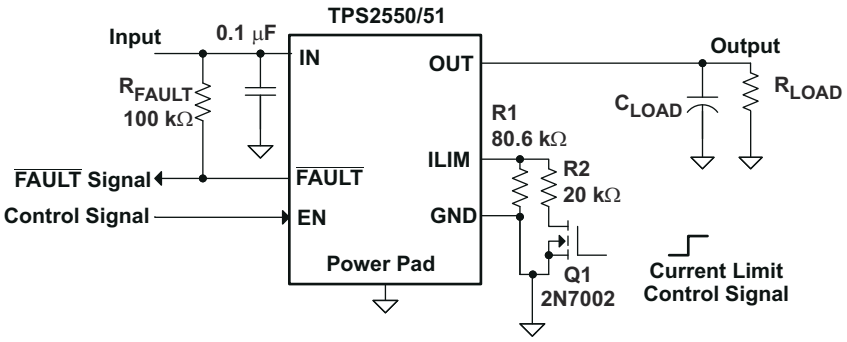



**Figure 10-1. Two-Level Current-Limit Circuit**

### 10.2.2 Design Requirements

For this example, use the parameters shown in Table 10-1.

**Table 10-1. Design Requirements**

| PARAMETER | VALUE |
|---|---|
| Input voltage | 5 V |
| Output voltage | 5 V |
| Above a minimum current limit | 1000 mA |
| Below a maximum current limit | 1250 mA |

### 10.2.3 Detail Design Procedures

#### 10.2.3.1 Designing Above a Minimum Current Limit

Some applications require that current-limiting cannot occur below a certain threshold. For this example, assume that 1 A must be delivered to the load so that the minimum desired current-limit threshold is 1000 mA. Use the $I_{OS}$ equations and Figure 9-1 to select $R_{ILIM}$.

- $I_{OS(min)}$ (mA) = 1000 mA
- $I_{OS(min)}$ (mA) = (39700 V) / ($R_{ILIM}$ (kΩ)) $^{1.342}$ + 50
- $R_{ILIM}$ (kΩ) = [(39700 V) / ($I_{OS(min)}$ (mA) - 50)]$^{1/1.342}$
- $R_{ILIM}$ = 16.14 kΩ

Select the closest 1% resistor less than the calculated value: $R_{ILIM}$ = 16 kΩ. This selection sets the minimum current-limit threshold at 1 A . Use the $I_{OC}$ equations, Figure 9-1, and the previously calculated value for $R_{ILIM}$ to calculate the maximum resulting current-limit threshold.

- $R_{ILIM}$ = 16 kΩ
- $I_{OC(max)}$ (mA) = (24500 V) / ($R_{ILIM}$ (kΩ)) $^{0.975}$ + 50
- $I_{OC(max)}$ (mA) = (24500 V) / (16 (kΩ))$^{0.975}$ + 50
- $I_{OC(max)}$ = 1691 mA

The resulting maximum current-limit threshold is 1.69 A with a 16 kΩ resistor.

#### 10.2.3.2 Designing Below a Maximum Current Limit

Some applications require that current-limiting must occur below a certain threshold. For this example, assume that the desired upper current-limit threshold must be below 1.25 A to protect an up-stream power supply. Use the $I_{OC}$ equations and Figure 9-1 to select $R_{ILIM}$.

- $I_{OC(max)}$ (mA) = 1250 mA
- $I_{OC(max)}$ (mA) = (24500 V) / ($R_{ILIM}$ (kΩ)) $^{0.975}$ + 50
- $R_{ILIM}$ (kΩ) = [(24500 V) / ($I_{OC(max)}$ (mA) - 50)]$^{1/0.975}$
- $R_{ILIM}$ = 22.05 kΩ

Select the closest 1% resistor greater than the calculated value: $R_{ILIM}$ = 22 kΩ. This selection sets the maximum current-limit threshold at 1.25 A . Use the $I_{OS}$ equations, Figure 9-1, and the previously calculated value for $R_{ILIM}$ to calculate the minimum resulting current-limit threshold.

- $R_{ILIM}$ = 22 kΩ
- $I_{OS(min)}$ (mA) = (39700 V) / ($R_{ILIM}$ (kΩ)) $^{1.342}$ + 50
- $I_{OS(min)}$ (mA) = (39700 V) / (22 (kΩ)) $^{1.342}$ + 50
- $I_{OS(min)}$ = 677 mA

The resulting minimum current-limit threshold is 677 mA with a 22 kΩ resistor.

#### 10.2.3.3 Input and Output Capacitance

Input and output capacitance improve the performance of the device; make sure to optimize the actual capacitance for the particular application. For all applications, a 0.01 µF to 0.1µF ceramic bypass capacitor between IN and GND is recommended as close to the device as possible for local noise de-coupling. This precaution reduces ringing on the input due to power-supply transients. Additional input capacitance may be needed on the input to reduce voltage overshoot from exceeding the absolute maximum voltage of the device during heavy transients, which is especially important during bench testing when long, inductive cables are used to connect the evaluation board to the bench power-supply.

Placing a high-value electrolytic capacitor on the output pin is recommended when the large transient currents are expected on the output. Additionally, bypassing the output with a 0.01 µF to 0.1 µF ceramic capacitor improves the immunity of the device to short-circuit transients.

### 10.2.4 Auto-Retry Functionality

Some applications require that an overcurrent condition disables the part momentarily during a fault condition and re-enables after a pre-set time. This *auto-retry* functionality can be implemented with an external resistor and capacitor. During a fault condition, $\overline{FAULT}$ pulls low disabling the part. The part is disabled when EN is pulled low, and $\overline{FAULT}$ goes high impedance allowing $C_{RETRY}$ to begin charging. The part re-enables when the

voltage on EN reaches the turnon threshold, and the auto-retry time is determined by the resistor/capacitor time constant. The part continues to cycle in this manner until the fault condition is removed.

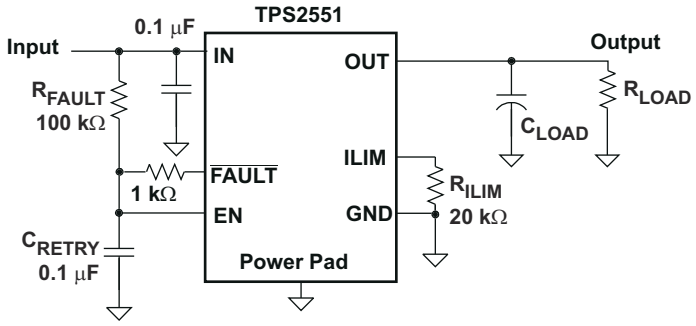



**Figure 10-2. Auto-Retry Functionality**

Some applications require auto-retry functionality and the ability to enable/disable with an external logic signal. The figure below shows how an external logic signal can drive EN through $R_{FAULT}$ and maintain auto-retry functionality. The resistor/capacitor time constant determines the auto-retry time-out period.

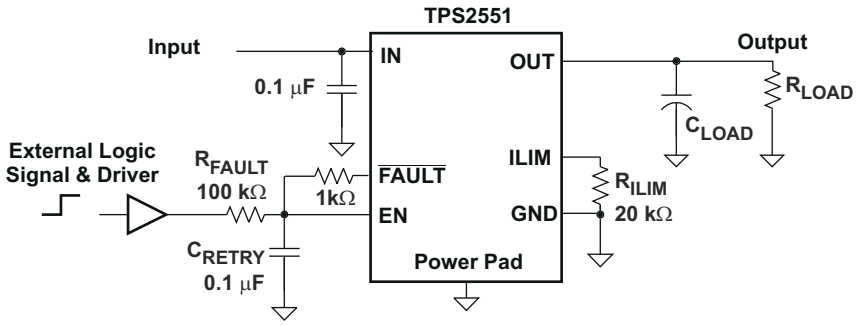



**Figure 10-3. Auto-Retry Functionality With External EN Signal**

### 10.2.5 Latch-Off Functionality

The circuit in Figure 10-4 uses an SN74HC00 quad-NAND gate to implement overcurrent latch-off. The SN74HC00 high-speed CMOS logic gate is selected because it operates over the 2.5V – 6.5V range of the TPS2550/51.

This circuit is designed to work with the active-high TPS2551. ENABLE must be logic low during start-up until $V_{IN}$ is stable to ensure that the switch initializes in the OFF state. A logic high on ENABLE turns on the switch after $V_{IN}$ is stable. $\overline{FAULT}$ momentarily pulls low during an overcurrent condition, which latches $\overline{STAT}$ logic low and disables the switch. The host can monitor $\overline{STAT}$ for an overcurrent condition. Toggling ENABLE resets $\overline{STAT}$ and re-enables the switch.

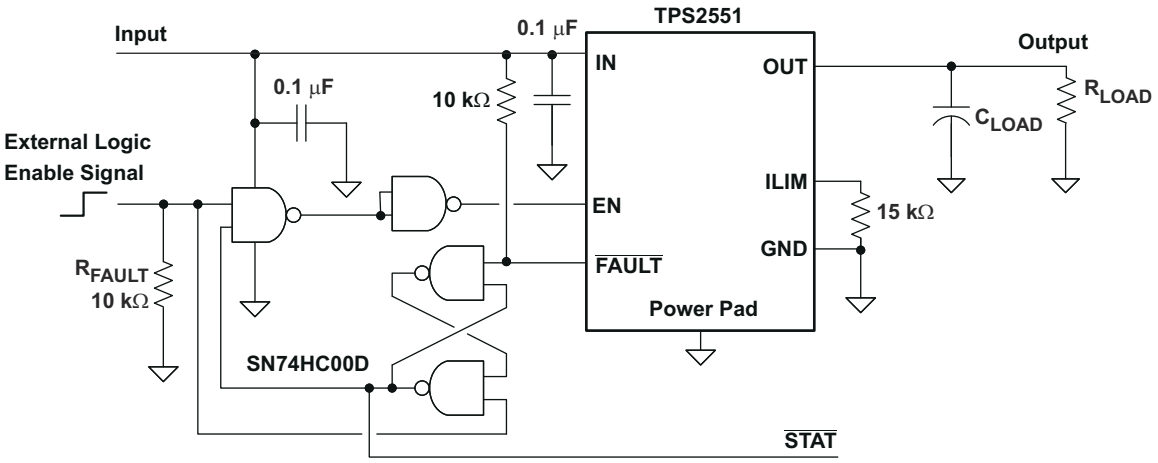



**Figure 10-4. Overcurrent Latch-Off Using a Quad-NAND Gate**

### 10.2.6 Typical Application as USB Power Switch

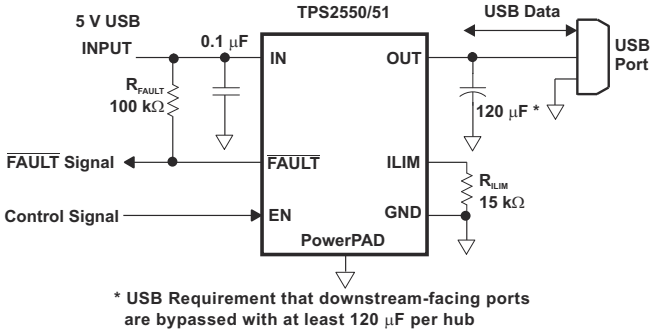



**Figure 10-5. Typical Application as USB Power Switch**

#### *10.2.6.1 Design Requirements*

For this example, use the parameters shown in Table 10-2.

**Table 10-2. Design Requirements**

| PARAMETER | VALUE |
|---|---|
| Input voltage | 5 V |
| Output voltage | 5 V |
| Current | 1250 mA |

##### 10.2.6.1.1 USB Power-Distribution Requirements

USB can be implemented in several ways regardless of the type of USB device being developed. Several power-distribution features must be implemented.

- SPHs must:
  - Current-limit downstream ports
  - Report overcurrent conditions
- BPHs must:
  - Enable/disable power to downstream ports
  - Power up at <100 mA
  - Limit inrush current (<44 Ω and 10 µF)
- Functions must:
  - Limit inrush currents

– Power up at <100 mA

The feature set of the TPS2550/51 meets each of these requirements. The integrated current-limiting and overcurrent reporting is required by self-powered hubs. The logic-level enable and controlled rise times meet the need of both input and output ports on bus-powered hubs and the input ports for bus-powered functions.

#### *10.2.6.2 Detail Design Procedures*

##### 10.2.6.2.1 Universal Serial Bus (USB) Power-Distribution Requirements

One application for this device is for current-limiting in universal serial bus (USB) applications. The original USB interface was a 12-Mb/s or 1.5-Mb/s, multiplexed serial bus designed for low-to-medium bandwidth PC peripherals (for example keyboards, printers, scanners, and mice). As the demand for more bandwidth increased, the USB 2.0 standard was introduced increasing the maximum data rate to 480-Mb/s. The four-wire USB interface is conceived for dynamic attach-detach (hot plug-unplug) of peripherals. Two lines are provided for differential data, and two lines are provided for 5-V power distribution.

USB data is a 3.3-V level signal, but power is distributed at 5 V to allow for voltage drops in cases where power is distributed through more than one hub across long cables. Each function must provide its own regulated 3.3 V from the 5-V input or its own internal power supply. The USB specification classifies two different classes of devices depending on its maximum current draw. A device classified as low-power can draw up to 100 mA as defined by the standard. A device classified as high-power can draw up to 500 mA. It is important that the minimum current-limit threshold of the current-limiting power-switch exceed the maximum current-limit draw of the intended application. Always reference the latest USB standard when considering the current-limit threshold

The USB specification defines two types of devices as hubs and functions. A USB hub is a device that contains multiple ports for different USB devices to connect and can be self-powered (SPH) or bus-powered (BPH). A function is a USB device that is able to transmit or receive data or control information over the bus. A USB function can be embedded in a USB hub. A USB function can be one of three types included in the list below.

- Low-power, bus-powered function
- High-power, bus-powered function
- Self-powered function

SPHs and BPHs distribute data and power to downstream functions. The TPS2550/51 has higher current capability than required for a single USB port allowing it to power multiple downstream ports.

## 10.3 Power Supply Recommendations

### 10.3.1 Self-Powered and Bus-Powered Hubs

A SPH has a local power supply that powers embedded functions and downstream ports. This power supply must provide between 4.75 V to 5.25 V to downstream facing devices under full-load and no-load conditions. SPHs are required to have current-limit protection and must report overcurrent conditions to the USB controller. Typical SPHs are desktop PCs, monitors, printers, and stand-alone hubs.

A BPH obtains all power from an upstream port and often contains an embedded function. It must power up with less than 100 mA. The BPH usually has one embedded function, and power is always available to the controller of the hub. If the embedded function and hub require more than 100 mA on power up, the power to the embedded function may need to be kept off until enumeration is completed, which is accomplished by removing power or by shutting off the clock to the embedded function. Power switching the embedded function is not necessary if the aggregate power draw for the function and controller is less than 100 mA. The total current drawn by the bus-powered device is the sum of the current to the controller, the embedded function, and the downstream ports, and it is limited to 500 mA from an upstream port.

### 10.3.2 Low-Power Bus-Powered and High-Power Bus-Powered Functions

Both low-power and high-power bus-powered functions obtain all power from upstream ports. Low-power functions always draw less than 100 mA; high-power functions must draw less than 100 mA at power up and can draw up to 500 mA after enumeration. If the load of the function is more than the parallel combination of 44 Ω and 10 µF at power up, the device must implement inrush current limiting.

### 10.3.3 Power Dissipation and Junction Temperature

The low on-resistance of the N-channel MOSFET allows small surface-mount packages to pass large currents. It is good design practice to estimate power dissipation and junction temperature. The below analysis gives an approximation for calculating junction temperature based on the power dissipation in the package. However, it is important to note that thermal analysis is strongly dependent on additional system level factors. Such factors include air flow, board layout, copper thickness and surface area, and proximity to other devices dissipating power. Good thermal design practice must include all system level factors in addition to individual component analysis.

Begin by determining the $r_{DS(on)}$ of the N-channel MOSFET relative to the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(on)}$ from the typical characteristics graph. Using this value, the power dissipation can be calculated by:

$$P_D = r_{DS(on)} \times I_{OUT}^2$$

Where:

$P_D$ = Total power dissipation (W)

$r_{DS(on)}$ = Power switch on-resistance (Ω)

$I_{OUT}$ = Maximum current-limit threshold (A)

This step calculates the total power dissipation of the N-channel MOSFET.

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\Theta JA} + T_A$$

Where:

$T_A$ = Ambient temperature (°C)

$R_{\Theta JA}$ = Thermal resistance (°C/W)

$P_D$ = Total power dissipation (W)

Compare the calculated junction temperature with the initial estimate. If they are not within a few degrees, repeat the calculation using the "refined" $r_{DS(on)}$ from the previous calculation as the new estimate. Two or three iterations are generally sufficient to achieve the desired result. The final junction temperature is highly dependent on thermal resistance $R_{\theta JA}$, and thermal resistance is highly dependent on the individual package and board layout. The "Dissipating Rating Table" at the beginning of this document provides example thermal resistance for specific packages and board layouts.

## 10.4 Layout

### 10.4.1 Layout Guidelines

- TI recommends placing the 100-nF bypass capacitor near the IN and GND pins, and make the connections using a low-inductance trace.
- TI recommends placing a high-value electrolytic capacitor and a 100-nF bypass capacitor on the output pin when large transient currents are expected on the output.
- The traces routing the RILIM resistor to the device must be as short as possible to reduce parasitic effects on the current limit accuracy.
- The PowerPAD must be directly connected to PCB ground plane using wide and short copper trace.

### 10.4.2 Layout Example

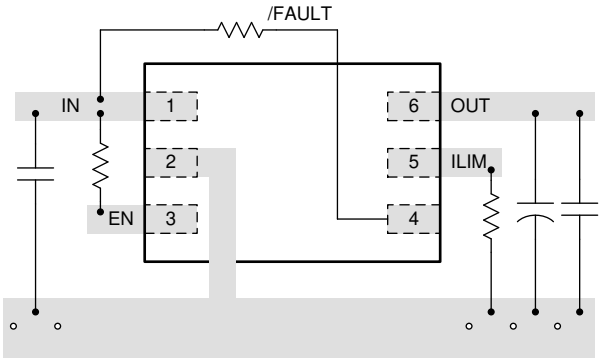



**Figure 10-6. Layout Recommendation**

# 11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

## 11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 11.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 11.3 Trademarks

PowerPAD™ and TI E2E™ are trademarks of Texas Instruments.
All trademarks are the property of their respective owners.

## 11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.5 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS2550DBVR | NRND | SOT-23 | DBV | 6 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 2550 | |
| TPS2550DBVT | NRND | SOT-23 | DBV | 6 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 2550 | |
| TPS2550DRVR | NRND | WSON | DRV | 6 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CKJ | |
| TPS2550DRVT | NRND | WSON | DRV | 6 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CKJ | |
| TPS2551DBVR | NRND | SOT-23 | DBV | 6 | 3000 | RoHS & Green | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 85 | 2551 | |
| TPS2551DBVT | NRND | SOT-23 | DBV | 6 | 250 | RoHS & Green | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 85 | 2551 | |
| TPS2551DRVR | NRND | WSON | DRV | 6 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CKK | |
| TPS2551DRVT | NRND | WSON | DRV | 6 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CKK | |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**OTHER QUALIFIED VERSIONS OF TPS2551 :**

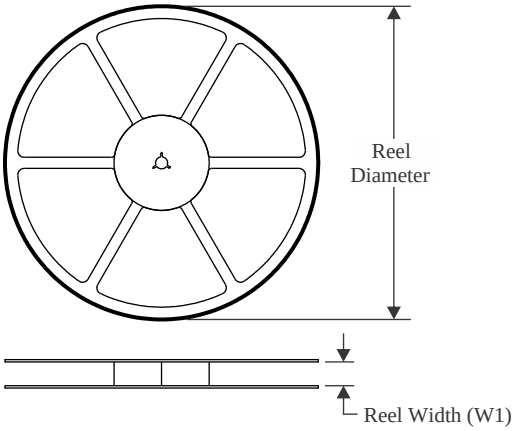
- Automotive : TPS2551-Q1

NOTE: Qualified Version Definitions:

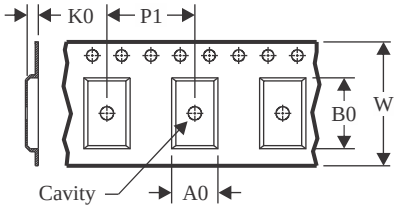
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

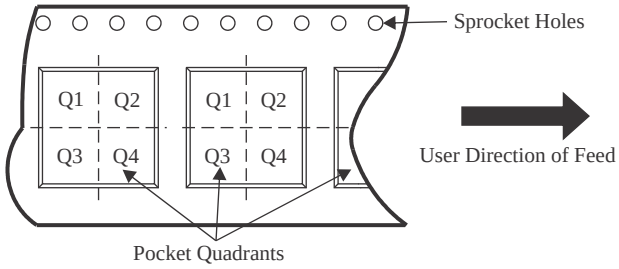



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

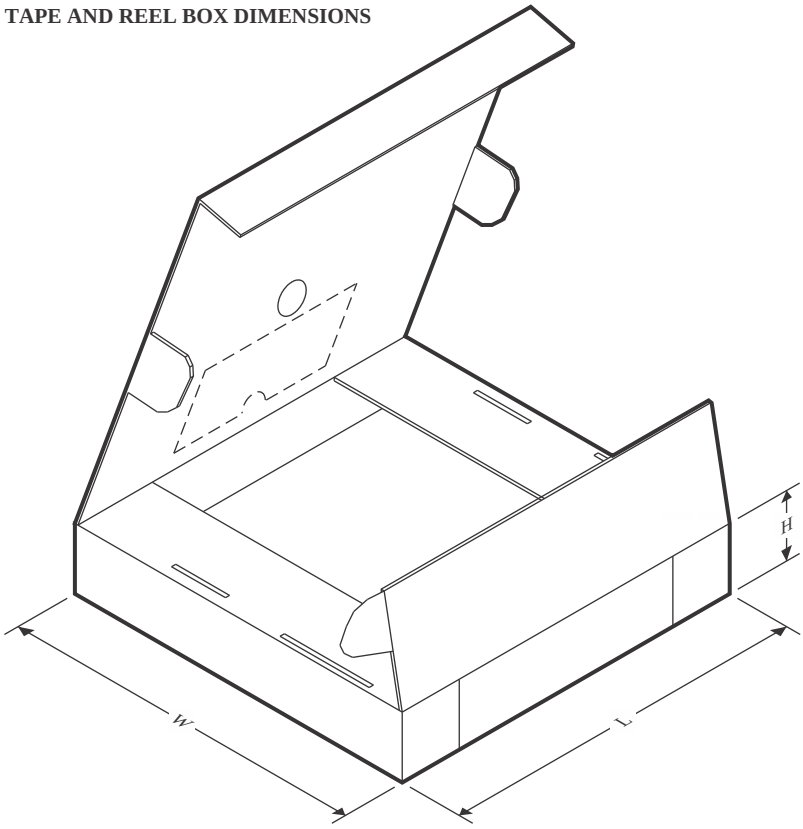
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS2550DBVR | SOT-23 | DBV | 6 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS2550DBVT | SOT-23 | DBV | 6 | 250 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS2550DRVR | WSON | DRV | 6 | 3000 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |
| TPS2550DRVT | WSON | DRV | 6 | 250 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |
| TPS2551DBVR | SOT-23 | DBV | 6 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS2551DBVR | SOT-23 | DBV | 6 | 3000 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS2551DBVT | SOT-23 | DBV | 6 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS2551DBVT | SOT-23 | DBV | 6 | 250 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS2551DRVR | WSON | DRV | 6 | 3000 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |
| TPS2551DRVT | WSON | DRV | 6 | 250 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS

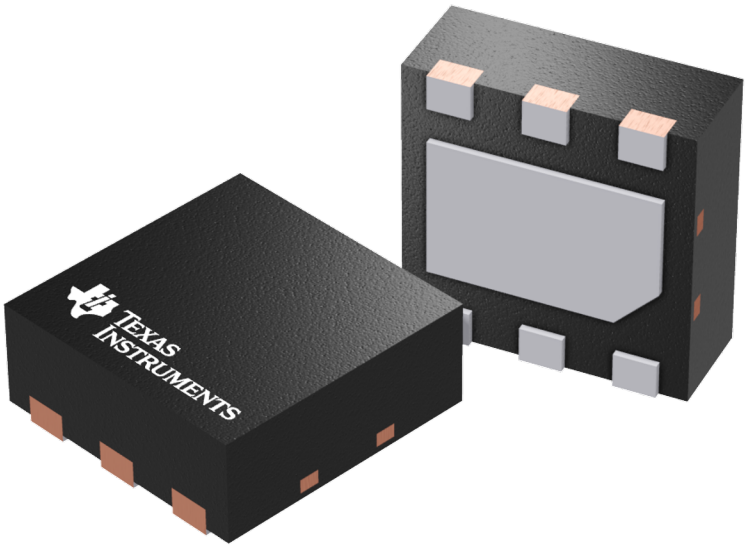



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS2550DBVR | SOT-23 | DBV | 6 | 3000 | 200.0 | 183.0 | 25.0 |
| TPS2550DBVT | SOT-23 | DBV | 6 | 250 | 200.0 | 183.0 | 25.0 |
| TPS2550DRVR | WSON | DRV | 6 | 3000 | 200.0 | 183.0 | 25.0 |
| TPS2550DRVT | WSON | DRV | 6 | 250 | 200.0 | 183.0 | 25.0 |
| TPS2551DBVR | SOT-23 | DBV | 6 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS2551DBVR | SOT-23 | DBV | 6 | 3000 | 200.0 | 183.0 | 25.0 |
| TPS2551DBVT | SOT-23 | DBV | 6 | 250 | 180.0 | 180.0 | 18.0 |
| TPS2551DBVT | SOT-23 | DBV | 6 | 250 | 203.0 | 203.0 | 35.0 |
| TPS2551DRVR | WSON | DRV | 6 | 3000 | 200.0 | 183.0 | 25.0 |
| TPS2551DRVT | WSON | DRV | 6 | 250 | 200.0 | 183.0 | 25.0 |

# DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



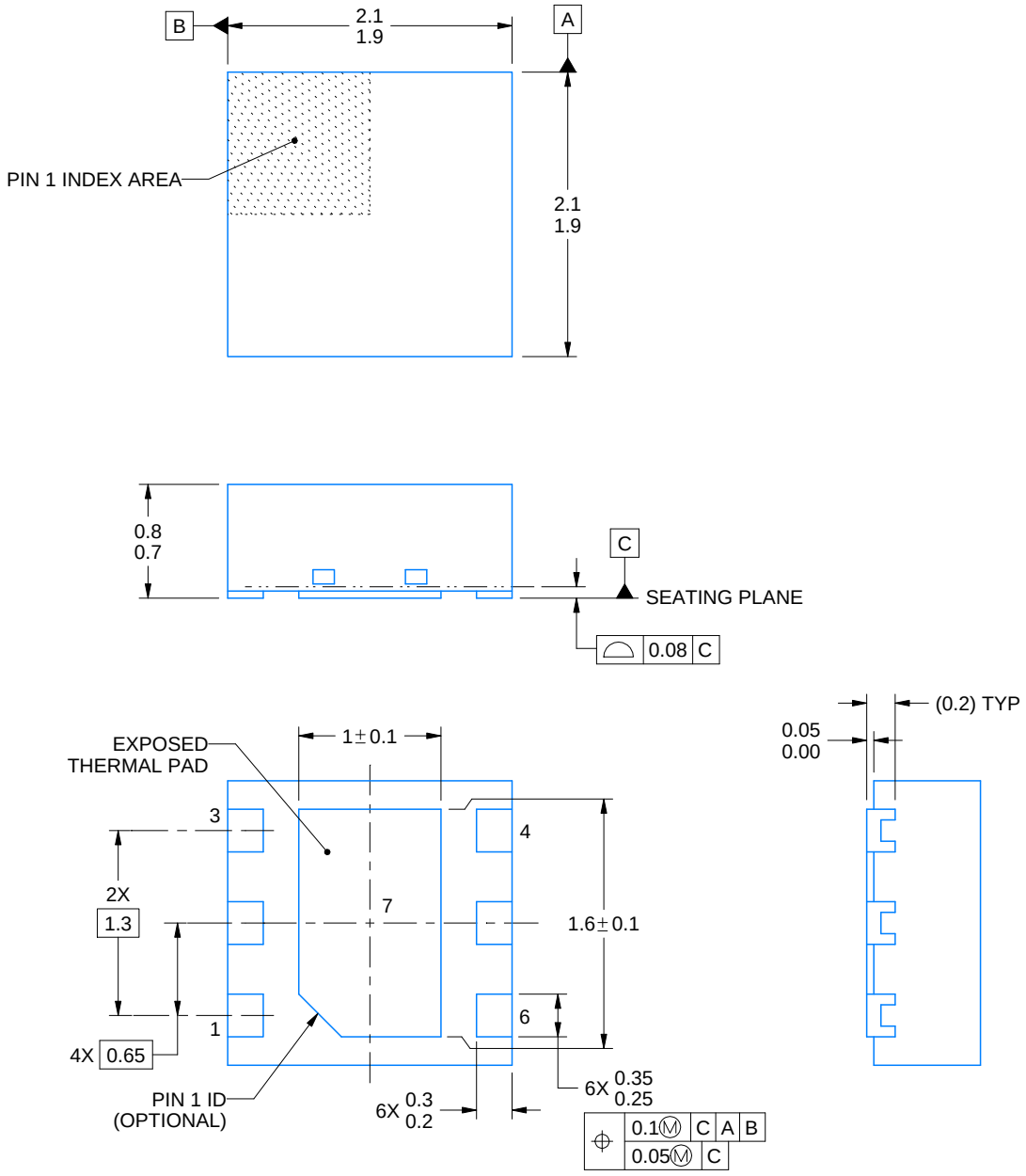

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

# DRV0006D

# PACKAGE OUTLINE

## WSON - 0.8 mm max height

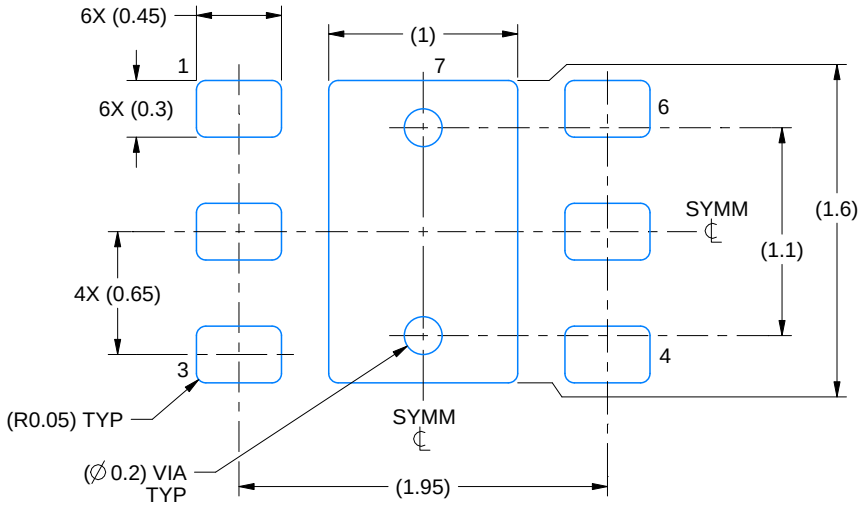
PLASTIC SMALL OUTLINE - NO LEAD



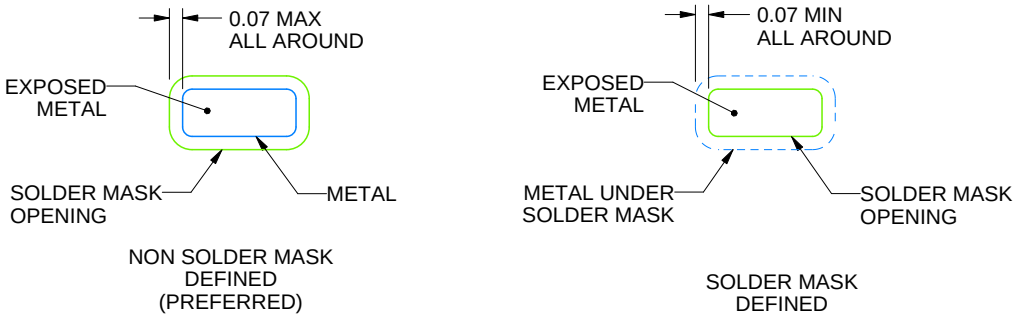

4225563/A 12/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X

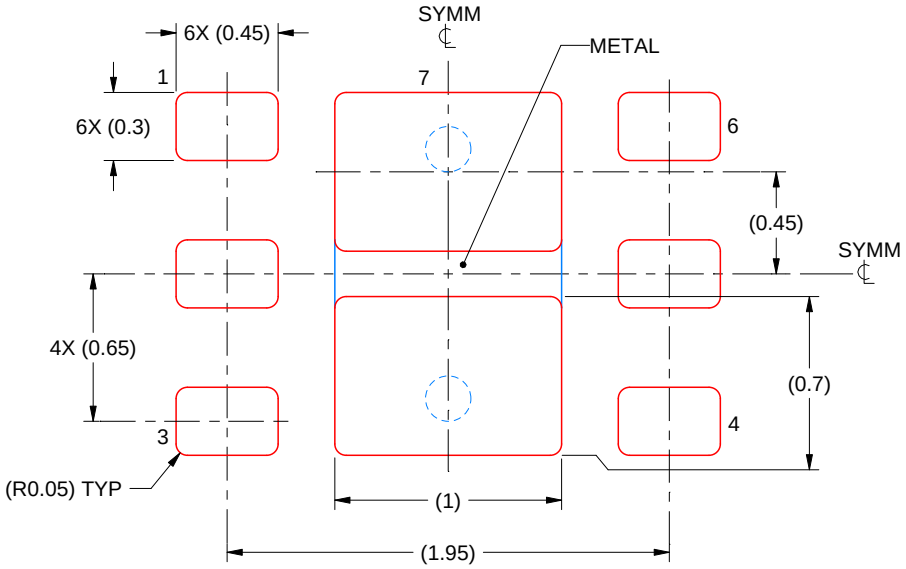



SOLDER MASK DETAILS

4225563/A 12/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4225563/A 12/2019

NOTES: (continued)

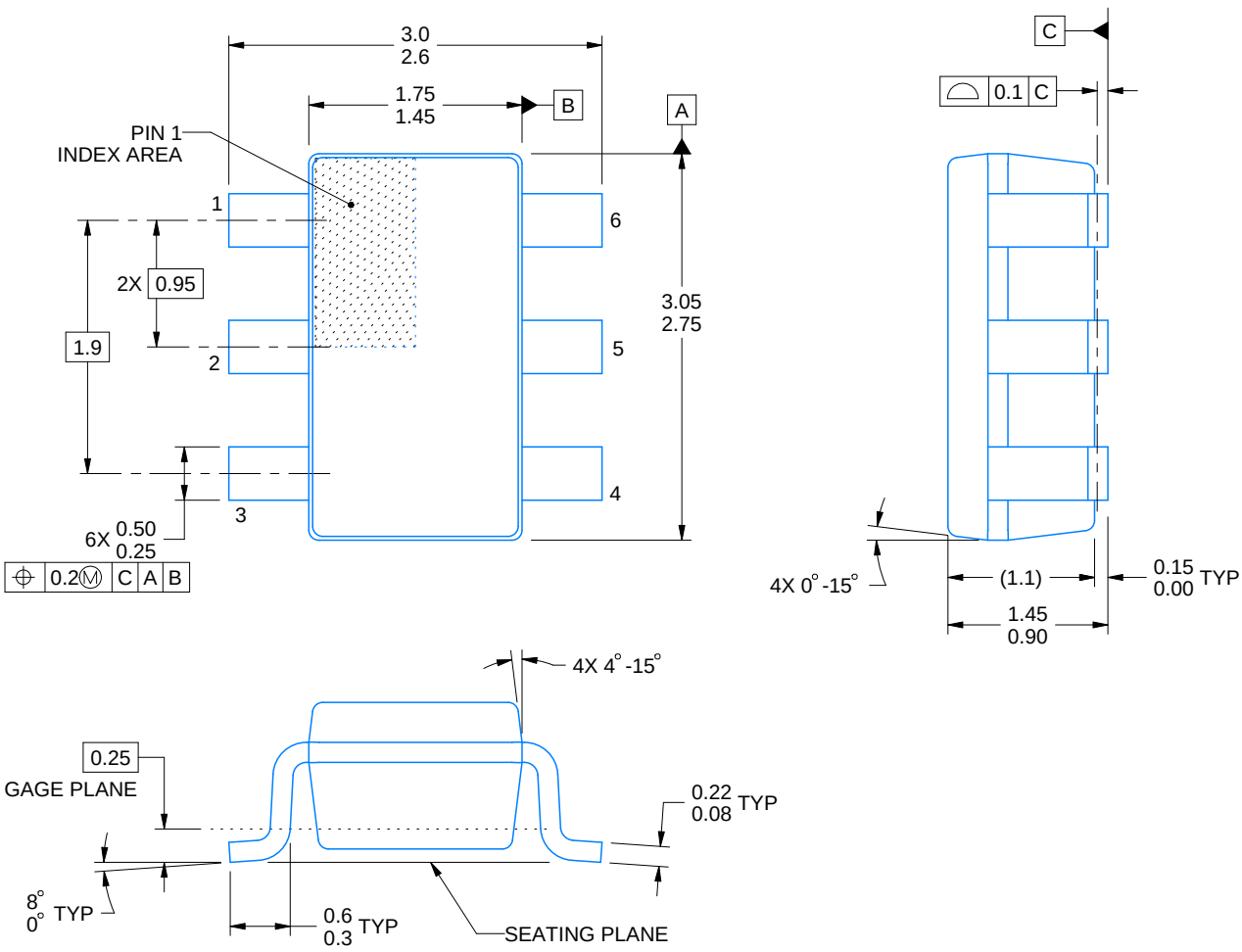
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# PACKAGE OUTLINE

## DBV0006A

## SOT-23 - 1.45 mm max height

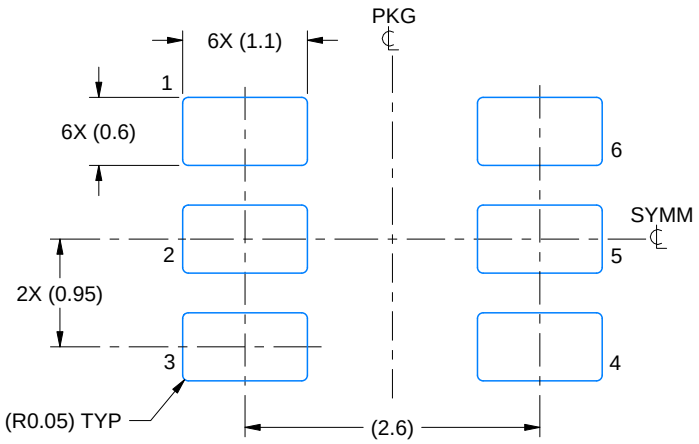
SMALL OUTLINE TRANSISTOR



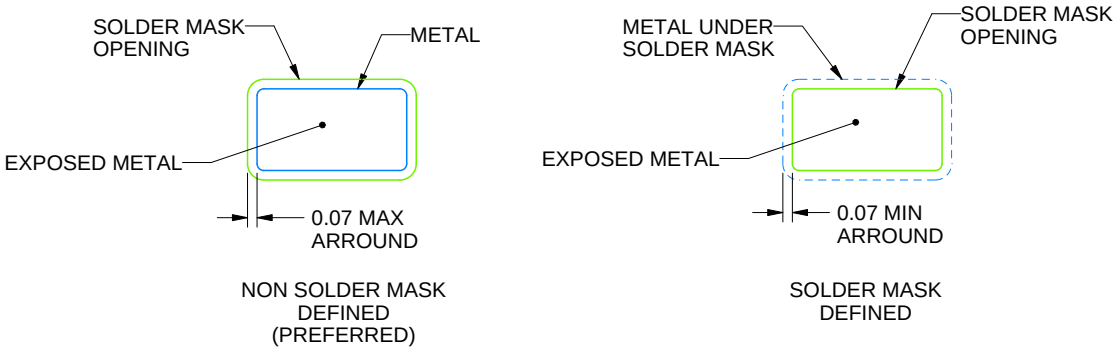

4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

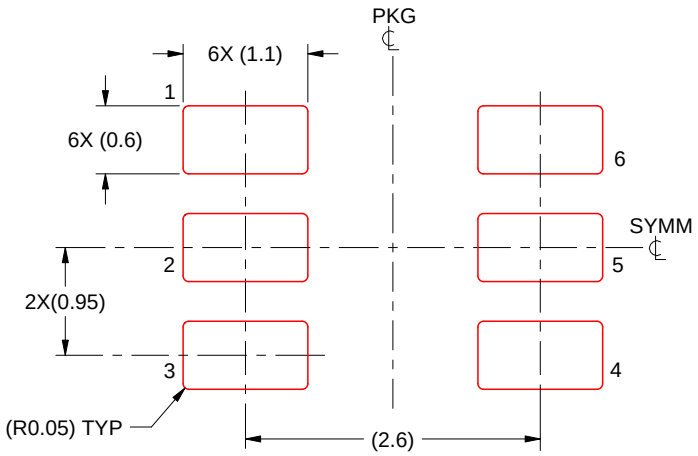



SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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