



### 3-Phase Brushless DC Motor Controller

#### FEATURES

- Hall-Effect Commutation
- 60° or 120° Sensor Spacing
- Integral High-Side Drive for all N-Channel MOSFET Bridges
- PWM Input
- Quadrature Selection
- Tachometer Output
- Reversible
- Braking
- Output Enable Control
- Cross Conduction Protection
- Current Limiting
- Undervoltage Lockout
- Internal Pull-Up Resistors

#### DESCRIPTION

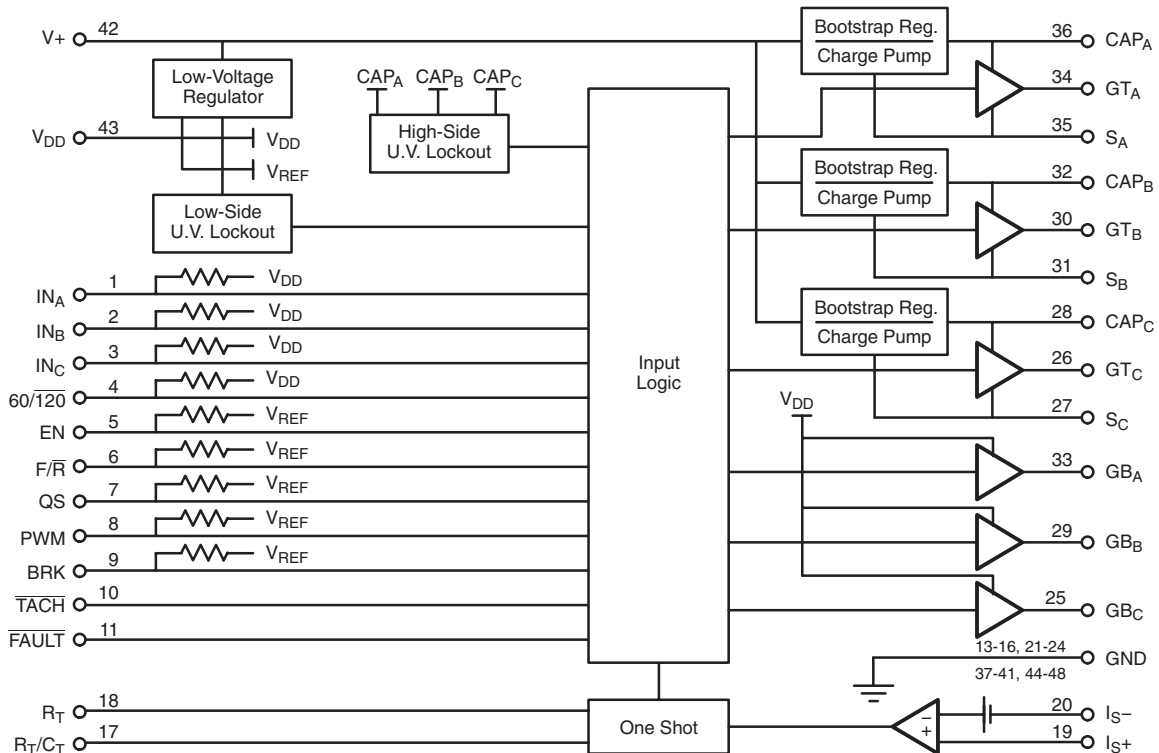
The Si9979 is a monolithic brushless dc motor controller with integral high-side drive circuitry. The Si9979 is configured to allow either 60° or 120° commutation sensor spacing. The internal low-voltage regulator allows operation over a wide input voltage range, 20- to 40-V dc.

quadrature select, and braking inputs are included for control along with a tachometer output. Protection features include cross conduction protection, current limiting, and undervoltage lockout. The FAULT output indicates when undervoltage, over current, disable, or invalid sensor shutdown has occurred.

The Si9979 provides commutation from Hall-effect sensors. The integral high-side drive, which utilizes combination bootstrap/charge pump supplies, allows implementation of an all n-channel MOSFET 3-phase bridge. PWM, direction, and

The Si9979 is available in both standard and lead (Pb)-free 48-pin SQFP packages and is specified to operate over the commercial temperature range of 0 to 70°C (C suffix), and the industrial temperature range of -40 to 85°C (D suffix).

#### FUNCTIONAL BLOCK DIAGRAM



### ABSOLUTE MAXIMUM RATINGS

Voltage on Pin 42	50 V
Voltage on Pins 1–4, 10, 11	–0.3 V to $V_{DD} + 0.3$ V
Voltage on Pins 5–9	–0.3 V to 5.5 V
Voltage on Pins 26, 28, 30, 32, 34, 36	60 V
Voltage on Pins 27, 31, 35	–2 to 50 V
Operating Temperature	
C Suffix	0 to 70°C
D Suffix	–40 to 85°C

Storage Temperature	–65 to 150°C
Junction Temperature ( $T_J$ )	150°C
Power Dissipation ( $P_D$ )	
C Suffix	0.70 W
D Suffix	0.55 W

### RECOMMENDED OPERATING RANGE

$V_+$	+20 to 40 $V_{DC}$
$R_T$	10 k $\Omega$ Min

SPECIFICATIONS								
Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 20$ to 40 V, $I_{DD} = 0$ mA		Limits			Unit	
				Min <sup>a</sup>	Typ <sup>b</sup>	Max <sup>a</sup>		
<b>Power</b>								
Supply Voltage Range	$V_+$			20		40	V	
Logic Voltage	$V_{DD}$		$-20$ mA $\leq I_{DD} \leq 0$ mA	14.5	16	17.5		
Supply Current	$I_+$				4.5		mA	
Logic Current	$I_{DD}$			–20				
Internal Reference <sup>d</sup>	$V_{REF}$				4.2		V	
<b>Commutation Inputs (<math>IN_A</math>, <math>IN_B</math>, <math>IN_C</math>, 60/120)</b>								
High-State	$V_{IH}$			4.0			V	
Low-State	$V_{IL}$					1.0		
High-State Input Current	$I_{IH}$		$V_{IH} = V_{DD}$			10	$\mu$ A	
Low-State Input Current	$I_{IL}$		$V_{IL} = 0$ V		–50			
<b>Logic Inputs (<math>F/\bar{R}</math>, EN, QS, PWM, BRK)</b>								
High-State	$V_{IH}$			2.0			V	
Low-State	$V_{IL}$					0.8		
High-State Input Current	$I_{IH}$		$V_{IH} = 5.5$ V			10	$\mu$ A	
Low-State Input Current	$I_{IL}$		$V_{IL} = 0$ V		–125			
<b>Outputs</b>								
Low-Side Gate Drive, High State	$V_{GBH}$			14	16	17.5	V	
Low-Side Gate Drive, Low State	$V_{GBL}$					0.1		
High-Side Gate Drive, High State	$V_{GTH}$	$T_A = 0$ to 70°C	C Suffix		16	18		
		$T_A = -40$ to 85°C	D Suffix		16	20		
High-Side Gate Drive, Low State	$V_{GTL}$					0.1		
Capacitor Voltage <sup>d</sup>	$V_{CAP}$		$V_+ = 40$ V		55		ns	
Low-Side Switching, Rise Time	$t_{rL}$		Risettime = 1 to 10 V Falltime = 10 to 1 V $C_L = 600$ pF		70			
Low-Side Switching, Fall Time	$t_{fL}$				25			
High-Side Switching, Rise Time	$t_{rH}$				100			
High-Side Switching, Fall Time	$t_{fH}$				40			
Break-Before-Make Time	$t_{BLH}$				100			
	$t_{BHL}$				300			
$\overline{TACH}$ Output/ $\overline{FAULT}$ Output	$V_{OL}$			$I_{OL} = 1.0$ mA		0.15	0.4	V
$\overline{TACH}$ Output Pulsewidth	$t_T$			300	600		ns	



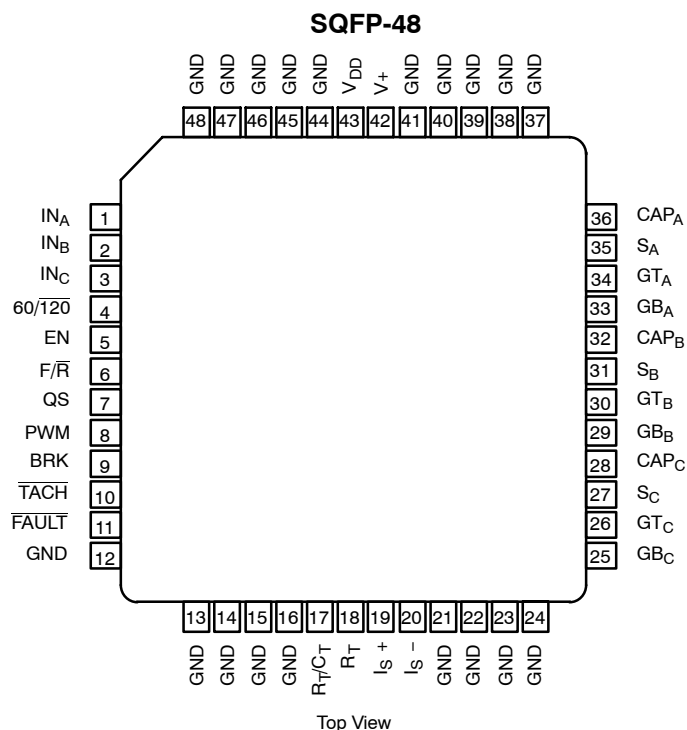
SPECIFICATIONS							
Parameter	Symbol	Test Conditions Unless Otherwise Specified		Limits			Unit
		V <sub>+</sub> = 20 to 40 V, I <sub>DD</sub> = 0 mA		Min <sup>a</sup>	Typ <sup>b</sup>	Max <sup>a</sup>	
<b>Protection</b>							
Low-Side Undervoltage Lockout	UVLL				12.2		V
Low-Side Hysteresis	V <sub>H</sub>				0.8		
High-Side Undervoltage Lockout	UVLH	S <sub>A, B, C</sub> = 0 V			V <sub>DD</sub> - 3.3		
<b>Current Limit</b>							
Comparator Input Bias Current	I <sub>IB</sub>			-5			μA
Comparator Threshold Voltage	V <sub>TH</sub>	T <sub>A</sub> = 0 to 70°C	C Suffix	90	100	110	mV
		T <sub>A</sub> = -40 to 85°C	D Suffix	85	100	125	
Common Mode Voltage	V <sub>CM</sub>			0		1	V
One Shot Pulse Width	t <sub>p</sub>	R <sub>T</sub> = 10 k, C <sub>T</sub> = 0.001 μF		8	10	12	μs
		R <sub>T</sub> = 10 k, C <sub>T</sub> = 0.01 μF		80	100	120	

Notes

- a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
- b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- c. The reference voltage is not available for external use.
- d. V<sub>CAP</sub> = (V<sub>+</sub>) + (V<sub>DD</sub>).

COMMUTATION TRUTH TABLE																	
Inputs										Outputs						Conditions	
Sensors (60° Spacing)			Sensors (120° Spacing)			EN	F/R	BR K	I <sub>S+</sub>	Top Drive			Bottom Drive				FAULT
I <sub>NA</sub>	I <sub>NB</sub>	I <sub>NC</sub>	I <sub>NA</sub>	I <sub>NB</sub>	I <sub>NC</sub>					GT- A	GT- B	GT- C	GB A	GB B	GB C	FAULT	
0	0	0	1	0	1	1	1	0	0	1	0	0	0	1	0	1	
1	0	0	1	0	0	1	1	0	0	1	0	0	0	0	1	1	
1	1	0	1	1	0	1	1	0	0	0	1	0	0	0	1	1	
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1	1	0	1	1	0	1	0	0	0	0	0	1	0	1	0	1	
1	1	1	0	1	0	1	0	0	0	1	0	0	0	1	0	1	
0	1	1	0	1	1	1	0	0	0	1	0	0	0	0	1	1	
0	0	1	0	0	1	1	0	0	0	0	1	0	0	0	1	1	
X	X	X	X	X	X	0	X	0	X	0	0	0	0	0	0	0	Disable
X	X	X	X	X	X	0	X	1	X	0	0	0	1	1	1	0	Power Down
L	L	L	L	L	L	1	X	1	0	0	0	0	1	1	1	1	Brake
L	L	L	L	L	L	1	X	1	1	0	0	0	1	1	1	0	Over I in BRK
L	L	L	L	L	L	1	X	0	1	0	0	0	0	0	0	0	Over I
1	0	1	1	1	1	1	X	0	X	0	0	0	0	0	0	0	
1	0	1	1	1	1	1	X	1	X	0	0	0	1	1	1	0	
0	1	0	0	0	0	1	X	0	X	0	0	0	0	0	0	0	
0	1	0	0	0	0	1	X	1	X	0	0	0	1	1	1	0	

- Notes: L. Any valid sensor combination  
X. Don't care

**PIN CONFIGURATION AND ORDERING INFORMATION**

**ORDERING INFORMATION**

Standard Part Number	Lead (Pb)-Free Part Number	Temperature Range	Package
Si9979CS	Si9979CS—E3	0 to 70 °C	SQFP-48
Si9979DS	Si9979DS—E3	-40 to 85 °C	

NOTE: Si9979CS and Si9979DS are supplied in trays.

**PIN DESCRIPTION**
**Pins 1–3: IN<sub>A</sub>, IN<sub>B</sub>, IN<sub>C</sub>**

IN<sub>A</sub>, IN<sub>B</sub>, and IN<sub>C</sub> are the commutation sensor inputs, and are intended to be driven by open collector Hall effect switches. These inputs have internal pull up resistors tied to V<sub>DD</sub>, which eliminates the need for external pull up resistors.

**Pin 4: 60/120**

The 60/120 input allows the use of the Si9979 with either a 60° or 120° commutation sensor spacing. An internal pull up resistor, which is tied to V<sub>DD</sub>, sets the default condition to 60° spacing. 120° spacing is selected by pulling this input to ground.

**Pin 5: EN (Enable)**

A logic “1” on this input allows commutation of the motor. This is the default condition as this pin is pulled up internally. When this pin is pulled to ground, all gate drive outputs are turned off.

**Pin 6: F/R (Forward/Reverse)**

A logic “1” on this input selects commutation for motor rotation in the “forward” direction. This is the default condition as this

pin is pulled up internally. When this pin is pulled to ground, the commutation sensor logic levels are inverted internally, causing reverse rotation.

**Pin 7: QS (Quadrature Select)**

This input determines whether the bottom MOSFETs or both bottom and top MOSFETs switch in response to the PWM signal. A logic “1” on this input enables only the bottom MOSFETs. This is the default condition as this pin is pulled up internally. When this pin is pulled to ground, both the bottom and top MOSFETs are enabled.

**Pin 8: PWM**

An open collector (drain) or TTL compatible signal is applied to this input to control the motor speed. The QS input determines which MOSFETs are switched in response to the PWM signal. If no PWM signal is being used, this input is left open. It is pulled up internally, which allows the MOSFETs to follow the commutation sequence.

**PIN DESCRIPTION (CONT'D)****Pin 9: BRK**

With this input at logic "1", the top MOSFETs are turned off and the bottom MOSFETs are turned on, shorting the motor windings together. This provides a braking torque which is dependent on the motor speed. This is the default condition as this pin is pulled up internally. When this pin is pulled to ground, the MOSFETs are allowed to follow the commutation sequence.

**Pin 10: TACH**

This output provides a minimum 300-nanosecond output pulse for every commutation sensor transition, yielding a 6 pulse per electrical revolution tachometer signal. This output is open drain.

**Pin 11: FAULT**

The FAULT output switches low to indicate that at least one of the following conditions exists, controller disable ( $\overline{EN}$ ), undervoltage lockout, invalid commutation sensor code shutdown, or overcurrent shutdown. This output is open drain.

**Pin 17:  $R_T/C_T$** 

The junction of the current limit one shot timing resistor and capacitor is connected to this pin. This one-shot is triggered by the current limit comparator when an overcurrent condition exists. This action turns off all the gate drives for the period defined by  $R_T$  and  $C_T$ , thus stopping the flow of current.

**Pin 18:  $R_T$** 

One side of the current limit one shot timing resistor is connected to this pin.

**Pin 19:  $I_S+$** 

This is the sensing input of the current limit comparator and should be connected to the positive side of the current sense resistor. When the voltage across the current sense resistor exceeds 100 mV, the comparator switches and triggers the current limit one-shot. The one-shot turns off all the gate drives for the period defined by  $R_T$  and  $C_T$ , thus stopping the flow of current. If the overcurrent condition remains after the shutdown period, the gate drives will be held off until the overcurrent condition no longer exists.

**Pin 20:  $I_S-$** 

This pin is the ground reference for the current limit comparator. It should be connected directly to the ground side of the current sense resistor to enhance noise immunity.

**Pins 12–16: 21–24, 37–41, 44–48, GND**

These pins are the return path for both the logic and gate drive circuits. Also, they serve to conduct heat out of the package, into the circuit board.

**Pin 25:  $GB_C$** 

This is the gate drive output for the bottom MOSFET in Phase C.

**Pin 26:  $GT_C$** 

This is the gate drive output for the top MOSFET in Phase C.

**Pin 27:  $S_C$** 

This pin is negative supply of the high-side drive circuitry. As such, it is the connection for the negative side of the bootstrap capacitor, the top MOSFET Source, the bottom MOSFET Drain, and the Phase C output.

**Pin 28:  $CAP_C$** 

This pin is the positive supply of the high-side circuitry. The bootstrap capacitor for Phase C is connected between this pin and  $S_C$ .

**Pin 29:  $GB_B$** 

This is the gate drive output for the bottom MOSFET in Phase B.

**Pin 30:  $GT_B$** 

This is the gate drive output for the top MOSFET in Phase B.

**Pin 31:  $S_B$** 

This pin is negative supply of the high-side drive circuitry. As such, it is the connection for the negative side of the bootstrap capacitor, the top MOSFET Source, the bottom MOSFET Drain, and the Phase B output.

**Pin 32:  $CAP_B$** 

This pin is the positive supply of the high-side circuitry. The bootstrap capacitor for Phase B is connected between this pin and  $S_B$ .

**Pin 33:  $GB_A$** 

This is the gate drive output for the bottom MOSFET in Phase A.

**PIN DESCRIPTION (CONT'D)**

**Pin 34:  $GT_A$**

This is the gate drive output for the top MOSFET in Phase A.

**Pin 35:  $S_A$**

This pin is negative supply of the high-side drive circuitry. As such, it is the connection for the negative side of the bootstrap capacitor, the top MOSFET Source, the bottom MOSFET Drain, and the Phase A output.

**Pin 36:  $CAP_A$**

This pin is the positive supply of the high-side circuitry. The bootstrap capacitor for Phase A is connected between this pin and  $S_A$ .

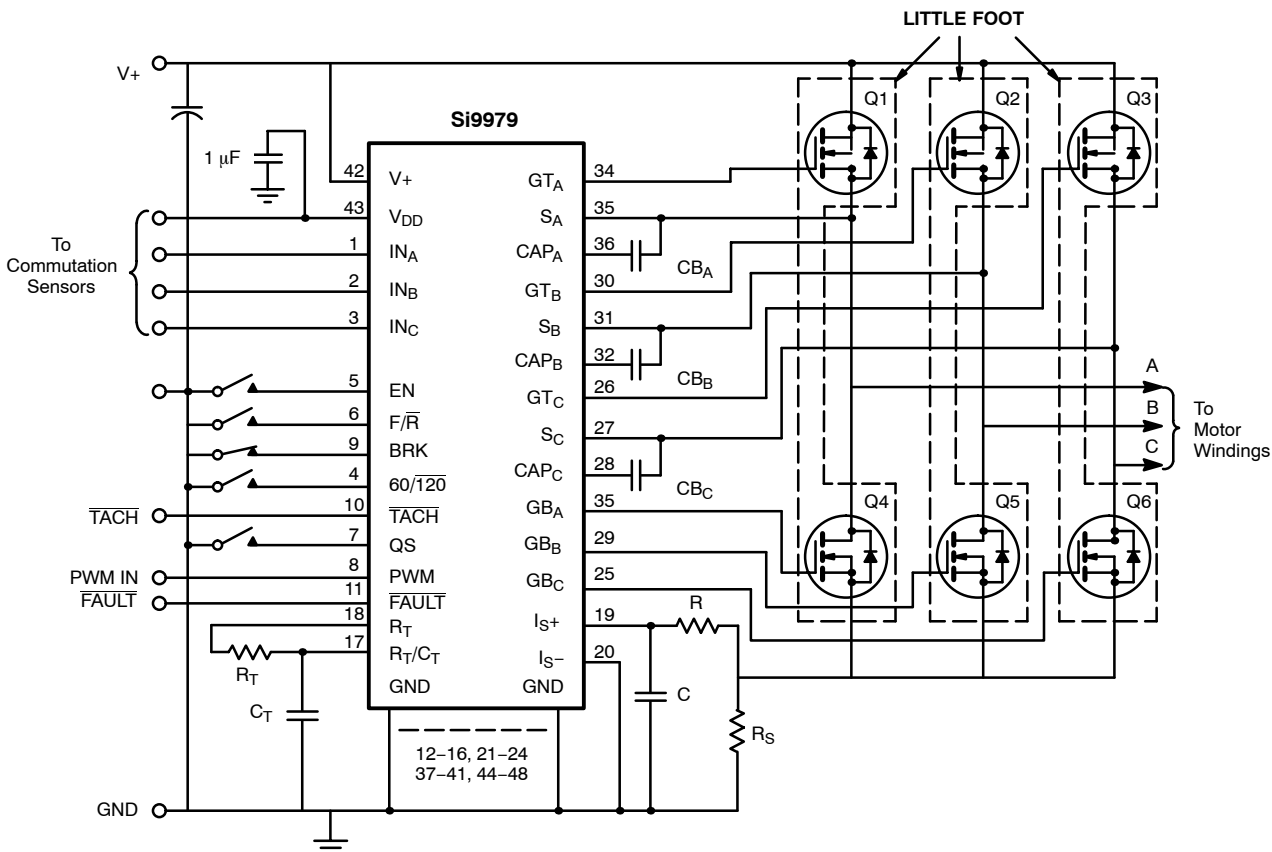
**Pin 42:  $V_+$**

The supply voltage for the Si9979 is connected between this pin and ground. The internal logic and high-side supply voltages are derived from  $V_+$ .

**Pin 43:  $V_{DD}$**

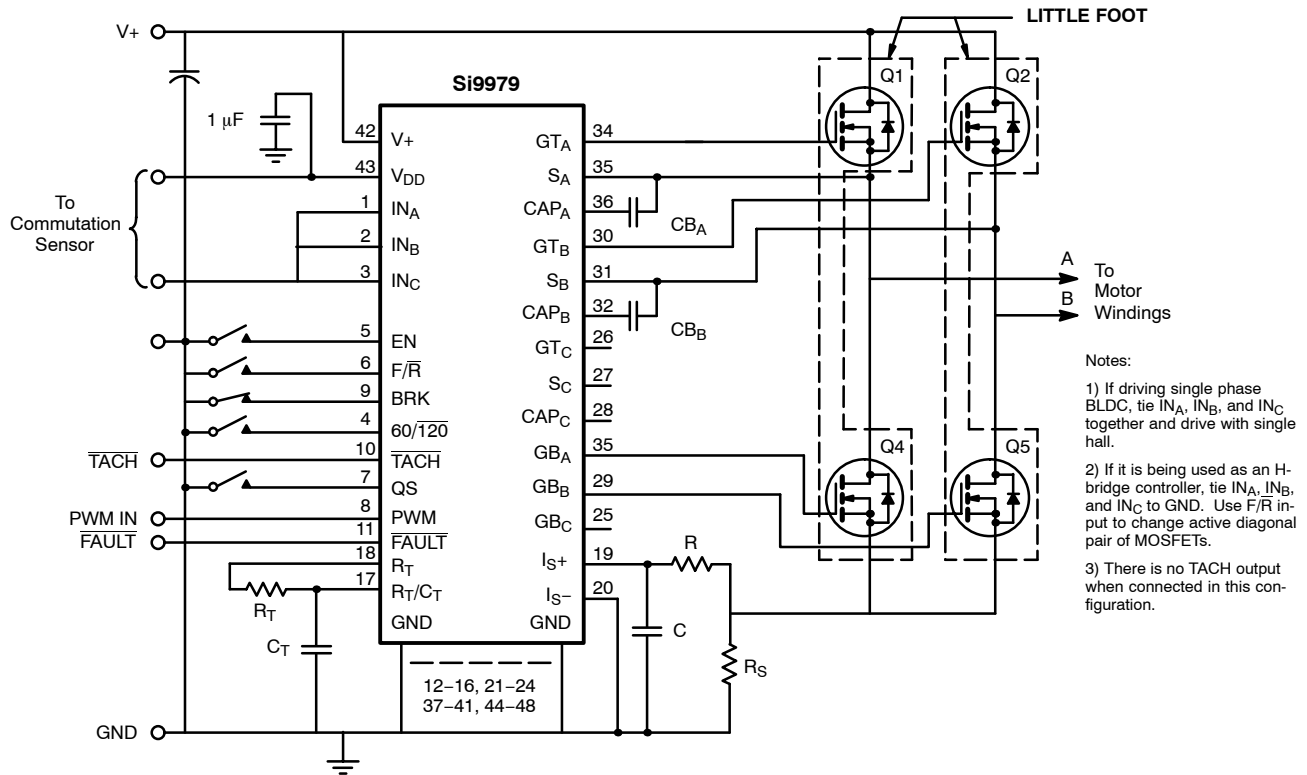
$V_{DD}$  is the internal logic and gate drive voltage. It is necessary to connect a capacitor between this pin and ground to insure that the current surges seen at the turn on of the bottom MOSFETs does not trip the undervoltage lockout circuitry.

**APPLICATION CIRCUITS**

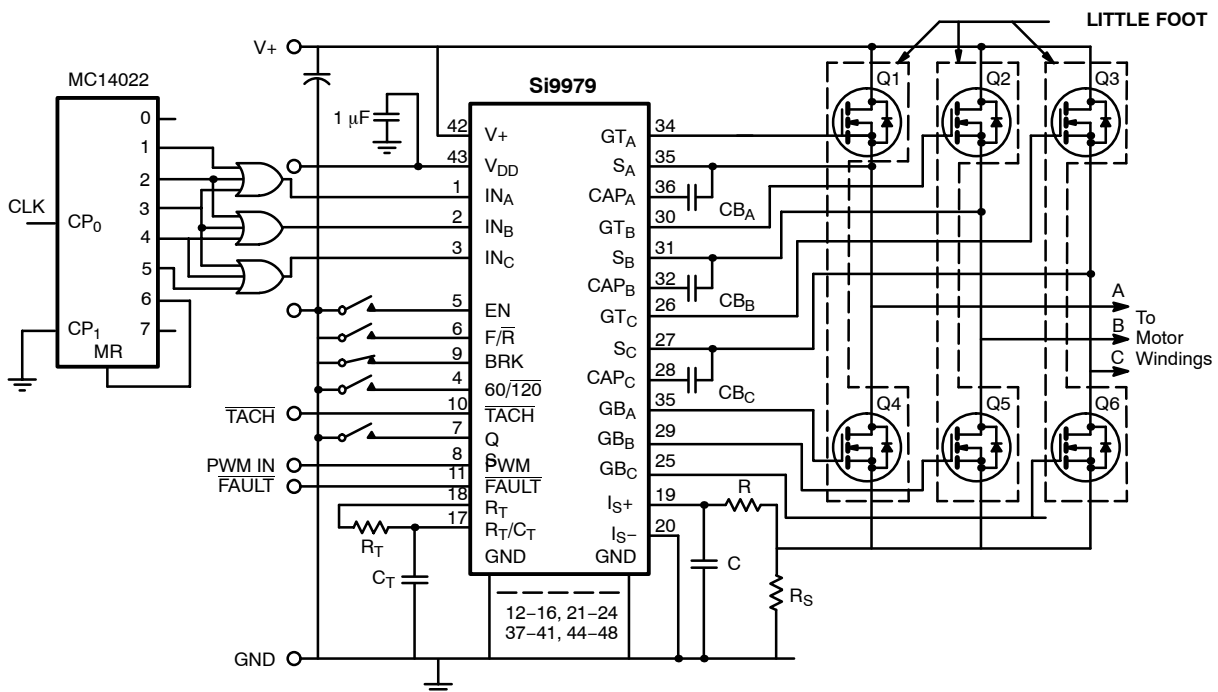


**FIGURE 1.** Three-Phase Brushless DC Motor Controller

**APPLICATION CIRCUITS**



**FIGURE 2.** Single H-Bridge Controller



**FIGURE 3.** Three-Phase AC Motor Controller

**APPLICATION CIRCUITS**

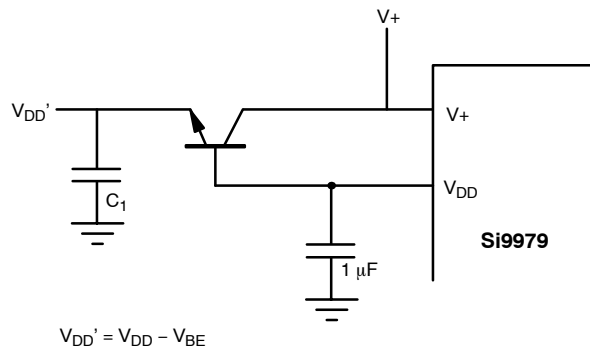
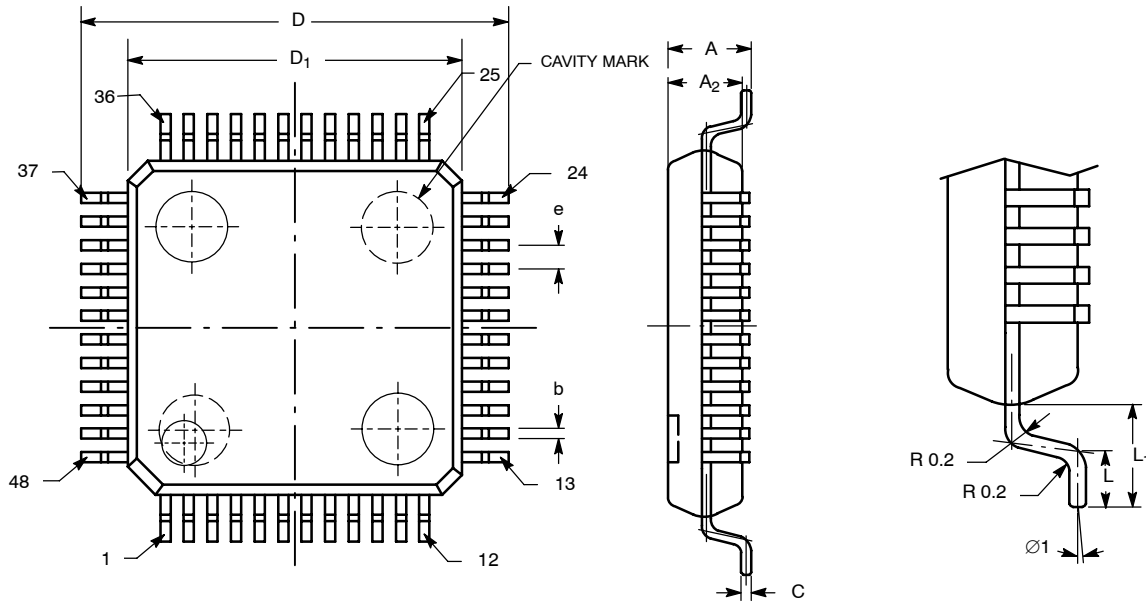


FIGURE 4. External V<sub>DD</sub> Regulator



**SQFP: 48-LEAD (7X7X1.4 MM) SQUARE (POWER IC ONLY)**



Dim	MILLIMETERS		INCHES*	
	Min	Max	Min	Max
<b>A</b>	1.40	1.60	0.055	0.063
<b>A<sub>1</sub></b>	0.05	0.15	0.002	0.006
<b>A<sub>2</sub></b>	1.35	1.45	0.053	0.057
<b>b</b>	0.17	0.26	0.006	0.010
<b>C</b>	0.117	0.177	0.005	0.007
<b>D</b>	8.70	9.30	0.343	0.366
<b>D<sub>1</sub></b>	6.90	7.10	0.270	0.280
<b>e</b>	0.50 TYP		0.020 TYP	
<b>L</b>	0.45	0.75	0.018	0.030
<b>L<sub>1</sub></b>	0.90	1.10	0.035	0.043
<b>Ø1</b>	0°	7°	0°	7°
ECN: S-40084—Rev. A, 02-Feb-04 DWG: 5928				

\* For reference only



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