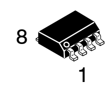
NCL30185

Power Factor Corrected Quasi-Resonant Primary Side Current-Mode Controller for LED Lighting with Line Step Dimming and Thermal Foldback

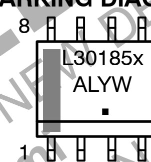
ON Semiconductor®

www.onsemi.com



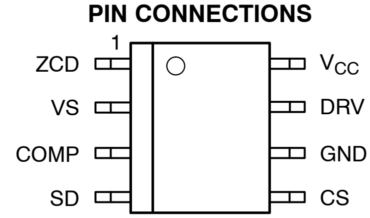
SOIC−8 NB
CASE 751

MARKING DIAGRAM



L30185x = Specific Device Code
x = A, B
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 27 of this data sheet.

The NCL30185 is a controller targeting isolated and non−isolated "smart−dimmable" constant−current LED drivers. Designed to support flyback, buck−boost, and SEPIC topologies, its proprietary current−control algorithm provides near−unity power factor and tightly regulates a constant LED current from the primary side, thus eliminating the need for a secondary−side feedback circuitry or an optocoupler.

Housed in the SOIC8, the NCL30185 is specifically intended for very compact space−efficient designs. The device is highly integrated with a minimum number of external components. A robust suite of safety protections is built in to simplify the design. To ensure reliable operation at elevated temperatures, a user configurable current foldback circuit is also provided. In addition, it supports step dimming which allows light output reduction by toggling the main AC switch on and off.

Pin−to−pin compatible to the NCL30085, the NCL30185 provides the same benefits with in addition, an increased resolution of the digital current−control algorithm for a 75% reduction in the LED current quantization ripple.

Features

- Quasi−resonant Peak Current−mode Control Operation
- Valley Lockout Optimizes Efficiency over the Line/Load Range
- Constant Current Control with Primary Side Feedback
- Tight LED Constant Current Regulation of ±2% Typical
- Power Factor Correction
- 3 Step Dimming (70/25/5%)
- Line Feedforward for Enhanced Regulation Accuracy
- Low Start−up Current (10 µA typ.)
- Wide V_{cc} Range
- 300 mA / 500 mA Totem Pole Driver with 12 V Gate Clamp
- Robust Protection Features
  - OVP on V_{CC}
  - Programmable Over Voltage / LED Open Circuit Protection
  - Cycle−by−cycle Peak Current Limit
  - Winding Short Circuit Protection
  - Secondary Diode Short Protection
  - Output Short Circuit Protection
  - Current Sense Short Protection
  - User Programmable NTC Based Thermal Foldback
  - Thermal Shutdown
  - V_{cc} Undervoltage Lockout
  - Brown−out Protection
- Pb−Free, Halide−Free MSL1 Product

Typical Applications

- Integral LED Bulbs and Tubes
- LED Light Engines
- LED Drivers/Power Supplies

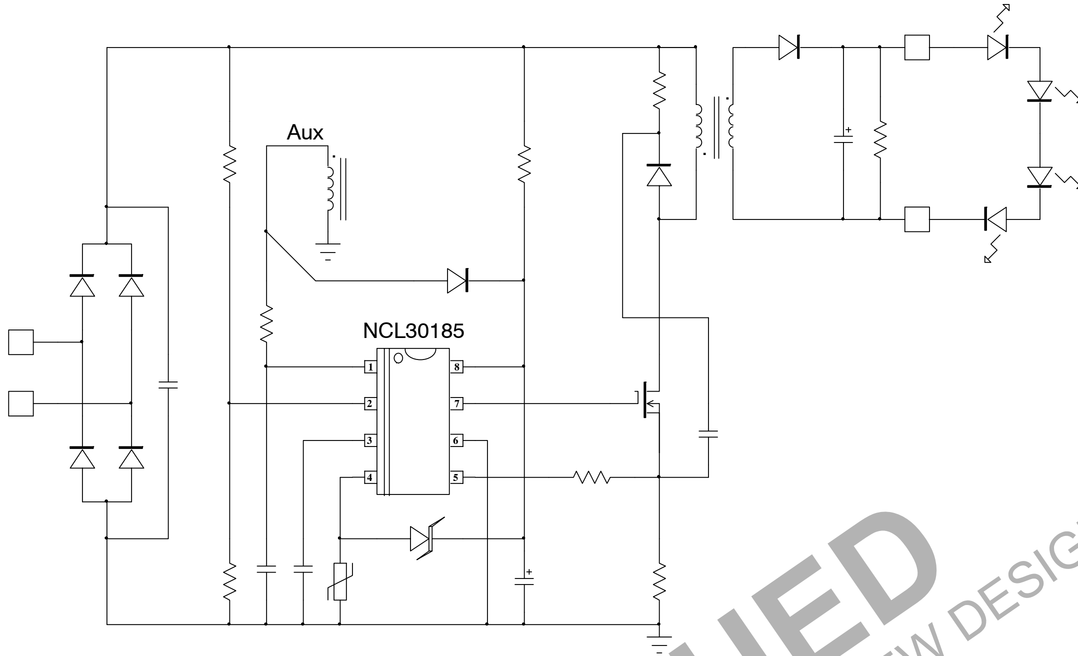


Figure 1. Typical Application Schematic in a Flyback Converter

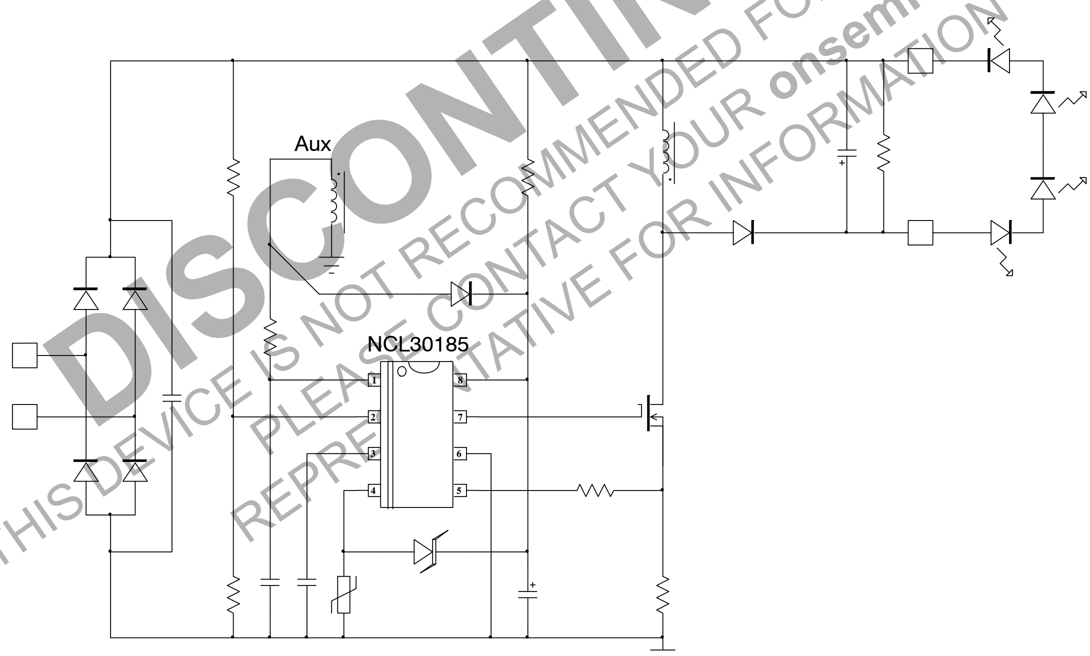


Figure 2. Typical Application Schematic in a Buck−Boost Converter

Table 1. PIN FUNCTION DESCRIPTION

Pin No	Pin Name	Function	Pin Description
1	ZCD	Zero Crossing Detection	Connected to the auxiliary winding, this pin detects the core reset event.
2	VS	Input Voltage Sensing	This pin observes the input voltage rail and protects the LED driver in case of too low mains conditions (brown−out). This pin also observes the input voltage rail for: − Power Factor Correction − Valley lockout − Step dimming
3	COMP	Filtering Capacitor	This pin receives a filtering capacitor for power factor correction. Typical values ranges from 1 − 4.70 μF
4	SD	Thermal Foldback and Shutdown	Connecting an NTC to this pin allows the user to program thermal current foldback threshold and slope. A Zener diode can also be used to pull−up the pin and stop the controller for adjustable OVP protection.
5	CS	Current Sense	This pin monitors the primary peak current.
6	GND	−	Controller ground pin.
7	DRV	Driver Output	The driver's output to an external MOSFET
8	V_{CC}	IC Supply Pin	This pin is the positive supply of the IC. The circuit starts to operate when V_{CC} exceeds 18 V and turns off when V_{CC} goes below 8.8 V (typical values). After start−up, the operating range is 9.4 V up to 26 V ($V_{CC(OVP)}$ minimum level).

Internal Circuit Architecture

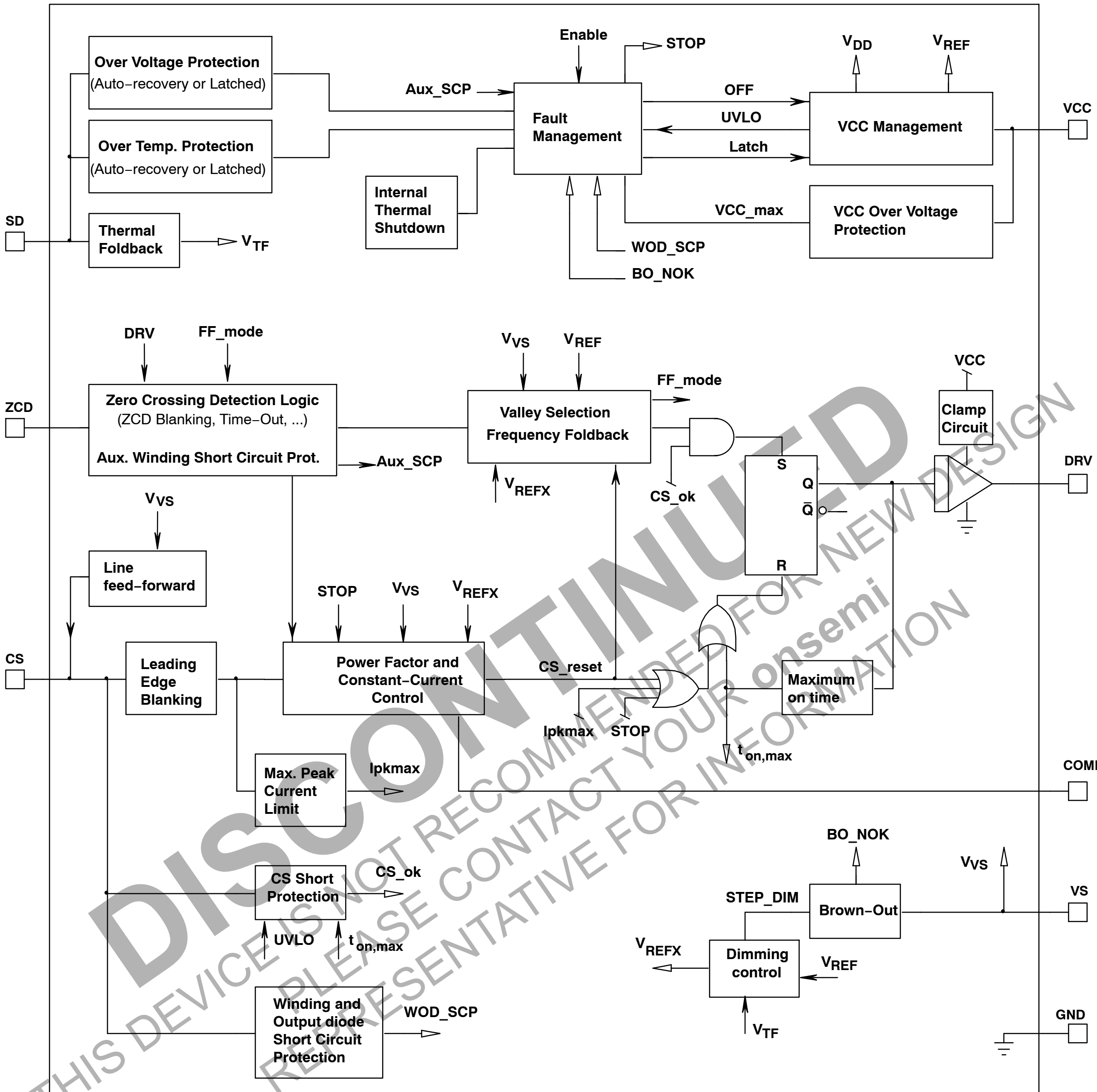


Figure 3. Internal Circuit Architecture

Table 2. MAXIMUM RATINGS TABLE

Symbol	Rating	Value	Unit
$V_{CC(MAX)}$ $I_{CC(MAX)}$	Maximum Power Supply voltage, V_{CC} pin, continuous voltage Maximum current for V_{CC} pin	−0.3 to 30 Internally limited	V mA
$V_{DRV(MAX)}$ $I_{DRV(MAX)}$	Maximum driver pin voltage, DRV pin, continuous voltage Maximum current for DRV pin	−0.3, V_{DRV} (Note 1) −300, +500	V mA
V_{MAX} I_{MAX}	Maximum voltage on low power pins (except DRV and V_{CC} pins) Current range for low power pins (except DRV and V_{CC} pins)	−0.3, 5.5 (Notes 2 and 5) −2, +5	V mA
$R_{\theta J-A}$	Thermal Resistance Junction−to−Air	180	°C/W
$T_{J(MAX)}$	Maximum Junction Temperature	150	°C
	Operating Temperature Range	−40 to +125	°C
	Storage Temperature Range	−60 to +150	°C
	ESD Capability, HBM model (Note 3)	3.5	kV
	ESD Capability, MM model (Note 3)	250	V
	ESD Capability, CDM model (Note 3)	2	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. V_{DRV} is the DRV clamp voltage $V_{DRV(high)}$ when V_{CC} is higher than $V_{DRV(high)}$. V_{DRV} is V_{CC} otherwise.
2. These levels are low enough not to exceed the maximum ratings of the internal ESD 5.5−V Zener diode. More positive and negative voltages can be applied if the pin current stays within the −2−mA / 5−mA range.
3. This device contains ESD protection and exceeds the following tests: Human Body Model 3500 V per JEDEC Standard JESD22−A114E, Machine Model Method 250 V per JEDEC Standard JESD22−A115B, Charged Device Model 2000 V per JEDEC Standard JESD22−C101E.
4. This device contains latch−up protection and has been tested per JEDEC Standard JESD78D, Class I and exceeds ±100 mA
5. **Recommended maximum V_S voltage for optimal operation is 4 V. −0.3 V to +4.0 V is hence, the V_S pin recommended range.**

Table 3. ELECTRICAL CHARACTERISTICS (Unless otherwise noted: For typical values T_J = 25°C, V_{CC} = 12 V, V_{ZCD} = 0 V, V_{CS} = 0 V, V_{SD} = 1.5 V) For min/max values T_J = −40°C to +125°C, V_{CC} = 12 V)

Description	Test Condition	Symbol	Min	Typ	Max	Unit
STARTUP AND SUPPLY CIRCUITS						
Supply Voltage Startup Threshold Minimum Operating Voltage Hysteresis $V_{CC(on)} - V_{CC(off)}$ Internal logic reset	 V_{CC} rising V_{CC} rising V_{CC} falling	 $V_{CC(on)}$ $V_{CC(off)}$ $V_{CC(HYS)}$ $V_{CC(reset)}$	 16.0 8.2 8 4	 18.0 8.8 – 5	 20.0 9.4 – 6	V
V_{CC} Over Voltage Protection Threshold		$V_{CC(OVP)}$	25.5	26.8	28.5	V
$V_{CC(off)}$ noise filter $V_{CC(reset)}$ noise filter		$t_{VCC(off)}$ $t_{VCC(reset)}$	– –	5 20	– –	µs
Startup current		$I_{CC(start)}$	–	13	30	µA
Startup current in fault mode		$I_{CC(sFault)}$		58	75	µA
Supply Current Device Disabled/Fault Device Enabled/No output load on pin 7 Device Switching (F_{SW} = 65 kHz)	 $V_{CC} > V_{CC(off)}$ F_{sw} = 65 kHz C_{DRV} = 470 pF, F_{sw} = 65 kHz	 I_{CC1} I_{CC2} I_{CC3}	 0.8 – –	 1.0 2.5 3.0	 1.2 4.0 4.5	mA
CURRENT SENSE						
Maximum Internal current limit		V_{ILIM}	0.95	1.00	1.05	V
Leading Edge Blanking Duration for V_{ILIM}		t_{LEB}	240	300	360	ns
Line feed−forward current	DRV high, V_{VS} = 2 V	I_{FF}	35	40	45	µA

6. Guaranteed by Design
7. A NTC is generally placed between the SD and GND pins. Parameters $R_{TF(start)}$, $R_{TF(stop)}$, $R_{OTP(off)}$ and $R_{OTP(on)}$ give the resistance the NTC must exhibit to respectively, enter thermal foldback, stop thermal foldback, trigger the OTP limit and allow the circuit recovery after an OTP situation.
8. At startup, when V_{CC} reaches $V_{CC(on)}$, the controller blanks OTP for more than 250 µs to avoid detecting an OTP fault by allowing the SD pin voltage to reach its nominal value if a filtering capacitor is connected to the SD pin.

Table 3. ELECTRICAL CHARACTERISTICS (Unless otherwise noted: For typical values T_J = 25°C, V_{CC} = 12 V, V_{ZCD} = 0 V, V_{CS} = 0 V, V_{SD} = 1.5 V) For min/max values T_J = −40°C to +125°C, V_{CC} = 12 V)

Description	Test Condition	Symbol	Min	Typ	Max	Unit
CURRENT SENSE						
Propagation delay from current detection to gate off−state		t_{ILIM}	–	100	150	ns
Maximum on−time		$t_{on(MAX)}$	26	36	46	μs
Threshold for immediate fault protection activation		$V_{CS(stop)}$	1.35	1.50	1.65	V
Leading Edge Blanking Duration for $V_{CS(stop)}$		t_{BCS}	–	150	–	ns
Current source for CS to GND short detection		$I_{CS(short)}$	400	500	600	μA
Current sense threshold for CS to GND short detection	V_{CS} rising	$V_{CS(low)}$	30	65	100	mV
GATE DRIVE						
Drive Resistance DRV Sink DRV Source		 R_{SNK} R_{SRC}	 – –	 13 30	 – –	Ω
Drive current capability DRV Sink (Note 6) DRV Source (Note 6)		 I_{SNK} I_{SRC}	 – –	 500 300	 – –	mA
Rise Time (10% to 90%)	C_{DRV} = 470 pF	t_r	–	40	–	ns
Fall Time (90% to 10%)	C_{DRV} = 470 pF	t_f	–	30	–	ns
DRV Low Voltage	V_{CC} = $V_{CC(off)}$+0.2 V C_{DRV} = 470 pF, R_{DRV}=33 kΩ	$V_{DRV(low)}$	8	–	–	V
DRV High Voltage	V_{CC} = $V_{CC(MAX)}$ C_{DRV} = 470 pF, R_{DRV}=33 kΩ	$V_{DRV(high)}$	10	12	14	V
ZERO VOLTAGE DETECTION CIRCUIT						
Upper ZCD threshold voltage	V_{ZCD} rising	$V_{ZCD(rising)}$	–	90	150	mV
Lower ZCD threshold voltage	V_{ZCD} falling	$V_{ZCD(falling)}$	35	55	–	mV
ZCD hysteresis		$V_{ZCD(HYS)}$	15	–	–	mV
Propagation Delay from valley detection to DRV high	V_{ZCD} falling	T_{DEM}	–	100	300	ns
Blanking delay after on−time	V_{REFX} > 30% V_{REF}	$T_{ZCD(blank1)}$	1.12	1.50	1.88	μs
Blanking Delay at light load	V_{REFX} < 25% V_{REF}	$T_{ZCD(blank2)}$	0.56	0.75	0.94	μs
Timeout after last DEMAG transition		T_{TIMO}	5.0	6.5	8.0	μs
Pulling−down resistor	V_{ZCD} = $V_{ZCD(falling)}$	$R_{ZCD(PD)}$	–	200	–	kΩ
CONSTANT CURRENT AND POWER FACTOR CONTROL						
Reference Voltage at T_J = 25°C		V_{REF}	245	250	255	mV
Reference Voltage T_J = 25°C to 100°C		V_{REF}	242.5	250.0	257.5	mV
Reference Voltage T_J = −40°C to 125°C		V_{REF}	240	250	260	mV
Current sense lower threshold	V_{CS} falling	$V_{CS(low)}$	20	50	100	mV
$V_{control}$ to current setpoint division ratio		V_{ratio}	–	4	–	–
Error amplifier gain	V_{REFX}=V_{REF} (no dimming) V_{REFX}=25%* V_{REF}	G_{EA}	40	50 200	60	μS

6. Guaranteed by Design
7. A NTC is generally placed between the SD and GND pins. Parameters $R_{TF(start)}$, $R_{TF(stop)}$, $R_{OTP(off)}$ and $R_{OTP(on)}$ give the resistance the NTC must exhibit to respectively, enter thermal foldback, stop thermal foldback, trigger the OTP limit and allow the circuit recovery after an OTP situation.
8. At startup, when V_{CC} reaches $V_{CC(on)}$, the controller blanks OTP for more than 250 μs to avoid detecting an OTP fault by allowing the SD pin voltage to reach its nominal value if a filtering capacitor is connected to the SD pin.

Table 3. ELECTRICAL CHARACTERISTICS (Unless otherwise noted: For typical values T_J = 25°C, V_{CC} = 12 V, V_{ZCD} = 0 V, V_{CS} = 0 V, V_{SD} = 1.5 V) For min/max values T_J = −40°C to +125°C, V_{CC} = 12 V)

Description	Test Condition	Symbol	Min	Typ	Max	Unit
CONSTANT CURRENT AND POWER FACTOR CONTROL						
Error amplifier current capability	V_{REFX}=V_{REF} (no dimming) V_{REFX}=25%* V_{REF}	I_{EA}		±60 ±240		μA
COMP Pin Start−up Current Source	No dimming, COMP pin grounded	I_{EA_STUP}		140		μA
LINE FEED FORWARD						
V_{VS} to $I_{CS(offset)}$ conversion ratio		K_{LFF}	18	20	22	μS
Line feed−forward current on CS pin	DRV high, V_{VS} = 2 V	I_{FF}	35	40	45	μA
Offset current maximum value	V_{VS} > 5 V	$I_{offset(MAX)}$	80	100	120	μA
VALLEY LOCKOUT SECTION						
Threshold for high− line range (HL) detection	V_{VS} rising	V_{HL}	2.28	2.40	2.52	V
Threshold for low−line range (LL) detection	V_{VS} falling	V_{LL}	2.18	2.30	2.42	V
Blanking time for line range detection		$t_{HL(blank)}$	15	25	35	ms
Valley Lockout First step valley in High−Line. Second step valley in High−Line. Third step valley in High−Line. First step valley in Low−Line. Second step valley in Low−Line. Third step valley in Low−Line.		 $V_{HL100\%}$ $V_{HL70\%}$ $V_{HL25\%}$ $V_{LL100\%}$ $V_{LL70\%}$ $V_{LL25\%}$		 2 3 6 1 2 5		
FREQUENCY FOLDBACK						
Additional dead time	V_{REFX} = 25%*V_{REF}	t_{FF1LL}	1.4	2.0	2.6	μs
Additional dead time	V_{REFX} = 5%*V_{REF}	t_{FF2HL}	−	40	−	μs
FAULT PROTECTION						
Thermal Shutdown (Note 6)	F_{SW} = 65 kHz	T_{SHDN}	130	150	170	°C
Thermal Shutdown Hysteresis		$T_{SHDN(HYS)}$	−	50	−	°C
Threshold voltage for output short circuit or aux. winding short circuit detection		$V_{ZCD(short)}$	0.8	1.0	1.2	V
Short circuit detection Timer	V_{ZCD} < $V_{ZCD(short)}$	t_{OVLD}	70	90	110	ms
Auto−recovery timer duration		$t_{recovery}$	3	4	5	s
SD pin Clamp series resistor		$R_{SD(clamp)}$		1.6		kΩ
Clamped voltage	SD pin open	$V_{SD(clamp)}$	1.13	1.35	1.57	V
SD pin detection level for OVP	V_{SD} rising	V_{OVP}	2.35	2.50	2.65	V
Delay before OVP or OTP confirmation (OVP and OTP)		$T_{SD(delay)}$	22.5	30.0	37.5	μs
Reference current for direct connection of an NTC (Note 8)		$I_{OTP(REF)}$	80	85	90	μA
Fault detection level for OTP (Note 7)	V_{SD} falling	$V_{OTP(off)}$	0.47	0.50	0.53	V
SD pin level for operation recovery after an OTP detection	V_{SD} rising	$V_{OTP(on)}$	0.66	0.70	0.74	V

6. Guaranteed by Design
7. A NTC is generally placed between the SD and GND pins. Parameters $R_{TF(start)}$, $R_{TF(stop)}$, $R_{OTP(off)}$ and $R_{OTP(on)}$ give the resistance the NTC must exhibit to respectively, enter thermal foldback, stop thermal foldback, trigger the OTP limit and allow the circuit recovery after an OTP situation.
8. At startup, when V_{CC} reaches $V_{CC(on)}$, the controller blanks OTP for more than 250 μs to avoid detecting an OTP fault by allowing the SD pin voltage to reach its nominal value if a filtering capacitor is connected to the SD pin.

Table 3. ELECTRICAL CHARACTERISTICS (Unless otherwise noted: For typical values T_J = 25°C, V_{CC} = 12 V, V_{ZCD} = 0 V, V_{CS} = 0 V, V_{SD} = 1.5 V) For min/max values T_J = −40°C to +125°C, V_{CC} = 12 V)

Description	Test Condition	Symbol	Min	Typ	Max	Unit
FAULT PROTECTION						
OTP blanking time when circuit starts operating (Note 8)		$t_{OTP(start)}$	250		370	μs
SD pin voltage at which thermal fold−back starts (V_{REF} is decreased)		$V_{TF(start)}$	0.94	1.00	1.06	V
SD pin voltage at which thermal fold−back stops (V_{REF} is clamped to V_{REF50})		$V_{TF(stop)}$	0.64	0.69	0.74	V
$V_{TF(start)}$ over $I_{OTP(REF)}$ ratio (Note 7)	T_J = +25°C to +125°C	$R_{TF(start)}$	10.8	11.7	12.6	kΩ
$V_{TF(stop)}$ over $I_{OTP(REF)}$ ratio (Note 7)	T_J = +25°C to +125°C	$R_{TF(stop)}$	7.4	8.1	8.8	kΩ
$V_{OTP(off)}$ over $I_{OTP(REF)}$ ratio (Note 7)	T_J = +25°C to +125°C	$R_{OTP(off)}$	5.4	5.9	6.4	kΩ
$V_{OTP(on)}$ over $I_{OTP(REF)}$ ratio (Note 7)	T_J = +25°C to +125°C	$R_{OTP(on)}$	7.5	8.1	8.7	kΩ
V_{REFX} @ V_{SD} = 600 mV (percent of V_{REF})	SD pin falling, no OTP detection	$V_{REF(50)}$	40	50	60	%
BROWN−OUT						
Brown−Out ON level (IC start pulsing)	V_S rising	$V_{BO(on)}$	0.95	1.00	1.05	V
Brown−Out OFF level (IC shuts down)	V_S falling	$V_{BO(off)}$	0.85	0.90	0.95	V
BO comparators delay		$t_{BO(delay)}$		30		μs
Brown−Out blanking time		$t_{BO(blank)}$	15	25	35	ms
V_S pin Pulling−down Current	$V_S = V_{BO(on)}$	$I_{BO(bias)}$	50	250	450	nA
Step Dimming Reset Time	$V_S < V_{BO(off)}$	$t_{step−reset}$	2.4	3.2	4.0	s

6. Guaranteed by Design
7. A NTC is generally placed between the SD and GND pins. Parameters $R_{TF(start)}$, $R_{TF(stop)}$, $R_{OTP(off)}$ and $R_{OTP(on)}$ give the resistance the NTC must exhibit to respectively, enter thermal foldback, stop thermal foldback, trigger the OTP limit and allow the circuit recovery after an OTP situation.
8. At startup, when V_{CC} reaches $V_{CC(on)}$, the controller blanks OTP for more than 250 μs to avoid detecting an OTP fault by allowing the SD pin voltage to reach its nominal value if a filtering capacitor is connected to the SD pin.

TYPICAL CHARACTERISTICS

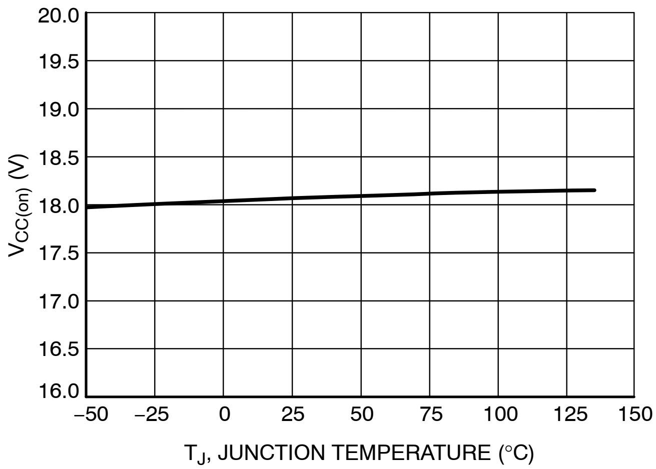


Figure 4. V_{CC} Start−up Threshold vs. Temperature

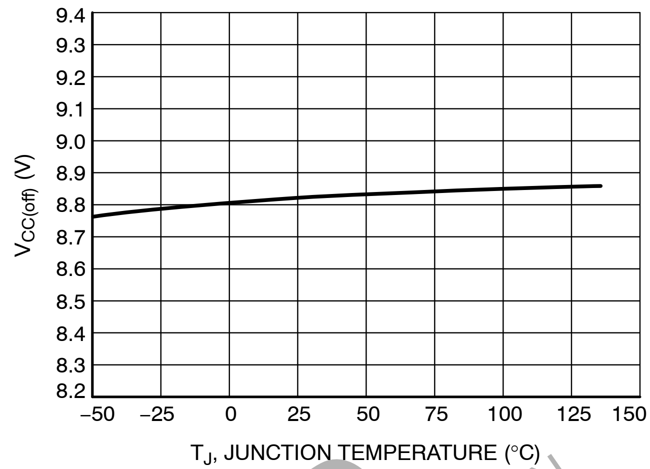


Figure 5. V_{CC} Minimum Operating Voltage vs. Temperature

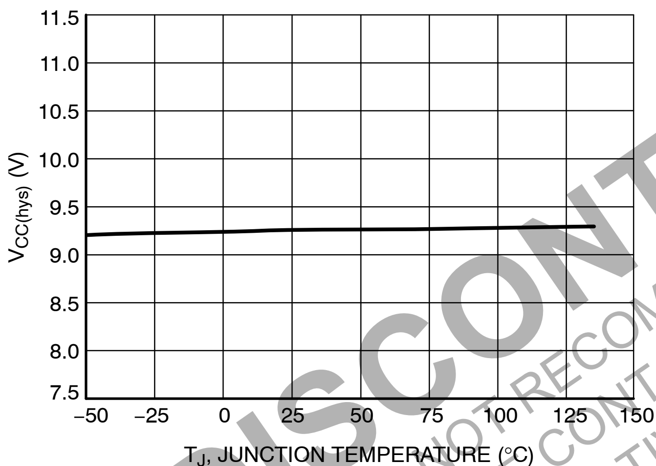


Figure 6. Hysteresis ($V_{CC(on)}$ – $V_{CC(off)}$) vs. Temperature

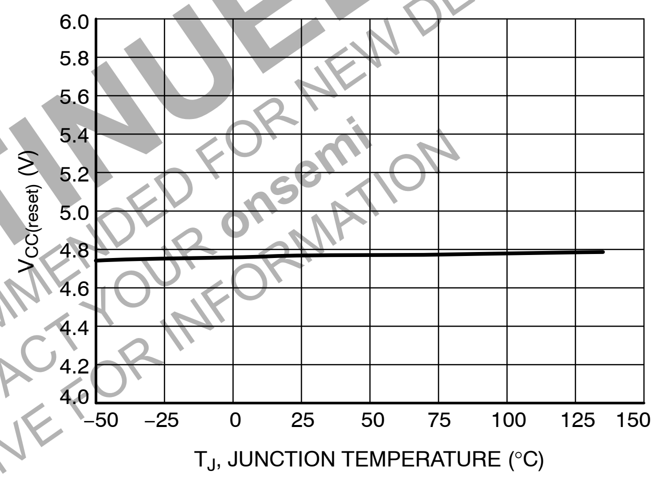


Figure 7. $V_{CC(reset)}$ vs. Temperature

TYPICAL CHARACTERISTICS

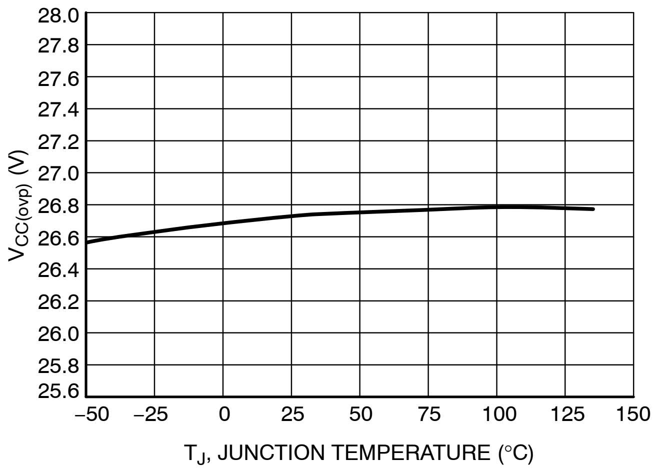


Figure 8. V_{CC} Over Voltage Protection Threshold vs. Temperature

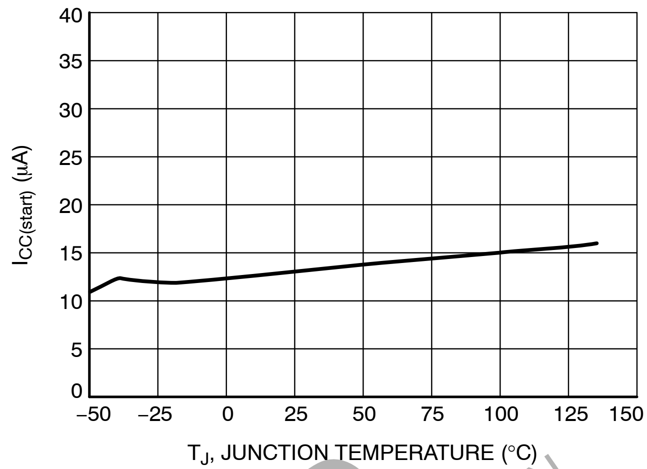


Figure 9. Start−up Current vs. Temperature

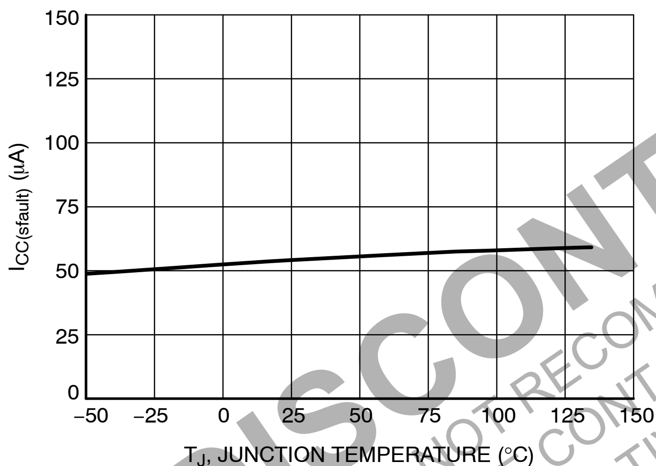


Figure 10. Start−up Current in Fault Mode vs. Temperature

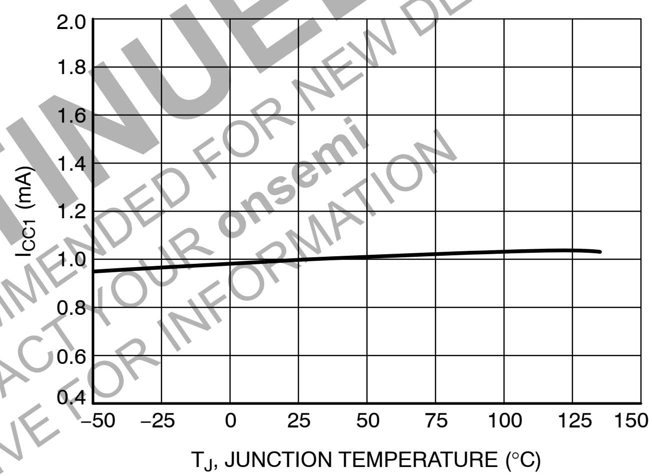


Figure 11. I_{CC1} vs. Temperature

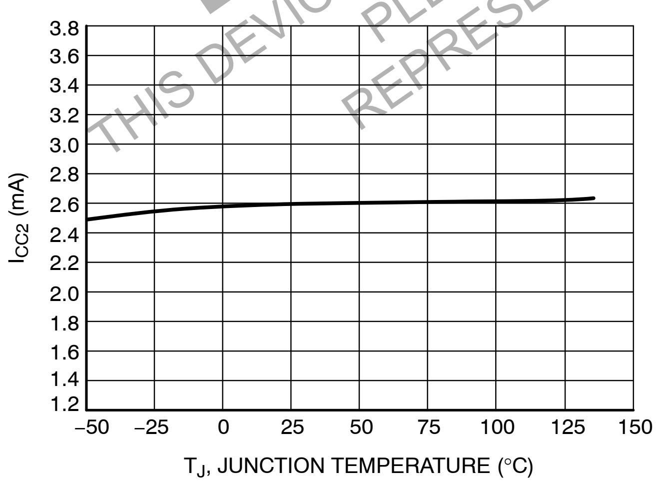


Figure 12. I_{CC2} vs. Temperature

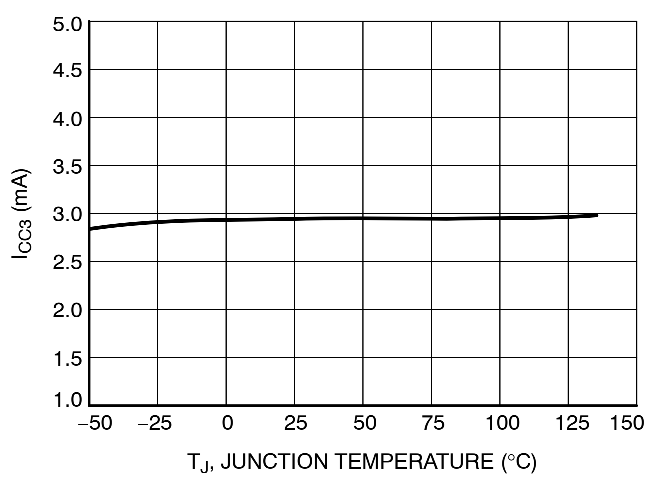


Figure 13. I_{CC3} vs. Temperature

TYPICAL CHARACTERISTICS

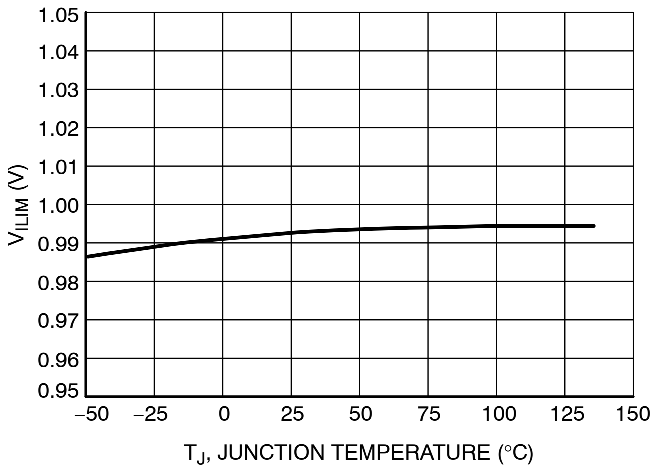


Figure 14. Maximum Internal Current Limit vs. Temperature

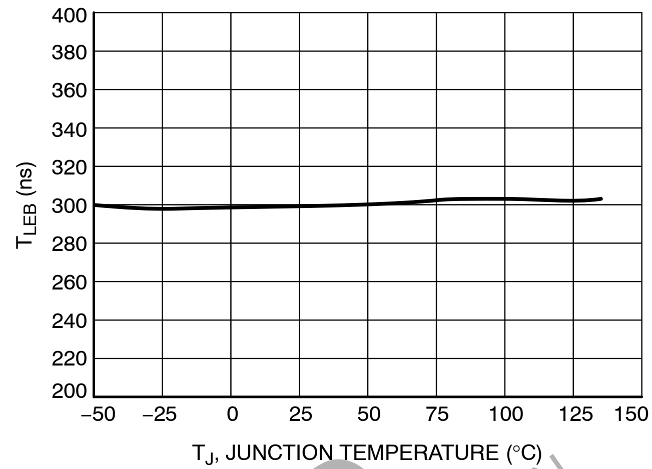


Figure 15. Leading Edge Blanking vs. Temperature

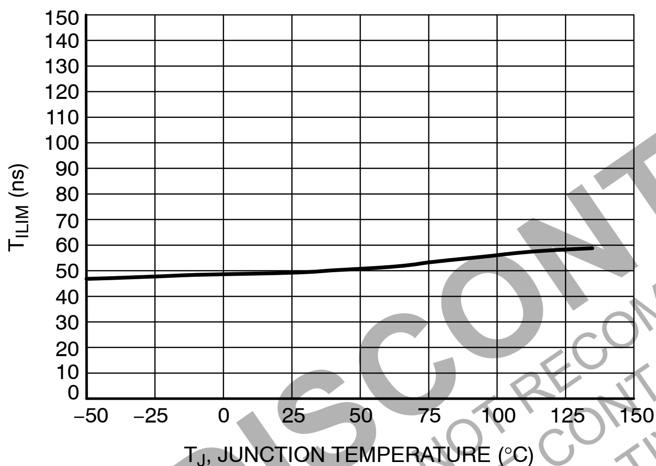


Figure 16. Current Limit Propagation Delay vs. Temperature

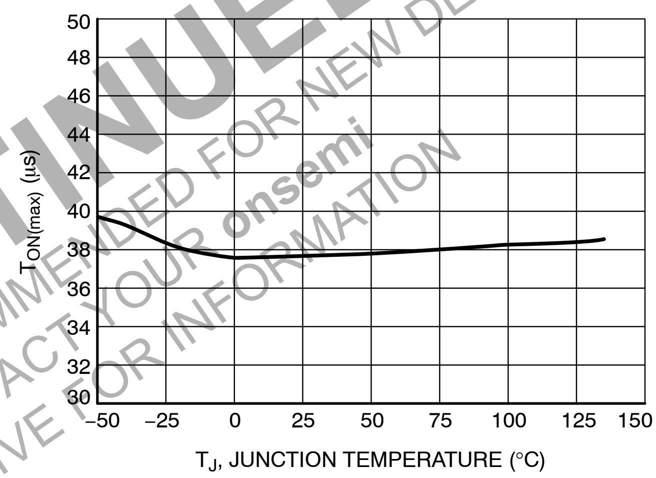


Figure 17. Maximum On−time vs. Temperature

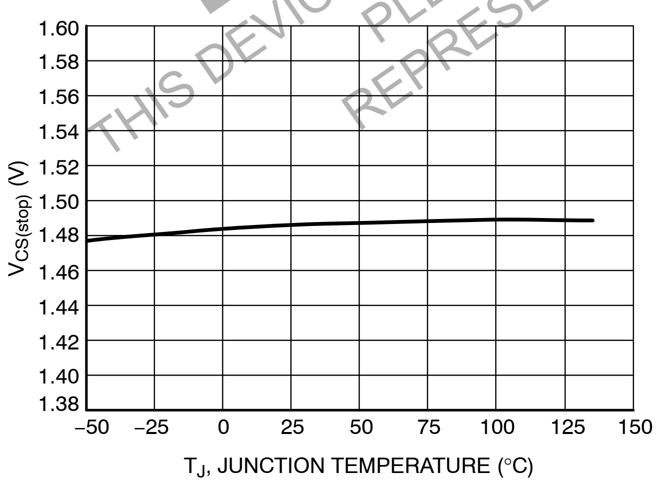


Figure 18. $V_{CS(stop)}$ vs. Temperature

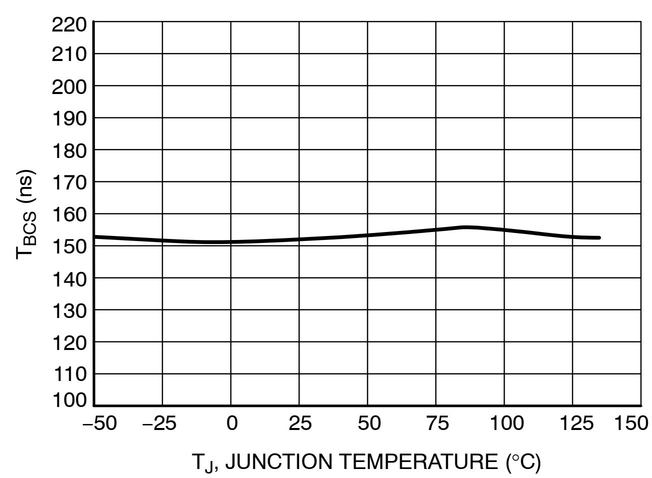


Figure 19. Leading Edge Blanking Duration for $V_{CS(stop)}$ vs. Temperature

TYPICAL CHARACTERISTICS

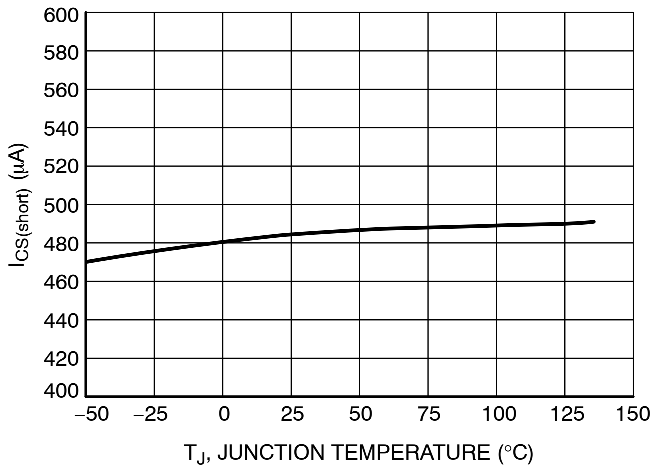


Figure 20. $I_{CS(short)}$ vs. Temperature

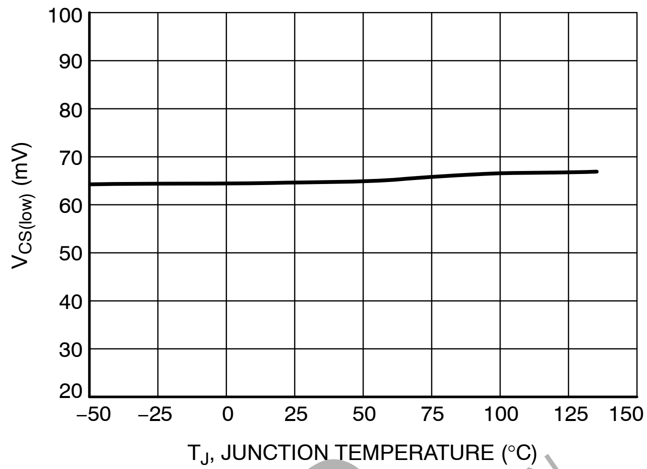


Figure 21. $V_{CS(low)}$, V_{CS} Rising vs. Temperature

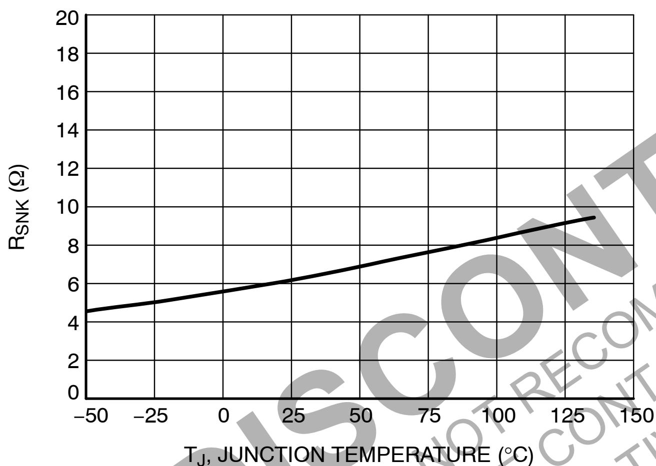


Figure 22. Sink Gate Drive Resistance vs. Temperature

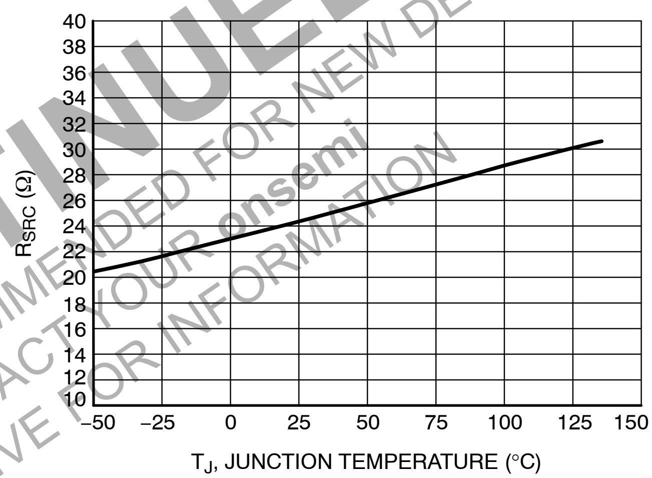


Figure 23. Source Gate Drive Resistance vs. Temperature

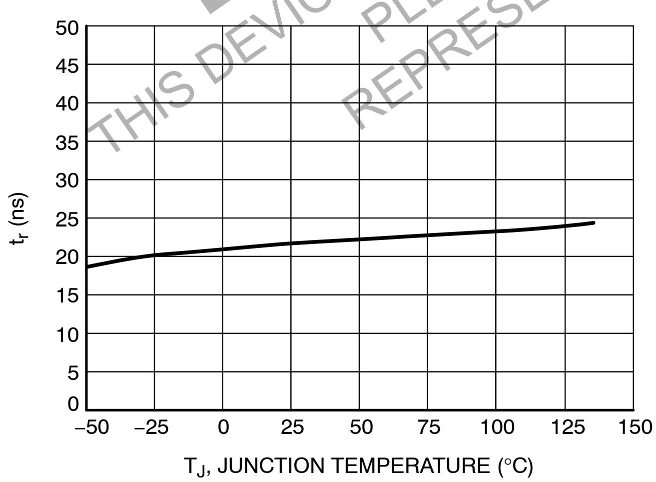


Figure 24. Gate Drive Rise Time vs. Temperature

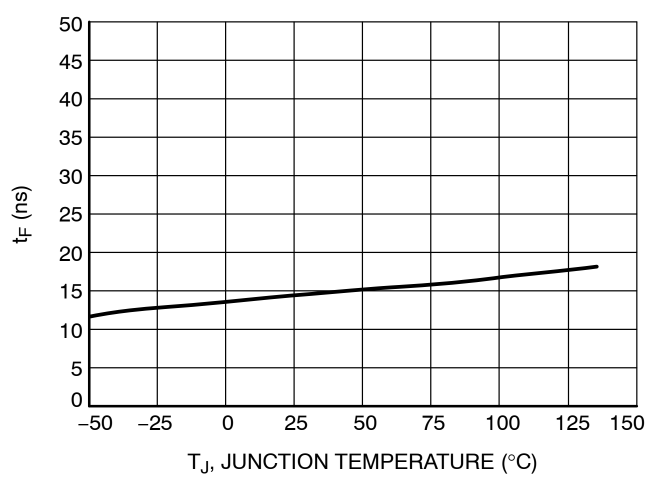


Figure 25. Gate Drive Fall Time (C_{DRV} = 470 pF) vs. Temperature

TYPICAL CHARACTERISTICS

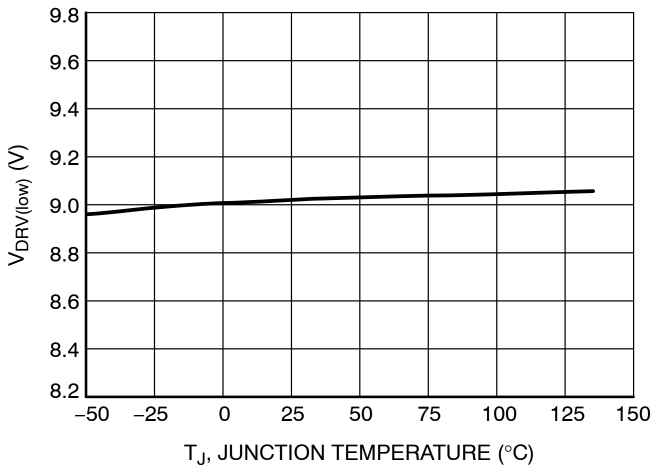


Figure 26. DRV Low Voltage vs. Temperature

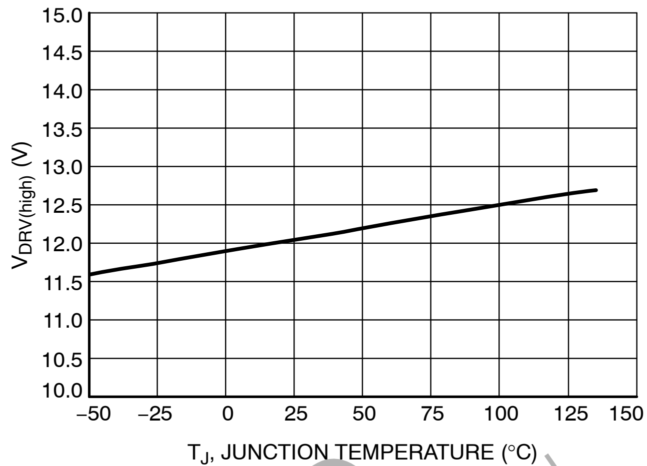


Figure 27. DRV High Voltage vs. Temperature

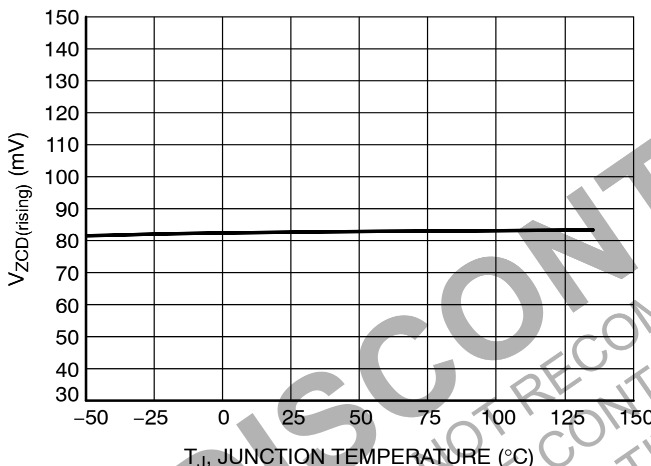


Figure 28. Upper ZCD Threshold Voltage vs. Temperature

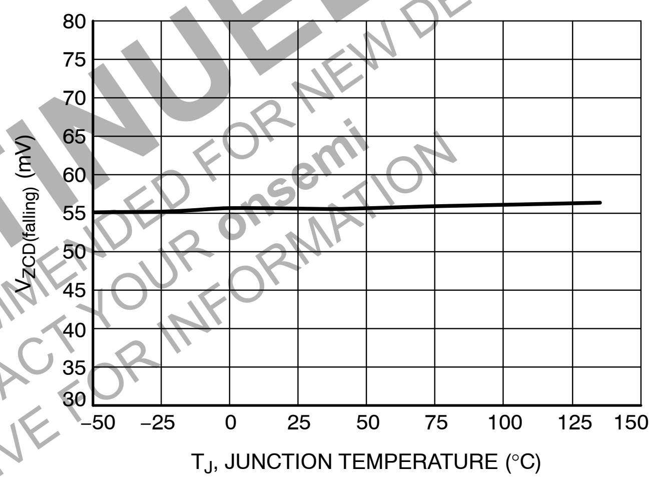


Figure 29. Lower ZCD Threshold vs. Temperature

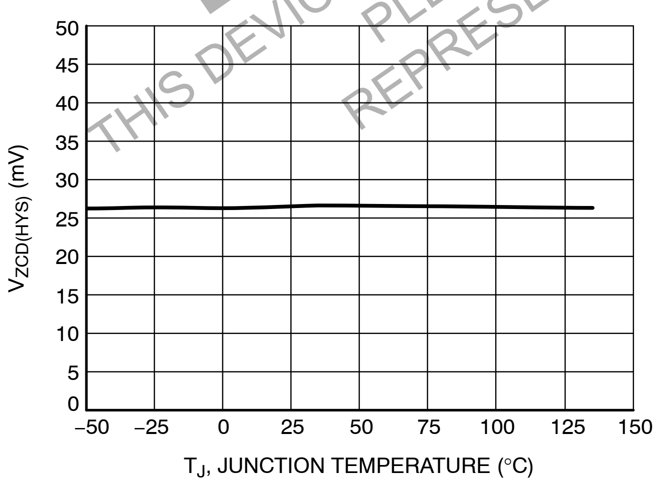


Figure 30. ZCD Hysteresis vs. Temperature

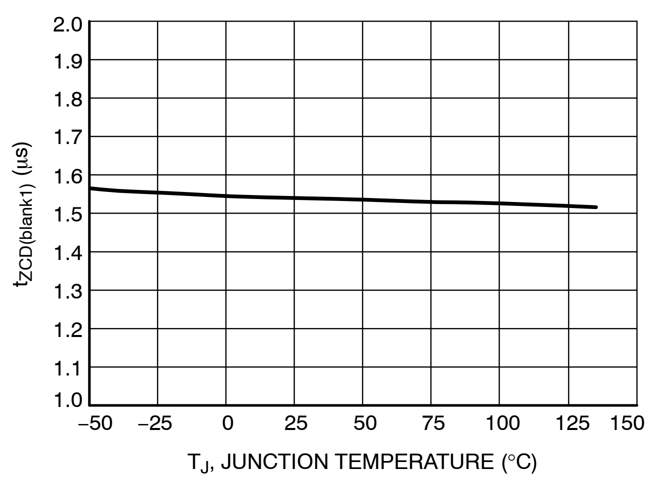


Figure 31. ZCD Blanking Delay vs. Temperature

TYPICAL CHARACTERISTICS

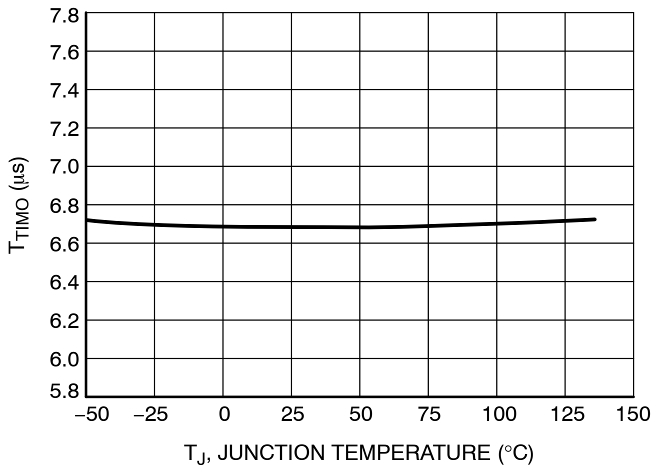


Figure 32. ZCD Time−out vs. Temperature

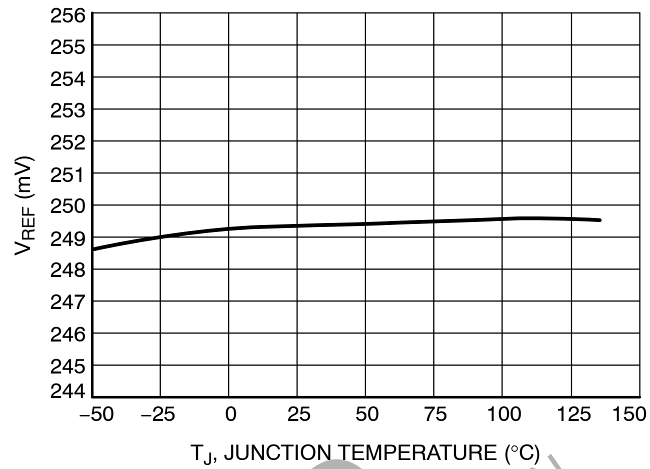


Figure 33. Reference Voltage vs. Temperature

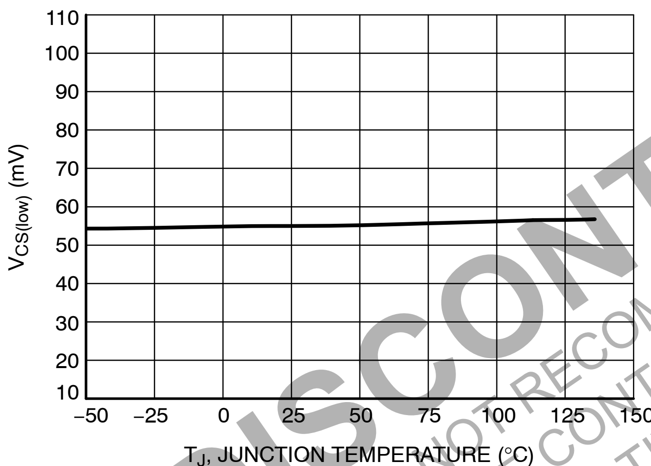


Figure 34. Current Sense Lower Threshold (V_{CS} Falling) vs. Temperature

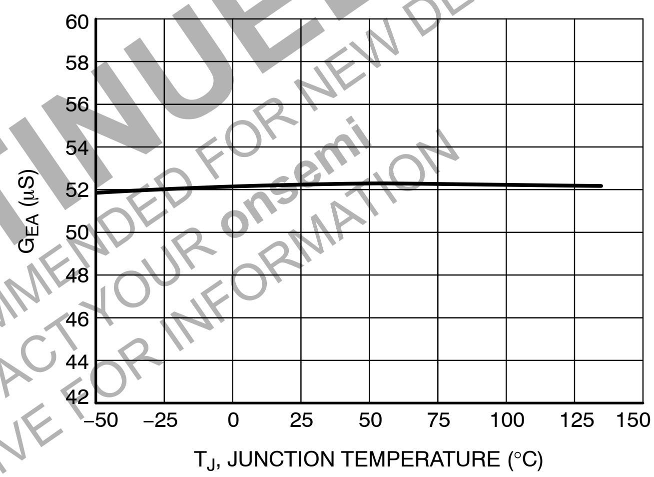


Figure 35. Error Amplifier Trans−conductance Gain vs. Temperature

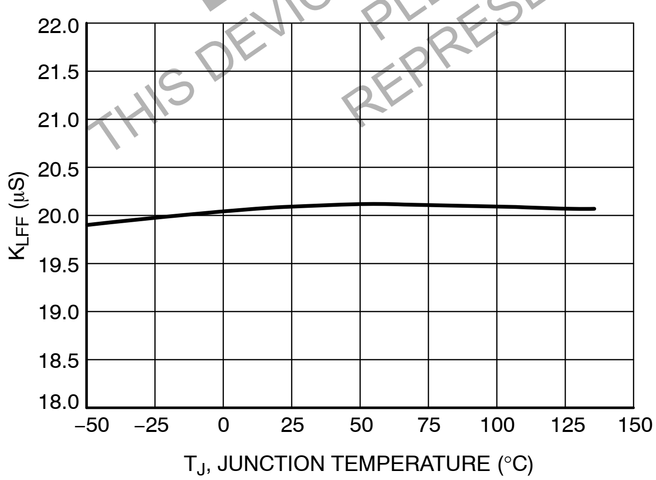


Figure 36. Feedforward V_{VS} to $I_{CS(offset)}$ Conversion Ratio vs. Temperature

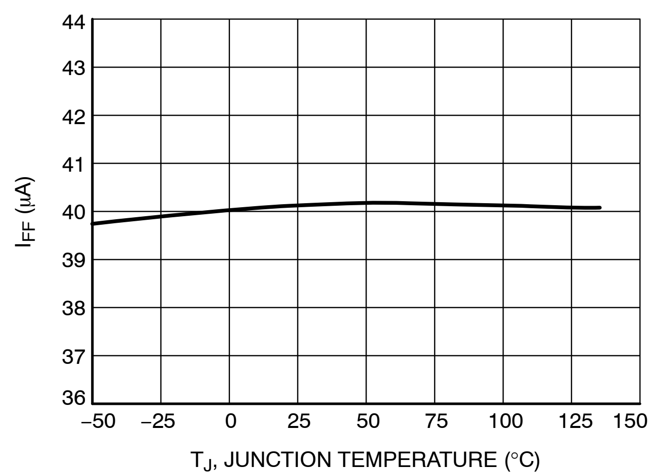


Figure 37. Line Feedforward Current on CS Pin (@ V_{VS} = 2 V) vs. Temperature

TYPICAL CHARACTERISTICS

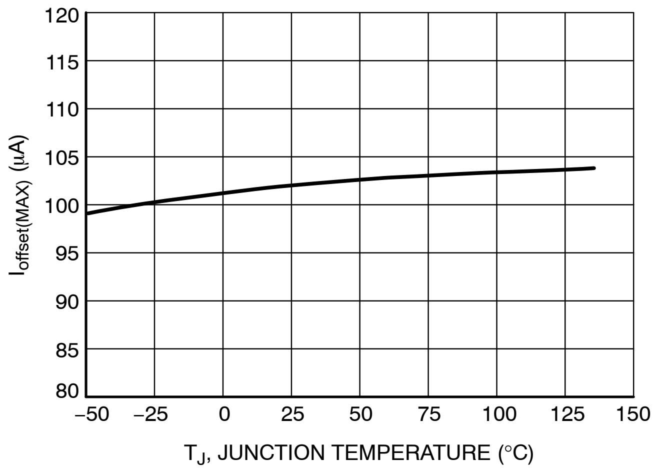


Figure 38. $I_{offset(MAX)}$ vs. Temperature

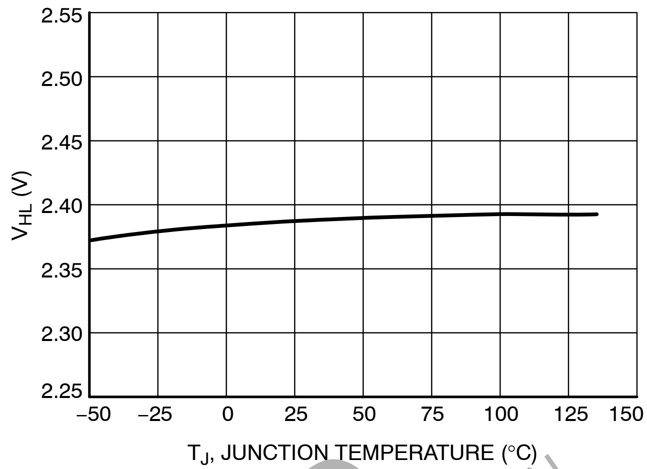


Figure 39. Threshold for High−line Range Detection vs. Temperature

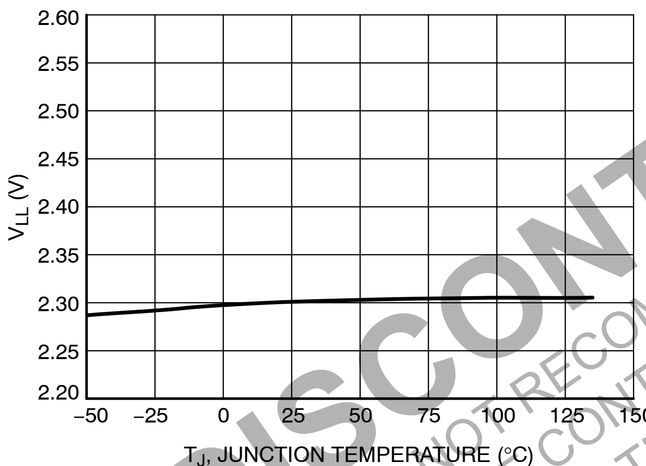


Figure 40. Threshold for Low−line Range Detection vs. Temperature

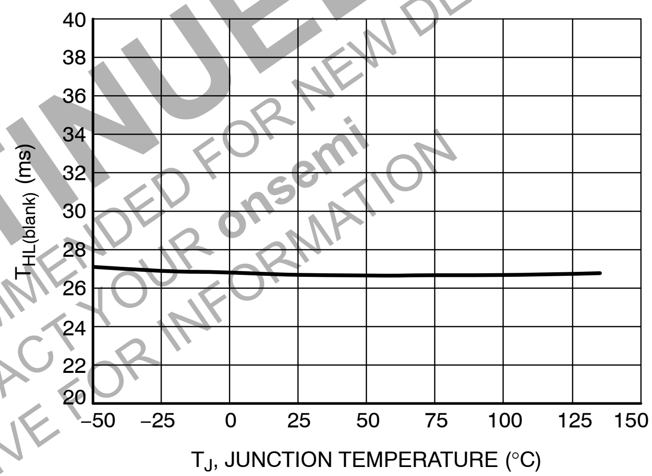


Figure 41. Blanking Time for Low−line Range Detection vs. Temperature

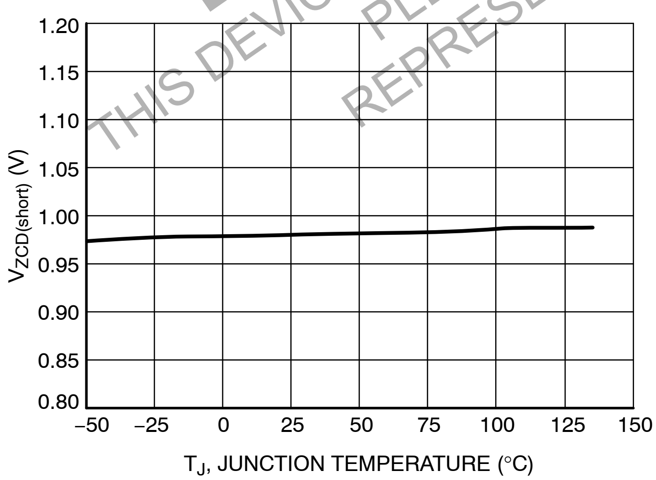


Figure 42. Threshold Voltage for Output Short Circuit Detection vs. Temperature

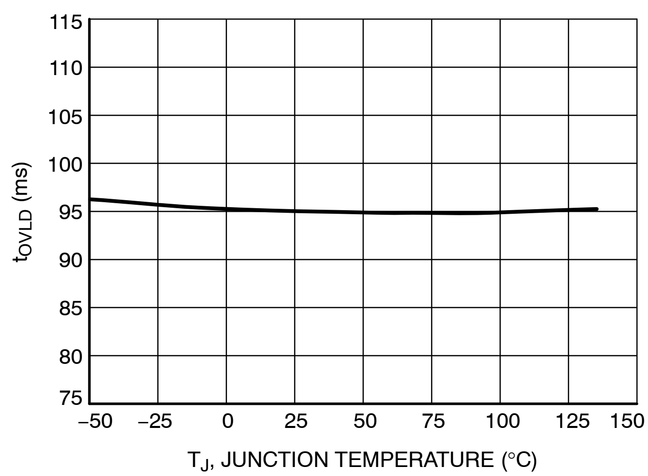


Figure 43. Short Circuit Detection Timer vs. Temperature

TYPICAL CHARACTERISTICS

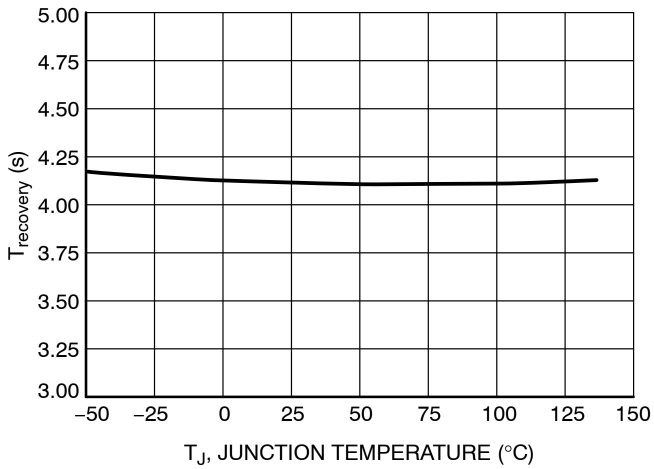


Figure 44. Auto−recovery Timer Duration vs. Temperature

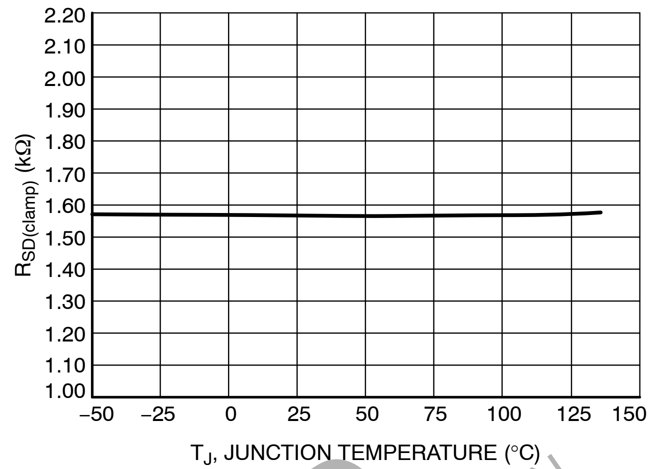


Figure 45. SD Pin Clamp Series Resistor vs. Temperature

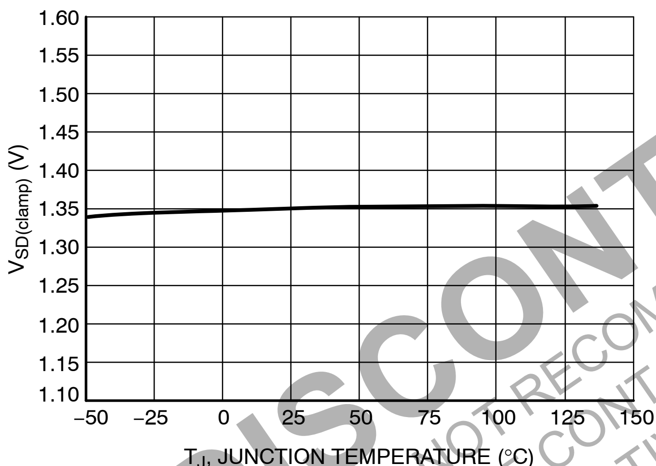


Figure 46. SD Pin Clamp Voltage vs. Temperature

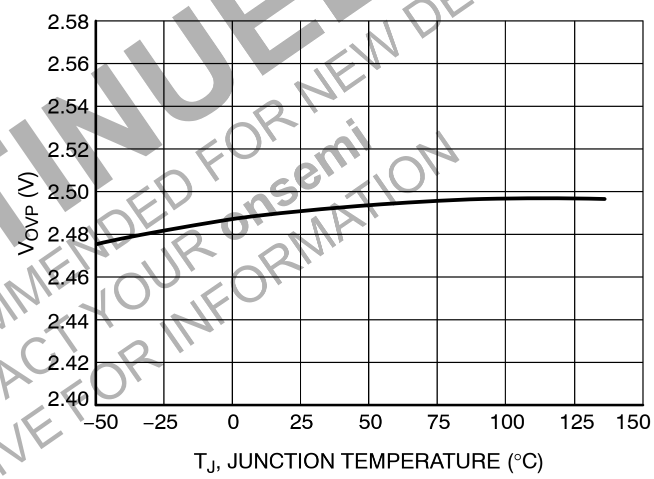


Figure 47. SD Pin OVP Threshold Voltage vs. Temperature

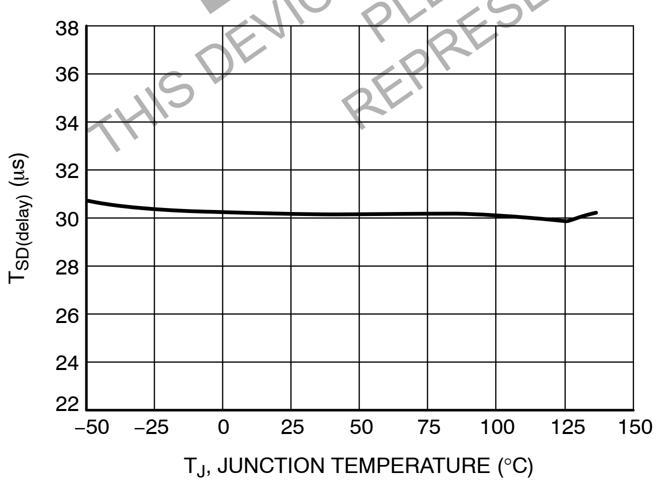


Figure 48. $T_{SD(delay)}$ vs. Temperature

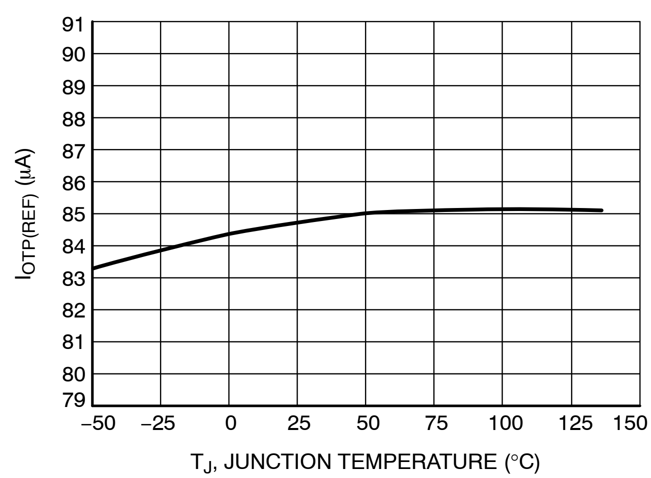


Figure 49. $I_{OTP(REF)}$ vs. Temperature

TYPICAL CHARACTERISTICS

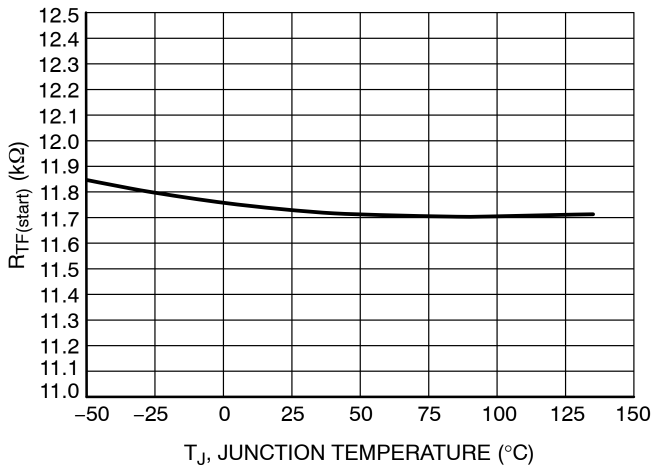


Figure 50. $R_{TF(start)}$ vs. Temperature

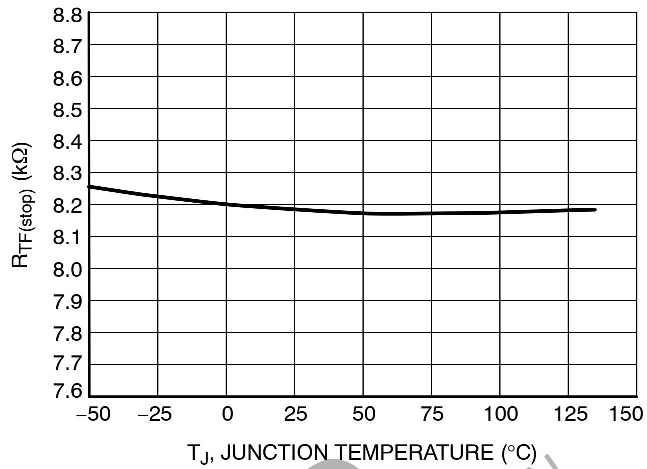


Figure 51. $R_{TF(stop)}$ vs. Temperature

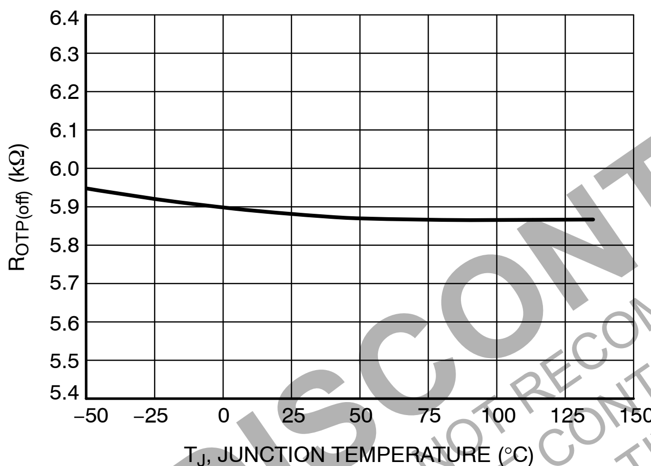


Figure 52. $R_{OTP(off)}$ vs. Temperature

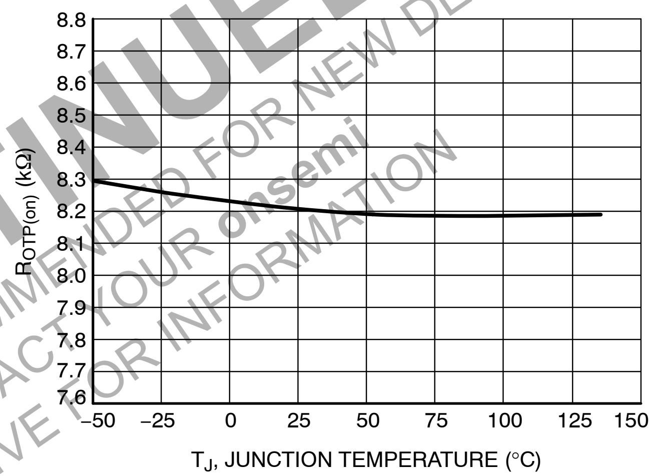


Figure 53. $R_{OTP(on)}$ vs. Temperature

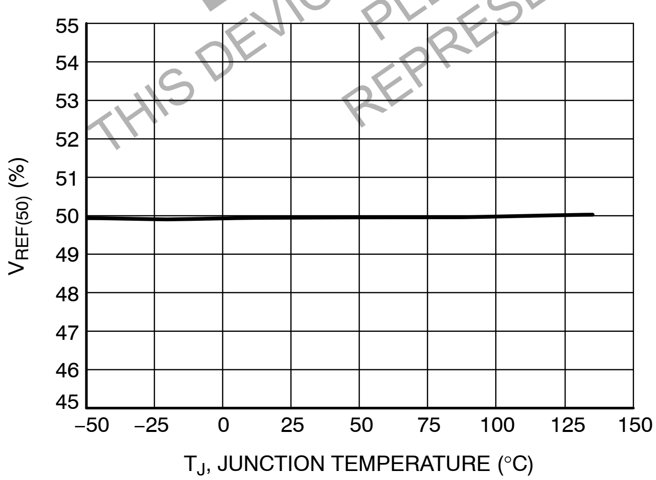


Figure 54. Ratio $V_{REF(50)}$ over V_{REF} vs. Temperature

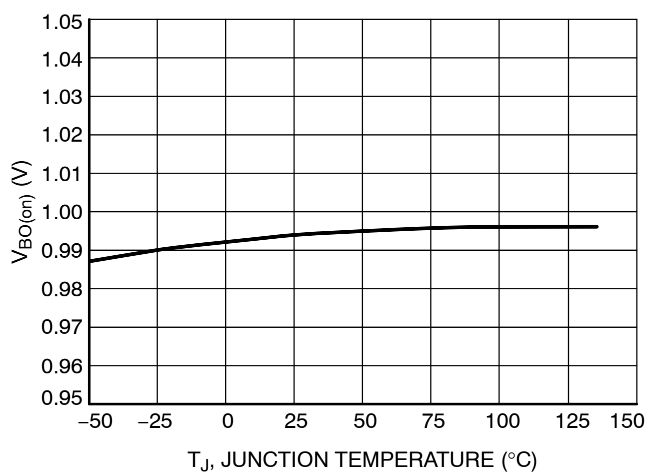


Figure 55. Brown−out ON Level vs. Temperature

TYPICAL CHARACTERISTICS

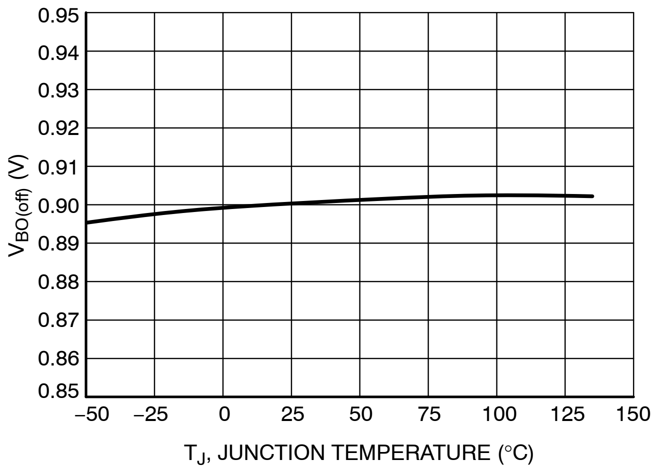


Figure 56. Brown−out OFF Level vs. Temperature

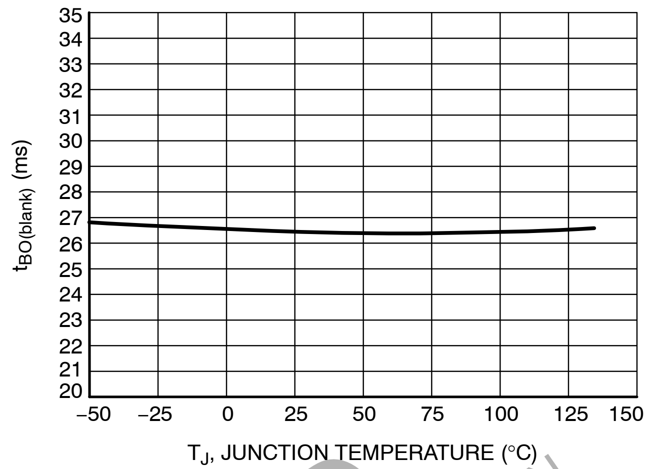


Figure 57. Brown−out Blanking Time vs. Temperature

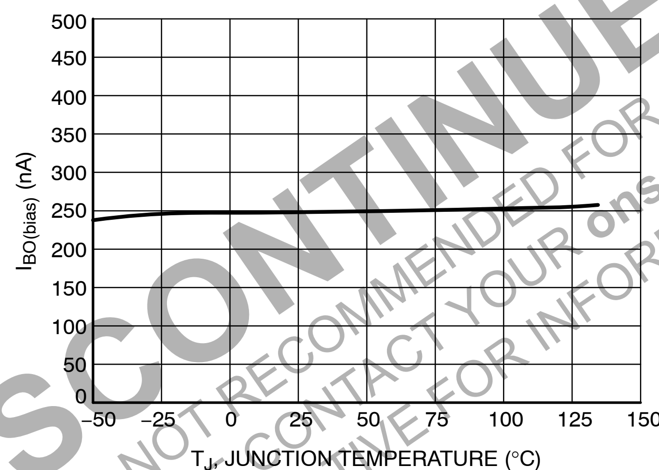


Figure 58. V_S Pin Pulling−down Current vs. Temperature

Application Information

The NCL30185 is a driver for power−factor corrected flyback and non−isolated buck−boost and SEPIC converters. It implements a current−mode, quasi−resonant architecture including valley lockout and frequency fold−back capabilities for maintaining high−efficiency performance over a wide load range. A proprietary circuitry ensures both accurate regulation of the output current (without the need for a secondary−side feedback) and near−unity power factor correction. The circuit contains a suite of powerful protections to ensure a robust LED driver design without the need for extra external components or overdesign.

- **Quasi−Resonance Current−Mode Operation:** implementing quasi−resonance operation in peak current−mode control, the NCL30185 optimizes the efficiency by turning on the MOSFET when its drain−source voltage is minimal (valley). In light−load conditions, the circuit changes valleys to reduce the switching losses. For stable operation, the valley at which the MOSFET switches on remains locked until the input voltage or the output current set−point significantly changes.
- **Primary−Side Constant−Current Control with Power Factor Correction:** a proprietary circuitry allows the LED driver to achieve both near−unity power factor correction and accurate regulation of the output current without requiring any secondary−side feedback (no optocoupler needed). A power factor as high as 0.99 and an output current deviation below ±2% are typically obtained.
- **Step dimming:** The step dimming function decreases the output current from 100% to 5% of its nominal value in 3 discrete steps. Whenever a brown−out is detected, the output current is decreased by reducing the reference voltage V_{REF}. The step−dimming function is reset if the V_S pin remains below the lower brown−out threshold ($V_{BO(off)}$) for more than 3 s typically.
- **Main protection features:**
  - **Over Temperature Thermal Fold−back / Shutdown/ Over Voltage Protection:** the NCL30185 features a gradual current foldback to protect the driver from excessive temperature down to 50% of the programmed current. This represents a power reduction of the LED by more than 50%. If the temperature continues to rise after this point to a second level, the controller stops operating. This mode would only be expected to be reached if there is a severe fault. The first and second temperature thresholds depend on the value of the NTC connected to the SD pin. Note, the SD pin can also be used to shutdown the device by pulling this pin below the $V_{OTP(off)}$ min level. A Zener diode can also be used to pull−up the pin and stop the controller for adjustable OVP protection. Both protections are latching−off (A version) or auto−recovery (the circuit can recover operation after 4−s delay has elapsed − B version).
  - **Cycle−by−cycle peak current limit:** when the current sense voltage exceeds the internal threshold V_{ILIM}, the MOSFET is immediately turned off for that switch cycle.
  - **Winding or Output Diode Short−Circuit Protection:** an additional comparator senses the CS signal and stops the controller if it exceeds 150% x V_{ILIM} for 4 consecutive cycles. This feature can protect the converter if a winding is shorted or if the output diode is shorted or simply if the transformer saturates. This protection is latching−off (A version) or auto−recovery (B version).
  - **Output Short−circuit protection:** if the ZCD pin voltage remains low for a 90−ms time interval, the controller detects that the output or the ZCD pin is grounded and hence, stops operation. This protection is latching−off (A version) or auto−recovery (B version).
  - **Open LED protection:** if the V_{CC} pin voltage exceeds the OVP threshold, the controller shuts down and waits 4 seconds before restarting switching operation.
  - **Floating or Short Pin Detection:** the circuit can detect most of these situations which helps pass safety tests.

Power Factor and Constant Current Control

The NCL30185 embeds an analog/digital block to control the power factor and regulate the output current by monitoring the ZCD, V_S and CS pin voltages (signals ZCD, V_{VS} and V_{CS} of Figure 59). This circuitry generates the current setpoint ($V_{CONTROL}/4$) and compares it to the current sense signal (V_{CS}) to dictate the MOSFET turning off event when V_{CS} exceeds $V_{CONTROL}/4$.

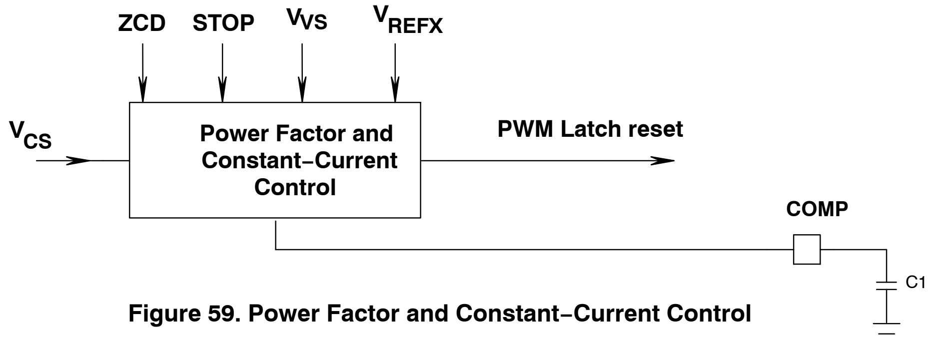


Figure 59. Power Factor and Constant−Current Control

As illustrated in Figure 59, the V_S pin provides the sinusoidal reference necessary for shaping the input current. The obtained current reference is further modulated so that when averaged over a half−line period, it is equal to the output current reference (V_{REFX}). This averaging process is made by an internal Operational Trans−conductance Amplifier (OTA) and the capacitor connected to the COMP pin (C1 of Figure 59). Typical COMP capacitance is 1 μF and should not be less than 470 nF to ensure stability. The COMP ripple does not affect the power factor performance as the circuit digitally eliminates it when generating the current setpoint.

If the V_S pin properly conveys the sinusoidal shape, power factor will be close to unity and the Total Harmonic Distortion (THD) will be low. In any case, the output current will be well regulated following the equation below:

$$I_{out} = \frac{V_{REFX}}{2N_{PS}R_{sense}} \quad \text{(eq. 1)}$$

Where:

- N_{PS} is the secondary to primary transformer turns $N_{PS} = N_S/N_P$
- R_{sense} is the current sense resistor (see Figure 1).
- V_{REFX} is the output current internal reference. $V_{REFX} = V_{REF}$ (250 mV typically) at full load.

The output current reference (V_{REFX}) is 250 mV typically (V_{REF}). In the event that step dimming is engaged, V_{REFX} takes a lower value based on the step−dimming level (see “step dimming” section) or if the temperature is high enough to activate the thermal fold−back (see “protections” section).

If a major fault is detected, the circuit enters the latched−off or auto−recovery mode and the COMP pin is grounded (except in an UVLO condition). This ensures a clean start−up when the circuit resumes operation.

Start−up Sequence

Generally an LED lamp is expected to emit light in < 1 sec and typically within 300 ms. The start−up phase consists of the time to charge the V_{CC} capacitor, initiate startup and begin switching and the time to charge the output capacitor until sufficient current flows into the LED string.

To speed−up this phase, the following defines the start−up sequence:

- The COMP pin is grounded when the circuit is off. The average COMP voltage needs to exceed the V_S pin peak value to have the LED current properly regulated (whatever the current target is). To speed−up the COMP capacitance charge and shorten the start−up phase, an internal 80−μA current source adds to the OTA sourced current (60 μA max typically) to charge up the COMP capacitance. The 80−μA current source remains on until the OTA starts to sink current as a result of the COMP pin voltage sufficient rise. At that moment, the COMP pin being near its steady−state value, it is only driven by the OTA.
- Whatever the step−dimming state is, the output current reference is set maximum ($V_{REFX} = V_{REF}$) until the ZCD pin voltage reaches the 1−V $V_{ZCD(short)}$ threshold. This prevents the circuit from detecting an output short (AUX_SCP protection trips if the ZCD pin voltage does not exceed 1−V $V_{ZCD(short)}$ threshold within a 90−ms delay) just because dimming would make the output voltage charge up slowly. If the system cannot start−up in one V_{CC} cycle, the AUX_SCP 90−ms blanking time is not reset and V_{REFX} remains maximum for all the necessary V_{CC} cycles until the ZCD pin voltage reaches the 1−V $V_{ZCD(short)}$ threshold.
- If V_{CC} drops below the $V_{CC(off)}$ threshold because the circuit fails to start−up properly on the first attempt, a new try takes place as soon as V_{CC} is recharged to $V_{CC(on)}$. The COMP voltage is not reset at that moment. Instead, the new attempt starts with the COMP level obtained at the end of the previous operating phase.
- If the load is shorted, the circuit will operate in hiccup mode with V_{CC} oscillating between $V_{CC(off)}$ and $V_{CC(on)}$ until the AUX_SCP protection trips (AUX_SCP is triggered if the ZCD pin voltage does not exceed 1 V within a 90−ms operation period of time thus indicating a short to ground of the ZCD pin or an excessive load preventing the output voltage from rising). The NCL30185A latches off in this case. With the B version, the AUX_SCP protection forces the 4−s auto−recovery delay to reduce the operation duty−ratio. Figure 60 illustrates a start−up sequence with the output shorted to ground, in this second case.

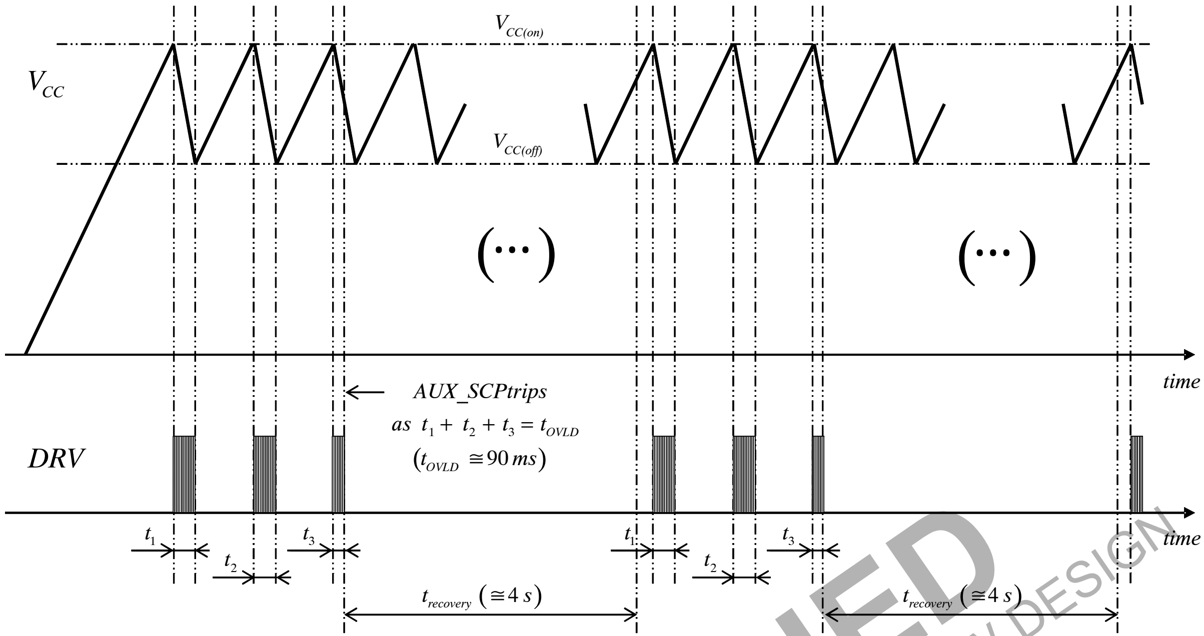


Figure 60. Start−up Sequence in a Load Short−circuit Situation (auto−recovery version)

Step Dimming

The step dimming function decreases the output current from 100% to 5% of its nominal value in 3 discrete steps. The table below shows the different steps value and the corresponding reference voltage value. Each time a brown−out is detected, the output current is decreased by decreasing the reference voltage V_{REF}.

A counter is incremented by the BO_NOK (brown−out not OK) signal and selects one of the four corresponding reference thresholds: V_{REF}, V_{REF70}, V_{REF25}, V_{REF5}. After counting up to 4, the counter is reset.

Table 4. DIMMING STEPS

Dimming Step	Iout
ON	100%
1	70%
2	25%
3	5%

Note:

The step dimming state is memorized until V_{CC} crosses $V_{CC(reset)}$ or V_{VS} is below $V_{BO(off)}$ for 3 s (typical).

The circuit consumption is optimized (in particular, it equals $I_{CC(fault)}$ when V_{CC} is lower than $V_{CC(off)}$) so that the V_{CC} voltage does not drop too fast for the step dimming brown−out event.

The power supply designer should use a split V_{CC} circuit as shown in Figure 61 where a small capacitor C_1 is used for a fast start−up while a larger C_2 capacitance provides the necessary storage capability for step dimming. During step dimming, at startup, the controller generates the first DRV pulses after 1 time−out pulse even if a higher valley number is selected by V_{REFX}. This avoids long startup time while dimming at low output current value.

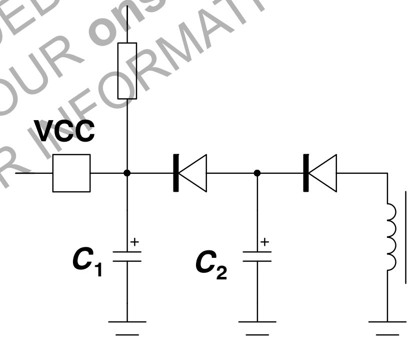


Figure 61. Split V_{CC} Supply

The step−dimming function is reset if the V_S pin is maintained below the $V_{BO(off)}$ brown−out threshold for the T_{step_reset} time. T_{step_reset} is 3 s typically. In other words, any brown−out event that is longer than T_{step_reset}, leads the controller to re−start at 100% current setting.

Zero Crossing Detection Block

The ZCD pin detects when the drain−source voltage of the power MOSFET reaches a valley by crossing below the 55−mV internal threshold. At startup or in case of extremely damped free oscillations, the ZCD comparator may not be able to detect the valleys. To avoid such a situation, the NCL30185 features a time−out circuit that generates pulses if the voltage on ZCD pin stays below the 55−mV threshold for 6.5 μs. The time−out also acts as a substitute clock for the valley detection and simulates a missing valley in case the free oscillations are too damped.

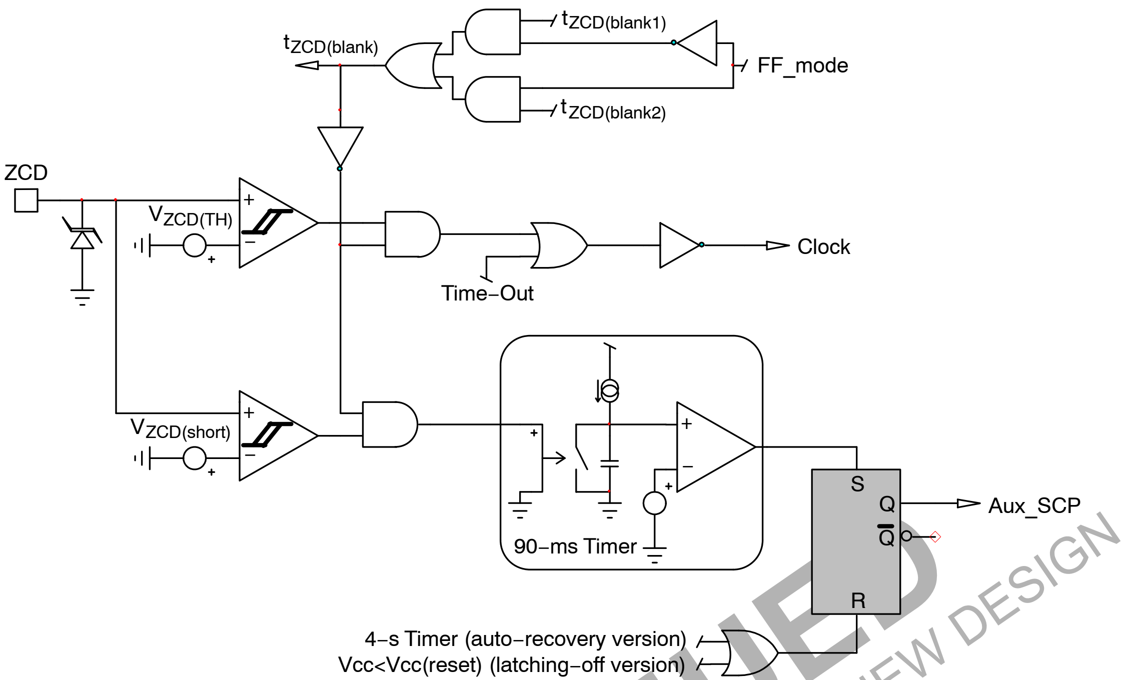


Figure 62. Zero Current Detection Block

If the ZCD pin or the auxiliary winding happen to be shorted, the time−out function would normally make the controller keep switching and hence lead to improper LED current value. The “AUX_SCP” protection prevents such a stressful operation: a secondary timer starts counting that is only reset when the ZCD voltage exceeds the $V_{ZCD(short)}$ threshold (1 V typically). If this timer reaches 90 ms (no ZCD voltage pulse having exceeded $V_{ZCD(short)}$ for this time period), the controller detects a fault and stops operation for 4 seconds (B version) or latches off (A version).

The “clock” shown in Figure 62 is used by the “valley selection frequency foldback” circuitry of the block diagram (Figure 3), to generate the next DRV pulse (if no fault prevents it):

- Immediately when the clock occurs in QR mode (heavy load)
- After the appropriate number of “clock” pulses in thermal foldback or step−dimming mode (see Table 5)

For an optimal operation, the maximum ZCD level should be maintained below 5 V to stay safely below the built in clamping voltage of the pin.

Line Range Detection and Valley Lockout

As sketched in Figure 63, this circuit detects the low−line range if the V_S pin remains below the V_{LL} threshold (2.3 V typical) for more than the 25−ms blanking time. High−line is detected as soon as the V_S pin voltage exceeds V_{HL} (2.4 V typical). These levels roughly correspond to 184−V rms and 192−V rms line voltages if the external resistors divider applied to the V_S pin is designed to provide a 1−V peak value at 80 V rms.

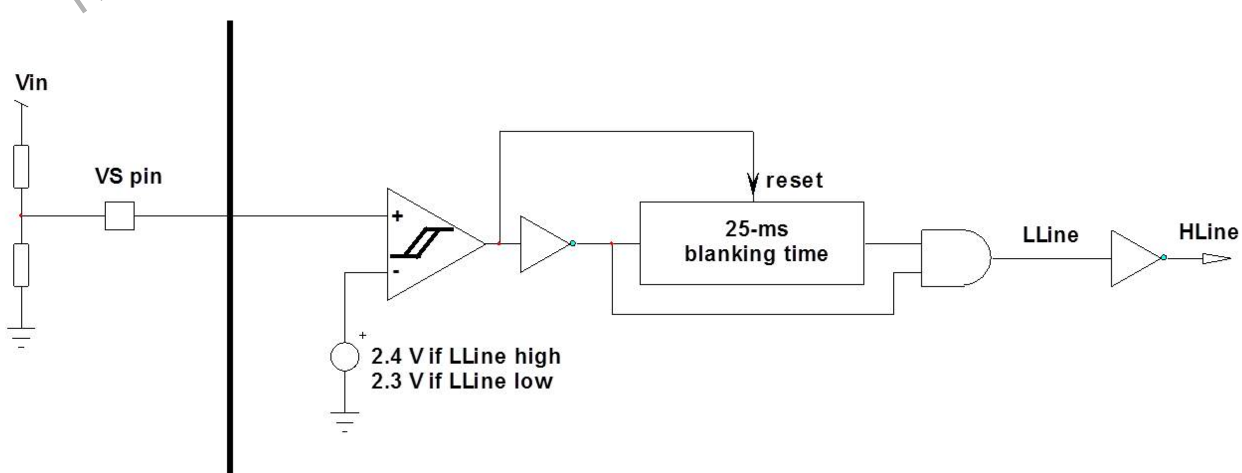


Figure 63. Line Range Detection

Quasi−square wave resonant systems have a wide switching frequency excursion. The switching frequency increases when the output load decreases or when the input voltage increases. The switching frequency of such systems must be limited.

Table 5. VALLEY SELECTION

Load	Low Line	High Line
100%	Valley 1 (QR)	Valley 2
70%	Valley 2	Valley 3
25%	Valley 5	Valley 6
5%	Frequency foldback	Frequency foldback

A decimal counter counts the valley detected by the ZCD logic block. In the low−line range, conduction losses are generally dominant. Hence, only a short dead−time is necessary to reach the MOSFET valley. In high−line conditions, switching losses generally are the most critical. It is thus efficient to skip a valley to lower the switching frequency. Hence, when the current is not dimmed, the NCL30185 optimizes the efficiency over the line range by turning on the MOSFET at the first valley in low−line conditions and at the second valley in the high−line case. This is illustrated in Figure 64 that sketches the MOSFET Drain−source voltage in both cases. In dimming cases, more valleys can be skipped. Table 5 summarizes the valley selection as a function of the output current.

Figure 64. Full−load Operation − Quasi−resonant Mode in low line (left), turn on at valley 2 when in high line (right)

Frequency Foldback (FF)

The valley lockout function can make the circuit skip operation until the 5th valley (6th valley) is detected in low−line case (high−line case) as obtained at 25% of the nominal load. At the lowest step (5% of the nominal load), the switching frequency is decreased by further adding dead−time after the 5th valley (low line) or the 6th valley (high line) is detected. This extra dead−time is typically 40 μs.

Line Feedforward

As illustrated by Figure 65, the input voltage is sensed by the V_S pin and converted into a current. By adding an external resistor in series between the sense resistor and the CS pin, a voltage offset proportional to the input voltage is added to the CS signal for the MOSFET on−time to compensate for the I_{peak} increase due to the propagation delay.

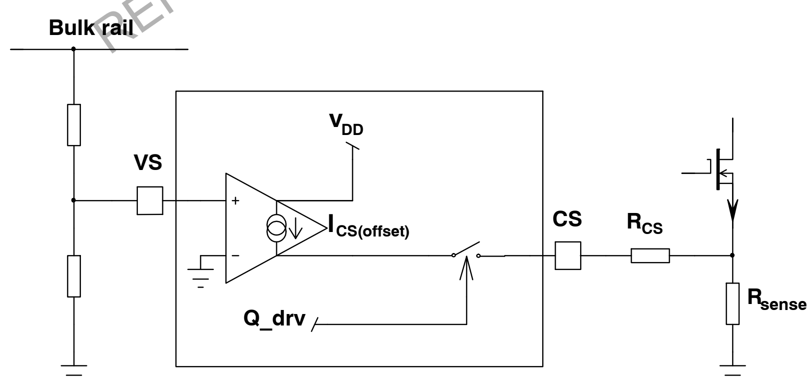


Figure 65. Line Feed−Forward Schematic

In Figure 65, Q_drv designates the output of the PWM latch which is high for the on−time and low otherwise.

Protections

The circuit incorporates a large variety of protections to make the LED driver very rugged. Among them, we can list:

Output Short Circuit Situation

An overload fault is detected if the ZCD pin voltage remains below $V_{ZCD(short)}$ for 90 ms. In such a situation, the circuit stops generating pulses until the 4−s delay auto−recovery time has elapsed (B version) or latches off (A version).

Winding or Output Diode Short Circuit Protection

If a transformer winding happens to be shorted, the primary inductance will collapse leading the current to ramp up in a very abrupt manner. The V_{ILIM} comparator (current limitation threshold) will trip to open the MOSFET and eventually stop the current rise. However, because of the abnormally steep slope of the current, internal propagation delays and the MOSFET turn−off time will make possible the current rise up to 50% or more of the nominal maximum value set by V_{ILIM}. As illustrated in Figure 66, the circuit uses this current overshoot to detect a winding short circuit. The leading edge blanking (LEB) time for short circuit protection (LEB2) is significantly faster than the LEB time for cycle−by−cycle protection (LEB1). Practically, if four consecutive switching periods lead the CS pin voltage to exceed ($V_{CS(stop)}$=150% $*V_{ILIM}$), the controller enters auto−recovery mode in version B (4−s operation interruption between active bursts) and latches off in version A. Similarly, this function can also protect the power supply if the output diode is shorted or if the transformer simply saturates.

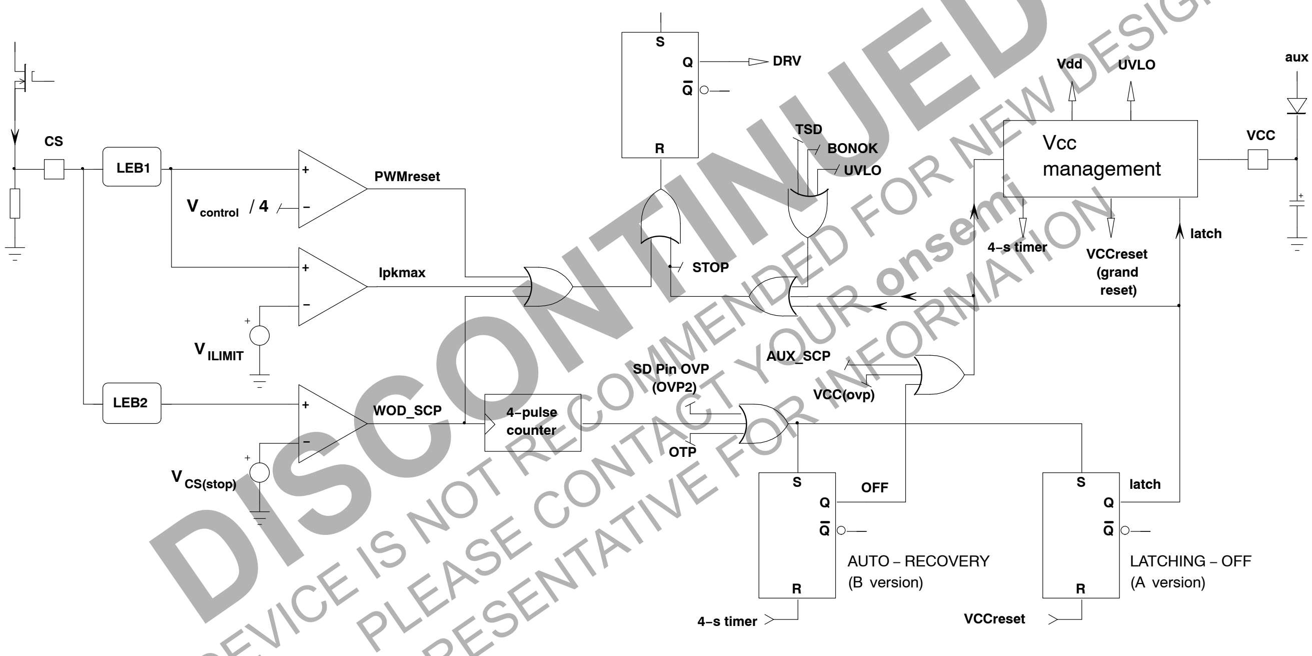


Figure 66. Winding Short Circuit Protection, Max. Peak Current Limit Circuits

V_{CC} Over Voltage Protection

The circuit stops generating pulses if V_{CC} exceeds $V_{CC(OVP)}$ and enters auto−recovery mode. This feature protects the circuit if the output LED string happens to open or is disconnected.

Programmable Over Voltage Protection (OVP2)

Connect a Zener diode between V_{CC} and the SD pin to set a programmable V_{CC} OVP (D_Z of Figure 67). The triggering level is (V_Z+V_{OVP}) where V_{OVP} is the 2.5−V internal threshold. If this protection trips, the NCL30185A latches off while the NCL30185B enters the auto−recovery mode.

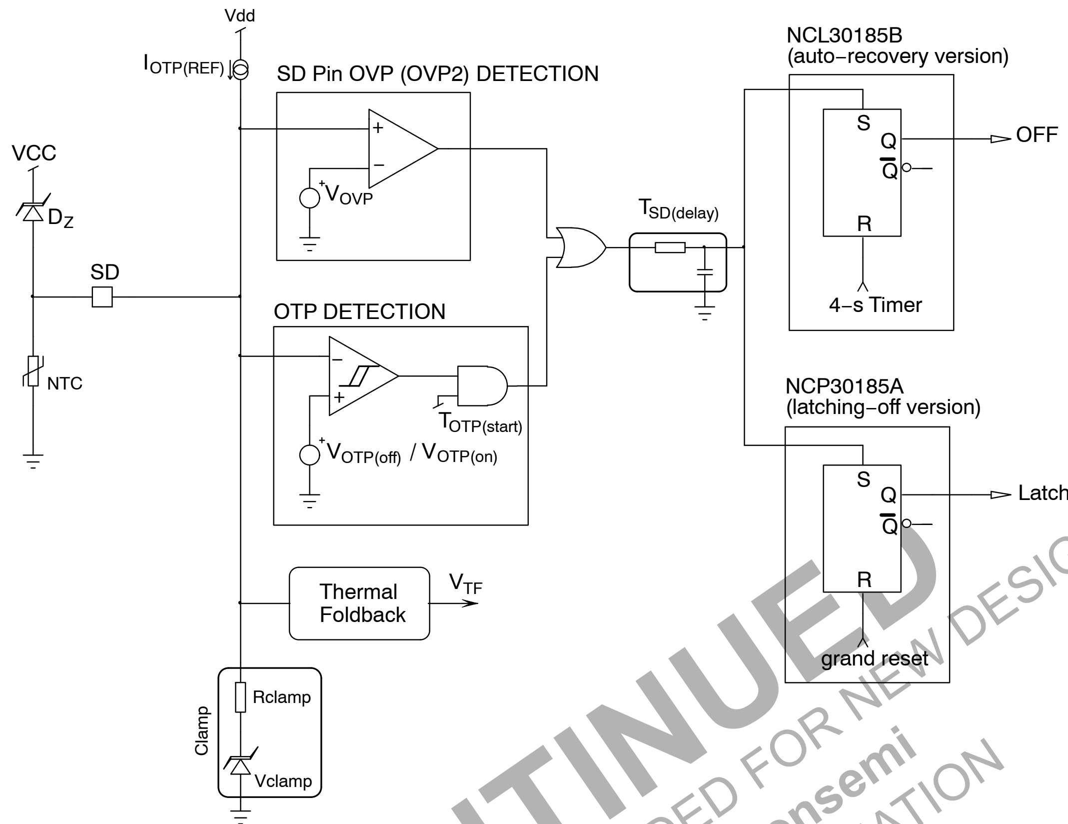


Figure 67. Thermal Foldback and OVP/OTP Circuitry

The SD pin is clamped to about 1.35 V (V_{clamp}) through a 1.6−kΩ resistor (R_{clamp}). It is then necessary to inject about

$$\left(\frac{V_{OVP} - V_{clamp}}{R_{clamp}}\right)$$

that is

$$\left(\frac{2.50 - 1.35}{1.6\ k} \cong 700\ \mu A\right)$$

typically, to trigger the OVP protection. This current helps ensure an accurate detection by using the Zener diode far from its knee region.

Programmable Over Temperature Foldback Protection (OTP)

Connect an NTC between the SD pin and ground to detect an over−temperature condition. In response to a high temperature (detected if V_{SD} drops below $V_{TF(start)}$), the circuit gradually reduces the LED current down 50% of its initial value when V_{SD} reaches $V_{TF(stop)}$, in accordance with the characteristic of Figure 68 (Note 9).

If this thermal foldback cannot prevent the temperature from rising (testified by V_{SD} drop below V_{OTP}), the circuit latches off (A version) or enters auto−recovery mode (B version) and cannot resume operation until V_{SD} exceeds $V_{OTP(on)}$ to provide some temperature hysteresis (around 10°C typically). The OTP thresholds nearly correspond to the following resistances of the NTC:

- Thermal foldback starts when $R_{NTC} \le R_{TF(start)}$ (11.7 kΩ, typically)
- Thermal foldback stops when $R_{NTC} \le R_{TF(stop)}$ (8.0 kΩ, typically)
- OTP triggers when $R_{NTC} \le R_{OTP(off)}$ (5.9 kΩ, typically)
- OTP is removed when $R_{NTC} \ge R_{OTP(on)}$ (8.0 kΩ, typically) (Note 10)

9. The above mentioned initial value is the output current before the system enters the thermal foldback, that is, its maximum level if step−dimming is not engaged or a lower one based on the step−dimming value.
10. This condition is sufficient for operation recovery of the B version. For the A version which latches off when OTP triggers, the circuit further needs to be reset by a V_{CC} drop below $V_{CC(reset)}$.

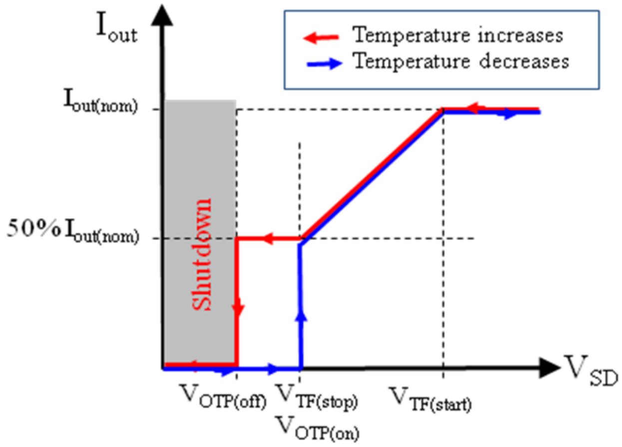


Figure 68. Output Current Reduction versus SD Pin Voltage

At startup, when V_{CC} reaches $V_{CC(on)}$, the OTP comparator is blanked for at least 180 μs in order to allow the SD pin voltage to reach its nominal value if a filtering capacitor is connected to the SD pin. This avoids flickering of the LED light during turn on.

Brown−Out Protection

The NCL30185 prevents operation when the line voltage is too low for proper operation. As illustrated in Figure 69, the circuit detects a brown−out situation if the V_S pin remains below the $V_{BO(off)}$ threshold (0.9 V typical) for more than the 25−ms blanking time. In this case, the controller stops operating. Operation resumes as soon as the V_S pin voltage exceeds $V_{BO(on)}$ (1.0 V typical) and V_{CC} is higher than $V_{CC(on)}$. To ease recovery, the circuit overrides the V_{CC} normal sequence (no need for V_{CC} cycling down below $V_{CC(off)}$). Instead, its consumption immediately reduces to $I_{CC(start)}$ so that V_{CC} rapidly charges up to $V_{CC(on)}$. Once done, the circuit re−starts operating.

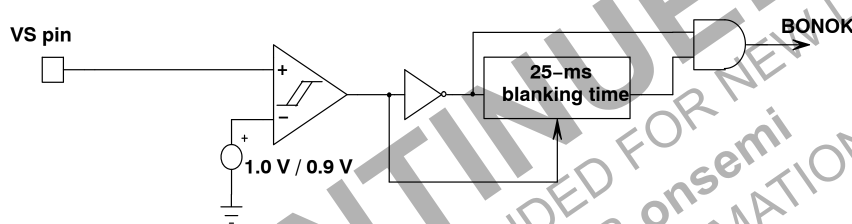


Figure 69. Brown−out Circuit

Die Over Temperature (TSD)

The circuit stops operating if the junction temperature (T_J) exceeds 150°C typically. The controller remains off until T_J goes below nearly 100°C.

Pin Connection Faults

The circuit addresses most pin connection fault cases:

- **CS pin short to ground**
  The circuit senses the CS pin impedance every time it starts−up and after DRV pulses terminated by the 36−μs maximum on−time. If the measured impedance does not exceed 120 ohm typically, the circuit stops operating. In practice, it is recommended to place a minimum of 250−ohm in series between the CS pin and the current sense resistor to take into account possible parametric deviations.
- **Fault of the GND connection**
  If the GND pin is properly connected, the supply current drawn from the positive terminal of the V_{CC} capacitor, flows out of the GND pin to return to the negative terminal of the V_{CC} capacitor. If the GND pin is not connected, the circuit ESD diodes offer another return path. The accidental non−connection of the GND pin is monitored by detecting that one of the ESD diode is conducting. Practically, the ESD diode of CS pin is monitored. If such a fault is detected for 200 μs, the circuit stops generating DRV pulses.

More generally, incorrect pin connection situations (open, grounded, shorted to adjacent pin) are covered by AND9204/D.

Fault Modes

The circuit turns off whenever a major faulty condition prevents it from operating:

- Severe OTP (V_{SD} level below $V_{OTP(off)}$)
- V_{CC} OVP
- OVP2 (additional OVP provided by SD pin)
- Output diode short circuit protection: "WOD_SCP high"
- Output / Auxiliary winding Short circuit protection: "Aux_SCP high"
- Die over temperature (TSD)

In this mode, the DRV pulses generation is interrupted.

In the case of a latching−off fault, the circuit stops pulsing until the LED driver is unplugged and V_{CC} drops below $V_{CC(reset)}$. At that moment, the fault is cleared and the circuit could resume operation.

In the auto−recovery case, the circuit cannot generate DRV pulses for the auto−recovery 4−s delay. When this time has elapsed, the circuit recovers operation as soon as the V_{CC} voltage has exceeded $V_{CC(on)}$.

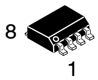
In the B version, all these protections are auto−recovery. The SD pin OTP and OVP, WOD_SCP and AUX_SCP are latching off in the A version (see Table 6).

Table 6. PROTECTION MODES

	AUX_SCP	WOD_SCP	SD Pin OTP	SD Pin OVP
NCL30185A*	Latching off	Latching off	Latching off	Latching off
NCL30185B	Auto−recovery	Auto−recovery	Auto−recovery	Auto−recovery

ORDERING INFORMATION

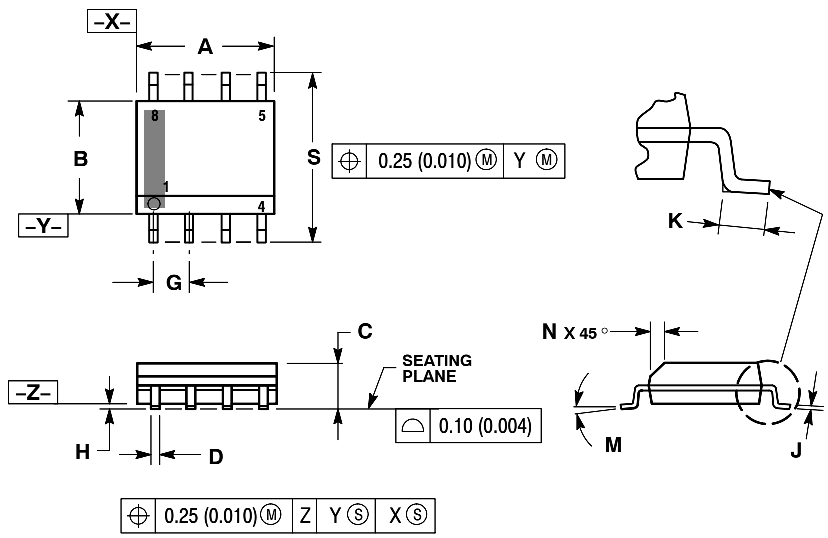
Device	Package Type	Shipping
NCL30185ADR2G	SOIC−8 (Pb−Free/Halide Free)	2500/Tape & Reel
NCL30185BDR2G	SOIC−8 (Pb−Free/Halide Free)	2500/Tape & Reel



SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

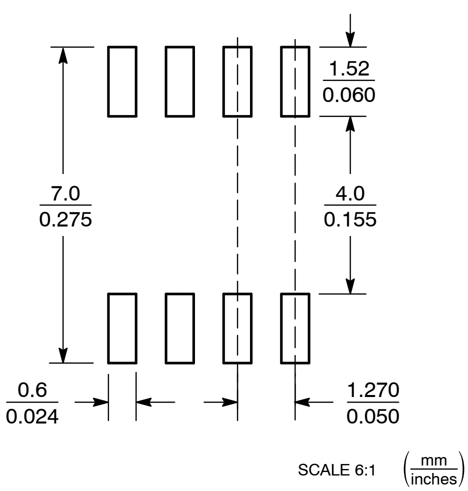
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

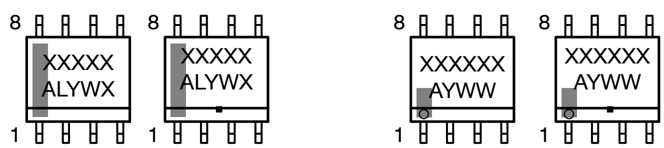
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC | IC (Pb−Free) | Discrete | Discrete (Pb−Free)

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42564B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	SOIC−8 NB	PAGE 1 OF 2

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales

◊