A6214 and A6216

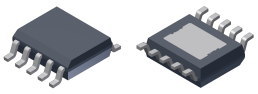
Automotive-Grade, Constant-Current 2 A PWM Dimmable Buck Regulator LED Driver

FEATURES AND BENEFITS

- AEC-Q100 qualified
- Supply voltage 4.5 to 55 V
- 2 A maximum output over operating temperature range
- Integrated MOSFET switch
- Able to use either Schottky or silicon low-side diode
- True average output current control
- Internal control loop compensation
- Integrated 5 V, 10 mA regulator for driving external load
- PWM dimming via direct logic input down to 0.1% at 200 Hz
- Standalone internal PWM dimming (A6216)
- Analog dimming for brightness calibration and thermal foldback
- Low-power shutdown (1 µA typical)
- Fault flag output (A6216)
- LED string open and short protection
- Cycle-by-cycle current limit
- Undervoltage lockout (UVLO) and thermal shutdown (TSD)
- Robust protection against:
  - □ Adjacent pin-to-pin short
  - □ Pin-to-GND short
  - □ Component open/short faults

PACKAGES:

A6214: 10-Pin SOICN (suffix LK)



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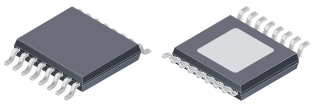
A6216: 16-Pin eTSSOP (suffix LP)



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DESCRIPTION

The A6214 is a single-IC switching regulator that provides constant-current output to drive high-power LEDs. It integrates a high-side N-channel DMOS switch for DC-to-DC step- down (buck) conversion. A true average current is output using a cycle-by-cycle, controlled on-time method.

Output current is user-selectable by an external current sense resistor. Output voltage is automatically adjusted to drive various numbers of LEDs in a single string. This ensures the optimal system efficiency.

LED dimming is accomplished by a direct logic input pulse-width-modulation (PWM) signal at the Enable pin. Alternatively, an Analog Dimming input can be used to calibrate the LED current, or implement thermal foldback in conjunction with external NTC thermistor.

The A6216 has the added capability to generate its own PWM dimming frequency and duty cycle in stand-alone mode.

The A6214 is provided in a compact 10-pin narrow SOIC package (suffix LK). The A6216 is in 16-pin TSSOP (suffix LP), both with exposed pad for enhanced thermal dissipation. It is lead (Pb) free, with 100% matte-tin leadframe plating.

APPLICATIONS:

Automotive lighting
- Daytime running lights
- Front and rear fog lights
- Turn/stop lights
- Map light
- Dimmable interior lights

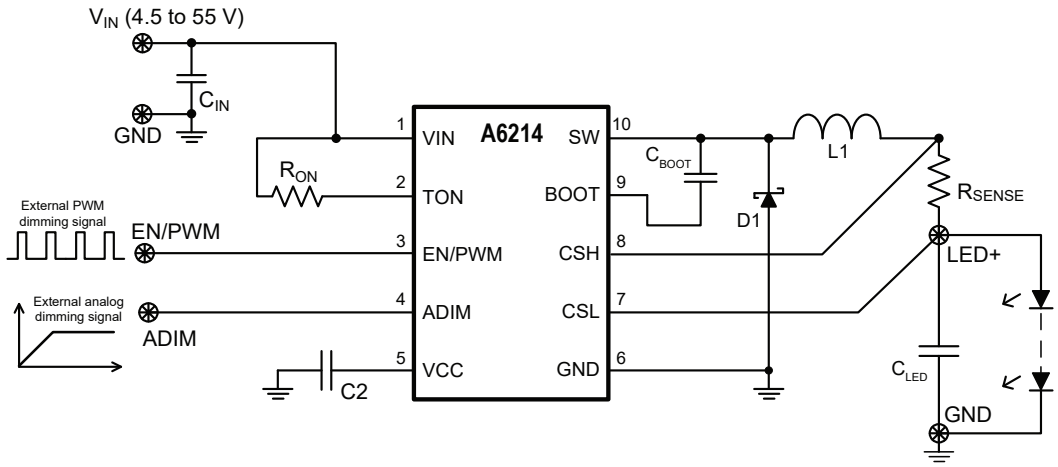

Figure 1: A6214 (LK Package) Typical Application Circuit

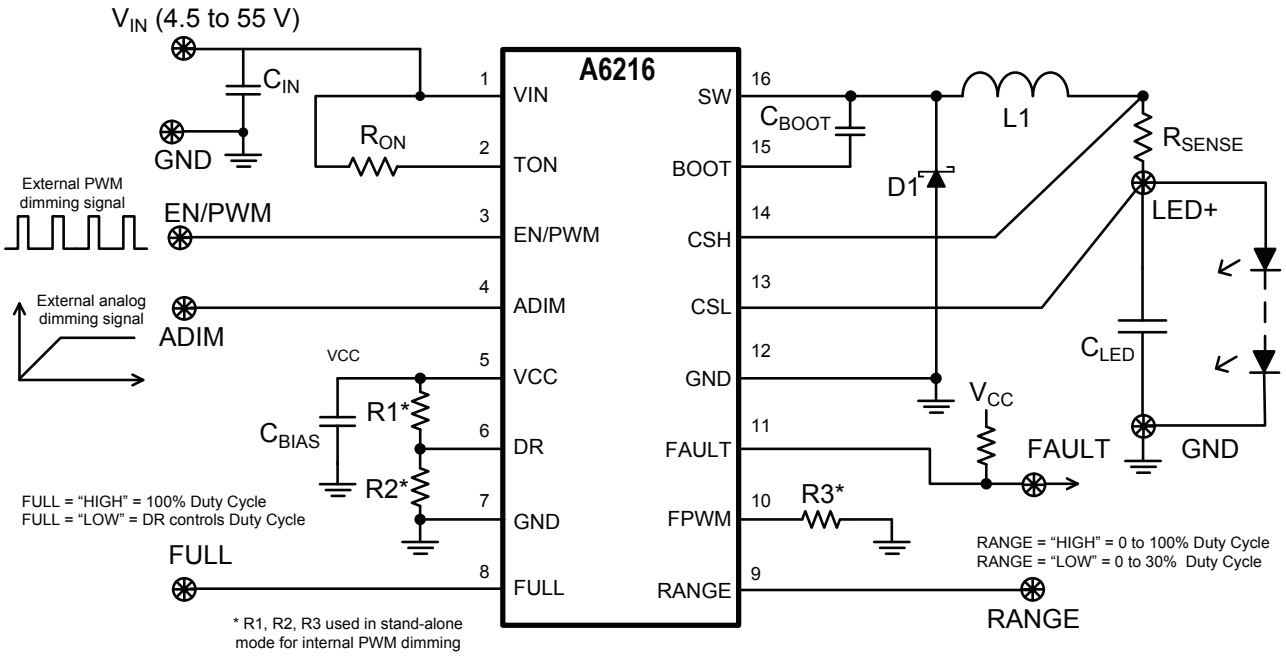

Figure 2: A6216 (LP Package) Typical Application Circuit

SELECTION GUIDE

Part Number	Internal PWM and FAULT Flag	Package	Packing
A6214KLKTR-T	No	10-pin SOICN with exposed thermal pad	3000 pieces per 13-in reel
A6216KLPTR-T	Yes	16-pin TSSOP with exposed thermal pad	4000 pieces per 13-in reel

Table of Contents

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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	V_{IN}		–0.3 to 60	V
Bootstrap Drive Voltage	V_{BOOT}		–0.3 to V_{IN} + 8	V
Switching Voltage	V_{SW}	Continuous	–0.3 to V_{IN} + 0.3	V
		Pulsed, t < 20 ns	–3 to V_{IN} + 3	V
Enable and TON Voltage	V_{EN}, V_{TON}		–0.3 to V_{IN} + 0.3	V
Linear Regulator Terminal	V_{CC}		–0.3 to 7	V
ADIM Pin Voltage	V_{ADIM}		–0.3 to 7	V
Current Sense Voltages	V_{CSH}, V_{CSL}		–0.3 to V_{IN} + 0.3	V
FAULT, FULL, RANGE, and FPWM Voltages	V_{FAULT}, V_{FULL}, V_{RANGE}, V_{FPWM}	A6216 only	–0.3 to 7	V
DR Pin Voltage	V_{DR}	A6216 only; DR pin voltage must not be higher than V_{CC} even when device is off (V_{CC} = 0 V)	–0.3 to V_{CC} + 0.3	V
Operating Ambient Temperature	T_A	K temperature range for automotive	–40 to 125	°C
Maximum Junction Temperature	T_J(max)		150	°C
Storage Temperature	T_{stg}		–55 to 150	°C

THERMAL CHARACTERISTICS*: May require derating at maximum conditions; see application section for optimization

Characteristic	Symbol	Test Conditions*		Value	Unit
Package Thermal Resistance (Junction to Ambient)	$R_{\theta JA}$	A6214 Package LK	On 4-layer PCB based on JEDEC standard	35	°C/W
		A6216 Package LP	On 4-layer PCB based on JEDEC standard	34	°C/W
			On 2-layer PCB with 3.8 $in.^2$ of copper area each side	43	°C/W
Package Thermal Resistance (Junction to Pad)	$R_{\theta JP}$			2	°C/W

*Additional thermal information available on the Allegro™ website.

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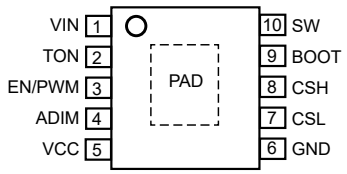
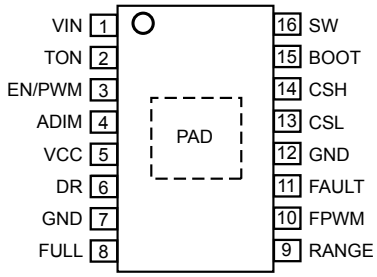
Pinout Diagram for A6214 (LK Package)



Terminal List Table for A6214 (LK Package)

Number	Name	Function
1	VIN	Supply voltage input voltage for IC and buck regulator
2	TON	Regulator on-time setting resistor terminal. Connect a resistor between VIN and TON to set the switching frequency.
3	EN/PWM	Logic input for Enable and PWM dimming
4	ADIM	Analog dimming control voltage input
5	VCC	Internal IC bias regulator output. Connect 1uF MLCC to GND. Can be used to supply up to 10mA for external load.
6	GND	Ground terminal
7	CSL	Current Sense (Lower end) feedback input for LED current
8	CSH	Current Sense (Higher end) feedback input for LED current
9	BOOT	DMOS gate driver bootstrap terminal
10	SW	Switched output terminal
-	PAD	Exposed pad for enhanced thermal dissipation; connect to GND

Pinout Diagram for A6216 (LP Package)



Terminal List Table for A6216 (LP Package)

Number	Name	Function
1	VIN	Supply voltage input voltage for IC and buck regulator
2	TON	Regulator on-time setting resistor terminal. Connect a resistor between VIN and TON to set the switching frequency
3	EN/PWM	Logic input for Enable and PWM dimming
4	ADIM	Analog dimming control voltage input
5	VCC	Internal IC bias regulator output. Connect 1uF MLCC to GND. Can be used to supply up to 10mA for external load
6	DR	Dimming Ratio control. In stand-alone mode: connect to resistor divider network from VCC to set the dimming PWM duty cycle
7	GND	Ground terminal
8	FULL	Selects 100% dimming duty cycle or DR control of duty cycle
9	RANGE	Selects DR control range, high range gives DR control from 5% to 100%, low range gives DR control from 5% to 33%.
10	FPWM	Dimming PWM frequency control. In stand-alone mode, connect a resistor to GND to set the dimming PWM frequency
11	FAULT	Open-drain output which is pulled low in case of fault. Connect through an external pull-up resistor to the desired logic level.
12	GND	Ground terminal
13	CSL	Current Sense (Lower end) feedback input for LED current
14	CSH	Current Sense (Higher end) feedback input for LED current
15	BOOT	DMOS gate driver bootstrap terminal
16	SW	Switched output terminal
-	PAD	Exposed pad for enhanced thermal dissipation; connect to GND

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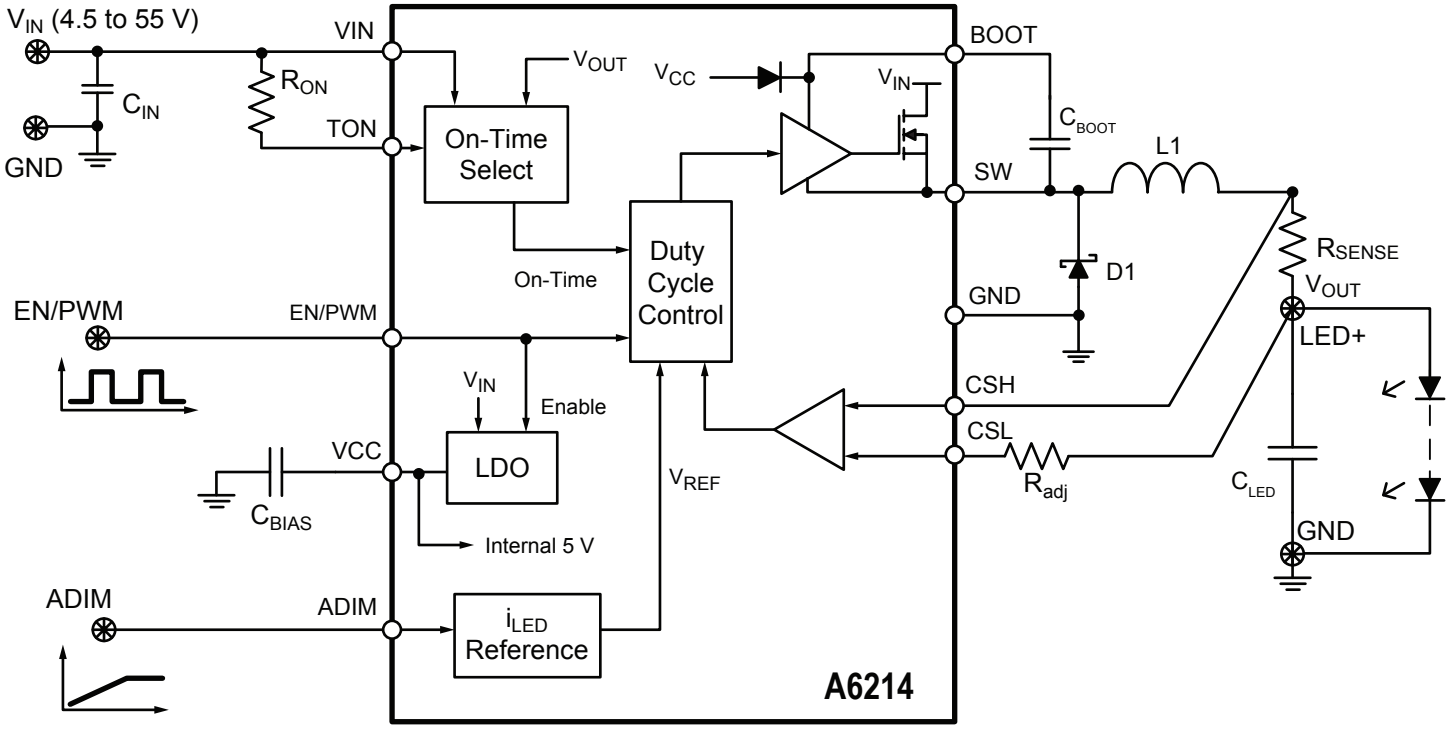
FUNCTIONAL BLOCK DIAGRAMS



Radj is optional. It can be used to fine-adjust the LED current in case the desired value of RSENSE is not available.

Figure 3: Simplified Functional Block Diagram for A6214

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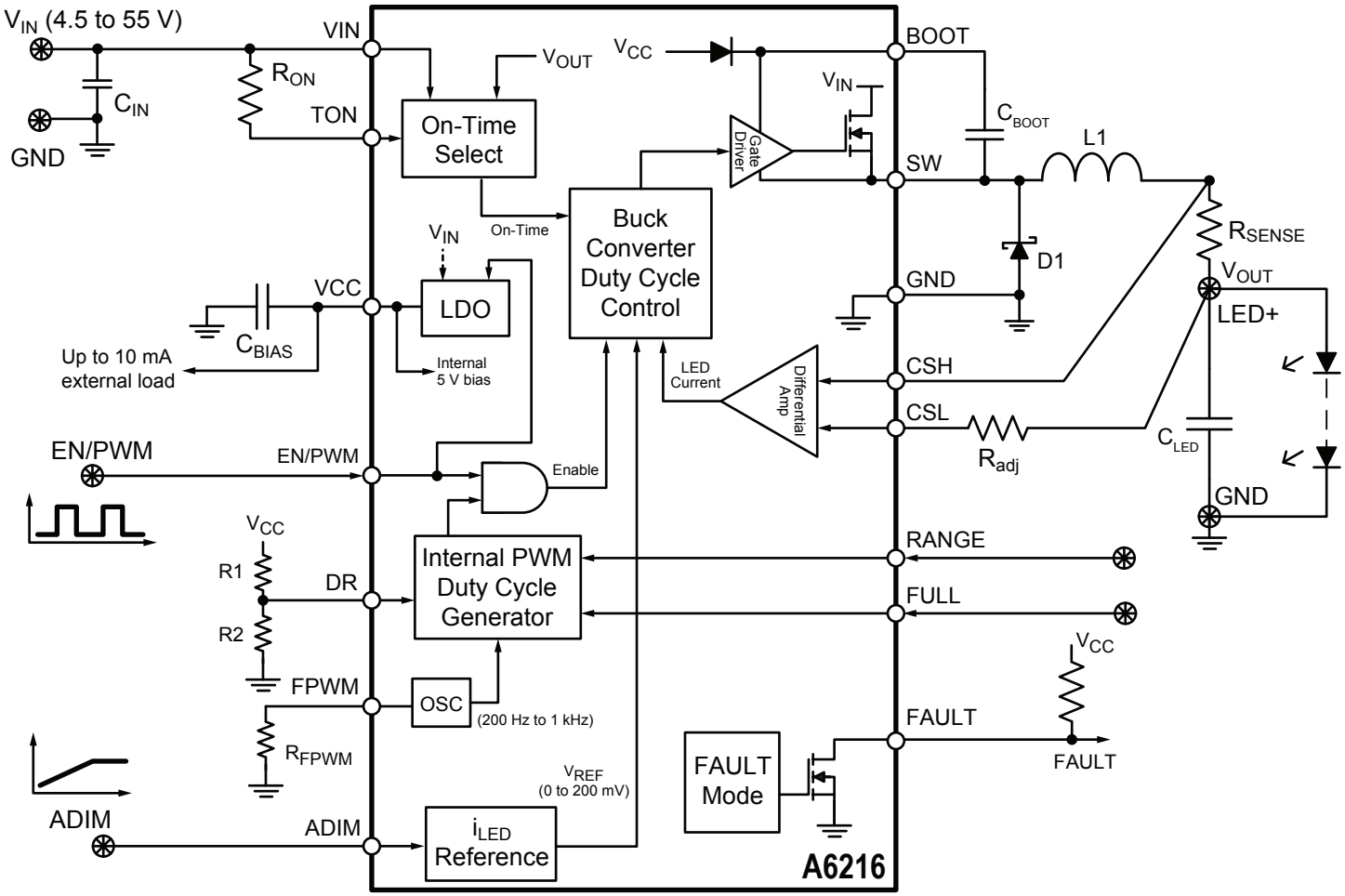

Figure 4: Simplified Functional Block Diagram for A6216

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ELECTRICAL CHARACTERISTICS: Valid at V_{IN} = 12 V, V_{OUT} = 6 V, T_A = –40°C to 125°C, typical values at T_A = 25°C, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input Supply Voltage	V_{IN}		4.5	–	55	V
V_{IN} Undervoltage Lockout Threshold	V_{UVLO}	V_{IN} increasing	–	–	4.3	V
V_{IN} Undervoltage Lockout Hysteresis	V_{UVLO_HYS}	V_{IN} decreasing	–	150	300	mV
VIN Pin Supply Current	I_{IN}	$V_{CSH} – V_{CSL}$ = 0.5 V, EN = V_{IH}, R_{ON} = 402 kΩ	–	5	–	mA
VIN Pin Shutdown Current	I_{INSD}	EN = V_{IL}	–	1	10	µA
Buck Switch Current Limit Threshold	I_{SWLIM}		2.5	3.25	4	A
Buck Switch On-Resistance	$R_{DS(on)}$	$V_{BOOT} = V_{IN}$ + 4.3 V, T_A = 25°C, I_{SW} = 0.5 A	–	0.25	0.4	Ω
BOOT Undervoltage Lockout Threshold	V_{BOOTUV}	V_{BOOT} to V_{SW} increasing	3.1	3.4	3.7	V
BOOT Undervoltage Lockout Hysteresis	$V_{BOTUVHYS}$	V_{BOOT} to V_{SW} decreasing	–	750	–	mV
Switching Minimum Off-Time	t_{OFFmin}	$V_{CSH} – V_{CSL}$ = 0 V	–	75	100	ns
Switching Minimum On-Time	t_{ONmin}	$V_{CSH} – V_{CSL}$ = 0.3 V	–	75	100	ns
Selected On-Time	t_{ON}	R_{ON} = 402 kΩ	800	1000	1200	ns
REGULATION COMPARATOR AND ERROR AMPLIFIER						
Load Current Sense Regulation Threshold at 100% [1]	V_{CSREG}	$V_{CSH} – V_{CSL}$ decreasing, SW turns on, ADIM tied to VCC	194	200	206	mV
Output Current Sense Common Mode Voltage (measured at CSL pin)	V_{OUT}	V_{IN} = 55 V, f_{SW} = 500 kHz, i_{LED} = 0.5 A	2.65	–	50	V
CSH Input Sense Current	I_{CSH}	$V_{CSH} – V_{CSL}$ = 0.2 V, V_{OUT} ≥ 5 V	–	–190	–	µA
CSL Input Sense Current	I_{CSL}	$V_{CSH} – V_{CSL}$ = 0.2 V, V_{OUT} ≥ 5 V	50	75	100	µA
INTERNAL LINEAR REGULATOR						
VCC Regulated Output	V_{CC}	0 mA < I_{CC} < 5 mA, V_{IN} > 6 V	4.85	5	5.15	V
VCC Current Limit [2]	i_{VCCLIM}	VCC ≥ 4.75 V	10	20	–	mA
VCC Dropout Voltage	V_{LDO}	Measure $V_{IN} – V_{CC}$. V_{IN} = 5 V, i_{VCC} = 9 mA	–	0.15	0.35	V
ENABLE/PWM INPUT						
Logic High Voltage	V_{IH}	V_{EN} increasing	1.8	–	–	V
Logic Low Voltage	V_{IL}	V_{EN} decreasing	–	–	0.4	V
EN Pin Pull-down Resistance	R_{ENPD}	V_{EN} = 5 V	–	100	–	kΩ
Maximum PWM Dimming Off-Time	t_{PWML}	Measured while EN = low, during dimming control, and internal references are powered-on (exceeding t_{PWML} results in shutdown)	10	17	–	ms
INTERNAL PWM DIMMING (A6216 ONLY)						
Internal PWM Dimming Frequency	f_{PWM}	External R_{FPWM} = 30 kΩ from FPWM pin to GND	180	200	220	Hz
FULL, RANGE Pins Input Low Voltage	V_{IL}		–	–	0.8	V
FULL, RANGE Pins Input High Voltage	V_{IH}		2	–	–	V
Internal PWM Duty Cycle	$D_{PWM5(L)}$	VDR driven by resistor divider from VCC, V_{CC} / V_{DR} = 9.72, f_{PWM} = 200 Hz, RANGE = low	4.75	5	5.25	%
	$D_{PWM5(H)}$	VDR driven by resistor divider from VCC, V_{CC} / V_{DR} = 29.2, f_{PWM} = 200 Hz, RANGE = high	4.5	5	5.5	%
	$D_{PWM90(H)}$	VDR driven by resistor divider from VCC, V_{CC} / V_{DR} = 1.62, f_{PWM} = 200 Hz, RANGE = high	87	90	93	%

Continued on the next page…

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ELECTRICAL CHARACTERISTICS (continued): Valid at V_{IN} = 12 V, V_{OUT} = 6 V, T_A = –40°C to 125°C, typical values at T_A = 25°C, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
ANALOG DIMMING INPUT						
Input Voltage for 100% LED Current	V_{ADIMH}	$V_{CSH} - V_{CSL} = V_{CSREG}$	2.1	–	–	V
Regulation Threshold at 50% Analog Dimming	$V_{CSREG50}$	V_{ADIM} = 1 V	–	100	–	mV
Regulation Threshold at 20% Analog Dimming	$V_{CSREG20}$	V_{ADIM} = 0.4 V	38.4	40	41.4	mV
FAULT PIN (A6216 ONLY)						
FAULT Pull-Down Voltage	$V_{FAULT(PD)}$	Fault condition asserted, pull-up current = 1 mA	–	–	0.4	V
FAULT Pin Leakage Current	$V_{FAULT(LKG)}$	Fault condition cleared, pull-up to 5 V	–	–	1	µA
TIMERS						
Cool Down Timer for Fault Retry	t_{RETRY}		–	1	–	ms
Delay Timer for Reporting LED Open Fault	t_{OPEN}		–	50	–	µs
THERMAL SHUTDOWN						
Thermal Shutdown Threshold [3]	T_{SD}		150	165	180	°C
Thermal Shutdown Hysteresis	T_{SDHYS}		–	25	–	°C

[1] In test mode, a ramp signal is applied across CSH and CSL pins to determine the CS regulation threshold voltage. In actual application, the *average* CS voltage is regulated at V_{CSREG} regardless of ripple voltage.
[2] The internal linear regulator is capable of supplying up to 10 mA to external devices.
[3] Determined by design and characterization. Not production tested.

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CHARACTERISTIC PERFORMANCE

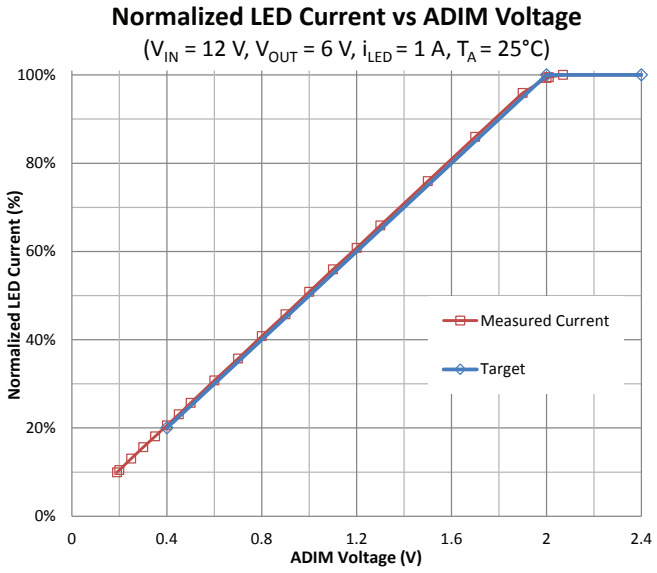

Figure 5: Analog Dimming Performance – LED current can be reduced linearly down to 10% using the ADIM pin voltage.

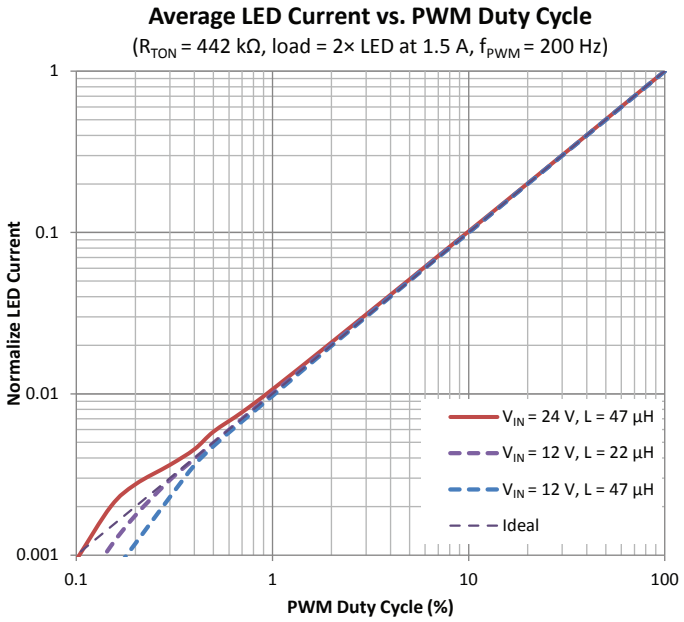

Figure 6: PWM Dimming Performance – Duty cycle down to ~0.1% (1000:1) can be achieved with higher V_{IN} or lower inductance.

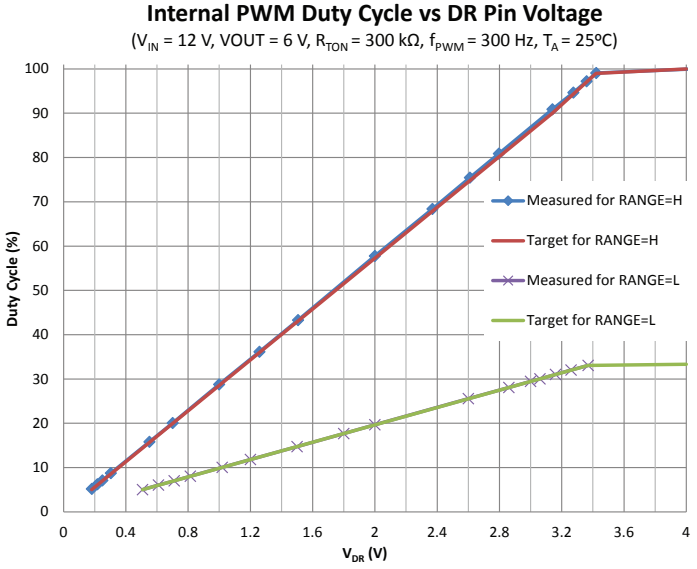

Figure 7: Internal PWM Dimming Operation (A6216 only) – Duty cycle is controlled by the voltage at DR pin.

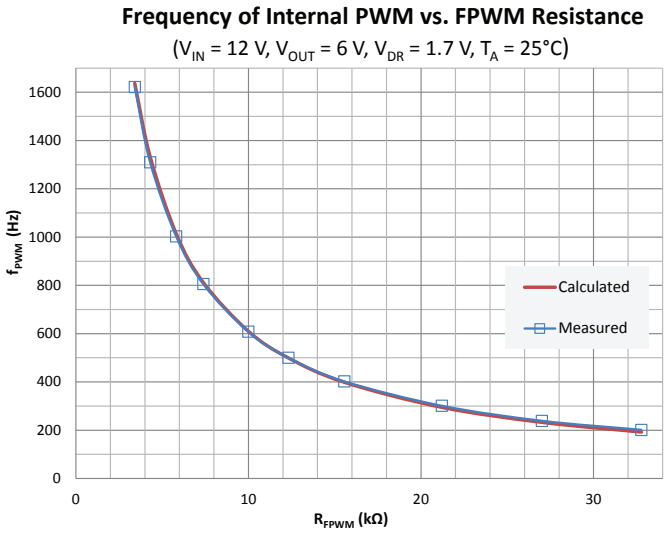

Figure 8: Internal PWM Dimming Frequency (A6216 only) as a function of FPWM Resistance

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CHARACTERISTIC PERFORMANCE (continued)

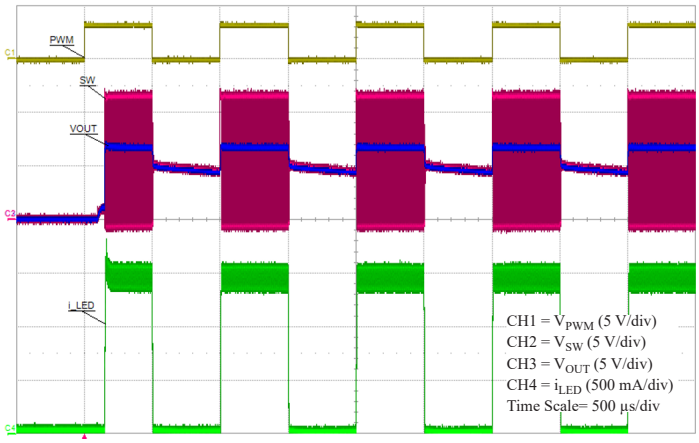

Figure 9: Startup for PWM Dimming operation – R_{TON} = 442 kΩ, L = 22 µH, V_{IN} = 12 V, Output = 2× LED at 1.5 A, PWM = 1 kHz 50%. Note that there is a ~150 µs delay for the first PWM = H pulse, but none for subsequent pulses.

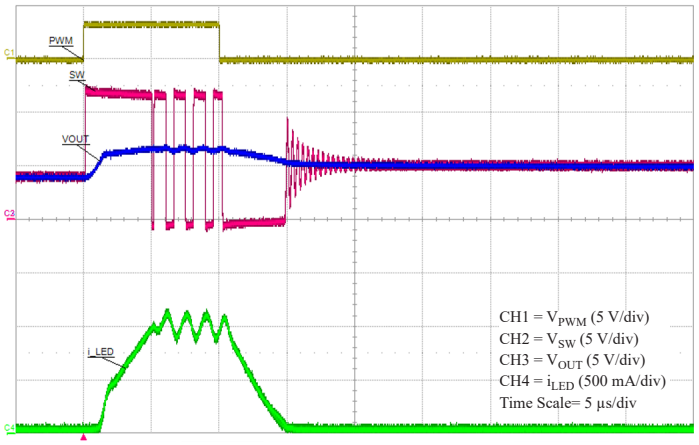

Figure 10: PWM Dimming with on-time of just 10 µs – R_{TON} = 442 kΩ, L = 22 µH, V_{IN} = 12 V, Output = 2× LED at 1 A. Note that the LED current takes ~5µs to ramp up to its steady-state value.

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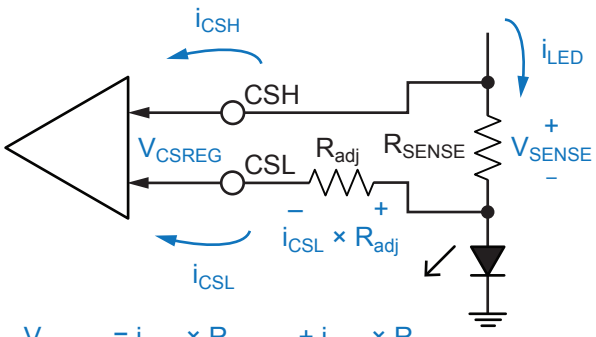
FUNCTIONAL DESCRIPTION

The A6214 is a buck regulator designed for driving a high-current LED string. It utilizes average current mode control to maintain constant LED current and consistent brightness. The LED current level is easily programmable by selection of an external sense resistor, with a value determined as follows:

$$R_{SENSE} = V_{CSREG} / i_{LED}$$

where $V_{CSREG} = V_{CSH} - V_{CSL} = 0.2$ V typical.

If necessary, a resistor can be inserted in series with the CSL pin to fine-tune the LED current, as shown below:



$V_{CSREG} = i_{LED} \times R_{SENSE} + i_{CSL} \times R_{adj}$

Therefore

$i_{LED} = (V_{CSREG} - i_{CSL} \times R_{adj}) / R_{SENSE}$

Figure 11: How To Fine-Tune LED Current Using R_{adj}

For example, with a desired LED current of 1.4 A, the required $R_{SENSE} = 0.2$ V / 1.4 A = 0.143 Ω. But the closest power resistor available is 0.13 Ω. Therefore, the difference is:

$$R_{adj} \times i_{CSL} = 0.2\ V - 1.4\ A \times 0.13\ \Omega = 0.018\ V$$

where $i_{CSL} = 75$ µA typical:

$$R_{adj} = 0.018\ V / 75\ \mu A = 240\ \Omega$$

Note that the effects of R_{adj} are only applicable when the output voltage is at least 5 V. If the LED string voltage is below 5 V, $R_{adj} = 0$ should be used.

The LED current is further modulated by the ADIM (Analog Dimming) pin voltage. This feature can be used for LED brightness calibration, or for thermal foldback protection. See Analog Dimming section for details.

Switching Frequency

The A6214 operates in fixed on-time mode during switching. The on-time (and hence switching frequency) is programmed using an external resistor connected between the VIN and TON pins, as given by the following equation:

$$t_{ON} = k \times (R_{TON} + R_{INT}) \times (V_{OUT} / V_{IN})$$

$$f_{SW} = 1 / [k \times (R_{TON} + R_{INT})]$$

where k = 0.00434, with f_{SW} in MHz, t_{ON} in µs, and R_{ON} and R_{INT} (internal resistance, 20 kΩ) in kΩ.

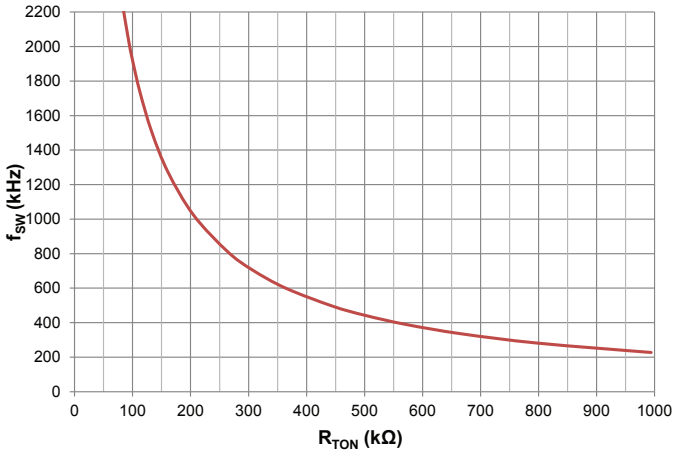


Figure 12: Switching Frequency vs. TON resistance

ENABLE AND DIMMING

The IC is activated when a logic high signal is applied to the EN (enable) pin. The buck converter ramps up the LED current to a target level set by R_{SENSE}.

When the EN pin is forced from high to low, the buck converter is turned off, but the IC remains in standby mode for up to 10 ms. If EN goes high again within this period, the LED current is turned on immediately. Active dimming of the LED is achieved by sending a PWM (pulse-width modulation) signal to the EN pin. The resulting LED brightness is proportional to the duty cycle (t_{ON}/Period) of the PWM signal. A practical range for PWM dimming frequency is between 100 Hz (Period = 10 ms) and 2 kHz.

If EN is low for more than 17 ms, the IC enters shutdown mode to reduce power consumption. The next high signal on EN will initialize a full startup sequence, which includes a startup delay of approximately 150 µs. This startup delay is not present during PWM operation.

The EN pin is high-voltage tolerant and can be directly connected to a power supply. However, if EN is higher than the V_{IN} voltage at any time, a series resistor (1-10 kΩ) is required to limit the current flowing into the EN pin. This series resistor is not necessary if EN is driven from a logic input.

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PWM DIMMING RATIO

The brightness of the LED string can be reduced by adjusting the PWM duty cycle at the EN pin as follows:

$$Dimming\ ratio = PWM\ on\text{-}time\ /\ PWM\ period$$

For example, by selecting a PWM period of 5 ms (200 Hz PWM frequency) and a PWM on-time of 5 µs, a dimming ratio of 0.1% can be achieved. This is sometimes referred to as "1000:1 dimming."

In an actual application, the minimum dimming ratio is determined by various system parameters, including: V_{IN}, V_{OUT}, inductance, LED current, switching frequency, and PWM frequency. As a general guideline, the minimum PWM on-time should be kept at 5 µs or longer. A shorter PWM on-time is acceptable under more favorable operating conditions, such as higher V_{IN} and lower inductance.

INTERNAL PWM DIMMING (A6216 ONLY)

In addition to external PWM dimming through EN pin, the A6216 is able to generate an internal PWM dimming signal in stand-alone mode. Frequency of the internal PWM signal can be set by connecting a resistor between FPWM pin and GND, as given by the following equation:

$$f_{PWM} = c\ /\ (R_{FPWM} + R_{INT})$$

where c = 6400, with f_{PWM} in Hz, and R_{FPWM} and R_{INT} (internal resistance, 0.5 kΩ) in kΩ.

This frequency can be between 200 Hz and 1 kHz when RANGE is High, or 200 Hz and 500 Hz when RANGE is Low. Duty cycle of PWM signal is linearly proportion to the voltage at DR (Dimming Ratio) pin. This is illustrated by the following chart:

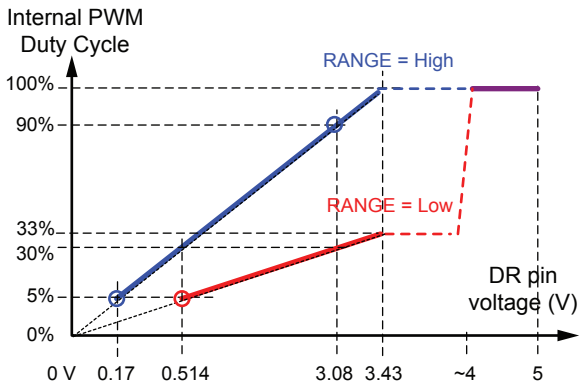

Figure 13: Variation of PWM Duty Cycle with respect to DR Pin Voltage

It should be noted that the internal PWM duty cycle depends on the ratio between V_{CC} and V_{DR}. The voltages shown in the chart are with V_{CC} = 5 V. For better accuracy, derive the DR pin voltage using a resistor divider connected between VCC and GND. A practical range of internal PWM duty cycle when RANGE = High is between 5% (V_{DR} = 0.17 V) and 90% (V_{DR} = 3.08 V). To improve accuracy at low duty cycles between 5% and 30%, set RANGE to Low. If DR pin is above 3.4 V, duty cycle stays at around 99% if RANGE = High, 33% if Low.

To disable internal PWM generation, tie DR pin to VCC pin. (Do NOT leave DR pin floating or connected to GND.) The FPWM pin can be either left open or tied to VCC. Note that at any time during stand-alone PWM dimming mode, if EN pin goes low, the LED is turned off immediately. This is illustrated in figure below.

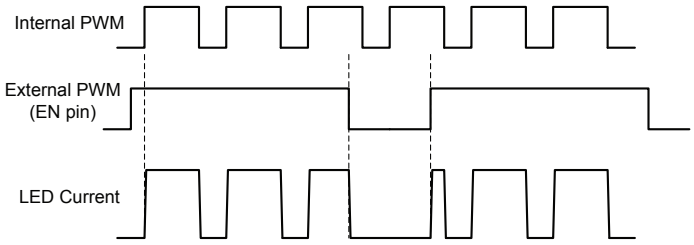

Figure 14: LED Current when Both Internal and External PWM Dimming Signals are Applied

ANALOG DIMMING

In addition to PWM dimming, the A6214/16 also provides an analog dimming feature. When V_{ADIM} is over 2 V, the LED current is at 100% level (as defined by the SENSE resistor). When V_{ADIM} is below 2 V, the LED current decreases linearly down to 20% at V_{ADIM} = 0.4 V. This is shown in the following figure:

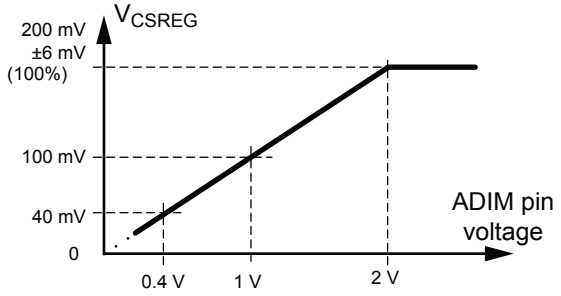

Figure 15: ADIM Pin Voltage Controls SENSE Reference Voltage (hence LED current)

It is possible to pull ADIM pin below 0.4 V to achieve lower than 20% analog dimming. However, the linearity may suffer if the LED ripple current become too large compared to the average current. For example, if the LED ripple current is ±100 mA, then the average current can only be dimmed down to 100 mA linearly.

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ADIM pin can be used in conjunction with PWM dimming to provide wider LED dimming range over 1000:1. In addition, the IC can provide thermal foldback protection by using an external NTC (negative temperature coefficient) thermistor, as shown below:

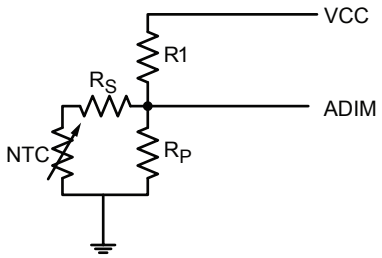


Figure 16: Using an External NTC Thermistor to Implement Thermal Foldback

If analog dimming is not required, the ADIM pin must be connected to VCC pin. (Do NOT leave ADIM pin floating or connected to GND.)

OUTPUT VOLTAGE AND DUTY CYCLE

The figure below provides simplified equations for approximating output voltage. The output voltage of a buck converter is approximately given as:

$$V_{OUT} = V_{IN} \times D - V_D \times (1 - D) \approx V_{IN} \times D, \text{ if } V_D << V_{IN}$$

$$D = t_{ON} / (t_{ON} + t_{OFF})$$

where D is the duty cycle, and V_D is the forward drop of the diode D1 (typically under 0.5 V for Schottky diode).

During SW on-time:

$$i_{RIPPLE} = (V_{IN} - V_{OUT}) / L \times t_{ON} = (V_{IN} - V_{OUT}) / L \times t \times D$$

where $D = t_{ON} / t$.

During SW off-time:

$$i_{RIPPLE} = (V_{OUT} + V_D) / L \times t_{OFF} = (V_{OUT} + V_D) / L \times t \times (1 - D)$$

Simplified equation for output voltage:

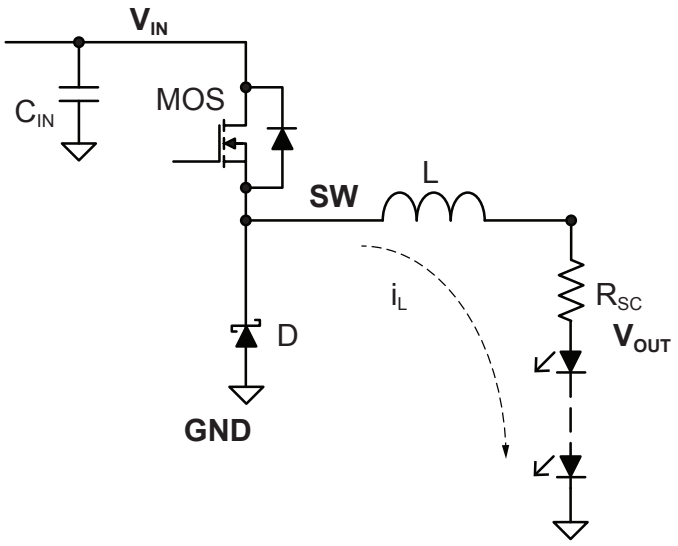
$$V_{OUT} = V_{IN} \times D - V_D \times (1 - D)$$

If $V_D << V_{IN}$, then $V_{OUT} = V_{IN} \times D$ approximately.

More precisely:

$$V_{OUT} = (V_{IN} - i_{AVG} \times R_{DS(on)}) \times D - V_D \times (1 - D) - i_{AVG} \times (DCR + R_{SC})$$

where DCR is the internal resistance of inductor and R_{SC} is the sense resistance.



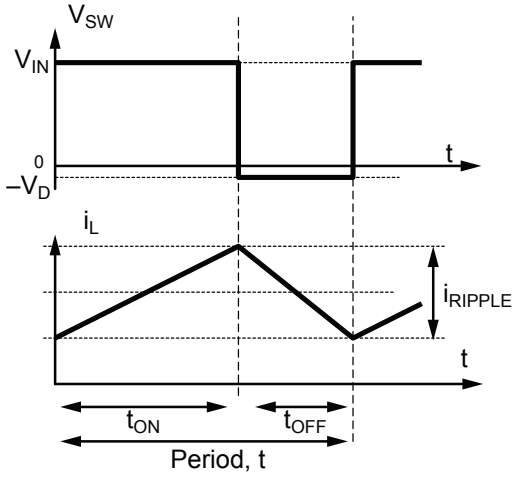


Figure 17: Simplified Waveforms for a Buck Converter

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MINIMUM AND MAXIMUM OUTPUT VOLTAGES

For a given input voltage, the maximum output voltage depends on the switching frequency and minimum t_{OFF}. For example, if t_{OFF}(min) = 150 ns and f_{SW} = 2 MHz, then the maximum duty cycle is 80%. So, for a 12.5 V input, the maximum output is approximately 10 V (based on the simplified equation of $V_{OUT} = V_{IN} \times D$). This means up to 3 LEDs can be operated in series, assuming V_f = 3.2 V or less for each LED.

The minimum output voltage depends on minimum t_{ON} and switching frequency. For example, if the minimum t_{ON} = 100 ns and f_{SW} = 1 MHz, then the minimum duty cycle is 10%. That means with V_{IN} = 24 V, the theoretical minimum V_{OUT} is just 2.4 V. However, the internal current sense amplifier is designed to operate down to V_{OUT} = 2.65 V. Therefore, the output voltage should not go lower than 2.65 V, or else the current accuracy will suffer.

To a lesser degree, the output voltage is also affected by other factors such as LED current, on-resistance of the high-side switch, DCR of the inductor, and forward drop of the low-side diode.

As a general rule, switching at lower frequencies allows a wider range of V_{OUT}, and hence more flexible LED configurations.

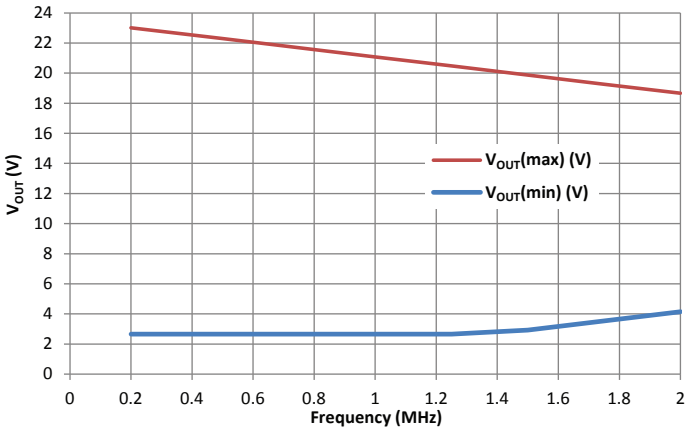

Figure 18: Minimum and Maximum Output Voltage vs. Switching Frequency (V_{IN} = 24 V, minimum t_{ON} and t_{OFF} of 100 ns)

If the required output voltage is lower than that permitted by the minimum t_{ON}, the controller will automatically extend the t_{OFF}, in order to maintain the correct duty cycle. This means that the switching frequency will drop lower when necessary, in order to keep the LED current in regulation.

If the LED string is completely shorted (V_{OUT} = 0 V), LED current regulation will become impossible. The output current will increase until it trips SW overcurrent protection. The IC then shuts down and retries after approximately 1 ms cooldown period.

THERMAL BUDGETING

The A6214 is capable of supplying a 2 A current through its high-side switch. However, depending on the duty cycle, the conduction loss in the high-side switch may cause the package to overheat. Therefore, care must be taken to ensure the total power loss of package is within budget. For example, if the maximum temperature rise allowed is ΔT = 50°C at the device case surface, then the maximum power dissipation of the IC is 1.4 W. Assuming the maximum $R_{DS(on)}$ = 0.4 Ω and a duty cycle of 85%, then the maximum LED current is limited to 2 A approximately. At a lower duty cycle, the LED current can be higher.

FAULT HANDLING

The A6214 is designed to handle the following faults:

- Pin-to-ground short
- Pin-to-neighboring pin short
- Pin open
- External component open or short
- Output short to GND

The waveform in the figure below illustrates how the A6214 responds in the case in which the current sense resistor or the CSH and CSL pins are shorted together. Note that the SW pin overcurrent protection is tripped at around 3.5 A, and the part shuts down immediately. The part then goes through startup retry after approximately 1 ms of cooldown period.

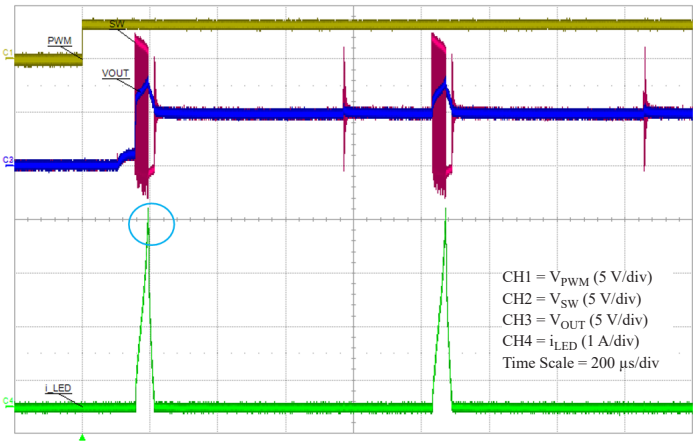

Figure 19: In case of sense resistor short fault – Output current rises until it trips SW OCP at ~3.5 A. The IC shuts off and retries after ~1 ms cooldown period.

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As another example, the waveform in figure below shows the fault case where external diode D1 is missing or open. As LED current builds up, a larger-than-normal negative voltage is developed at the SW node during off-time. This voltage trips the missing detection function of the IC. The IC then shuts down immediately and waits for a cooldown period before retry.

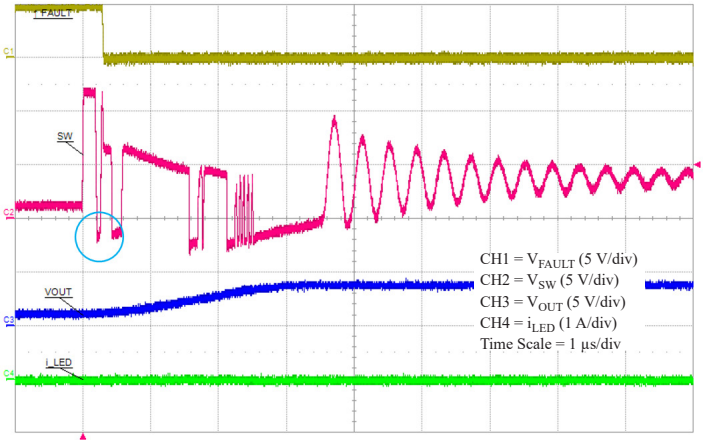

Figure 20: In case of missing low-side diode – SW voltage fall below –2 V and trips Missing-Diode fault. FAULT pin (A6216 only) is pulled Low immediately. The IC shuts off and retries after cooldown period.

COMPONENT SELECTIONS

The inductor is often the most critical component in a buck converter. Follow the procedure below to derive the correct parameters for the inductor:

1. Determine the saturation current of the inductor. This can be done by simply adding 20% to the average LED current:

$$i_{SAT} \geq i_{LED} \times 1.2.$$

2. Determine the ripple current amplitude (peak-to-peak value). As a general rule, ripple current should be kept between 10% and 30% of the average LED current:

$$0.1 < i_{RIPPLE(pk\text{-}pk)} / i_{LED} < 0.3.$$

3. Calculate the inductance based on the following equations:

$$L = (V_{IN} - V_{OUT}) \times D \times t / i_{RIPPLE}, \text{ and}$$

$$D = (V_{OUT} + V_D) / (V_{IN} + V_D),$$

where

D is the duty cycle,
t is the period $1/f_{SW}$, and
V_D is the forward voltage drop of the Schottky diode D1.

OUTPUT FILTER CAPACITOR

The A6214 is designed to operate in current regulation mode. Therefore, it does not require a large output capacitor to stabilize the output voltage. This results in lower cost and smaller PCB area. In fact, having a large output capacitor is not recommended.

In most applications, however, it is beneficial to add a small filter capacitor (around 0.1 µF) across the LED string. This cap serves as a filter to eliminate switching spikes seen by the LED string. This is very important in reducing EMI noises, and may also help in ESD testing.

ADDITIONAL NOTES ON RIPPLE CURRENT

• For consistent switching frequency, it is recommended to choose the inductor and switching frequency to ensure the inductor ripple current percentage is at least 10% over normal operating voltage range (ripple current is lowest at lowest V_{IN}).

If ripple current is less than 10%, the switching frequency may jitter due to insufficient ripple voltage across CSH and CSL pins. However, the average LED current is still regulated.

• For best accuracy in LED current regulation, a low current ripple of less than 20% is required.

• There is no hard limit on the highest ripple current percentage allowed. A 40% ripple current is still acceptable, as long as both the inductor and LEDs can handle the peak current (average current × 1.2 in this case). However, higher ripple current % affects the accuracy of LED current, and limits the minimum current that can be regulated when using ADIM.

• In general, allowing a higher ripple current percentage enables lower-inductance inductors to be used, which results in smaller size and lower cost.

• If lower ripple current is required for the LED string, one solution is to add a small capacitor (such as 1 to 2.2 µF) across the LED string from LED+ to GND. In this case, the inductor ripple current remains high while the LED ripple current is greatly reduced.

• The effectiveness of this filter capacitor depends on many factors, such as: switching frequency, inductors used, PCB layout, LED voltage and current, and so forth.

• The addition of this capacitor introduces a longer delay in LED current during PWM dimming operation. Therefore, the accuracy of average LED current is reduced at short PWM on-time.

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INDUCTOR SELECTION CHART

The chart in figure below summarizes the relationship between LED current, switching frequency, and inductor value. Based on this chart: assuming LED current = 1 A and L = 22 µH, then minimum f_{SW} = 0.7 MHz in order to keep the ripple current at 20% or lower. (Note: $V_{OUT} = V_{IN} / 2$ is the worst case for ripple current). If the switching frequency is lower, then a larger inductance must be used to meet the same ripple current requirement.

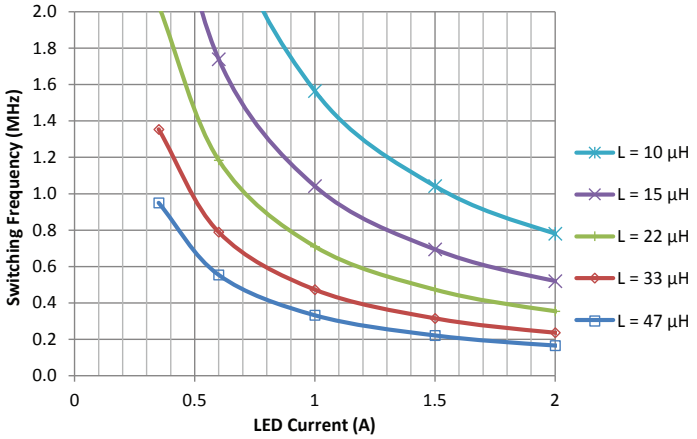

Figure 21: Relation between minimum switching frequency and LED current, given different inductance used (V_{IN} = 12 V, V_{OUT} = 6 V, ripple current = 20%)

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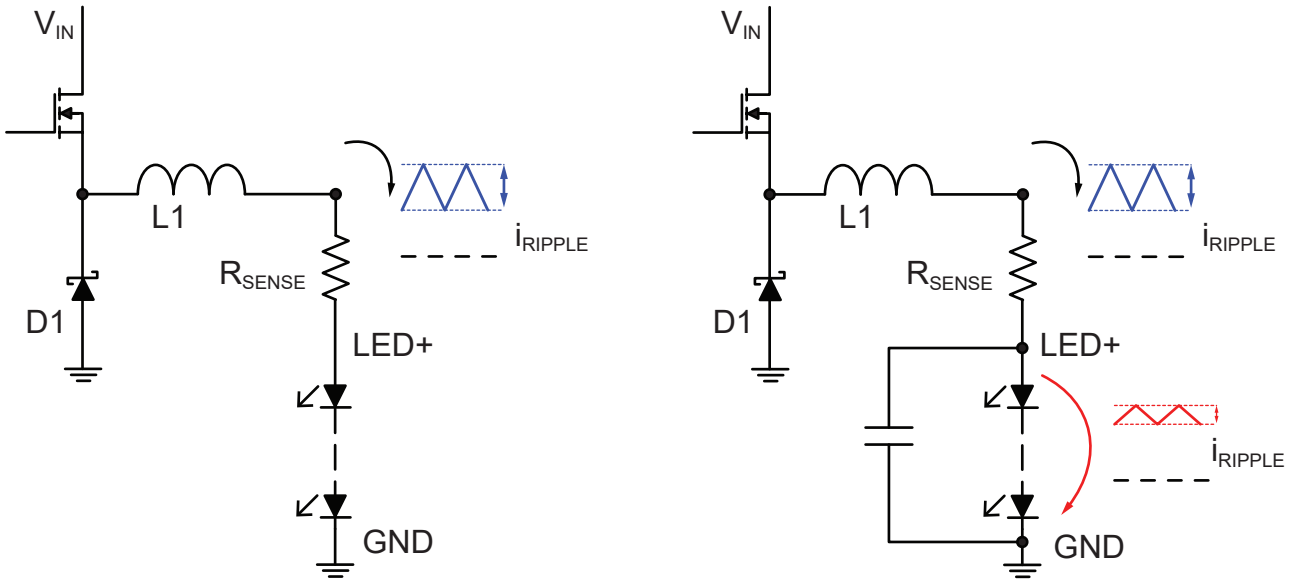
Effects of Output Capacitor on LED Ripple Current



Without output capacitor:
The same inductor ripple current flows through sense resistor and LED string.

With a small capacitor across LED string:
Ripple current through LED string is reduced, while ripple voltage across R_{SENSE} remains high.

Figure 22: Using an Output Filter Capacitor to Reduce Ripple Current in LED String

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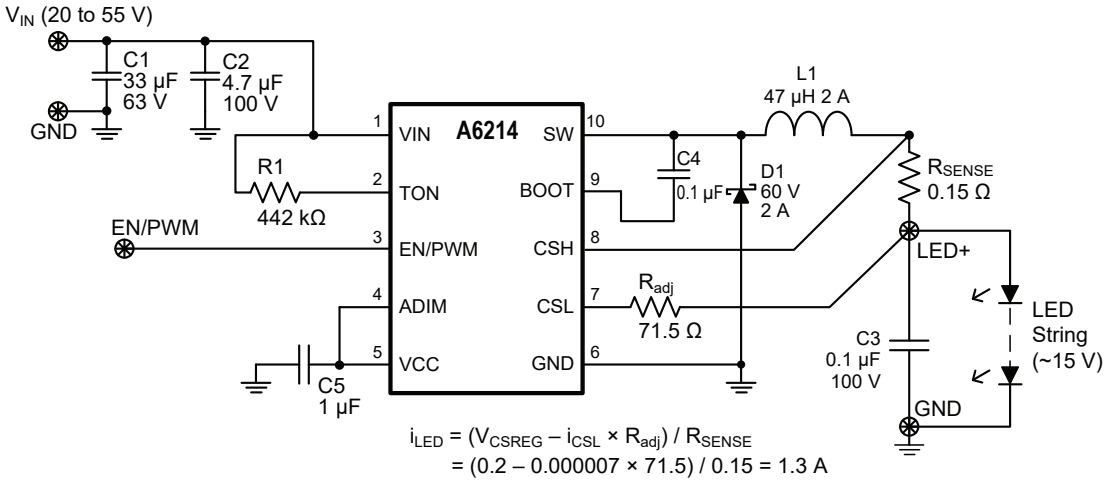
APPLICATION CIRCUIT DIAGRAMS



Suggested Components

Symbol	Part Number	Manufacturer
C1	HHXA630ARA330MHA0G	United Chemi-Con
C2	C3225X7S2A475M200AB	TDK
C3	CGA4J2X7R2A104M125AA	TDK
L1	CDRH105RNP-470NC	Sumida
D1	10MQ060NTRPBF	Vishay
R_{SENSE}	RL1632R-R150-F	Susumu

Figure 23: Application Circuit Example for A6214 (for driving 15 V LED at 1.3 A, f_{SW} = 500 kHz)

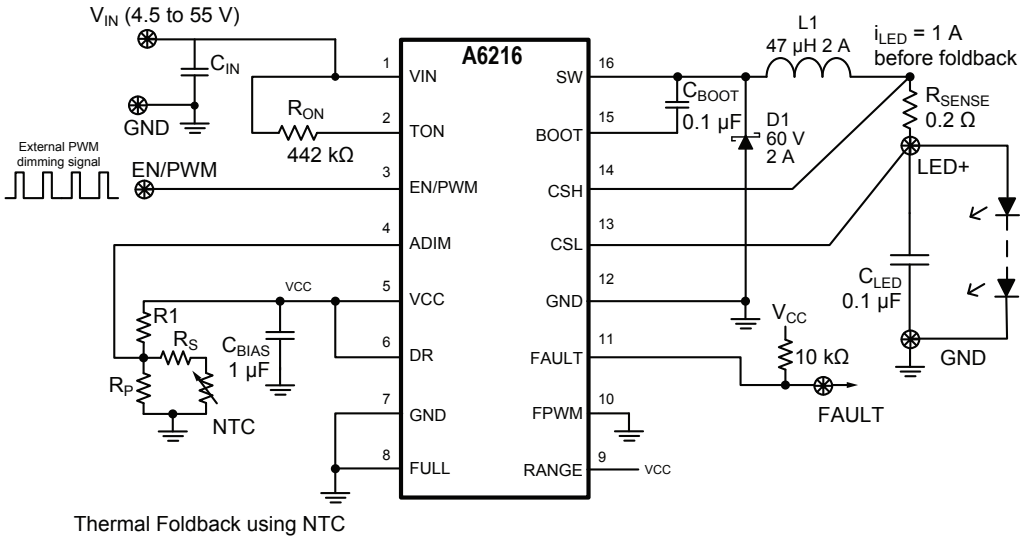


Figure 24: Application Circuit Example for A6216 (with External PWM and Thermal Foldback)

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APPLICATION CIRCUIT DIAGRAMS (continued)

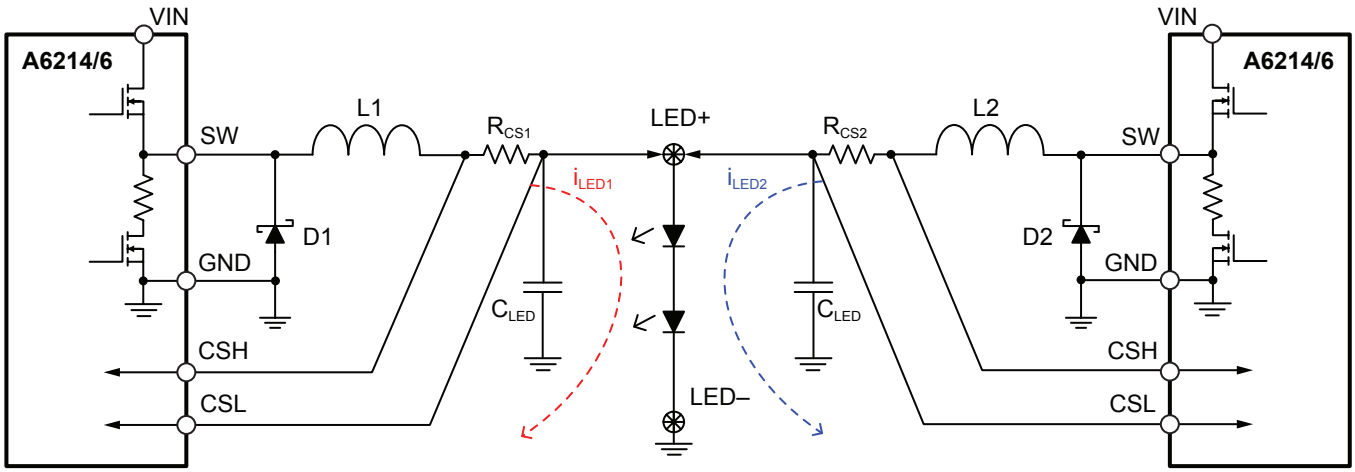

Figure 25: Using two (or more) A6214/16 in parallel to drive the same LED string. Total LED current is the sum of currents from each driver.

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APPLICATION CIRCUIT DIAGRAMS (continued)

PROTECTION FROM OUTPUT LC-RESONANCE

During normal operation, if the LED load becomes disconnected (due to a bad connector, for example), the output capacitor C_{LED} will be charged up to $V_{OUT} = V_{IN}$. Later, when the LED load is reconnected, higher voltage stored in C_{LED} will create a huge current spike through the load. Normally this does not create any problems, since the current spike will decay within a few microseconds. However, if the LED load is connected through long cables, the parasitic inductance L_K in the cable will form an LC-resonant circuit with C_{LED}. If the resonant circuit is under-damped, V_{OUT} may oscillate and becomes negative. This could subject CSH and CSL pins to negative spike voltage exceeding their Absolute Maximum Ratings. Therefore, the following precautions are recommended to avoid output oscillation:

- Use shortest possible LED cables to reduce L_K.
- Use lower capacitance for C_{LED} to reduce stored energy ($E_C = 0.5 \times C_{LED} \times V_{IN}^2$).
- Critically damp the output LC-resonant circuit, as shown in Figure 26. The drawback is additional power loss during PWM dimming operation (since C1 is charged and discharged through R1 during each PWM cycle).

In case the output LC resonance cannot be eliminated (due to long LED cables, for example), consider adding a Schottky barrier diode (SBD) in parallel with C_{LED}, as shown in Figure 28. The SBD clamps the negative spike of the LC resonance, so CSH and CSL pins are protected. This is the most effective protection with minimal side effects.

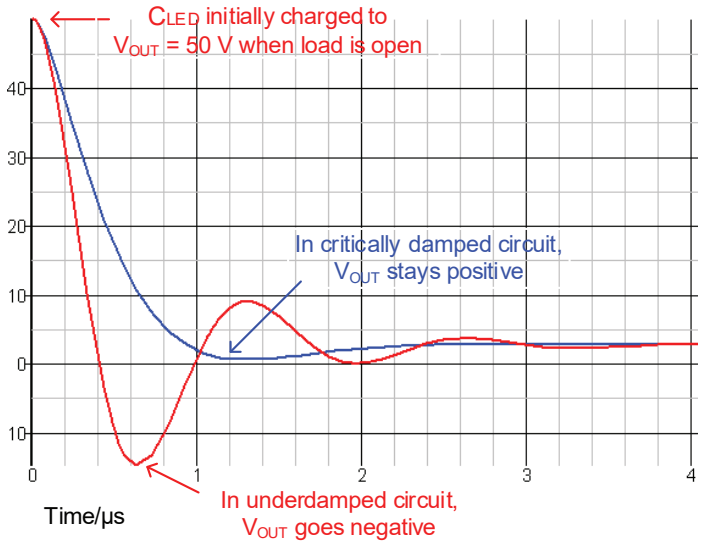

Figure 27: Simulation Results Showing Difference in V_{OUT} Between Underdamped and Critically-Damped Circuits

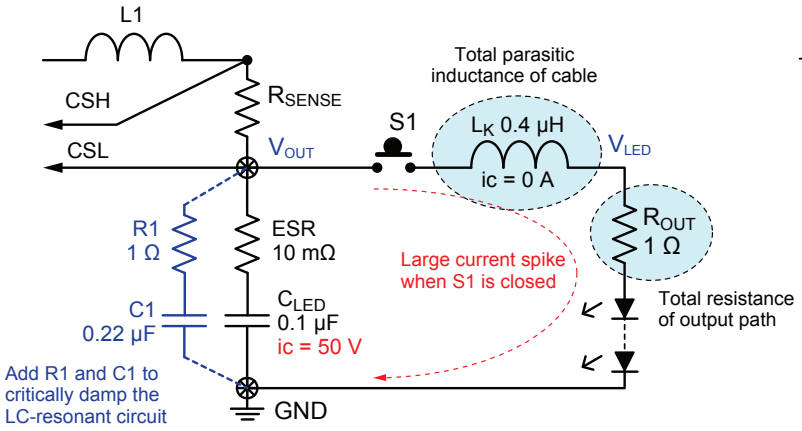

Figure 26: Countermeasure to Prevent V_{OUT} Oscillation During Output Intermittent Open/Short Fault

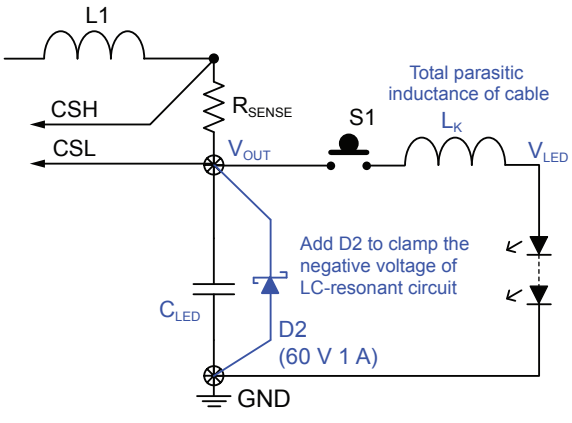

Figure 28: Using Schottky Diode to Clamp the Negative spike from Output LC-Resonance

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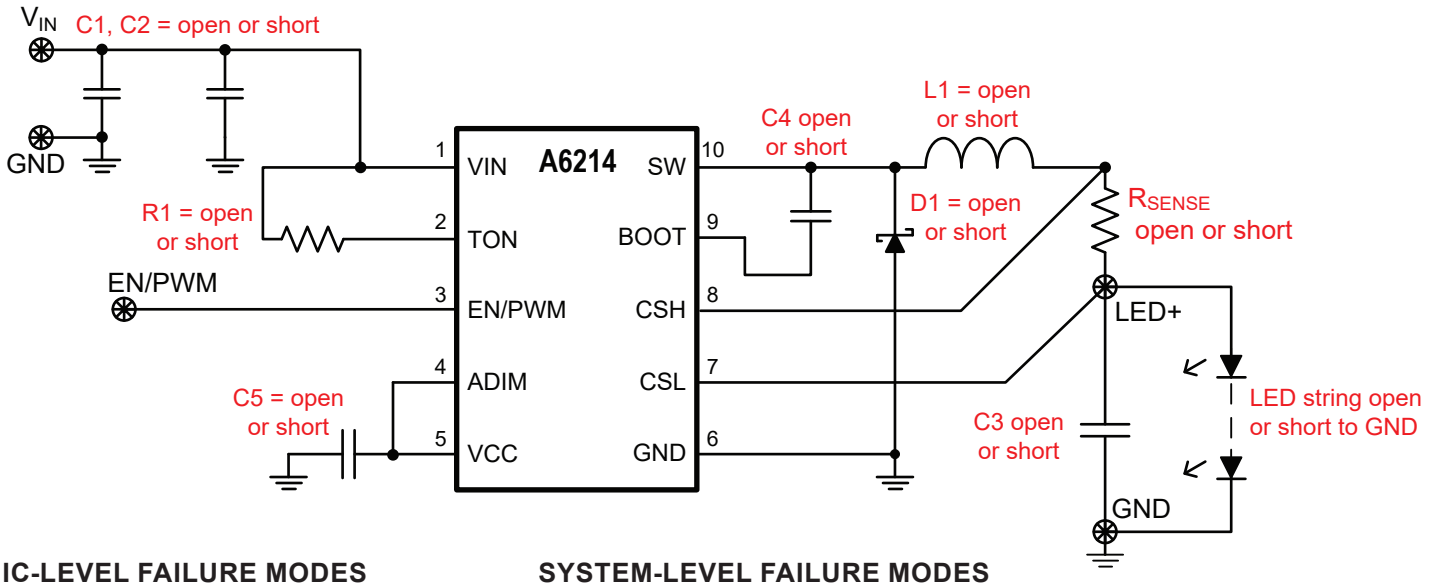
SYSTEM FAILURE DETECTION AND PROTECTION



IC-LEVEL FAILURE MODES

Protected against:

- Any pin open
- Any pin shorted to GND
- Adjacent pin-to-pin short

SYSTEM-LEVEL FAILURE MODES

Protected against open/short fault for all external components, including:

- LED string
- Sense resistor
- Inductor
- Diode
- Input/output caps, etc.

Figure 29: Showing Various Possible Fault Cases in an Application Circuit

System Failure Mode Table (partial)

Failure Mode	Symptom Observed	FAULT flag (A6216) asserted?	A6214/16 Response
Inductor shorted	Dim light from LED	Yes	Current spike trips SW secondary OCP and turns off switching. Retries after 1 ms.
Sense resistor open	No light from LED	Yes	High differential sense voltage causes IC to shut off switching. Retries after 1 ms.
Sense resistor shorted	Dim light from LED	Yes	Increases SW current, which eventually trips SW secondary OCP fault. Retries after 1 ms.
Diode open	Dim light from LED	Yes	Detects missing diode fault and shuts off switching. Retries after 1 ms.
Diode shorted	No light from LED	Yes	Trips SW secondary OCP and turns off switching. Retries after 1 ms.
LED string open	No light from LED	Yes*	Continue to switch at maximum t_{ON} (Since this fault cannot be distinguished from V_{IN} too low for LED forward drop)
LED string shorted to GND, or Output cap shorted	No light from LED	Yes*	IC unable to regulate LED current at V_{OUT} = 0 V. SW current increases and trips OCP. IC shuts down and retries after 1 ms.
LED string partially shorted	Some LEDs are not on	NO	Normal operation (since IC has no way to know how many LED is supposed to be in series).

Continued on the next page…

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System Failure Mode Table (partial) (continued)

Failure Mode	Symptom Observed	FAULT flag (A6216) asserted?	A6214/16 Response
Output cap open	Normal light from LED	NO	Normal operation (since IC only monitors inductor current).
Boot cap open	Dim light from LED	Yes*	IC attempts to switch but can't fully turn on SW. Short current spikes through LED string.
Boot cap shorted	No light from LED	Yes*	IC detects undervoltage fault across Boot cap and will not start switching.
TON resistor open	Dim light from LED	Yes	SW turns on and hits secondary current limit, then shuts down. Retries after 1 ms.
TON resistor shorted	Dim light from LED	NO	Operates at maximum switching frequency (minimum t_{ON} and t_{OFF}). May hit thermal limit.

Note (*)

- In case of LED current not in regulation, FAULT flag is asserted after approximately 50 µs timeout delay.
- For PWM dimming operation with on-time < 50 µs, FAULT flag is asserted if LED current fails to reach regulation after 16 PWM = H pulses.
- For PWM dimming operation with on-time > 50 µs, FAULT flag is only asserted when PWM = H. However, if the fault persists for 16 consecutive PWM cycles, FAULT flag will be pulled Low and then it stays Low until the fault is cleared.

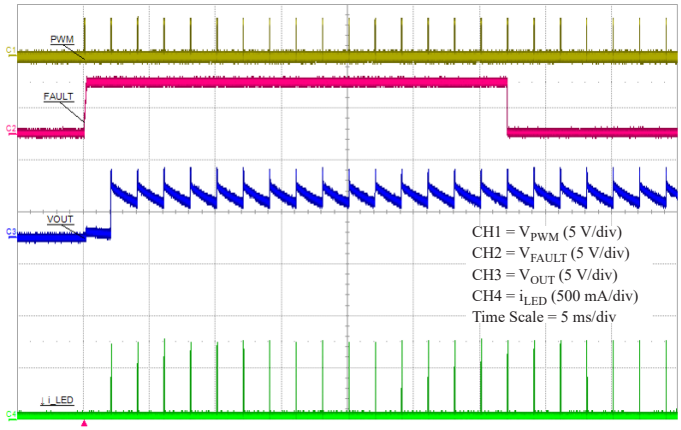

Figure 30: V_{IN} too low for LED regulation. PWM = 500 Hz 2% (40 µs). FAULT = L after 16 PWM pulses.

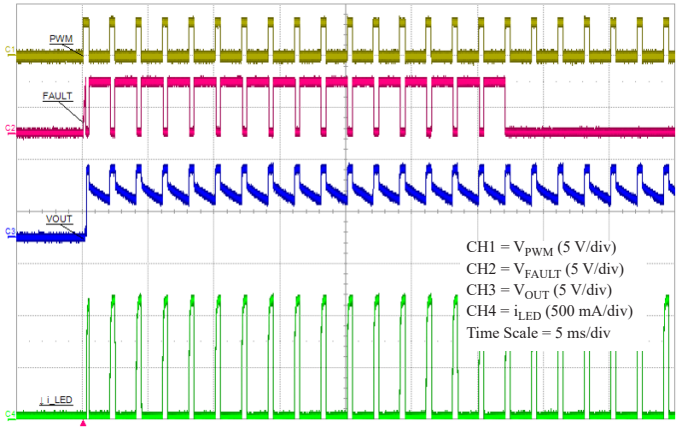

Figure 31: VIN too low for LED regulation. PWM = 500 Hz 20% (400 µs). FAULT toggles each time PWM = H, but stays Low after 16 PWM pulses.

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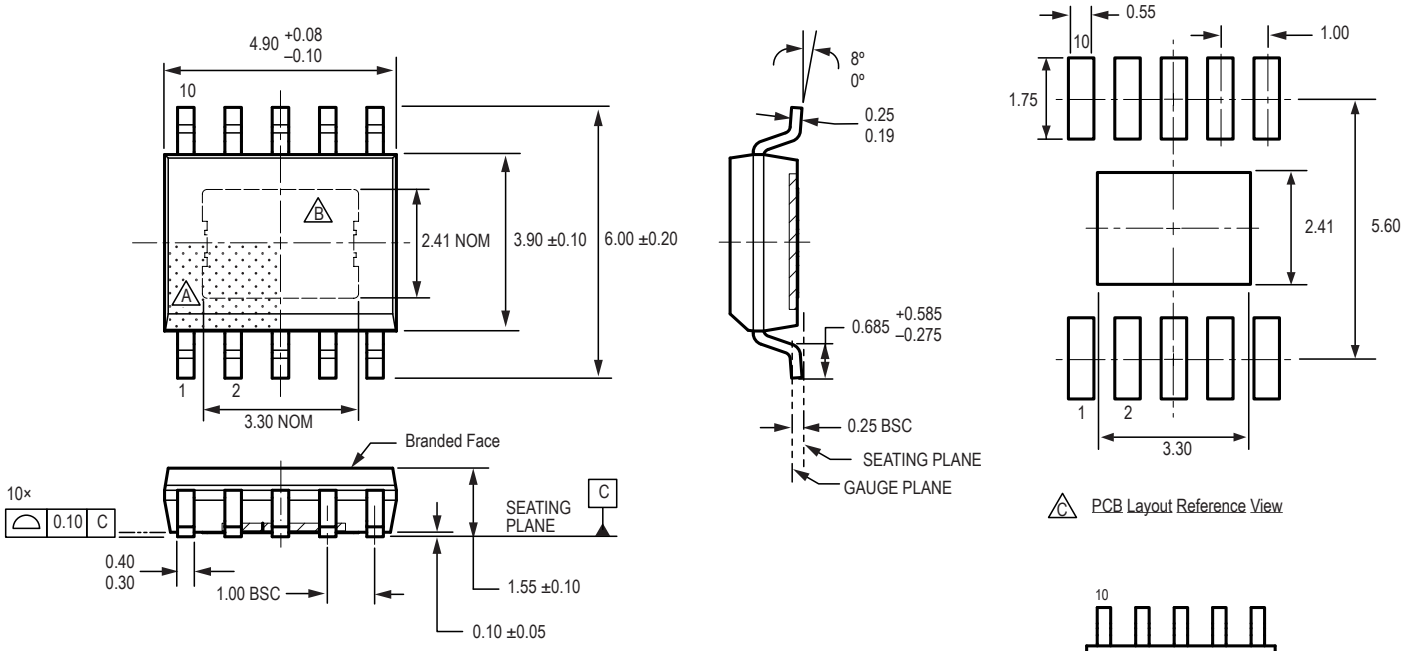
PACKAGE OUTLINE DRAWINGS

For Reference Only – Not for Tooling Use

(Reference DWG-0000380, Rev. 1)
NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



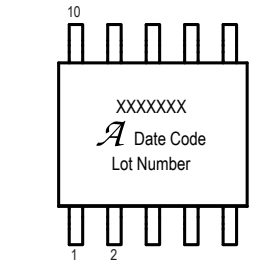
A Terminal #1 mark area

B Exposed thermal pad (bottom surface)

C Reference land pattern layout; all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Branding scale and appearance at supplier discretion

C PCB Layout Reference View



D Standard Branding Reference View

Line 1, 2: Maximum 7 characters per line
Line 3: Maximum 5 characters

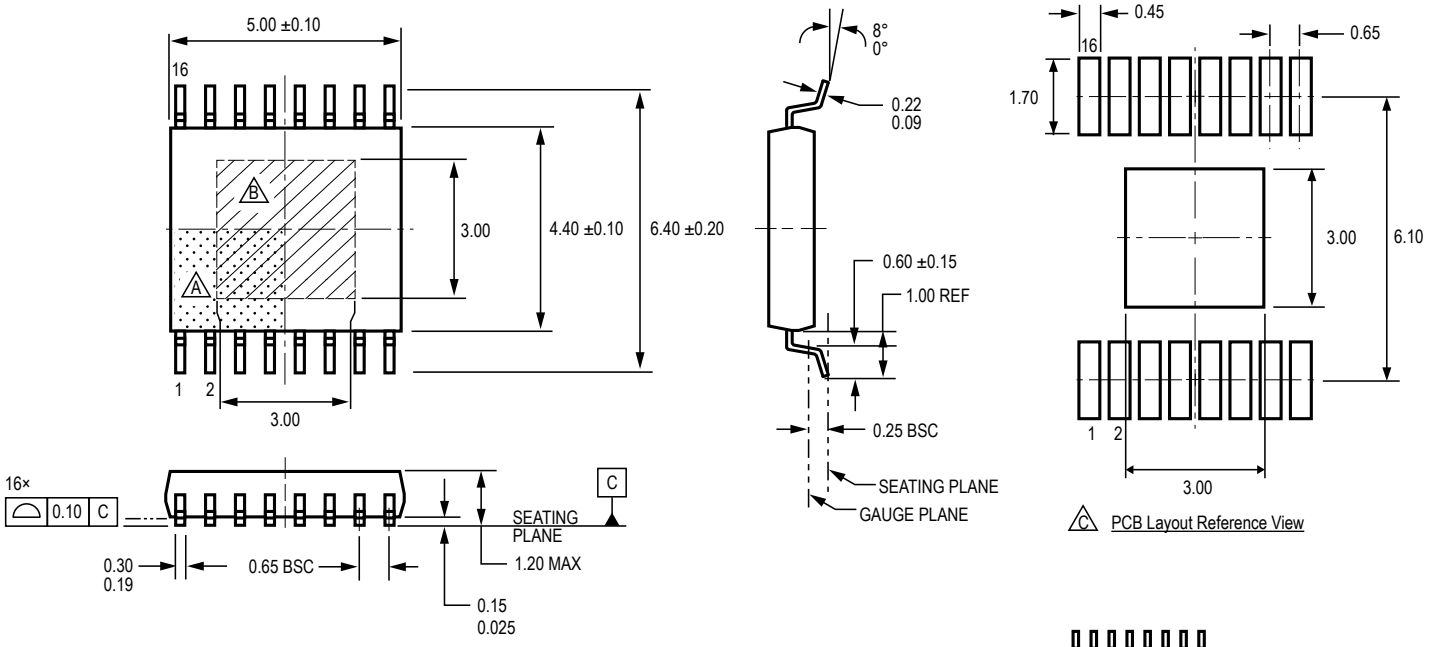
Line 1: Part Number
Line 2: Logo A, 4-digit Date Code
Line 3: Characters 5, 6, 7, 8 of Assembly Lot Number

Package LK, 10-Pin SOICN with Exposed Thermal Pad

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

For Reference Only – Not for Tooling Use

(Reference JEDEC MO-153 ABT; Allegro DWG-0000379, Rev. 3)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Exposed thermal pad (bottom surface)

C Reference land pattern layout (reference IPC7351 SOP65P640X110-17M); All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Branding scale and appearance at supplier discretion

D Standard Branding Reference View

Line 1, 2 = 7 characters
Line 3 = 5 characters

Line 1: Part Number
Line 2: Logo A, 4 digit Date Code
Line 3: Characters 5, 6, 7, 8 of Assembly Lot Number

Package LP, 16-Pin TSSOP with Exposed Thermal Pad

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Revision History

Number	Date	Description
–	September 23, 2015	Initial release
1	March 17, 2016	Added Load Current Sense Regulation Threshold footnote (page 7-8); updated Additional Notes on Ripple Current (page 15).
2	April 6, 2016	Added Parallel Operation figure (page 19) and SBD Protection figure (page 20); updated Protection from Output LC-Resonance (page 19); corrected LK package drawing dimension (page 23).
3	June 17, 2016	Updated k value (page 11).
4	November 1, 2016	Updated Functional Description (page 11); added Table of Contents.
5	June 1, 2020	Updated LK package drawing and minor editorial updates
6	December 1, 2020	Updated CSH and CSL Input Sense Current test conditions (page 7) and Functional Description (page 11) to clarify that R_{adj} should only be used when $V_{OUT} \geq 5$ V.
7	March 5, 2021	Corrected Switching Voltage absolute maximum ratings (page 3) and other minor editorial updates.
8	March 18, 2022	Updated package drawing (page 24)

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