LM5067 Negative Hot Swap / Inrush Current Controller with Power Limiting

1 Features

- Wide operating range: –9 V to –80 V
- In-rush current limit for safe board insertion into live power sources
- Programmable maximum power dissipation in the external pass device
- Adjustable current limit
- Circuit breaker function for severe overcurrent events
- Adjustable undervoltage lockout (UVLO) and hysteresis
- Adjustable overvoltage lockout (OVLO) and hysteresis
- Initial insertion timer allows ringing and transients to subside after system connection
- Programmable fault timer avoids nuisance trips
- Active high open drain POWER GOOD output
- Available in latched fault and automatic restart versions

2 Applications

- Server backplane systems
- In-Rush current limiting
- Solid state circuit breaker
- Transient voltage protector
- Solid state relay
- Undervoltage lock-out
- Power good detector and indicator

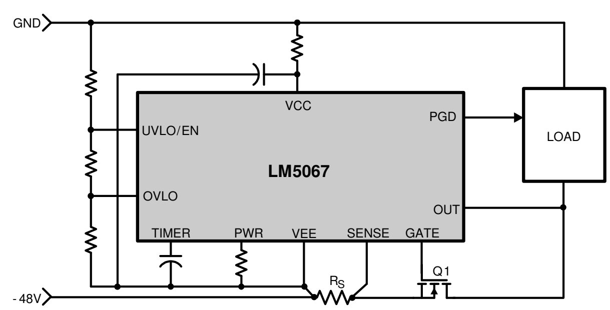
3 Description

The LM5067 negative hot swap controller provides intelligent control of the power supply connections during insertion and removal of circuit cards from a live system backplane or other "hot" power sources. The LM5067 provides in-rush current control to limit system voltage droop and transients. The current limit and power dissipation in the external series pass N-Channel MOSFET are programmable, ensuring operation within the Safe Operating Area (SOA). In addition, the LM5067 provides circuit protection by monitoring for over-current and over-voltage conditions. The POWER GOOD output indicates when the output voltage is close to the input voltage. The input under-voltage and over-voltage lockout levels and hysteresis are programmable, as well as the fault detection time. The LM5067-1 latches off after a fault detection, while the LM5067-2 automatically attempts restarts at a fixed duty cycle. The LM5067 is available in a 10-pin VSSOP package and a 14-pin SOIC package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM5067	VSSOP (10)	3.00 mm x 3.00 mm
	SOIC (14)	8.99 mm x 7.49 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.



Negative Power Bus In-Rush and Fault Protection

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4 Revision History

Changes from Revision C (March 2013) to Revision D (August 2020) **Page**

- Added *ESD Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1
- Updated the numbering format for tables, figures and cross-references throughout the document.................. 1
- Updated *Applications* section.................. 1
- Deleted text : "LM5067A is available..." 1

Changes from Revision B (September 2009) to Revision C (March 2013) **Page**

- Changed layout of National Data Sheet to TI format.................. 30

5 Device Comparison

Table 5-1. Device Comparison Table

DEVICE NUMBER	RETRY BEHAVIOR AFTER FAULT	PACKAGE
LM5067-1	Latch-off	VSSOP (10), SOIC (14)
LM5067-2	Auto-retry	VSSOP (10), SOIC (14)

6 Pin Configuration and Functions

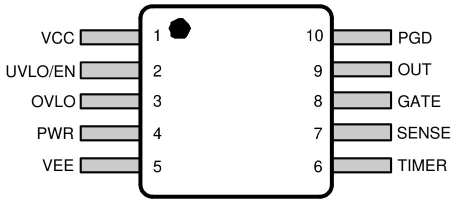

Figure 6-1. 10-Lead VSSOP Top View

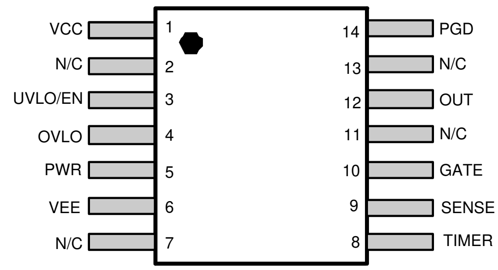

Figure 6-2. 14-Lead SOIC Top View

Pin Functions

Name	Pin		I/O	Description
	VSSOP-10	SOIC-14		
VCC	1	1	I	Positive supply input: Connect to system ground through a resistor. Connect a bypass capacitor to VEE. The voltage from VCC to VEE is nominally 13 V set by an internal zener diode.
UVLO/EN	2	3	I	Under-voltage lockout: An external resistor divider from the system input voltage sets the under-voltage turn-on threshold. The enable threshold at the pin is 2.5 V above VEE. An internal 22 µA current source provides hysteresis. This pin can be used for remote enable and disable.
OVLO	3	4	I	Overvoltage lockout: An external resistor divider from the system input voltage sets the overvoltage turn-off threshold. The disable threshold at the pin is 2.5 V above VEE. An internal 22 µA current source provides hysteresis.
PWR	4	5	I	Power limit set: An external resistor at this pin, in conjunction with the current sense resistor (R_S), sets the maximum power dissipation in the external series pass MOSFET.
VEE	5	6	I	Negative supply input: Connect to the system negative supply voltage (typically -48V).
TIMER	6	8	I/O	Timing capacitor: An external capacitor at this pin sets the insertion time delay and the fault timeout period. The capacitor also sets the restart timing of the LM5067-2.
SENSE	7	9	I	Current sense input: The voltage across the current sense resistor (R_S) is measured from VEE to this pin. If the voltage across R_S reaches 50 mV the load current is limited and the fault timer activates.
GATE	8	10	O	Gate drive output: Connect to the external N-channel MOSFET's gate.
OUT	9	12	I	Output feedback: Connect to the external MOSFET's drain. Internally used to determine the MOSFET V_{DS} voltage for power limiting, and to control the PGD output pin.
PGD	10	14	0	Power Good indicator: An open drain output capable of sustaining 80 V when off. When the external MOSFET V_{DS} decreases below 1.23 V the PGD pin switches high. When the external MOSFET V_{DS} increases above ≅2.5 V the PGD pin switches low.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [(1)]

		MIN	MAX	UNIT
Input voltage	OUT, PGD to VEE	–0.3	100	V
	UVLO, OVLO to VEE	–0.3	17	V
	SENSE to VEE	–0.3	0.3	V
Current	Into VCC (100 µs pulse)		100	mA
Junction Temperature			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (LM50672NPA variant)[(1)]	±1750	V
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (all other variants)[(1)]	±2000	
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[(2)]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Current into VCC [(1)]	2			mA
OUT Voltage above VEE	0		80	V
PGD Off Voltage above VEE	0		80	V
Junction Temperature	−40		125	°C

(1) Maximum continuous current into VCC is limited by power dissipation and die temperature. See the Thermal Considerations section.

7.4 Thermal Information

THERMAL METRIC[(1) (2)]		LM5067		UNIT
		VSSOP	SOIC	
		10 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	94	90	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance	44	27	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.
(2) Tested on a 4 layer JEDEC board with 2 vias under the package. See JEDEC standards JESD51-7 and JESD51-3. See the Thermal Considerations section.

7.5 Electrical Characteristics

Limits in standard type are for T_J = 25°C only; limits in boldface type apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: I_{CC} = 2 mA, OUT Pin = 48V above VEE, all voltages are with respect to VEE. See [(1)].

PARAMETER		TETS CONDITIONS	MIN	TYP	MAX	UNIT
Input						
V_Z	Operating voltage, VCC – VEE	I_{CC} = 2 mA, UVLO = 5V	**12.35**	13	**13.65**	V
I_{CC-EN}	Internal operating current, enabled	VCC-VEE = 11V, UVLO = 5V		0.8	**1**	mA
I_{CC-DIS}	Internal operating current, disabled	VCC-VEE = 11V, UVLO = 2V		480	**660**	µA
POR_{IT}	Threshold voltage to start insertion timer	VCC-VEE increasing		7.7	**8.2**	V
POR_{EN}	Threshold voltage to enable all functions	VCC-VEE increasing		8.4	**8.7**	V
POR_{EN-HYS}	POR_{EN} hysteresis	VCC-VEE decreasing		125		mV
OUT Pin						
I_{OUT-EN}	OUT bias current, enabled	OUT = VEE, Normal operation		0.1		µA
$I_{OUT-DIS}$	OUT bias current, disabled	Disabled, OUT = VEE + 48V		50		
SENSE Pin						
I_{SNS-EN}	SENSE bias current, enabled	OUT = VEE, Normal operation		-6		µA
$I_{SNS-DIS}$	SENSE bias current, disabled	Disabled, OUT = VEE + 48V		-50		
UVLO, OVLO Pins						
$UVLO_{TH}$	UVLO threshold		**2.45**	2.5	**2.55**	V
$UVLO_{HYS}$	UVLO hysteresis current	UVLO = VEE + 2V	**10**	22	**34**	µA
$UVLO_{BIAS}$	UVLO bias current	UVLO = VEE + 5V			**1**	µA
$OVLO_{TH}$	OVLO threshold		**2.43**	2.5	**2.57**	V
$OVLO_{HYS}$	OVLO hysteresis current	OVLO = VEE+2.8V	**-34**	-22	**-10**	µA
$OVLO_{BIAS}$	OVLO bias current	OVLO = VEE + 2.4V			**1**	µA
Gate Control (GATE Pin)						
I_{GATE}	Source current	Normal Operation	**-72**	-52	**-32**	µA
	Sink current	UVLO < 2.5V	**1.9**	2.2	**2.68**	mA
		SENSE - VEE =150 mV or VCC - VEE < POR_{IT}, V_{GATE} = 5V	**45**	110	**200**	
V_{GATE}	Gate output voltage in normal operation	GATE-VEE voltage		V_Z		V
Current Limit						
V_{CL}	Threshold voltage	SENSE - VEE voltage	**44**	50	**56**	mV
Circuit Breaker						
V_{CB}	Threshold voltage	SENSE - VEE voltage	**70**	100	**130**	mV
Power Limit (PWR Pin)						
PWR_{LIM}	Power limit sense voltage (SENSE - VEE)	OUT - SENSE = 24V, R_{PWR} = 75 kΩ	**16.5**	22	**27.5**	mV
I_{PWR}	PWR pin current	V_{PWR} = 2.5V		-23		µA
Timer (TIMER Pin)						
V_{TMRH}	Upper threshold		**3.76**	4	**4.16**	V
V_{TMRL}	Lower threshold	Restart cycles (LM5067-2)	**1.18**	1.25	**1.32**	V
		End of 8th cycle (LM5067-2)		0.3		V
		Re-enable threshold (LM5067-1)		0.3		V
I_{TIMER}	Insertion time current	TIMER pin = 2V	**-9.5**	-6	**-2.5**	µA
	Sink current, end of insertion time	TIMER pin = 2V	**1.2**	1.55	**1.9**	mA
	Fault detection current	TIMER pin = 2V	**-140**	-95	**-44**	µA
	Sink current, end of fault time		**0.9**	2.5	**4.25**	µA
DC_{FAULT}	Fault Restart Duty Cycle	LM5067-2		0.5%		
Power Good (PGD Pin)						

7.5 Electrical Characteristics (continued)

Limits in standard type are for T_J = 25°C only; limits in boldface type apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: I_{CC} = 2 mA, OUT Pin = 48V above VEE, all voltages are with respect to VEE. See [(1)].

PARAMETER		TETS CONDITIONS	MIN	TYP	MAX	UNIT
PGD_{TH}	Threshold measured at OUT - SENSE	Decreasing	**1.162**	1.23	**1.285**	V
		Increasing, relative to decreasing threshold	**1.143**	1.25	1.325	
PGD_{VOL}	Output low voltage	I_{SINK} = 2 mA		60	**150**	mV
PGD_{IOH}	Off leakage current	V_{PGD} = 80V			**5**	µA

(1) Current out of a pin is indicated as a negative value.

7.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
UVLO, OVLO Pins						
$UVLO_{DEL}$	UVLO hysteresis current	Delay to GATE high		26		µs
		Delay to GATE low		12		µs
$OVLO_{DEL}$	OVLO delay	Delay to GATE high		26		µs
		Delay to GATE low		12		µs
Current Limit						
t_{CL}	Response time	SENSE - VEE stepped from 0 mV to 80 mV		25		µs
Circuit Breaker						
t_{CB}	Response time	SENSE - VEE stepped from 0 mV to 150 mV, time to GATE low, no load		0.65	**1.0**	µs
Timer (TIMER Pin)						
t_{FAULT}	Fault to GATE low delay	TIMER pin reaches 4.0V		15		µs

7.7 Typical Characteristics

Unless otherwise specified the following conditions apply: T_J = 25°C.

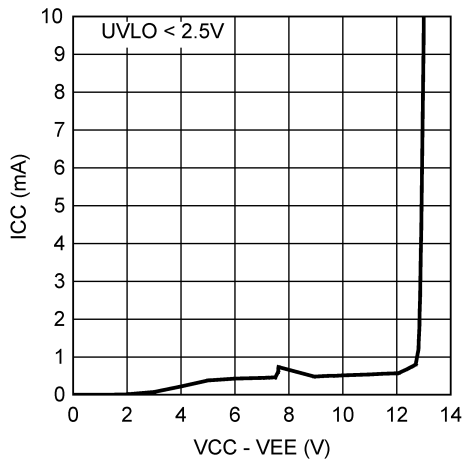

Figure 7-1. ICC vs Operating Voltage - Disabled

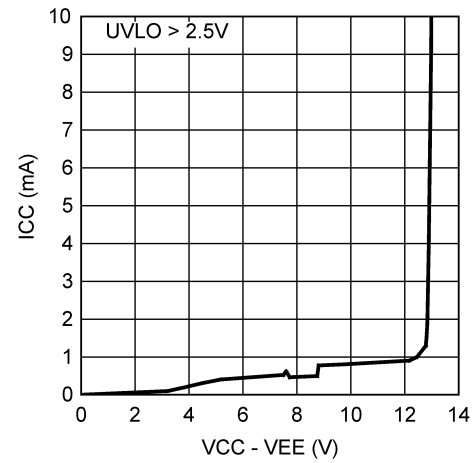

Figure 7-2. ICC vs Operating Voltage - Enabled

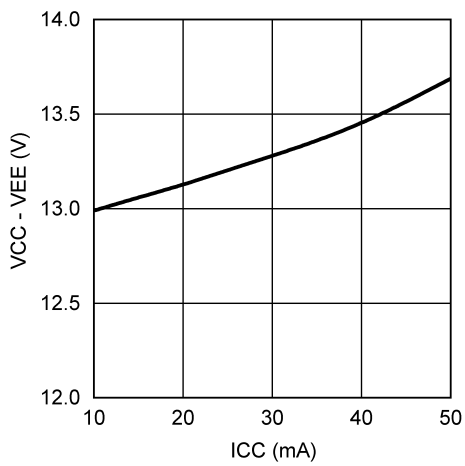

Figure 7-3. Operating Voltage vs ICC

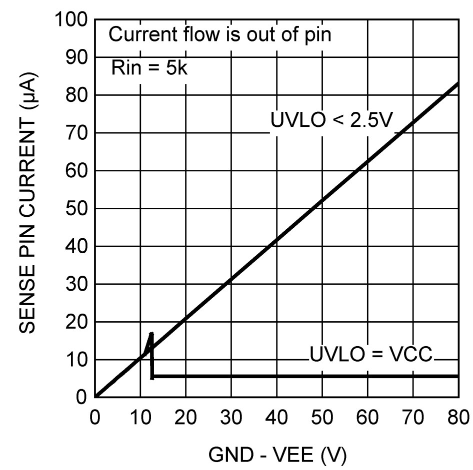

Figure 7-4. SENSE Pin Current vs System Voltage

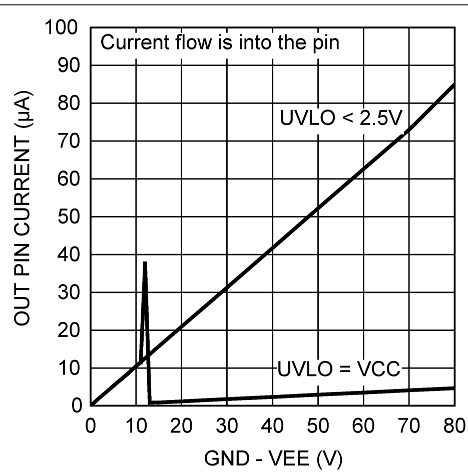

Figure 7-5. OUT Pin Current vs System Voltage

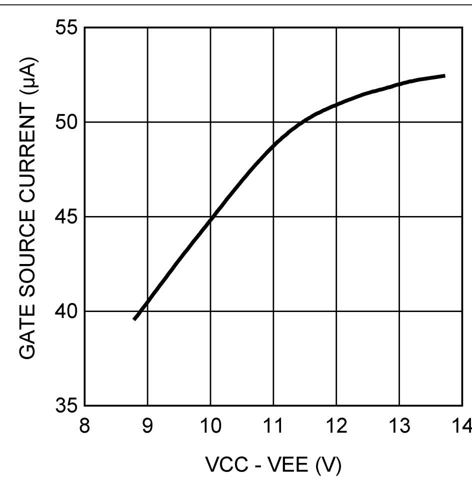

Figure 7-6. GATE Source Current vs Operating Voltage

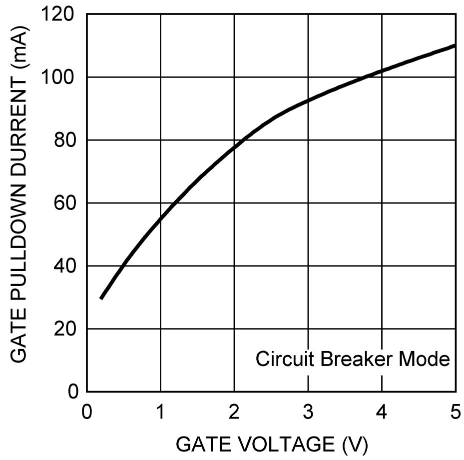

Figure 7-7. GATE Pull-Down Current, Circuit Breaker vs GATE Voltage

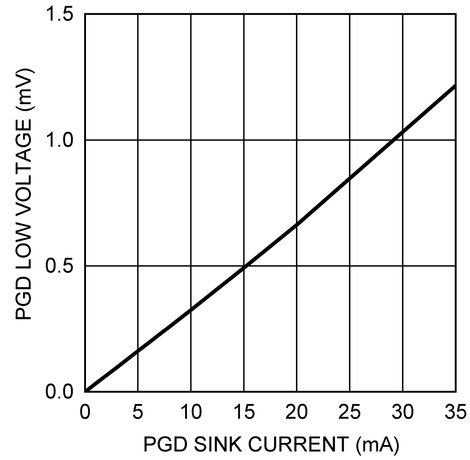

Figure 7-8. PGD Low Voltage vs Sink Current

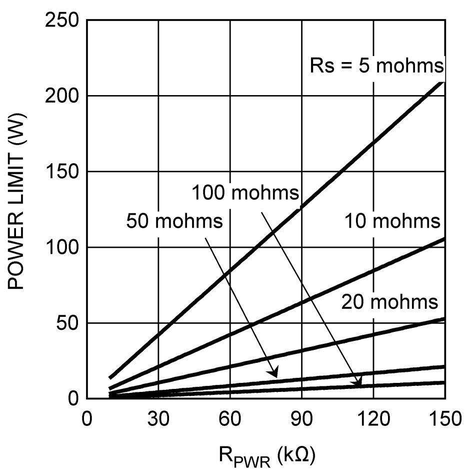

Figure 7-9. MOSFET Power Dissipation Limit vs R_{PWR} and R_S

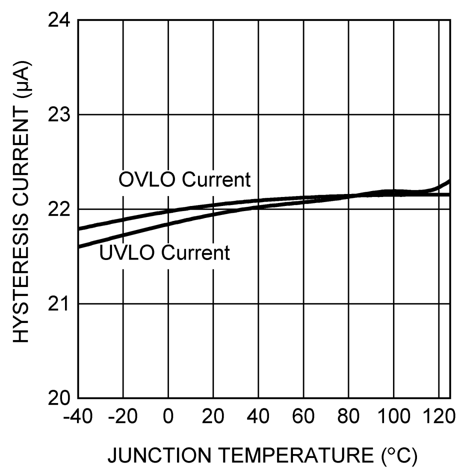

Figure 7-10. UVLO and OVLO Hysteresis Current vs Temperature

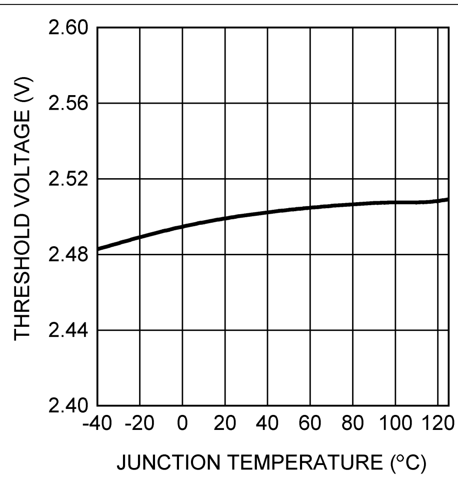

Figure 7-11. UVLO, OVLO Threshold Voltage vs UVLO, OVLO Threshold Voltage

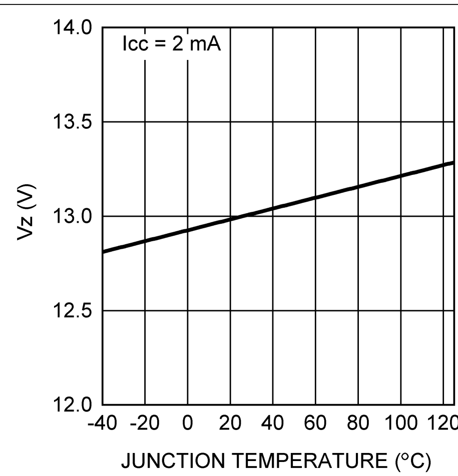

Figure 7-12. V_Z Operating Voltage vs Temperature

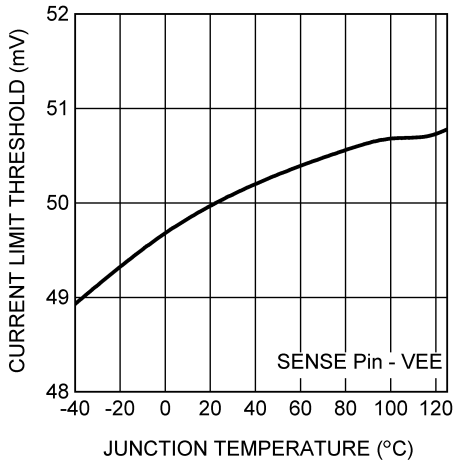

Figure 7-13. Current Limit Threshold vs Temperature

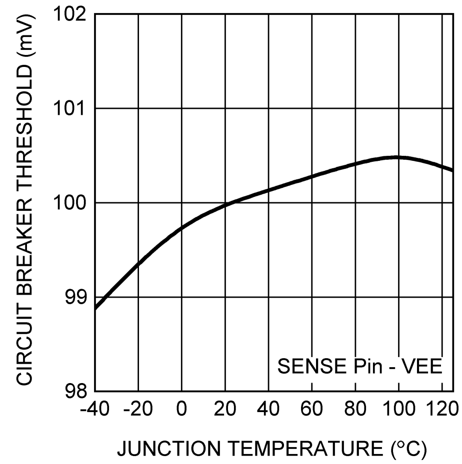

Figure 7-14. Circuit Breaker Threshold vs Temperature

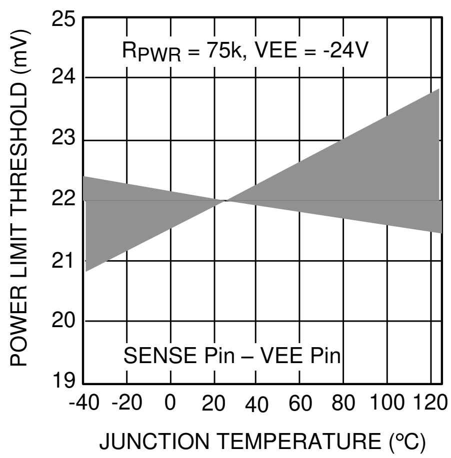

Figure 7-15. Power Limit Threshold vs Temperature

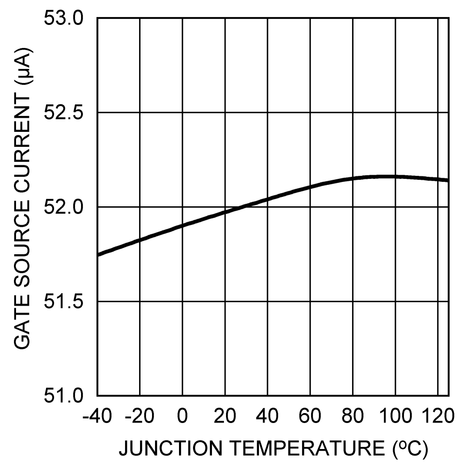

Figure 7-16. Gate Source Current vs Temperature

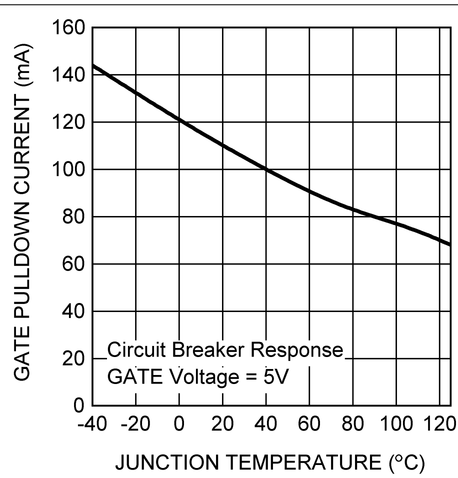

Figure 7-17. GATE Pull-Down Current, Circuit Breaker vs Temperature

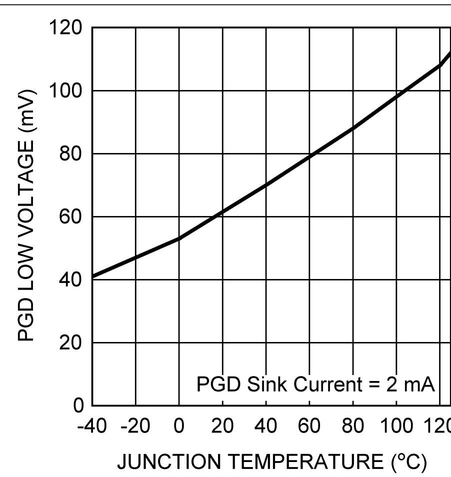

Figure 7-18. PGD Pin Low Voltage vs Temperature

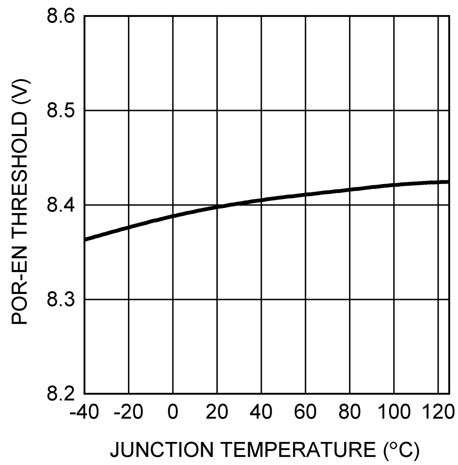

Figure 7-19. POR_{EN} Threshold vs Temperature

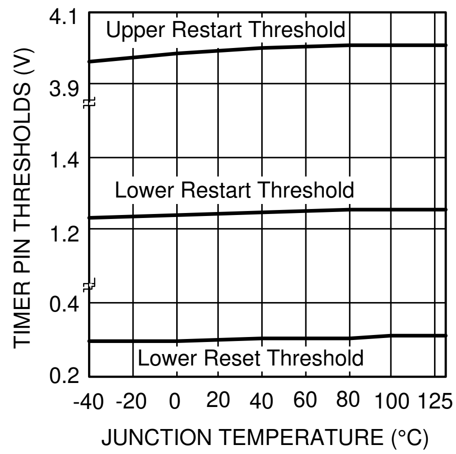

Figure 7-20. TIMER Pin Thresholds vs Temperature

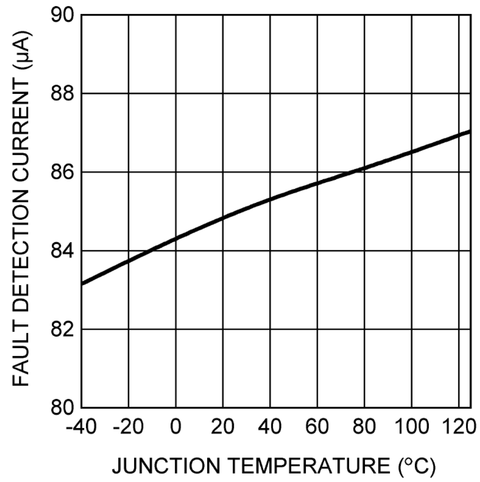

Figure 7-21. TIMER Pin Fault Detection Current vs Temperature

8 Detailed Description

8.1 Overview

The LM5067 is designed to control the in-rush current to the load upon insertion of a circuit card into a live backplane or other “hot” power source, thereby limiting the voltage sag on the backplane’s supply voltage, and the dV/dt of the voltage applied to the load. Effects on other circuits in the system are minimized, preventing possible unintended resets. During the system power up, the maximum power dissipation in the series pass device is limited to a safe value within the device’s Safe Operating Area (SOA). After the system power up is complete, the LM5067 monitors the load for excessive currents due to a fault or short circuit at the load. Limiting the load current and/or the power in the external MOSFET for an extended period of time results in the shutdown of the series pass MOSFET. After a fault event, the LM5067-1 latches off until the circuit is re-enabled by external control, while the LM5067-2 automatically restarts with defined timing. The circuit breaker function quickly switches off the series pass device upon detection of a severe over-current condition caused by, e.g. a short circuit at the load. The Power Good (PGD) output pin indicates when the output voltage is close to the normal operating value. Programmable undervoltage lock-out (UVLO) and overvoltage lock-out (OVLO) circuits shut down the LM5067 when the system input voltage is outside the desired operating range. The typical configuration of a circuit card with LM5067 hot swap protection is shown in Figure 8-1.

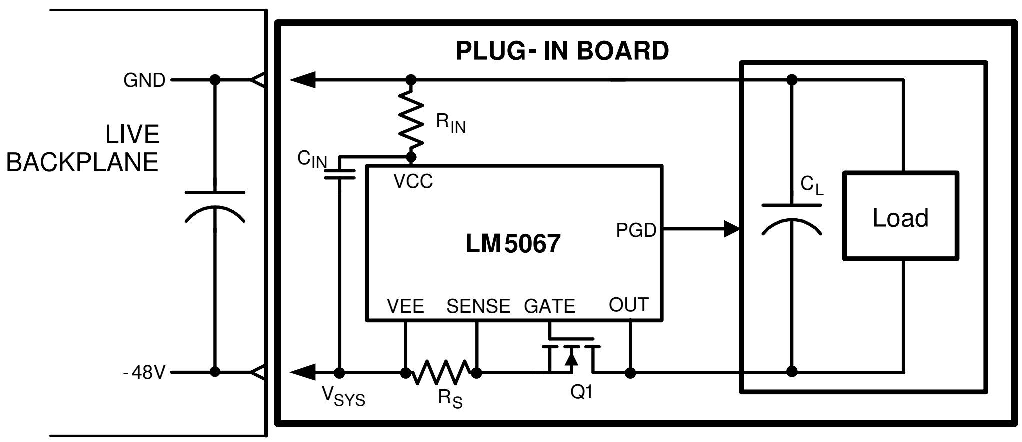

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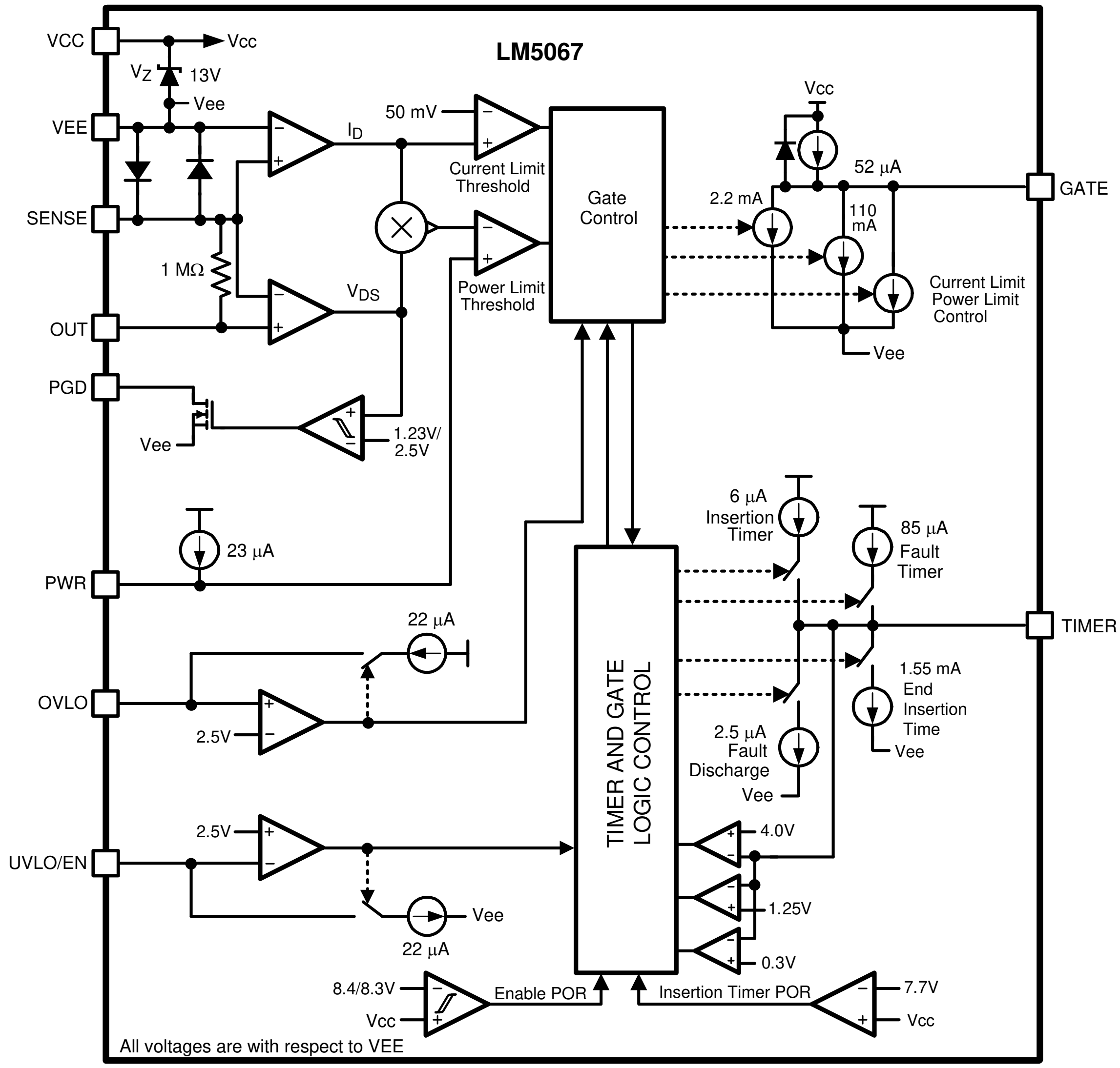
Figure 8-1. LM5067 Application

The LM5067 can be used in a variety of applications, other than plug-in boards, to monitor for excessive load current, provide transient protection, and ensuring the voltage to the load is within preferred limits. The circuit breaker function protects the system from a sudden short circuit at the load. Use of the UVLO/EN pin allows the LM5067 to be used as a solid state relay. The PGD output provides a status indication of the voltage at the load relative to the input system voltage.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Power Up Sequence

The system voltage range of the LM5067 is –9 V to –80 V, with a transient capability to -100 V. Referring to the *Functional Block Diagram*, Figure 9-1, and Figure 8-2, as the system voltage (V_{SYS}) initially increases from zero, the external N-channel MOSFET (Q1) is held off by an internal 110 mA pull-down current at the GATE pin. The strong pull-down current at the GATE pin prevents an inadvertent turn-on as the MOSFET's gate-to-drain (Miller) capacitance is charged. When the operating voltage of the LM5067 (VCC – VEE) reaches the POR_{IT} threshold (7.7V) the insertion timer starts. During the insertion time, the capacitor at the TIMER pin (C_T) is charged by a 6 µA current source, and Q1 is held off by a 2.2 mA pull-down current at the GATE pin regardless of the system voltage. The insertion time delay allows ringing and transients at V_{SYS} to settle before Q1 can be enabled. The insertion time ends when the TIMER pin voltage reaches 4 V above VEE, and C_T is then quickly discharged by an internal 1.5 mA pull-down current. After the insertion time, the LM5067 control circuitry is enabled when the operating voltage reaches the POR_{EN} threshold (8.4 V). As V_{SYS} continues to increase, the LM5067 operating voltage is limited at ≅13 V by an internal zener diode. The remainder of the system voltage is dropped across the input resistor R_{IN}.

The GATE pin switches on Q1 when V_{SYS} exceeds the UVLO threshold (UVLO pin >2.5V above VEE). If V_{SYS} exceeds the UVLO threshold at the end of the insertion time, Q1 is switched on at that time. The GATE pin sources 52 µA to charge Q1's gate capacitance. The maximum gate-to-source voltage of Q1 is limited by the LM5067's operating voltage (V_Z) to approximately 13 V. During power up, as the voltage at the OUT pin increases in magnitude with respect to Ground, the LM5067 monitors Q1's drain current and power dissipation. In-rush current limiting and/or power limiting circuits actively control the current delivered to the load. During the in-rush limiting interval (t2 in Figure 8-2) an internal current source charges C_T at the TIMER pin. When the load current reduces from the limiting value to a value determined by the load the in-rush limiting interval is complete and C_T is discharged. The PGD pin switches high when the voltage at the OUT pin reaches to within 1.25 V of the voltage at the SENSE pin.

If the TIMER pin voltage reaches 4.0V before in-rush current limiting or power limiting ceases (during t2), a fault is declared and Q1 is turned off. See *Fault Timer and Restart* for a complete description of the fault mode.

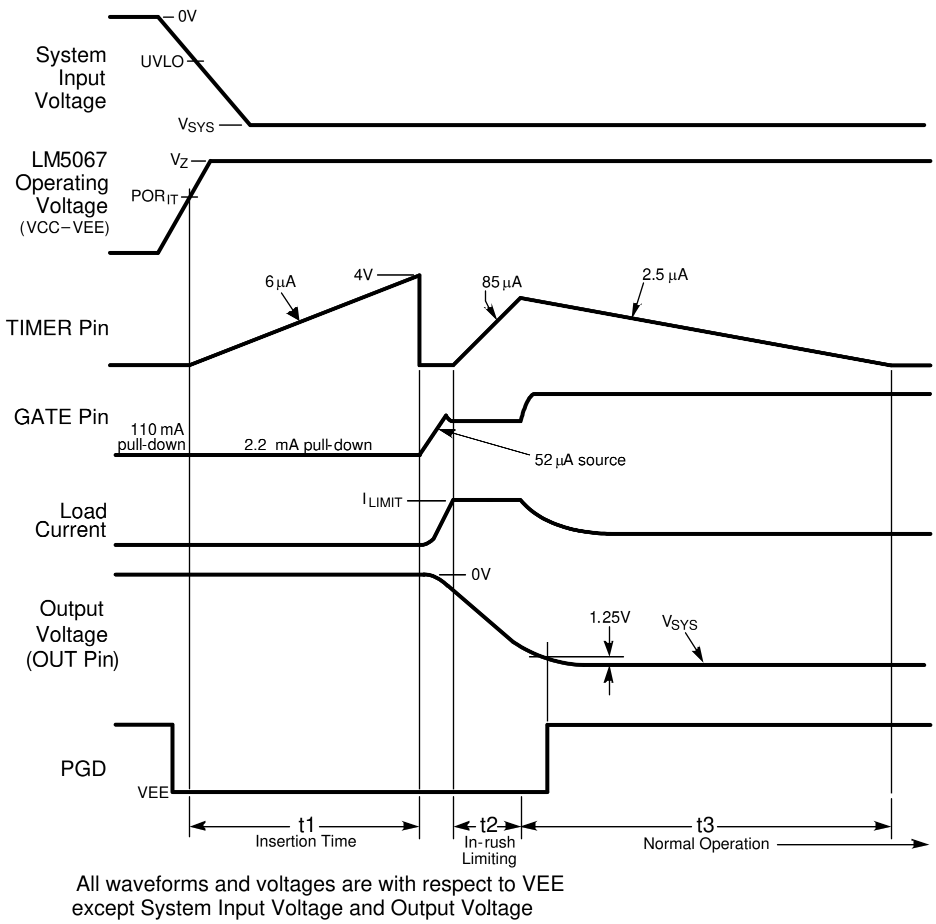


Figure 8-2. Power Up Sequence (Current Limit only)

8.3.2 Gate Control

The external N-channel MOSFET is turned on when the GATE pin sources 52 µA to enhance the gate. During normal operation (t3 in Figure 8-2) Q1's gate is held charged to approximately 13V above VEE, typically within 20 mV of the voltage at VCC. If the maximum V_{GS} rating of Q1 is less than 13V, a lower voltage external zener diode must be added between the GATE and SENSE pins. The external zener diode must have a forward current rating of at least 110 mA.

When the system voltage is initially applied (before the operating voltage reaches the POR_{IT} threshold), the GATE pin is held low by a 110 mA pull-down current. The pull-down current helps prevent an inadvertent turn-on of the MOSFET through its drain-gate capacitance as the applied system voltage increases.

During the insertion time (t1 in Figure 8-2) the GATE pin is held low by a 2.2 mA pull-down current. This maintains Q1 in the off-state until the end of t1, regardless of the voltage at VCC and UVLO.

Following the insertion time, during t2 in Figure 8-2, the gate voltage of Q1 is modulated to keep the current or Q1's power dissipation level from exceeding the programmed levels. Current limiting and power limiting are considered fault conditions, during which the voltage on the TIMER pin capacitor increases. If the current and power limiting cease before the TIMER pin reaches 4 V the TIMER pin capacitor is discharged, and the circuit enters normal operation. See *Fault Timer and Restart* for details on the fault timer.

If the system input voltage falls below the UVLO threshold, or rises above the OVLO threshold, the GATE pin is pulled low by the 2.2 mA pull-down current to switch off Q1.

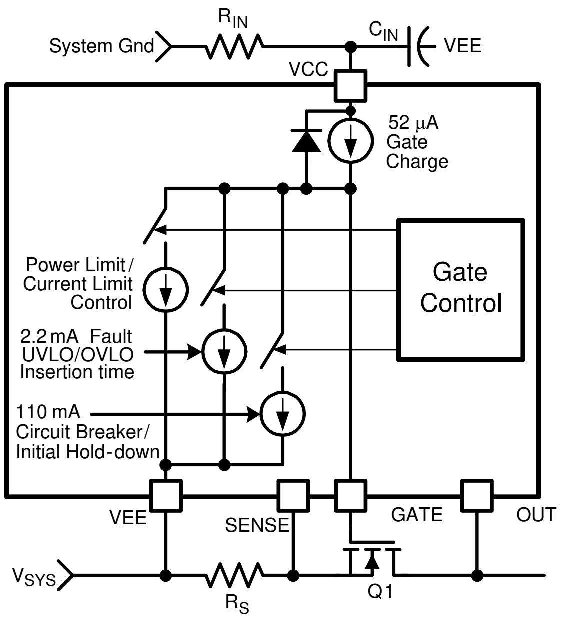


Figure 8-3. Gate Control

8.3.3 Current Limit

The current limit threshold is reached when the voltage across the sense resistor R_S (SENSE to VEE) reaches 50 mV. In the current limiting condition, the GATE voltage is controlled to limit the current in MOSFET Q1. While the current limit circuit is active, the fault timer is active as described in the *Section 8.3.6* section. If the load current reduces below the current limit threshold before the end of the Fault Timeout Period, the LM5067 resumes normal operation. For proper operation, the R_S resistor value should be no larger than 100 mΩ.

8.3.4 Circuit Breaker

If the load current increases rapidly (e.g., the load is short-circuited) the current in the sense resistor (R_S) may exceed the current limit threshold before the current limit control loop is able to respond. If the current exceeds approximately twice the current limit threshold (100 mV/R_S), Q1's gate is quickly pulled down by the 110 mA pull-down current at the GATE pin, and a Fault Timeout Period begins. When the voltage across R_S falls below 100 mV the 110 mA pull-down current at the GATE pin is switched off, and the gate voltage of Q1 is then determined by the current limit or the power limit functions. If the TIMER pin reaches 4.0V before the current limiting or power limiting condition ceases, Q1 is switched off by the 2.2 mA pull-down current at the GATE pin as described in the Fault Timer & Restart section.

8.3.5 Power Limit

An important feature of the LM5067 is the MOSFET power limiting. The Power Limit function can be used to maintain the maximum power dissipation of MOSFET Q1 within the device SOA rating. The LM5067 determines the power dissipation in Q1 by monitoring its drain-source voltage (OUT to SENSE), and the drain current through the sense resistor (SENSE to VEE). The product of the current and voltage is compared to the power limit threshold programmed by the resistor at the PWR pin. If the power dissipation reaches the limiting threshold, the GATE voltage is modulated to reduce the current in Q1, and the fault timer is active as described in the *Fault Timer and Restart* section.

8.3.6 Fault Timer and Restart

When the current limit or power limit threshold is reached during turn-on or as a result of a fault condition, the gate-to-source voltage of Q1 is modulated to regulate the load current and power dissipation in Q1. When either limiting function is active, an 85 µA fault timer current source charges the external capacitor (C_T) at the TIMER pin as shown in Figure 8-5 (Fault Timeout Period). If the fault condition subsides before the TIMER pin reaches 4.0V, the LM5067 returns to the normal operating mode and C_T is discharged by the 2.5 µA current sink. If the TIMER pin reaches 4.0V during the Fault Timeout Period, Q1 is switched off by a 2.2 mA pull-down current at the GATE pin. The subsequent restart procedure depends on which version of the LM5067 is in use.

The LM5067-1 latches the GATE pin low at the end of the Fault Timeout Period, and C_T is discharged by the 2.5 µA fault current sink. The GATE pin is held low until a power up sequence is externally initiated by cycling the input voltage (V_{SYS}), or momentarily pulling the UVLO/EN pin within 2.5V of VEE with an open-collector or open-drain device as shown in Figure 8-4. The voltage across C_T must be <0.3V for the restart procedure to be effective.

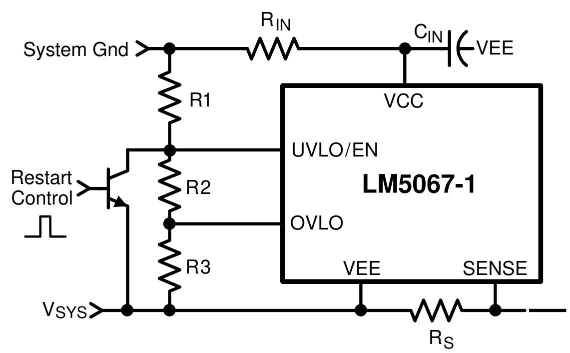


Figure 8-4. Latched Fault Restart Control

The LM5067-2 provides an automatic restart sequence which consists of the TIMER pin cycling between 4 V and 1.25 V seven times after the Fault Timeout Period, as shown in Figure 8-5. The period of each cycle is determined by the 85 µA charging current, and the 2.5 µA discharge current, and the value of the capacitor C_T. When the TIMER pin reaches 0.3 V during the eighth high-to-low ramp, the 52 µA current source at the GATE pin turns on Q1. If the fault condition is still present, the Fault Timeout Period and the restart cycle repeat.

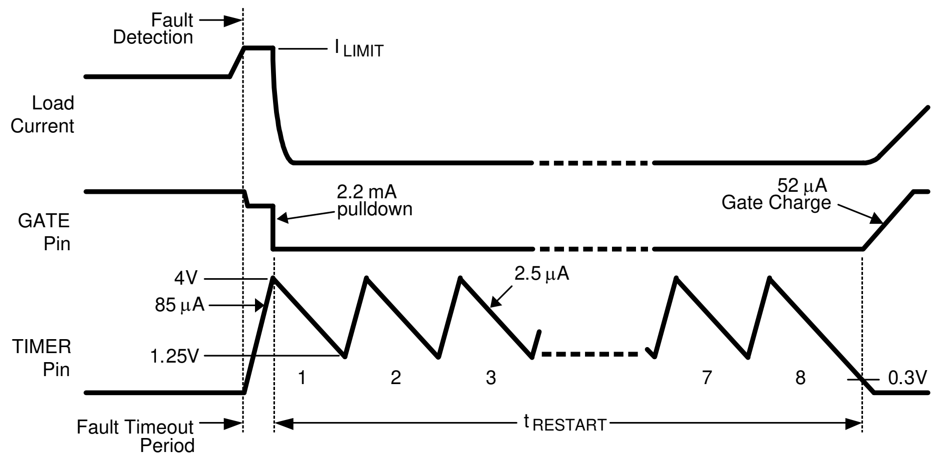


Figure 8-5. Restart Sequence (LM5067-2)

8.3.7 Undervoltage Lock-Out (UVLO)

The series pass MOSFET (Q1) is enabled when the input supply voltage (V_{SYS}) is within the operating range defined by the programmable undervoltage lockout (UVLO) and overvoltage lock-out (OVLO) levels. Typically the UVLO level at V_{SYS} is set with a resistor divider (R1-R3) as shown in Figure 9-1. When V_{SYS} is less than the UVLO level, the internal 22 µA current sink at UVLO/EN is enabled, the current source at OVLO is off, and Q1 is held off by the 2.2 mA pull-down current at the GATE pin. V_{SYS} reaches its UVLO level when the voltage at the UVLO/EN pin reaches 2.5V above VEE. Upon reaching the UVLO level, the 22 µA current sink at the UVLO/EN pin is switched off, increasing the voltage at the pin, providing hysteresis for this threshold. With the UVLO/EN pin above 2.5V, Q1 is switched on by the 52 µA current source at the GATE pin.

See *Application Information* for a procedure to calculate the values of the threshold setting resistors (R1-R3). The minimum possible UVLO level can be set by connecting the UVLO/EN pin to VCC. In this case Q1 is enabled when the operating voltage (VCC – VEE) reaches the POR_{EN} threshold (8.4V).

8.3.8 Overvoltage Lock-Out (OVLO)

The series pass MOSFET (Q1) is enabled when the input supply voltage (V_{SYS}) is within the operating range defined by the programmable undervoltage lockout (UVLO) and overvoltage lock-out (OVLO) levels. Typically the OVLO level at V_{SYS} is set with a resistor divider (R1-R3) as shown in Figure 9-1. If V_{SYS} raises the OVLO pin voltage more than 2.5 V above VEE Q1 is switched off by the 2.2 mA pull-down current at the GATE pin, denying power to the load. When the OVLO pin is above 2.5 V, the internal 22 µA current source at OVLO is switched on, raising the voltage at OVLO and providing threshold hysteresis. When the voltage at the OVLO pin is reduced below 2.5 V the 22 µA current source is switched off, and Q1 is enabled. See Figure 9-1 for a procedure to calculate the threshold setting resistor values.

8.3.9 Power Good Pin

The Power Good output indicator pin (PGD) is connected to the drain of an internal N-channel MOSFET. An external pull-up resistor is required at PGD to an appropriate voltage to indicate the status to downstream circuitry. The off-state voltage at the PGD pin must be more positive than VEE, and can be up to 80V above VEE with transient capability to 100 V. PGD is switched high at the end of the turn-on sequence when the voltage from OUT to SENSE (the external MOSFET's V_{DS}) decreases below 1.23 V. PGD switches low if the MOSFET's V_{DS} increases past 2.5 V, if the system input voltage goes below the UVLO threshold or above the OVLO threshold, or if a fault is detected. The PGD output is high when the operating voltage (VCC-VEE) is less than 2 V.

8.4 Device Functional Modes

8.4.1 Shutdown / Enable Control

Figure 8-6 shows how to use the UVLO/EN pin for remote shutdown and enable control. Taking the UVLO/EN pin below its 2.5V threshold (with respect to VEE) shuts off the load current. Upon releasing the UVLO/EN pin the LM5067 switches on the load current with in-rush current and power limiting. In Figure 8-7 the OVLO pin is used for remote shutdown and enable control. When the external transistor is off, the OVLO pin is above its 2.5 V threshold (with respect to VEE) and the load current is shut off. Turning on the external transistor allows the LM5067 to switch on the load current with in-rush current and power limiting.

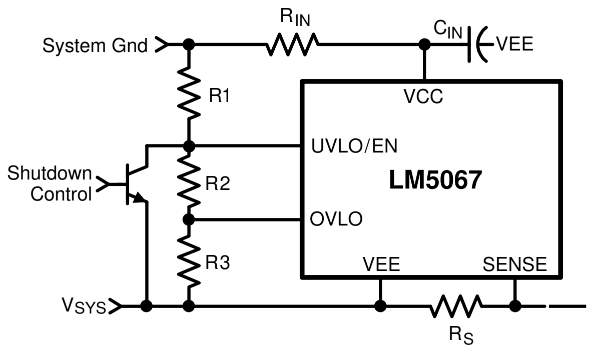


Figure 8-6. Shutdown/Enable Using the UVLO/EN Pin

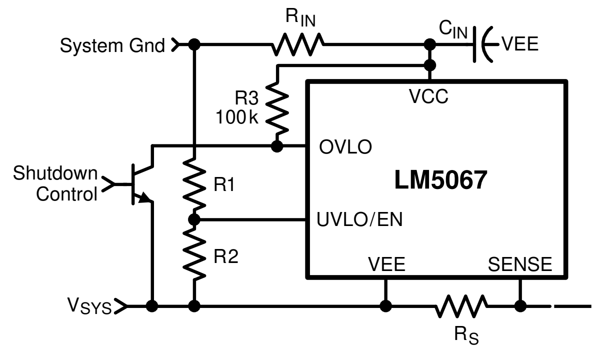


Figure 8-7. Shutdown/Enable Using the OVLO Pin

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The LM5067 is a hotswap controller which is used to manage inrush current and protect in case of faults.

When designing a hotswap, three key scenarios should be considered:

- Start-up
- Output of a hotswap is shorted to ground when the hotswap is on. This is often referred to as a hot-short.
- Powering-up a board when the output and ground are shorted. This is usually called a start-into-short.

All of these scenarios place a lot of stress on the hotswap MOSFET and need special care when designing the hotswap circuit to keep the MOSFET within its SOA. A detailed design example is provided in the following sections and similar procedure can be followed for a custom design with different system target specifications. Alternatively, a spreadsheet design tool LM5067 Design Calculator is available for simplified calculations..

9.2 Typical Application

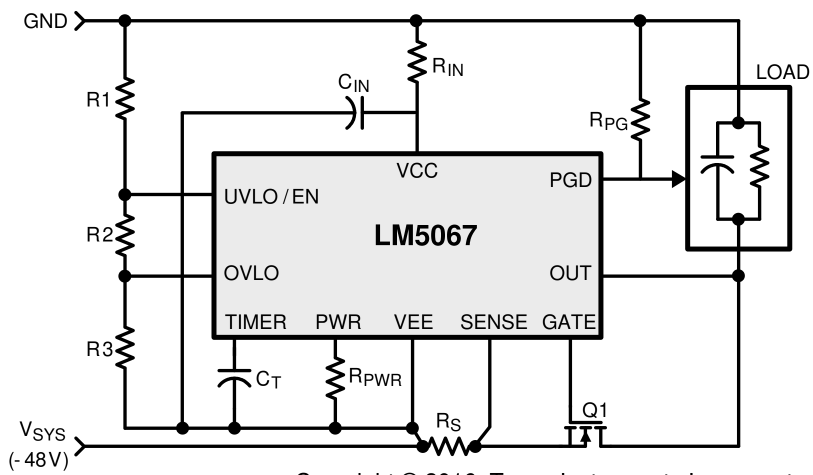


Figure 9-1. Basic Application Circuit

9.2.1 Design Requirements

The recommended design-in procedure for the LM5067 is as follows:

- Determine the minimum and maximum system voltages (VEE). Select the input resistor (R_{IN}) to provide at least 2 mA into the VCC pin at the minimum system voltage. The resistor's power rating must be suitable for its power dissipation at maximum system voltage ($(V_{SYS} – 13V)^2/R_{IN}$).
- Determine the current limit threshold (I_{LIM}). This threshold must be higher than the normal maximum load current, allowing for tolerances in the current sense resistor value and the LM5067 Current Limit threshold voltage. Use equation 1 to determine the value for R_S.
- Determine the maximum allowable power dissipation for the series pass FET (Q1), using the device's SOA information. Use equation 2 to determine the value for R_{PWR}.
- Determine the value for the timing capacitor at the TIMER pin (C_T) using Equation 3. **The fault timeout period (t_{FAULT}) must be longer than the circuit's turn-on-time**. The turn-on time can be estimated using the equations in the Turn-on Time section of this data sheet, but should be verified experimentally. Allow for

tolerances in the values of the external capacitors, sense resistor, and the LM5067 Electrical Characteristics for the TIMER pin, current limit and power limt. Review the resulting insertion time, and the restart timing if the LM5067-2 is used.
- Choose option A, B, C, or D from the UVLO, OVLO section of the Application Information for setting the UVLO and OVLO thresholds and hysteresis. Use the procedure in the appropriate option to determine the resistor values at the UVLO and OVLO pins.
- Choose the appropriate voltage, and pull-up resistor, for the Power Good output.

9.2.2 Detailed Design Procedure

9.2.2.1 R_{IN}, C_{IN}

The LM5067 operating voltage is determined by an internal 13 V shunt regulator which receives its current from the system voltage via R_{IN}. When the system voltage exceeds 13V, the LM5067 operating voltage (VCC – VEE) is between VEE and VEE + 13 V. The remainder of the system voltage is dropped across the input resistor R_{IN}, which must be selected to pass at least 2 mA into the LM5067 at the minimum system voltage. The resistor's power rating must be selected based on the power dissipation at maximum system voltage, calculated from:

$$P_{RIN} = (V_{SYS(max)} - 13\ V)^2/R_{IN} \tag{1}$$

9.2.2.2 Current Limit, R_S

The LM5067 monitors the current in the external MOSFET (Q1) by measuring the voltage across the sense resistor (R_S), connected from SENSE to VEE. The required resistor value is calculated from:

$$R_S = \frac{50\ mV}{I_{LIM}} \tag{2}$$

where

- I_{LIM} is the desired current limit threshold

When the voltage across R_S reaches 50 mV, the current limit circuit modulates the gate of Q1 to regulate the current at I_{LIM}. While the current limiting circuit is active, the fault timer is active as described in the *Fault Timer and Restart* section. For proper operation, R_S must be no larger than 100 mΩ.

While the maximum load current in normal operation can be used to determine the required power rating for resistor R_S, basing it on the current limit value provides a more reliable design since the circuit can operate near the current limit threshold continuously. The resistor's surge capability must also be considered since the circuit breaker threshold is approximately twice the current limit threshold. Connections from R_S to the LM5067 should be made using Kelvin techniques. In the suggested layout of Figure 9-2 the small pads at the upper corners of the sense resistor connect only to the sense resistor terminals, and not to the traces carrying the high current. With this technique, only the voltage across the sense resistor is applied to VEE and SENSE, eliminating the voltage drop across the high current solder connections.

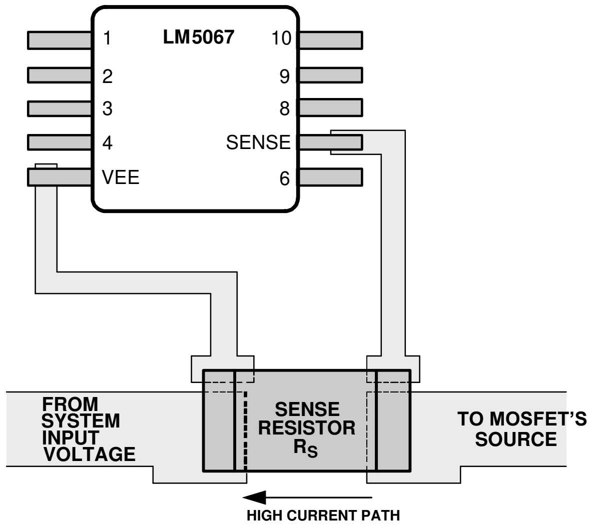


Figure 9-2. Sense Resistor Connections

9.2.2.3 Power Limit Threshold

The LM5067 determines the power dissipation in the external MOSFET (Q1) by monitoring the drain current (the current in R_S), and the V_{DS} of Q1 (OUT to SENSE pins). The resistor at the PWR pin (R_{PWR}) sets the maximum power dissipation for Q1, and is calculated from the following equation:

$$R_{PWR} = 1.42 \times 10^5 \times R_S \times P_{FET(LIM)} \tag{3}$$

where

- $P_{FET(LIM)}$ is the desired power limit threshold for Q1
- R_S is the current sense resistor described in the Current Limit section

For example, if R_S is 10 mΩ, and the desired power limit threshold is 60W, R_{PWR} calculates to 85.2 kΩ. If the Q1 power dissipation reaches the power limit threshold, the Q1 gate is modulated to control the load current, keeping Q1 power from exceeding the threshold. For proper operation of the power limiting feature, R_{PWR} must be ≤150 kΩ. While the power limiting circuit is active, the fault timer is active as described in the *Fault Timer and Restart* section. Typically, power limit is reached during startup, or when the V_{DS} of Q1 increases due to a severe overload or short circuit.

The programmed maximum power dissipation should have a reasonable margin relative to the maximum power defined by the SOA chart if the LM5067-2 is used since the FET will be repeatedly stressed during fault restart cycles. The FET manufacturer should be consulted for guidelines. The PWR pin can be left open if the application does not require use of the power limit function.

9.2.2.4 Turn-On Time

The output turn-on time depends on whether the LM5067 operates in current limit only, or in both power limit and current limit, during turn-on.

9.2.2.4.1 Turn-on With Current Limit Only

If the current limit threshold is less than the current defined by the power limit threshold at maximum V_{DS} the circuit operates only at the current limit threshold during turn-on. Referring to Figure 9-5a, as the drain current reaches I_{LIM}, the gate-to-source voltage is controlled at V_{GSL} to maintain the current at I_{LIM}. As the output voltage reaches its final value (V_{DS} ≅ 0 V) the drain current reduces to the value defined by the load, and the gate is charged to approximately 13 V (V_{GATE}). The time for the OUT pin voltage to transition from zero volts to V_{SYS} is equal to:

$$t_{ON} = \frac{V_{SYS} \times C_L}{I_{LIM}} \tag{4}$$

where

- C_L is the load capacitance

For example, if V_{SYS} = –48 V, C_L = 1000 µF, and I_{LIM} = 1 A, t_{ON} calculates to 48 ms. The maximum instantaneous power dissipated in the MOSFET is 48W. This calculation assumes the time from t1 to t2 in Figure 9-5a is small compared to t_{ON}, and the load does not draw any current until after the output voltage has reached its final value, and PGD switches high (Figure 9-3).

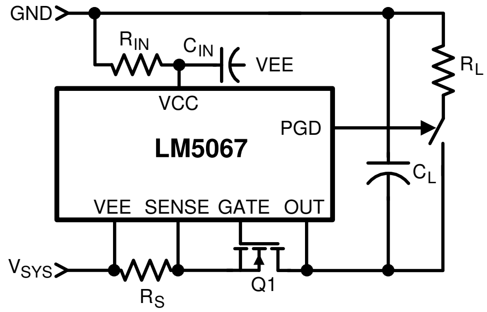


Figure 9-3. No Load Current During Turn-on

If the load draws current during the turn-on sequence (Figure 9-4), the turn-on time is longer than the above calculation, and is approximately equal to:

$$t_{ON} = -(R_L \times C_L) \times \left[\frac{(I_{LIM} \times R_L) - V_{SYS}}{(I_{LIM} \times R_L)}\right] \quad (5)$$

where

- R_L is the load resistance and V_{SYS} is the absolute value of the system input voltage

Note

The Fault Timeout Period must be set longer than t_{ON} to prevent a fault shutdown before the turn-on sequence is complete.

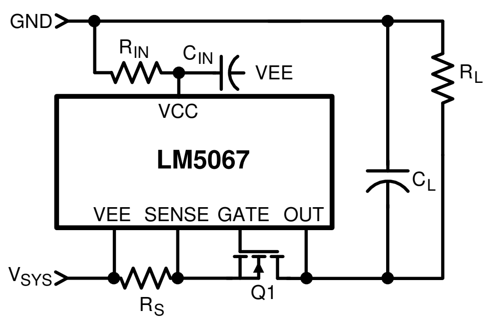


Figure 9-4. Load Draws Current During Turn-On

9.2.2.4.2 Turn-on With Power Limit and Current Limit

The power dissipation limit in Q1 ($P_{FET(LIM)}$) is defined by the resistor at the PWR pin, and the current sense resistor R_S. See *Power Limit Threshold*. If the current limit threshold (I_{LIM}) is higher than the current defined by the power limit threshold at maximum V_{DS} ($P_{FET(LIM)}/V_{SYS}$) the circuit operates initially in power limit mode when the V_{DS} of Q1 is high, and then transitions to current limit mode as the current increases to I_{LIM} as V_{DS} decreases. See Figure 9-5b. Assuming the load (R_L) is not connected during turn-on, the time for the output voltage to reach its final value is approximately equal to:

$$t_{ON} = \frac{C_L \times V_{SYS}^2}{2 \times P_{FET(LIM)}} + \frac{C_L \times P_{FET(LIM)}}{2 \times I_{LIM}2} \quad (6)$$

For example, if V_{SYS} = –48 V, C_L = 1000 µF, I_{LIM} = 1 A, and $P_{FET(LIM)}$ = 20 W, t_{ON} calculates to ≅ 68 ms, and the initial current level (I_P) is approximately 0.42A.

Note

The Fault Timeout Period must be set longer than t_{ON}

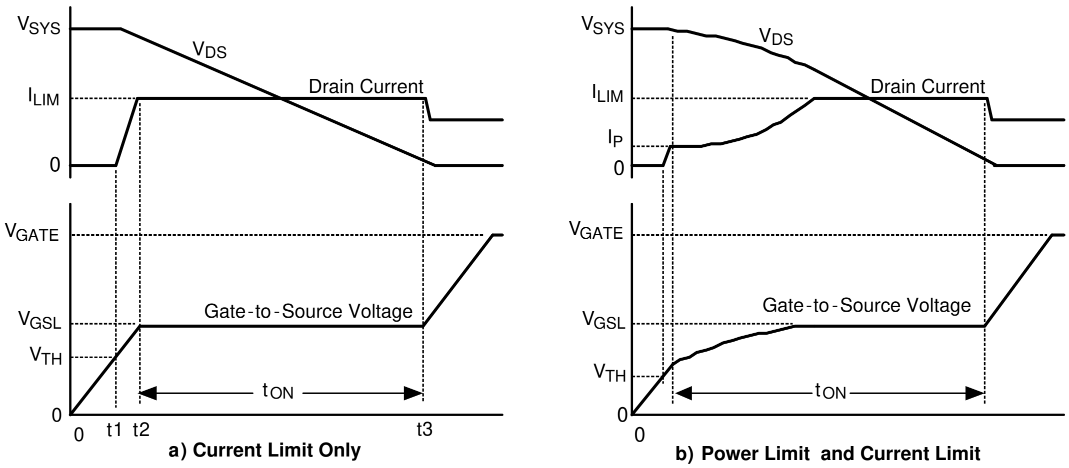


Figure 9-5. MOSFET Power Up Waveforms

9.2.2.5 MOSFET Selection

It is recommended that the external MOSFET (Q1) selection be based on the following criteria:

- The BV_{DSS} rating should be greater than the maximum system voltage (V_{SYS}), plus ringing and transients which can occur at V_{SYS} when the circuit card, or adjacent cards, are inserted or removed.
- The maximum continuous current rating should be based on the current limit threshold (50 mV/R_S), not the maximum load current, since the circuit can operate near the current limit threshold continuously.
- The Pulsed Drain Current spec (I_{DM}) must be greater than the current threshold for the circuit breaker function (100 mV/R_S).
- The SOA (Safe Operating Area) chart of the device, and the thermal properties, should be used to determine the maximum power dissipation threshold set by the R_{PWR} resistor. The programmed maximum power dissipation should have a reasonable margin from the maximum power defined by the FET's SOA chart if the LM5067-2 is used since the FET will be repeatedly stressed during fault restart cycles. The FET manufacturer should be consulted for guidelines.
- $R_{DS(on)}$ should be sufficiently low that the power dissipation at maximum load current ($I_{L(max)}$ ^{2} x $R_{DS(on)}$) does not raise its junction temperature above the manufacturer's recommendation.

If the device chosen for Q1 has a maximum V_{GS} rating less than 13V, an external zener diode must be added from its gate to source, with the zener voltage less than the maximum V_{GS} rating. The zener diode's forward current rating must be at least 110 mA to conduct the GATE pull-down current during startup and in the circuit breaker mode.

9.2.2.6 Timer Capacitor, C_T

The TIMER pin capacitor (C_T) sets the timing for the insertion time delay, fault timeout period, and restart timing of the LM5067-2.

9.2.2.6.1 Insertion Delay

- Upon applying the system voltage (V_{SYS}) to the circuit, the external MOSFET (Q1) is held off during the insertion time (t1 in Figure 8-2) to allow ringing and transients at V_{SYS} to settle. Since each backplane's response to a circuit card plug-in is unique, the worst case settling time must be determined for each application. The insertion time starts when the operating voltage (VCC-VEE) reaches the POR_{IT} threshold, at which time the internal 6 µA current source charges C_T from 0 V to 4 V. The required capacitor value is calculated from:

$$C_T = \frac{t1 \times 6\ \mu A}{4\ V} = t1 \times 1.5 \times 10^{-6} \tag{7}$$

where

- t1 is the desired insertion delay

For example, if the desired insertion delay is 250 ms, C_T calculates to 0.38 µF. At the end of the insertion delay, C_T is quickly discharged by a 1.5 mA current sink.

9.2.2.6.2 Fault Timeout Period

- During turn-on of the output voltage, or upon detection of a fault condition where the current limit and/or power limit circuits regulate the current through Q1, C_T is charged by the fault timer current source (85 µA). The Fault Timeout Period is the time required for the TIMER pin voltage to reach 4.0V above VEE, at which time Q1 is switched off. The required capacitor value for the desired Fault Timeout Period t_{FAULT} is calculated from:

$$C_T = \frac{t_{FAULT} \times 85\ \mu A}{4\ V} = t_{FAULT} \times 2.13 \times 10^{-5} \tag{8}$$

For example, if the desired Fault Timeout Period is 16 ms, C_T calculates to 0.34 µF. After a fault timeout, if the LM5067-1 is in use, C_T must be allowed to discharge to < 0.3 V by the 2.5 µA current sink, after which a power up sequence can be initiated by external circuitry. See Fault Timer and Restart and Latched Fault Restart Control. If the LM5067-2 is in use, after the Fault Timeout Period expires a restart sequence begins as described below (Restart Timing).

Since the LM5067 normally operates in power limit and/or current limit during a power up sequence, the Fault Timeout Period **MUST** be longer than the time required for the output voltage to reach its final value. See Turn-On Time.

9.2.2.6.3 Restart Timing

If the LM5067-2 is in use, after the Fault Timeout Period described above, C_T is discharged by the 2.5 µA current sink to 1.25 V. The TIMER pin then cycles through seven additional charge/discharge cycles between 1.25 V and 4 V as shown in Figure 8-5. The restart time ends when the TIMER pin voltage reaches 0.3 V during the final high-to-low ramp. The restart time, after the Fault Timeout Period, is equal to:

$$t_{RESTART} = C_T \times \left[\frac{7 \times 2.75\ V}{2.5\ \mu A} + \frac{7 \times 2.75\ V}{85\ \mu A} + \frac{3.7\ V}{2.5\ \mu A}\right] = C_T \times 9.4 \times 10^{6} \tag{9}$$

For example, if C_T = 0.33 µF, $t_{RESTART}$ = 3.1 seconds. At the end of the restart time, Q1 is switched on. If the fault is still present, the fault timeout and restart sequence repeats. The on-time duty cycle of Q1 is approximately 0.5% in this mode.

9.2.2.7 UVLO, OVLO

By programming the UVLO and OVLO thresholds the LM5067 enables the series pass device (Q1) when the input supply voltage (V_{SYS}) is within the desired operational range. If V_{SYS} is below the UVLO threshold, or above the OVLO threshold, Q1 is switched off, denying power to the load. Hysteresis is provided for each threshold.

Note

All voltages are with respect to Vee in the discussions below. Use absolute values in the equations.

9.2.2.7.1 Option A:

The configuration shown in Figure 9-6 requires three resistors (R1-R3) to set the thresholds.

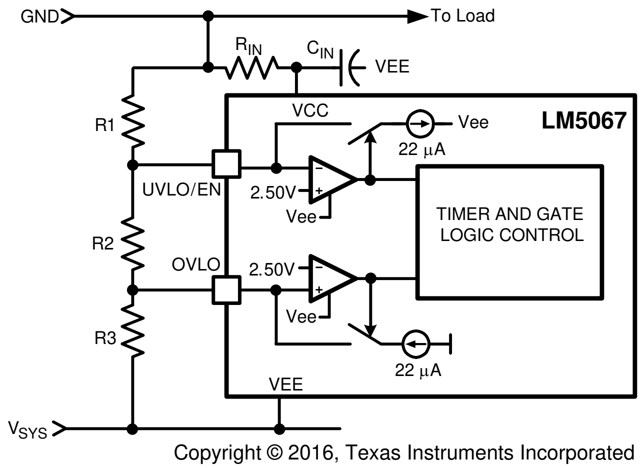


Figure 9-6. UVLO and OVLO Thresholds Set By R1-R3

The procedure to calculate the resistor values is as follows:

- Determine the upper UVLO threshold (V_{UVH}) to enable Q1, and the lower UVLO threshold (V_{UVL}) to disable Q1.
- Determine the upper OVLO threshold (V_{OVH}) to disable Q1.
- The lower OVLO threshold (V_{OVL}), to enable Q1, cannot be chosen in advance in this case, but is determined after the values for R1-R3 are determined. If V_{OVL} must be accurately defined in addition to the other three thresholds, see Option B below.

The resistors are calculated as follows:

$$R1 = \frac{V_{UVH} - V_{UVL}}{22\ \mu A} = \frac{V_{UV(HYS)}}{22\ \mu A}$$

$$R3 = \frac{2.5\ V \times R1 \times V_{UVL}}{V_{OVH} \times (V_{UVL} - 2.5\ V)}$$

$$R2 = \frac{2.5\ V \times R1}{V_{UVL} - 2.5\ V)} - R3 \tag{10}$$

The lower OVLO threshold is calculated from:

$$V_{OVL} = +\left[(R1 + R2 \times \left(\frac{2.5\ V}{R2} - 22\ \mu A\right)\right] + 2.5\ V \tag{11}$$

As an example, assume the application requires the following thresholds: V_{UVH} = -36V, V_{UVL} = -32V, V_{OVH} = -60V.

$$R1 = \frac{36\text{ V} - 32\text{ V}}{22\ \mu\text{A}} = \frac{4\text{ V}}{22\ \mu\text{A}} = 182\text{ k}\Omega$$

$$R3 = \frac{2.5\text{ V} \times 182\text{ k}\Omega \times 32\text{ V}}{60\text{ V} \times (32\text{ V} - 2.5\text{ V})} = 8.23\text{ k}\Omega$$

$$R2 = \frac{2.5\text{ V} \times 182\text{ k}\Omega}{(32\text{ V} - 2.5\text{ V})} = -8.23\text{ k}\Omega = 7.19\text{ k}\Omega \quad (12)$$

The lower OVLO threshold calculates to -55.8V, and the OVLO hysteresis is 4.2V. Note that the OVLO hysteresis is always slightly greater than the UVLO hysteresis in this configuration.

When the R1-R3 resistor values are known, the threshold voltages and hysteresis are calculated from the following:

$$V_{UVH} = 2.5\text{ V} + \left[R1 \times \left(22\ \mu\text{A} + \frac{2.5\text{ V}}{R2 + R3}\right)\right]$$

$$V_{UVL} = \frac{2.5\text{ V} \times (R1 + R2 + R3)}{R2 + R3}$$

$$V_{UV(HYS)} = R1 \times 22\ \mu\text{A}$$

$$V_{OVH} = \frac{2.5\text{ V} \times (R1 + R2 + R3)}{R3}$$

$$V_{OVL} = \left[(R1 + R2) \times \left(\frac{2.5\text{ V}}{R3} - 22\ \mu\text{A}\right)\right] + 2.5\text{ V}$$

$$V_{OV(HYS)} = (R14 + R2) \times 22\ \mu\text{A} \quad (13)$$

Note

Ensure the voltages at the UVLO and OVLO pins do not exceed the Absolute Maximum ratings for those pins when the system voltage is at maximum.

9.2.2.7.2 Option B:

If all four thresholds must be accurately defined, the configuration in Figure 9-7 can be used.

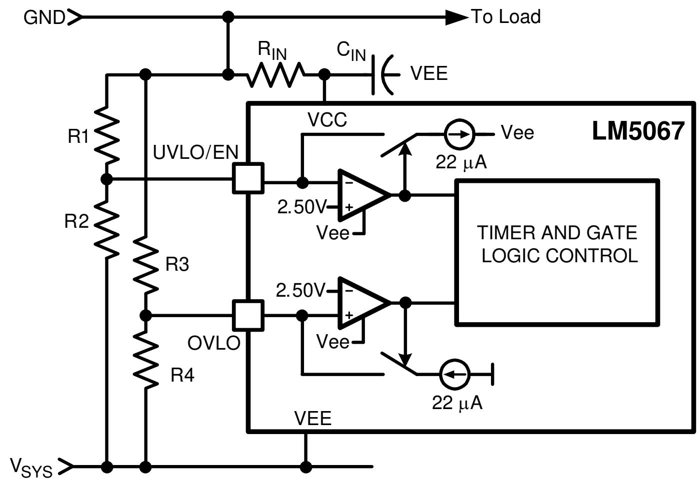


Figure 9-7. Programming the Four Thresholds

The four resistor values are calculated as follows:

- Determine the upper UVLO threshold (V_{UVH}) to enable Q1, and the lower UVLO threshold (V_{UVL}) to disable Q1.

$$R1 = \frac{V_{UVH} - V_{UVL}}{22\ \mu A} = \frac{V_{UV(HYS)}}{22\ \mu A}$$

$$R2 = \frac{2.5\ V \times R1}{(V_{UVL} - 2.5\ V)} \tag{14}$$

- Determine the upper OVLO threshold (V_{OVH}) to disable Q1, and the lower OVLO threshold (V_{OVL}) to enable Q1.

$$R3 = \frac{V_{OVH} - V_{OVL}}{22\ \mu A} = \frac{V_{OV(HYS)}}{22\ \mu A}$$

$$R4 = \frac{2.5\ V \times R3}{(V_{OVL} - 2.5\ V)} \tag{15}$$

As an example, assume the application requires the following thresholds: V_{UVH} = –22 V, V_{UVL} = –17 V, V_{OVH} = –60 V, and V_{OVL} = –58 V. Therefore $V_{UV(HYS)}$ = 5 V, and $V_{OV(HYS)}$ = 2 V. The resistor values are:

R1 = 227 kΩ, R2 = 39.1 kΩ

R3 = 90.9 kΩ, R4 = 3.95 kΩ

Where the R1-R4 resistor values are known, the threshold voltages and hysteresis are calculated from the following:

$$V_{UVH} = 2.5\text{ V} + \left[R1 \times \left(\frac{2.5\text{ V}}{R2} + 22\ \mu A\right)\right]$$

$$V_{UVL} = \frac{2.5\text{ V} \times (R1 + R2)}{R2}$$

$$V_{UV(HYS)} = R1 \times 22\ \mu A$$

$$V_{OVH} = \frac{2.5\text{ V} \times (R3 + R4)}{R4}$$

$$V_{OVL} = 2.5\text{ V} + \left[R3 \times \left(\frac{2.5\text{ V}}{R4} - 22\ \mu A\right)\right]$$

$$V_{OV(HYS)} = R3 \times 22\ \mu A \tag{16}$$

Note

Ensure the voltages at the UVLO and OVLO pins do not exceed the Absolute Maximum ratings for those pins when the system voltage is at maximum.

9.2.2.7.3 Option C:

The minimum UVLO level is obtained by connecting the UVLO pin to VCC as shown in Figure 9-8. Q1 is switched on when the operating voltage reaches the POR_{EN} threshold (≅8.4V). The OVLO thresholds are set by R3 and R4 using the procedure in Option B.

Note

Ensure the voltage at the OVLO pin does not exceed the Absolute Maximum ratings for that pin when the system voltage is at maximum.

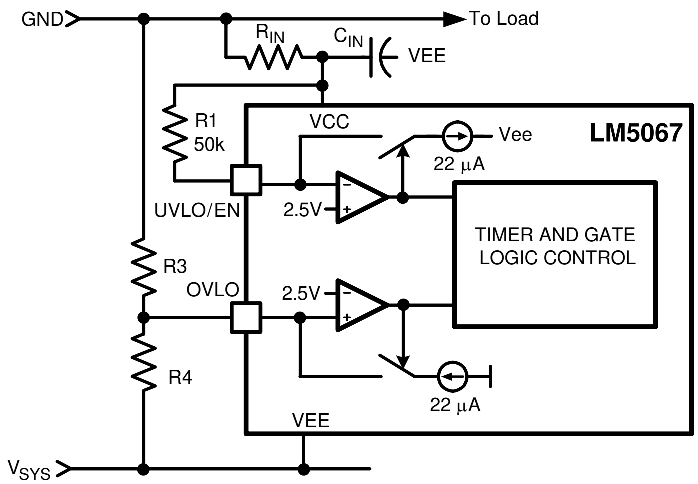


Figure 9-8. UVLO = POR_{EN}

9.2.2.7.4 Option D:

The OVLO function can be disabled by connecting the OVLO pin to VEE. The UVLO thresholds are set as described in Option B or Option C.

9.2.2.8 Thermal Considerations

The LM5067 should be operated so that its junction temperature does not exceed 125°C. The junction temperature is equal to:

$$T_J = T_A + (R_{\theta JA} \times P_D) \tag{17}$$

where

- T_A is the ambient temperature
- $R_{\theta JA}$ is the thermal resistance of the LM5067

P_D is the power dissipated within the LM5067, calculated from:

$$P_D = 13V \times I_{CC} \tag{18}$$

where

- I_{CC} is the current into the VCC pin (the current through the R_{IN} resistor).

Values for $R_{\theta JA}$ and $R_{\theta JC}$ are in *Thermal Information*.

9.2.2.9 System Considerations

Continued proper operation of the LM5067 hot swap circuit requires capacitance be present on the supply side of the connector into which the hot swap circuit is plugged in, as depicted in Figure 8-1. The capacitor in the “Live Backplane” section is necessary to absorb the transient generated whenever the hot swap circuit shuts off the load current. If the capacitance is not present, inductance in the supply lines will generate a voltage transient at shut-off which can exceed the absolute maximum rating of the LM5067, resulting in its destruction.

If the load powered via the LM5067 hot swap circuit has inductive characteristics, a diode is required across the LM5067's output to provide a recirculating path for the load's current. Adding the diode prevents possible damage to the LM5067 as the OUT pin will be taken above ground by the inductive load at shutoff. See Figure 9-9

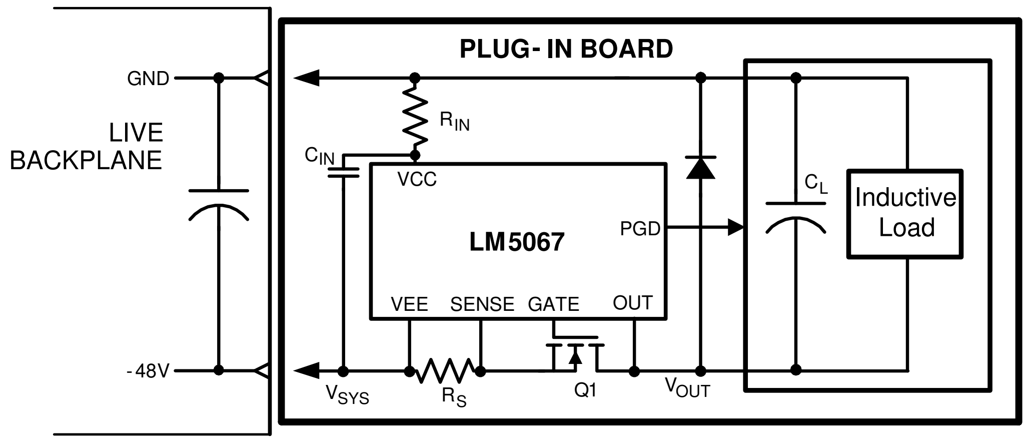


Figure 9-9. Output Diode Required for Inductive Loads

9.2.2.9.1 System Considerations During Surge Events

The control MOSFET, Q1, has a body-diode, illustrated in Figure 9-10, where current can freely flow in the reverse direction. The most common cause of a reverse current is a discharge event at the input of the hot-swap circuit when the output capacitance discharges to the input. Normally, reverse current flow presents no issue for hotswap devices during events such as shutdown and minor input power perturbations. However, extreme situations such as high energy lighting surge line disturbances can expose the hot-swap circuit to pulses of ultra fast - high amplitude reverse currents. It is common to observe current amplitudes on the order of 1000 A in these situations. Figure 9-10 illustrates what an extreme input discharge event may look like and how it affects the circuit.

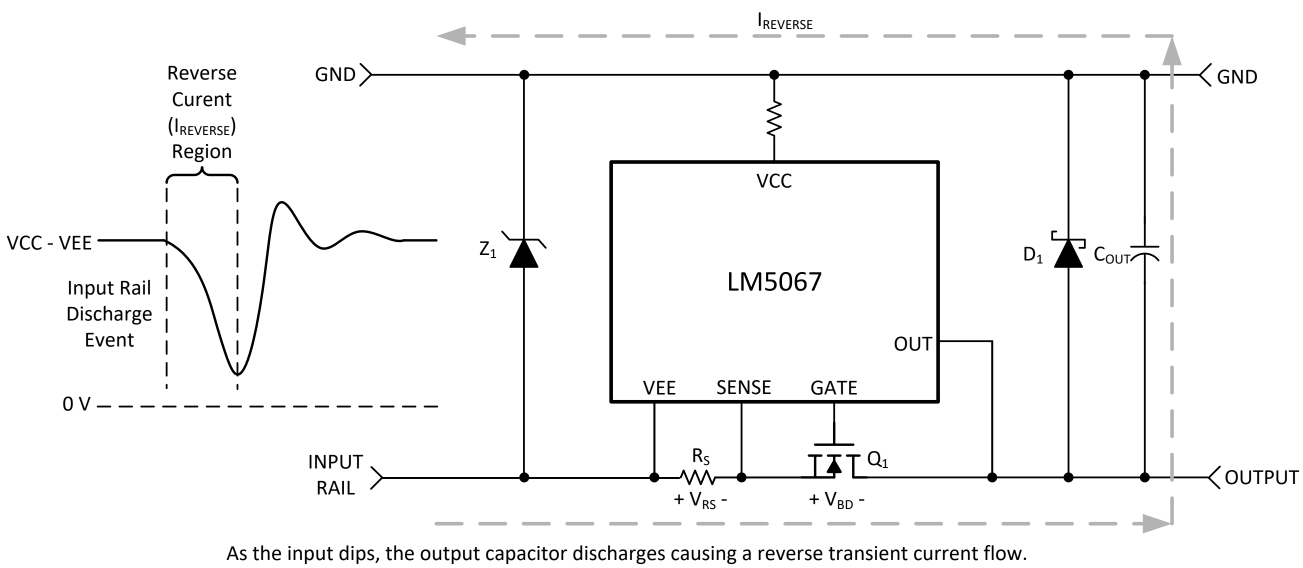
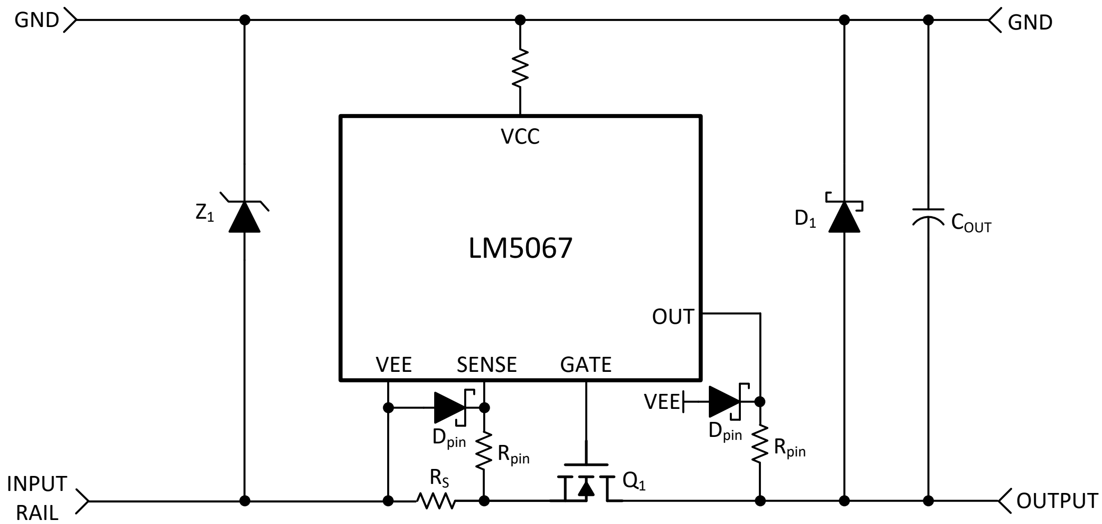


Figure 9-10. Differential Voltage Across Sense Resistor

Figure 9-10 shows how the induced reverse current spike causes a differential voltage across the sense resistor, VRS, and the Q1 body-diode, VBD. The transient reverse current, IREVERSE, is approximately equal to IREVERSE = COUT x dVIN/dt because the output capacitor is discharged through the input. Faster discharge rates (dVIN/dt) will induce larger IREVERSE currents. If IREVERSE is extremely high, it can cause a large negative voltage at the SENSE and OUT pins with respect to the VEE pin of the LM5067. If the negative absolute maximum voltage rating is greatly exceeded, harmful currents can flow into the affected pins. Series pin resistors can be implemented to limit the pin current caused by the negative voltage excursion. Schottky diodes may also be implemented to completely clamp the voltage at these pins, Figure 9-11 illustrates this.



Series resistors are used to limit harmful negative pin currents and schottky diodes are used to clamp the voltage at each pin.

Figure 9-11. Schottky Diodes Used to Clamp Pin Voltage

A typical value of Rpin can be 22 Ω to effectively limit the pin current during extreme negative voltage spikes. If schottky diodes are used, they only need to be applied to SENSE_K, SENSE, and OUT. Each schottky diode return pin should be coupled closely with the VEE plane to provide the most effective clamping. The schottky diode at OUT should be able to withstand at least 100 V. VEE_K needs a series resistor even though it's not subjected to negative voltage spikes in order to balance the differential current sense voltage signal. Protecting the SENSE_K, SENSE, and OUT pins from negative voltage spikes will facilitate a robust hot-swap circuit and smooth operation during extreme reverse current surge events.

9.2.2.10 Power Good Pin

During initial power up, the Power Good pin (PGD) is high until the operating voltage (VCC – VEE) increases above ≊2V. PGD then switches low, remaining low as the system voltage and the operating voltage increase. After Q1 is switched on, when the voltage at the OUT pin is within 1.23 V of the SENSE pin (Q1 V_{DS} <1.23 V), PGD switches high indicating the output voltage is at, or nearly at, its final value. Any of the following situations will cause PGD to switch low within ≊10 µs:

- The V_{DS} of Q1 increases above 2.5 V.
- The system input voltage decreases below the UVLO level.
- The system input voltage increase above the OVLO level.
- The TIMER pin increases to 4V due to a fault condition.

A pull-up resistor is required at PGD as shown in Figure 9-12. The pull-up voltage (V_{PGD}) can be as high as 80 V above VEE, with transient capability to 100 V, and can be higher or lower than the system ground.

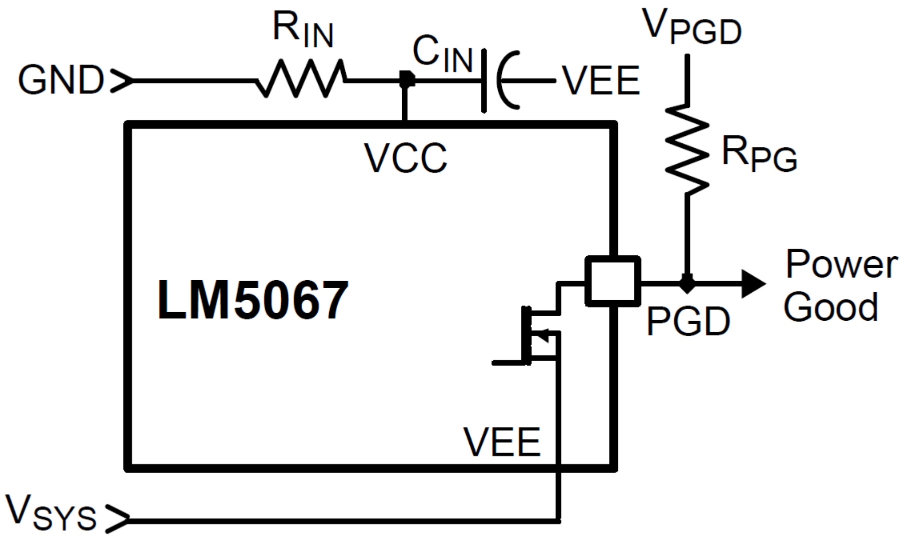


Figure 9-12. Power Good Output

If a delay is required at PGD, suggested circuits are shown in the following figure. In Figure 9-13, capacitor C_{PG} adds delay to the rising edge, but not to the falling edge. In Figure 9-14, the rising edge is delayed by R_{PG1} + R_{PG2} and C_{PG}, while the falling edge is delayed a lesser amount by R_{PG2} and C_{PG}. Adding a diode across R_{PG2}. Figure 9-15 allows for equal delays at the two edges, or a short delay at the rising edge and a long delay at the falling edge.

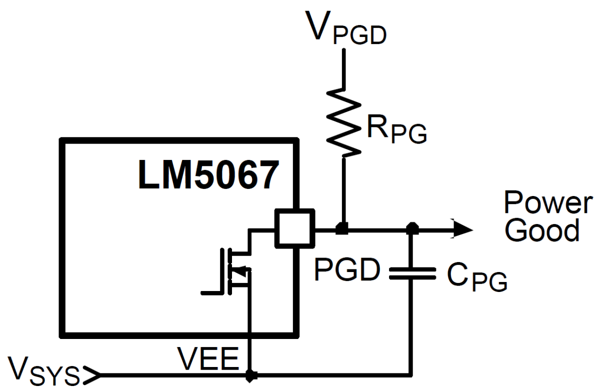


Figure 9-13. Adding Delay to the Power Good Output Pin - Delay Rising Edge Only

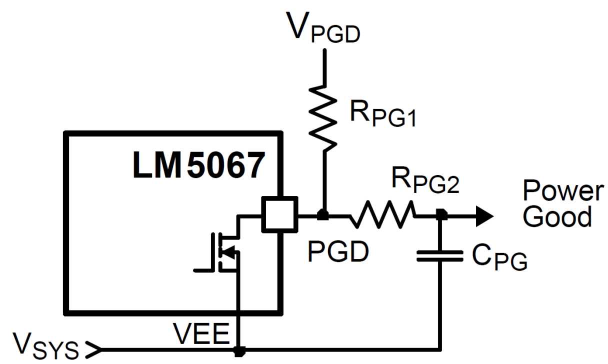


Figure 9-14. Adding Delay to the Power Good Output Pin - Long Delay at Rising Edge, Short Delay at Falling Edge

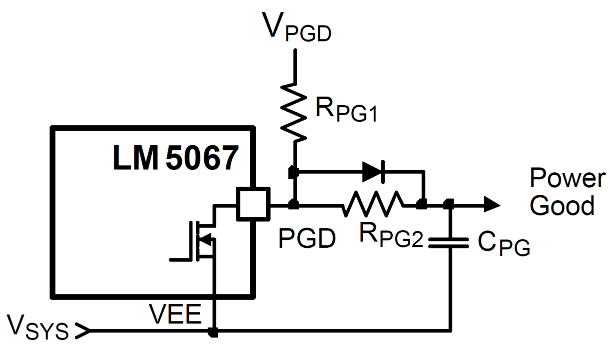


Figure 9-15. Adding Delay to the Power Good Output Pin - Short Delay at Rising Edge and Long Delay at Falling Edge, or Equal Delays

9.2.3 Application Curves

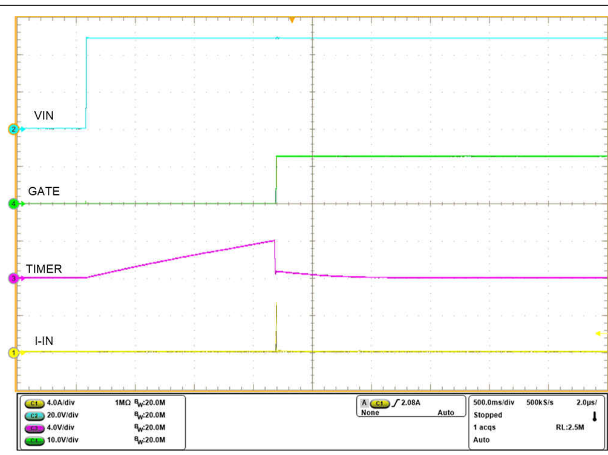


Figure 9-16. Insertion Delay

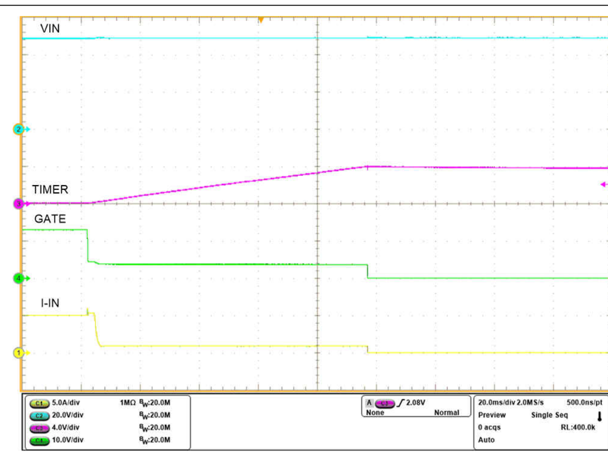


Figure 9-17. Overload During Steady State

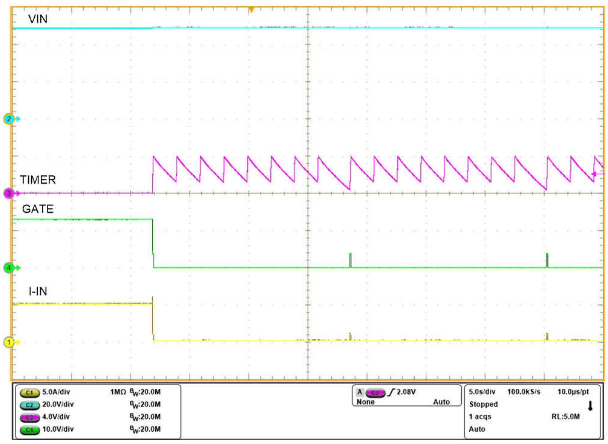


Figure 9-18. Overload With Retry

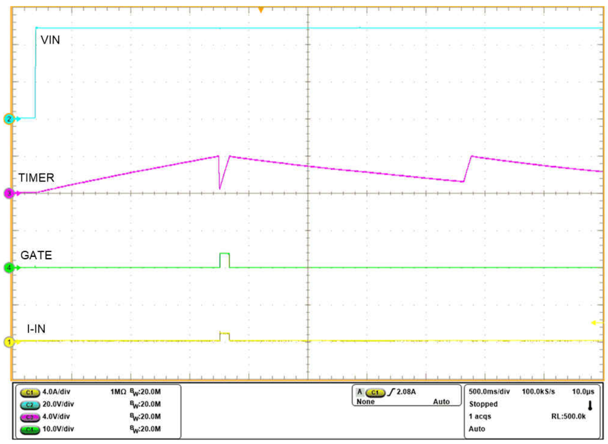


Figure 9-19. Power Into Short

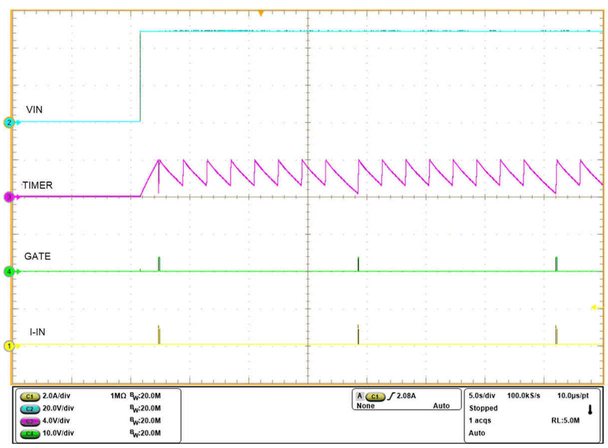


Figure 9-20. Power Into Short Retry Zoomed Out

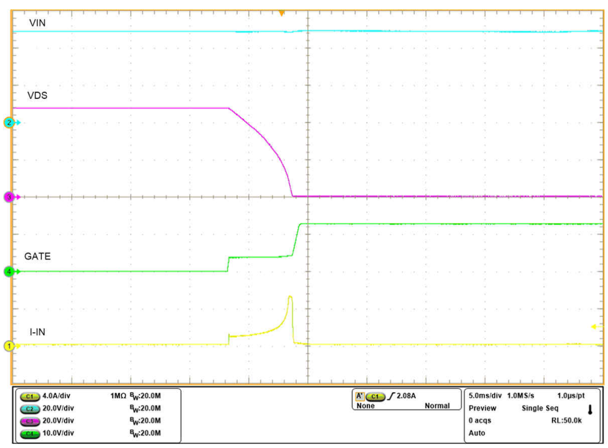


Figure 9-21. Power Limited Startup

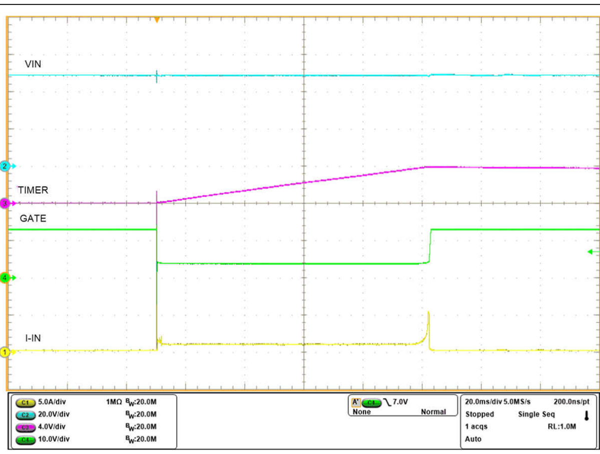


Figure 9-22. Short Circuit and Release

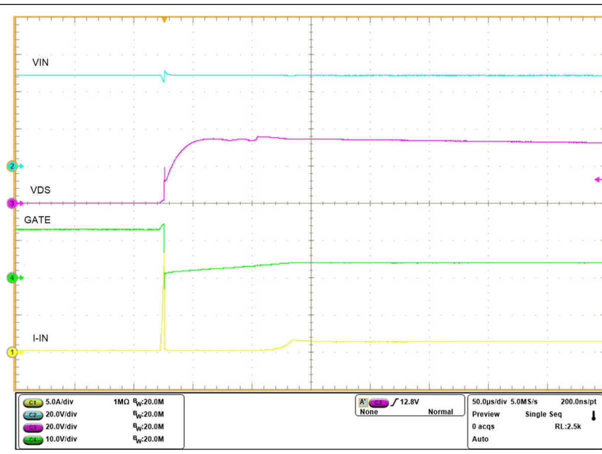


Figure 9-23. Short Circuit Zoomed In

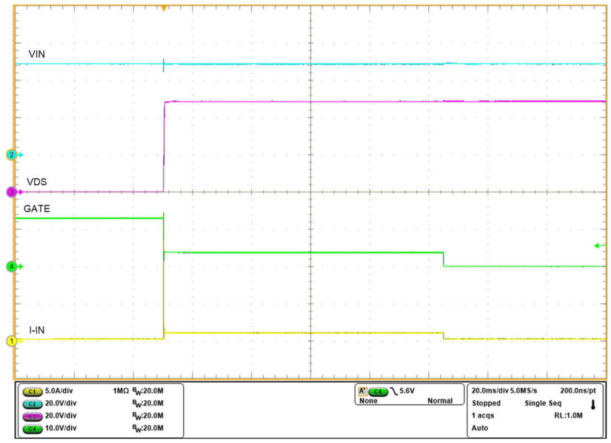


Figure 9-24. Short Circuit Zoomed Out

10 Power Supply Recommendations

10.1 Operating Voltage

The LM5067 operating voltage is the voltage from VCC to VEE. The maximum operating voltage is set by an internal 13V zener diode. With the IC connected as shown in Figure 9-1, the LM5067 controller operates in the voltage range between VEE and VEE+13V. The remainder of the system voltage is dropped across the input resistor R_{IN}, which must be selected to pass at least 2 mA into the LM5067 at the minimum system voltage.

11 Layout

11.1 Layout Guidelines

The following guidelines should be followed when designing the PC board for the LM5067:

- Place the LM5067 close to the board's input connector to minimize trace inductance from the connector to the FET.
- Place R_{IN} and C_{IN} close to the VCC and VEE pins to keep transients below the Absolute Maximum rating of the LM5067. Transients of several volts can easily occur when the load current is shut off.
- The sense resistor (R_S) should be close to the LM5067, and connected to it using the Kelvin techniques shown in Figure 9-2.
- The high current path from the board's input to the load, and the return path (via Q1), should be parallel and close to each other wherever possible to minimize loop inductance.
- The VEE connection for the various components around the LM5067 should be connected directly to each other, and to the LM5067's VEE pin, and then connected to the system VEE at one point. Do not connect the various components to each other through the high current VEE track.
- Provide adequate heat sinking for the series pass device (Q1) to help reduce thermal stresses during turn-on and turn-off.
- The board's edge connector can be designed to shut off the LM5067 as the board is removed, before the supply voltage is disconnected from the LM5067. In Figure 11-1 the voltage at the UVLO/EN pin goes to VEE before V_{SYS} is removed from the LM5067 due to the shorter edge connector pin. When the board is inserted into the edge connector, the system voltage is applied to the LM5067's VEE and VCC pins before voltage is applied to the UVLO/EN pin.
- If power dissipation within the LM5067 is high, an exposed copper pad should be provided beneath the package, and that pad should be connected to exposed copper on the board's other side with as many vias as possible. See Thermal Considerations.

11.2 Layout Example

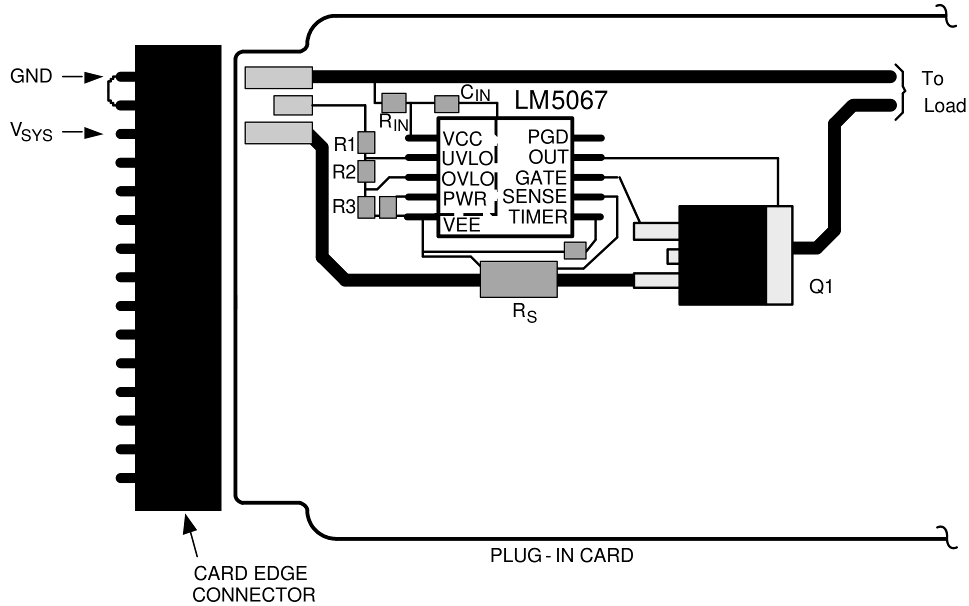


Figure 11-1. Suggested Board Connector Design

12 Device and Documentation Support

12.1 Trademarks

All trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.3 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM50672NPAR	ACTIVE	SOIC	NPA	14	1000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	LM50672 NPA	Samples
LM5067MM-1/NOPB	ACTIVE	VSSOP	DGS	10	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	SRUB	Samples
LM5067MM-2/NOPB	ACTIVE	VSSOP	DGS	10	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	SRVB	Samples
LM5067MMX-2/NOPB	ACTIVE	VSSOP	DGS	10	3500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	SRVB	Samples
LM5067MW-1/NOPB	ACTIVE	SOIC	NPA	14	50	RoHS & Green	SN	Level-3-260C-168 HR		LM5067 MW-1	Samples
LM5067MWX-1/NOPB	ACTIVE	SOIC	NPA	14	1000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	LM5067 MW-1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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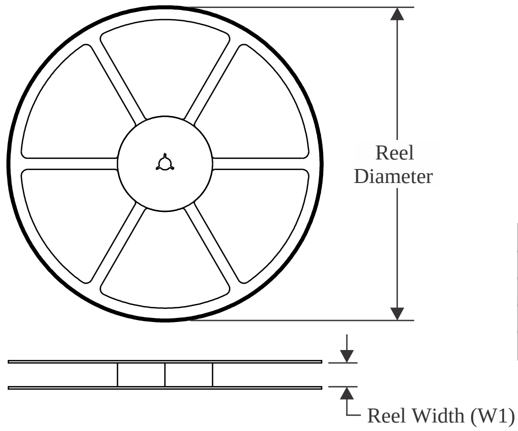
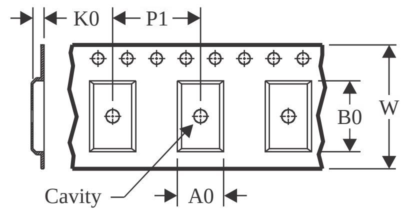
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

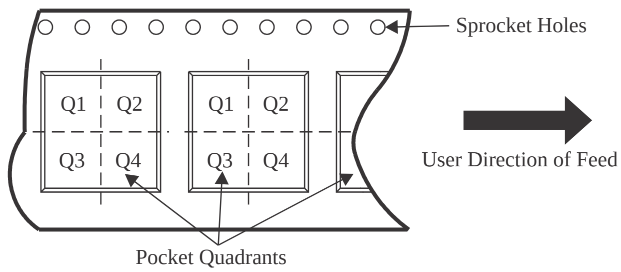


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

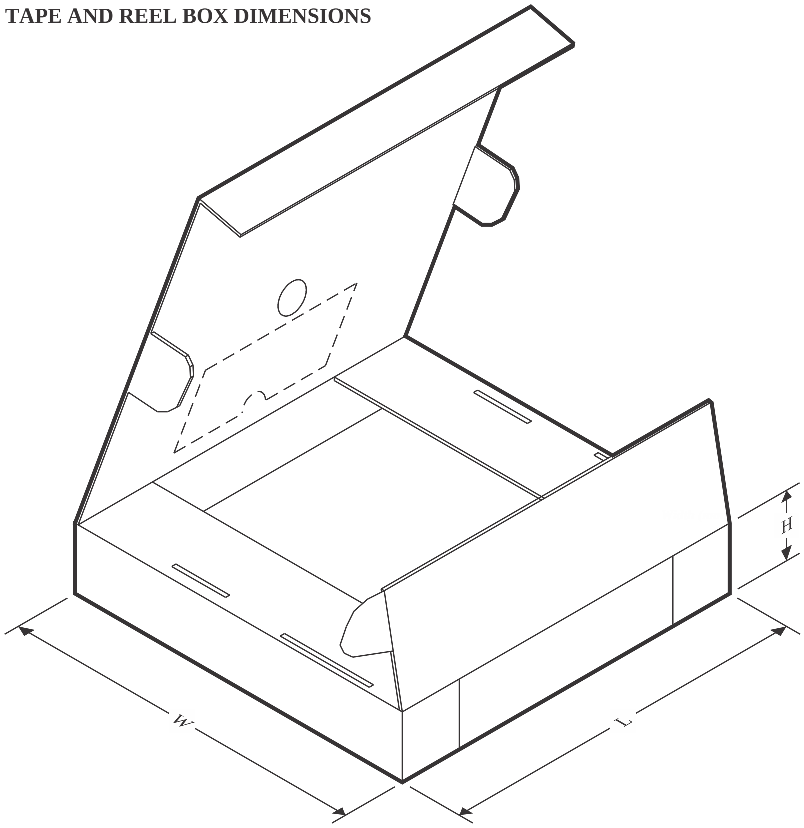
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM50672NPAR	SOIC	NPA	14	1000	330.0	16.4	10.9	9.5	3.2	12.0	16.0	Q1
LM5067MM-1/NOPB	VSSOP	DGS	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5067MM-2/NOPB	VSSOP	DGS	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5067MMX-2/NOPB	VSSOP	DGS	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5067MWX-1/NOPB	SOIC	NPA	14	1000	330.0	16.4	10.9	9.5	3.2	12.0	16.0	Q1

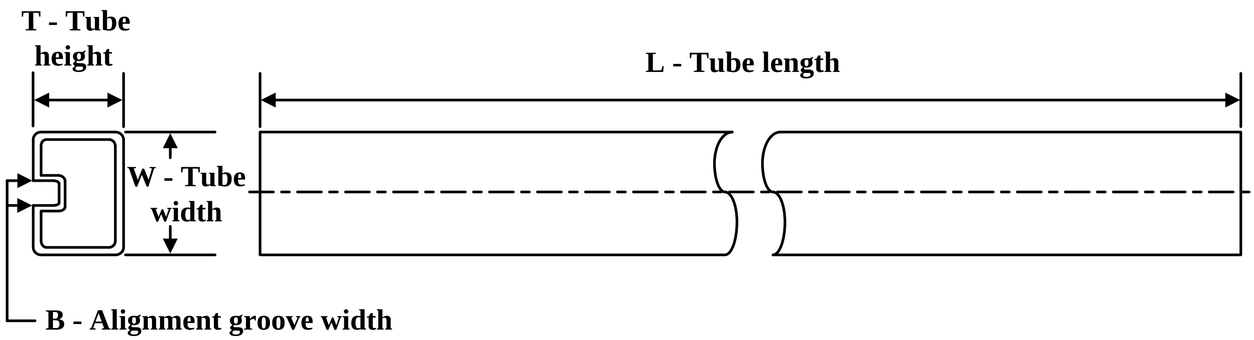
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM50672NPAR	SOIC	NPA	14	1000	356.0	356.0	36.0
LM5067MM-1/NOPB	VSSOP	DGS	10	1000	208.0	191.0	35.0
LM5067MM-2/NOPB	VSSOP	DGS	10	1000	208.0	191.0	35.0
LM5067MMX-2/NOPB	VSSOP	DGS	10	3500	367.0	367.0	35.0
LM5067MWX-1/NOPB	SOIC	NPA	14	1000	356.0	356.0	36.0

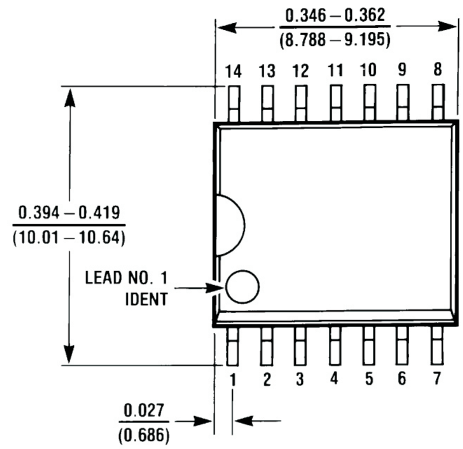
TUBE

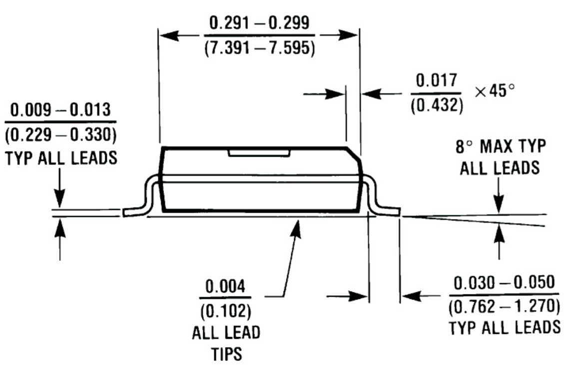


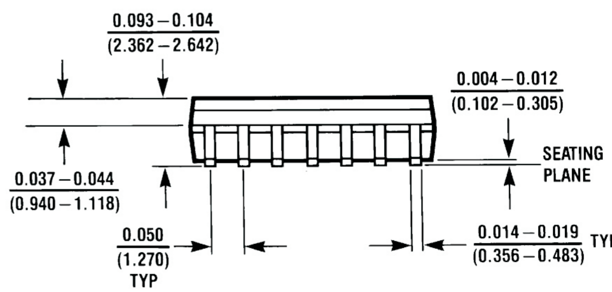
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM5067MW-1/NOPB	NPA	SOIC	14	50	495	15	5842	7.87

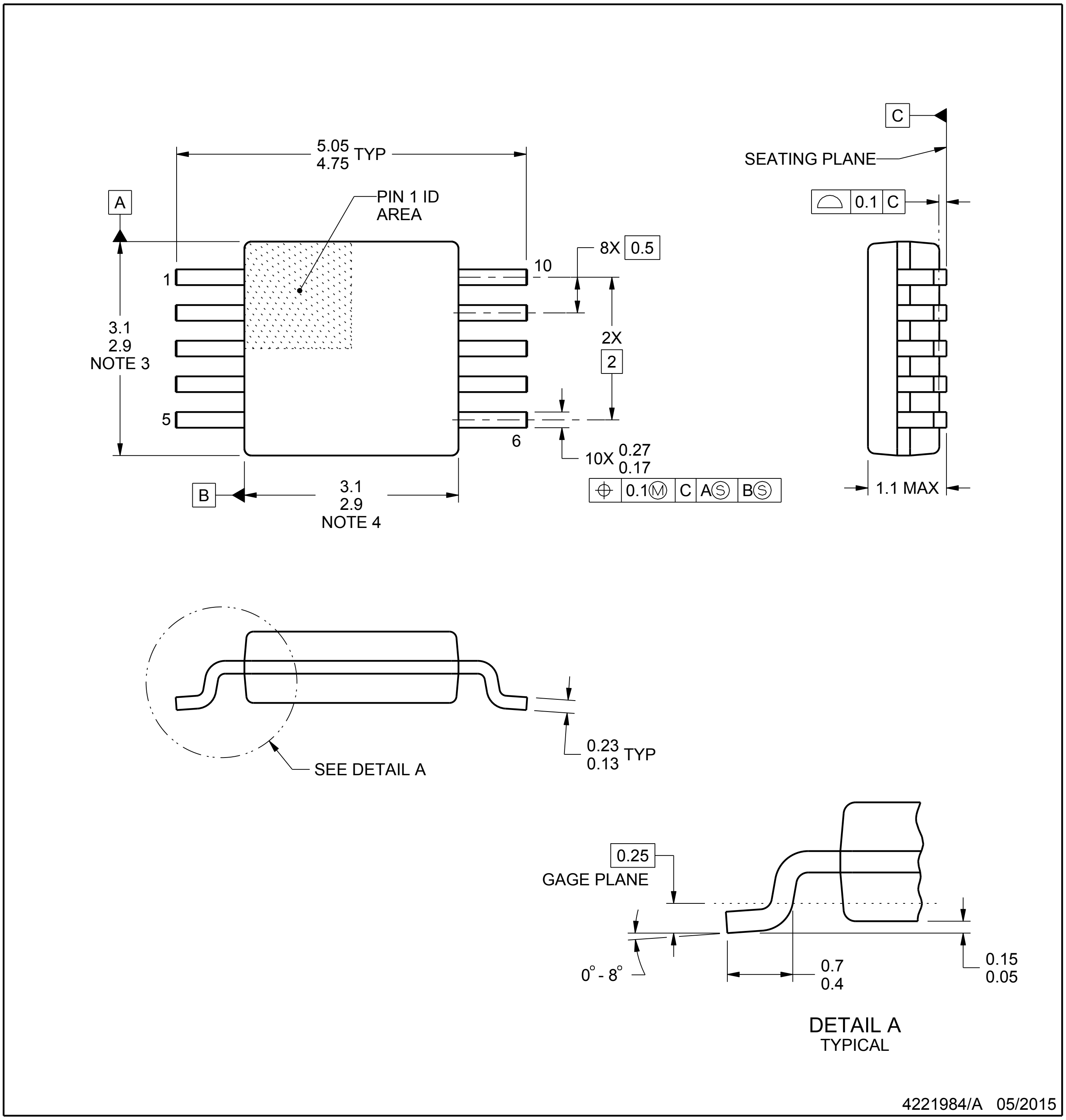
NPA0014B





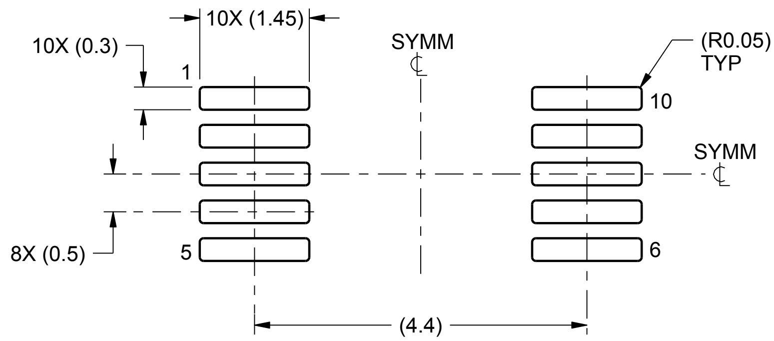


M14B (REV D)

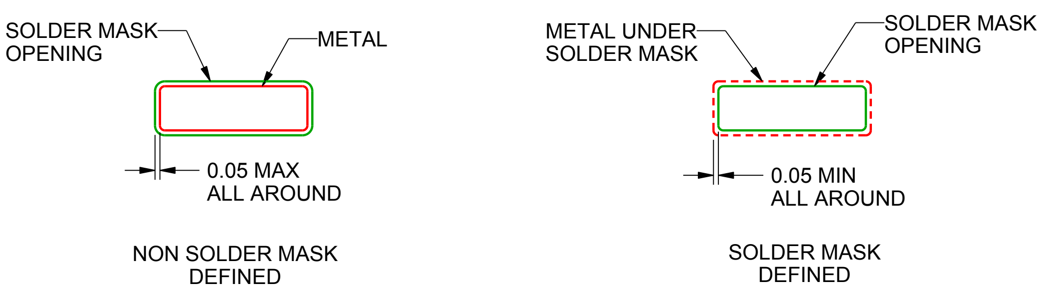


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

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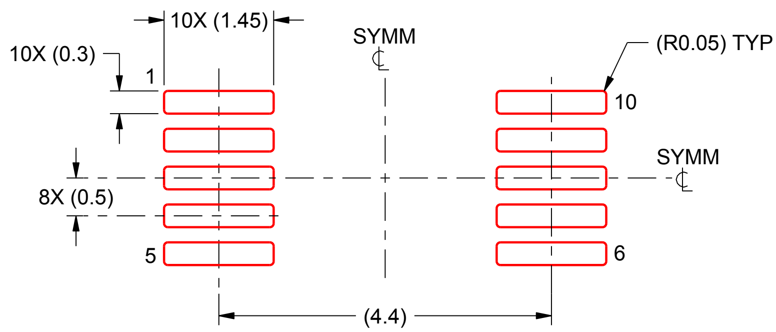
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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