

Standard LCD Segment Drivers

BU9795AFV MAX 108 segments (SEG27×COM4)

•Features

- Integrated RAM for display data (DDRAM) :
27 × 4bit (Max 108 Segment)
- LCD drive output :
4 Common output, Max 27Segment output
- Integrated Buffer AMP for LCD driving
- Integrated Oscillator circuit
- No external components
- Low power consumption design

•Applications

- Telephone
- FAX
- Portable equipment (POS, ECR, PDA etc.)
- DSC
- DVC
- Car audio
- Home electrical appliance
- Meter equipment
- etc.

•Key Specifications

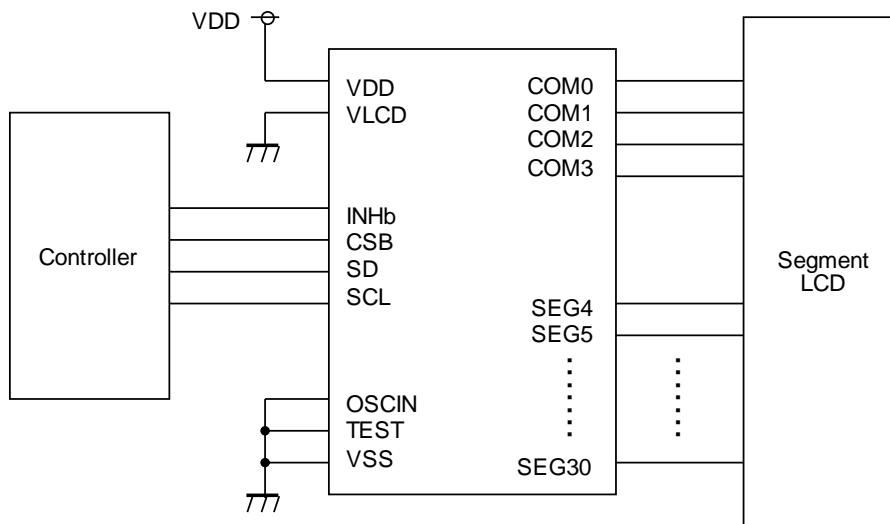
- Supply Voltage Range: +2.5V to +5.5V
- Operating Temperature Range: -40°C to +85°C
- Max Segments: 108 Segments
- Display Duty: 1/4
- Bias: 1/2, 1/3 selectable
- Interface: 3wire serial interface

•Packages

W (Typ) x D (Typ) x H (Max)



•Typical Application Circuit



Internal oscillator circuit mode

Figure 1. Typical application circuit

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays.

●Block Diagrams / Pin Configurations / Pin Descriptions

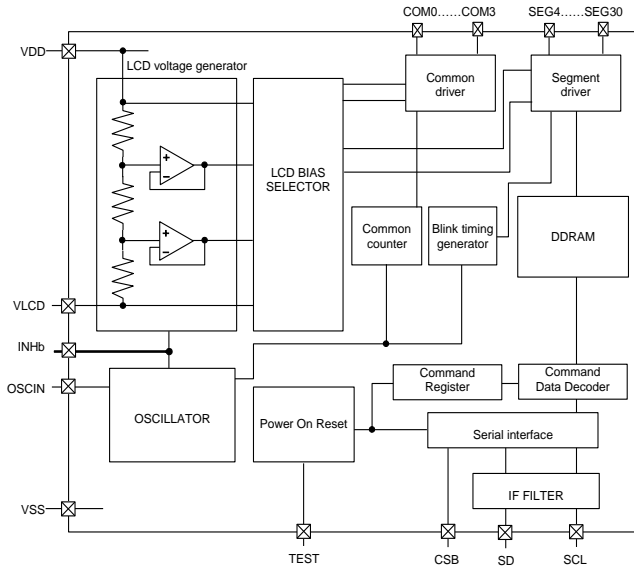


Figure 2. Block Diagram

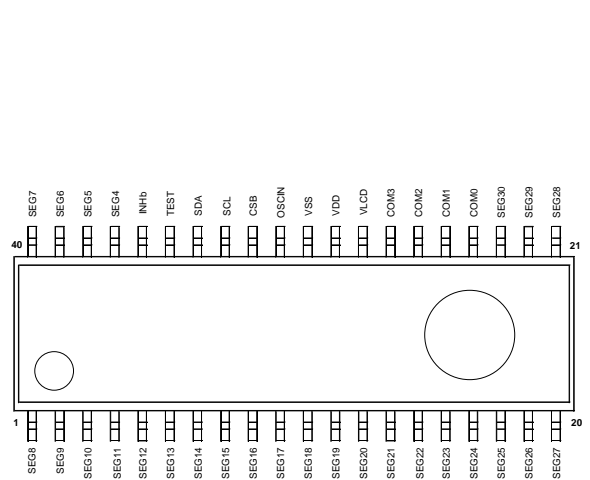


Figure 3. Pin Configuration (TOP VIEW)

Table 1 Pin Description

| Pin name | Pin No. | I/O | Function |
|---------------|----------------------|-----|--|
| INHb | 36 | I | Input terminal for turn off display H : turn on display L : turn off display |
| TEST | 35 | I | Test input (ROHM use only) Must be connected to VSS |
| OSCIN | 31 | I | External clock input Ex clock and Int clock can be changed by command. Must be connected to VSS when using internal oscillation circuit. |
| SD | 34 | I | Serial data input |
| SCL | 33 | I | Serial data transfer clock |
| CSB | 32 | I | Chip select : "L" active |
| VSS | 30 | | GND |
| VDD | 29 | | Power supply |
| VLCD | 28 | I | Power supply for LCD driving |
| SEG4 to SEG30 | 1 to 23, 37 to 40 | O | SEGMENT output for LCD driving |
| COM0 to COM3 | 24 to 27 | O | COMMON output for LCD driving |

●Absolute Maximum Ratings (VSS=0V)

| Parameter | Symbol | Ratings | Unit | Remark |
|-------------------------------|--------|-----------------|------|--|
| Power supply voltage1 | VDD | -0.5 to +7.0 | V | Power supply |
| Power supply voltage2 | VLCD | -0.5 to VDD | V | LCD drive voltage |
| Power dissipation | Pd | 0.7 | W | When use more than Ta=25°C, subtract 7mW per degree (Package only) |
| Input voltage range | VIN | -0.5 to VDD+0.5 | V | |
| Operational temperature range | Topr | -40 to +85 | °C | |
| Storage temperature range | Tstg | -55 to +125 | °C | |

●Recommended Operating Ratings(Ta=-40°C to +85°C,VSS=0V)

| Parameter | Symbol | Ratings | | | Unit | Remark |
|-----------------------|--------|---------|------|----------|------|-------------------|
| | | Min. | Typ. | Max. | | |
| Power Supply voltage1 | VDD | 2.5 | - | 5.5 | V | Power supply |
| Power Supply voltage2 | VLCD | 0 | - | VDD -2.4 | V | LCD drive voltage |

* Please use VDD-VLCD≥2.4V condition.

●Electrical Characteristics

DC Characteristics (VDD=2.5V to 5.5V, VSS=0V, Ta=-40°C to +85°C, unless otherwise specified)

| Parameter | Symbol | Limits | | | Unit | Conditions | |
|--------------------------|-----------------|--------|------|----------|------|--|--------------------------|
| | | MIN | TYP | MAX | | | |
| "H" level input voltage | VIH | 0.7VDD | - | VDD | V | | |
| "L" level input voltage | VIL | VSS | - | 0.3VDD | V | | |
| "H" level input current | I _{IH} | - | - | 1 | μA | | |
| "L" level input current | I _{IL} | -1 | - | - | μA | | |
| LCD Driver on resistance | SEG | RON | - | 3.5 | - | kΩ | I _{load} =±10μA |
| | COM | RON | - | 3.5 | - | kΩ | |
| VLCD supply voltage | VLCD | 0 | - | VDD -2.4 | V | VDD-VLCD≥2.5V | |
| Standby current | I _{st} | - | - | 5 | μA | Display off, Oscillator off | |
| Power consumption 1 | IDD1 | - | 12.5 | 30 | μA | VDD=3.3V, Ta=25°C, Power save mode1, FR=70Hz 1/3 bias, Frame inverse | |
| Power consumption 2 | IDD2 | - | 20 | 40 | μA | VDD=3.3V, Ta=25°C, Normal mode, FR=80Hz 1/3 bias, Line inverse | |

●Electrical Characteristics - continued

Oscillation Characteristics (VDD=2.5V to 5.5V, VSS=0V, Ta=-40°C to +85°C)

| Parameter | Symbol | Limits | | | Unit | Conditions |
|------------------|-------------------|--------|-----|-----|------|-------------------|
| | | MIN | TYP | MAX | | |
| Frame frequency | f _{CLK} | 56 | 80 | 104 | Hz | FR = 80Hz setting |
| Frame frequency1 | f _{CLK1} | 70 | 80 | 90 | Hz | VDD=3.5V, 25°C |

MPU interface Characteristics (VDD=2.5V to 5.5V, VSS=0V, Ta=-40°C to +85°C)

| Parameter | Symbol | Limits | | | Unit | Conditions |
|---------------------|-------------------|--------|-----|-----|------|------------|
| | | MIN | TYP | MAX | | |
| Input rise time | t _r | - | - | 80 | ns | |
| Input fall time | t _f | - | - | 80 | ns | |
| SCL cycle time | t _{SCYC} | 400 | - | - | ns | |
| "H" SCL pulse width | t _{SHW} | 100 | - | - | ns | |
| "L" SCL pulse width | t _{SLW} | 100 | - | - | ns | |
| SD setup time | t _{SDS} | 20 | - | - | ns | |
| SD hold time | t _{SDH} | 50 | - | - | ns | |
| CSB setup time | t _{CSS} | 50 | - | - | ns | |
| CSB hold time | t _{CSH} | 50 | - | - | ns | |
| "H" CSB pulse width | t _{CHW} | 50 | - | - | ns | |

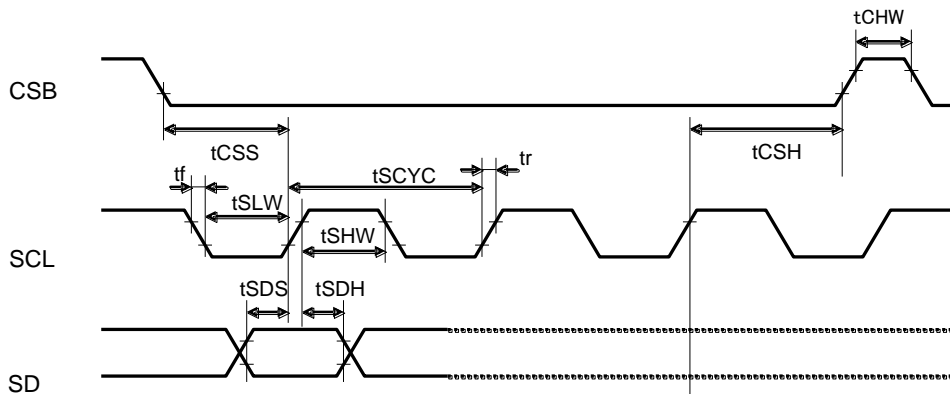


Figure 4. Interface Timing

●I/O equivalent circuit

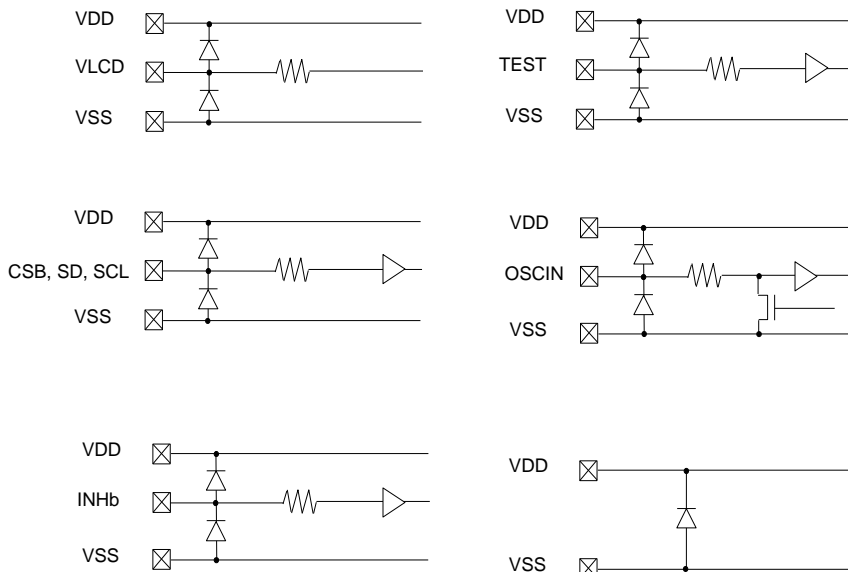
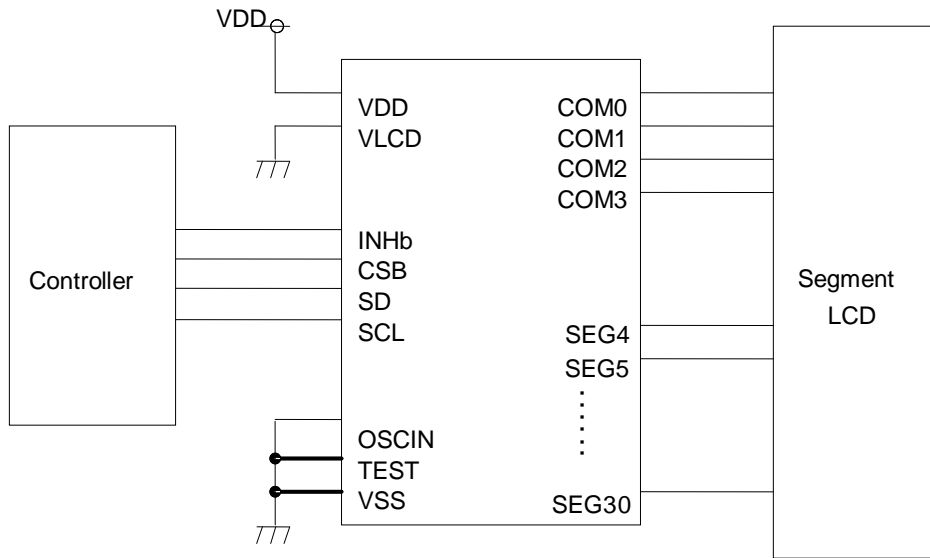
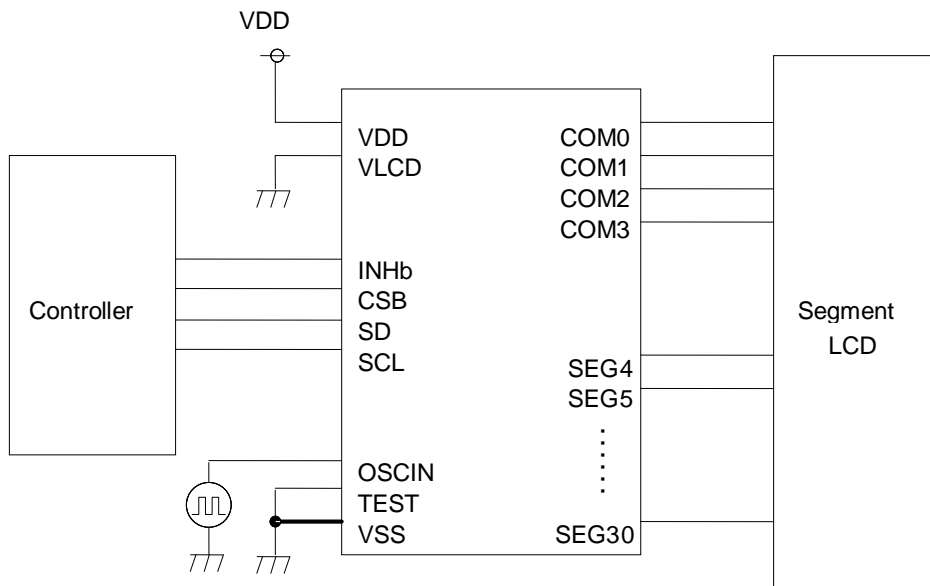


Figure 5. I/O equivalent circuit

●Example of recommended circuit



Using internal oscillator circuit mode



Using external oscillator mode

Figure 6. example recommended circuit

•Function Description

- Command and data transfer method
- 3-SPI (3wire Serial interface)

This device is controlled by 3-wire signal (CSB, SCL, and SD).
 First, Interface counter is initialized with CSB="H", and CSB="L" makes SD and SCL input enable.
 The protocol of 3-SPI transfer is as follows.
 Each command starts with Command or Data judgment bit (D/C) as MSB data, followed by D6 to D0 during CSB = "L".
 (Internal data is latched at the rising edge of SCL, it is converted to 8bits parallel data at the falling edge of 8th CLK.)

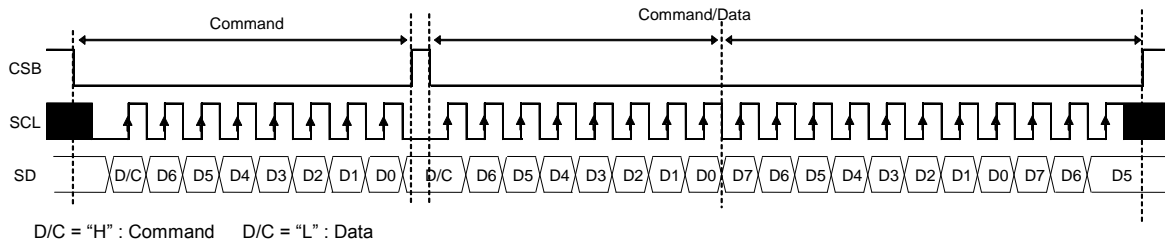
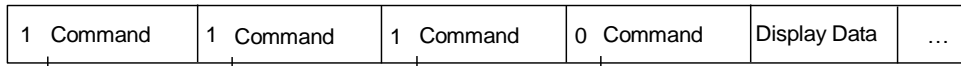


Figure 7. 3-SPI Command/Data transfer format

- Command transfer method

After CSB="H"→"L", 1st byte is always a command input.
 MSB of the command input data will be judged that the next byte data, it is a command or display data (This bit is called "command or data judgment bit").
 When set "command or data judge bit"='1', next byte will be (continuously) command.
 When set "command or data judge bit"='0', next byte data is display data.



Once it becomes display data transfer condition, it will not be back to command input condition even if D/C=1.
 So if you want to send command data again, please set CSB="L"→"H".
 (CSB "L"→"H" will cancel data transfer condition.)
 Command transfer is done by 8bits unit, so if CSB="L"→"H" with less than 8bits data transfer, command will be cancelled.
 It will be able to transfer command with CSB="L" again.

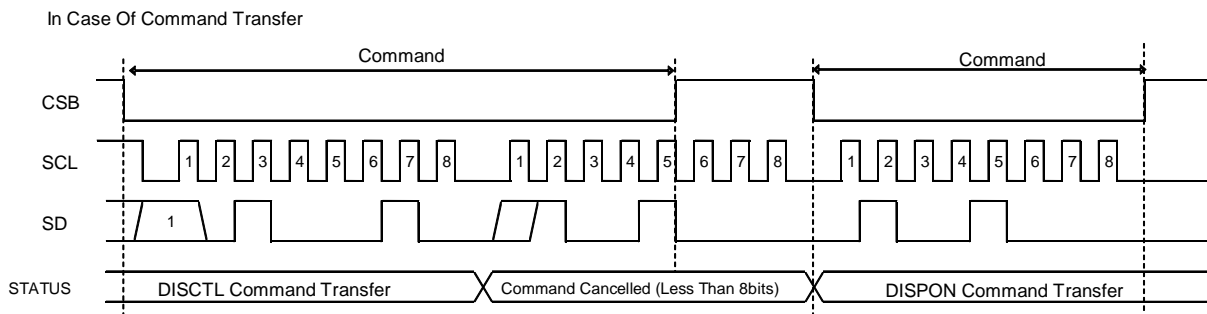
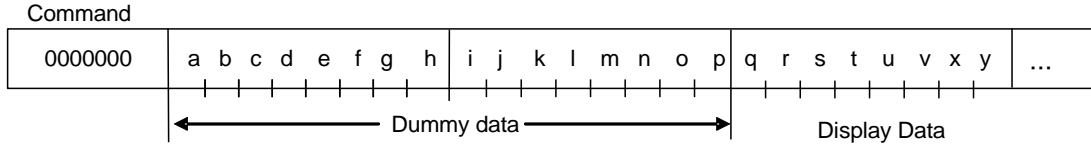


Figure 8. Command transfer format

○Write display data and transfer method

This LSI has Display Data RAM (DDRAM) of 27×4=108bit.

As SEG0, SEG1, SEG2, SEG3, SEG31, SEG32, SEG33, SEG34 are not output, these address will be dummy address. The relationship between data input and display data, DDRAM data and address are as follows.



8 bit data will be stored in DDRAM. The address to be written is the address specified by ADSET command, and the address is automatically incremented in every 4bit data.

Data can be continuously written in DDRAM by transmitting Data continuously.

(When RAM data is written successively after writing RAM data to 22h (SEG34), the address is returned to 00h (SEG0) by the auto-increment function.

| BIT | Dummy data | | | | DDRAM address | | | | | | | | | | | | | Dummy data | | | | COM |
|-----|------------|-------|-------|-------|---------------|-------|-------|-------|-------|--------|--------|--------|--------|--------|---|---|---|------------|------|--|--|-----|
| | 00h | 01h | 02h | 03h | 04h | 05h | 06h | 07h | | 1Eh | 1Fh | 20h | 21h | 22h | 0 | 1 | 2 | 3 | | | | |
| 0 | a | e | i | m | q | u | | | | | | | | | | | | | COM0 | | | |
| 1 | b | f | j | n | r | v | | | | | | | | | | | | | COM1 | | | |
| 2 | c | g | k | o | s | x | | | | | | | | | | | | | COM2 | | | |
| 3 | d | h | l | p | t | y | | | | | | | | | | | | | COM3 | | | |
| | SEG 0 | SEG 1 | SEG 2 | SEG 3 | SEG 4 | SEG 5 | SEG 6 | SEG 7 | | SEG 30 | SEG 31 | SEG 32 | SEG 33 | SEG 34 | | | | | | | | |

As data transfer to DDRAM happens every 4bit data, it will be cancelled if it changes CSB="L"→"H" before 4bits data transfer.

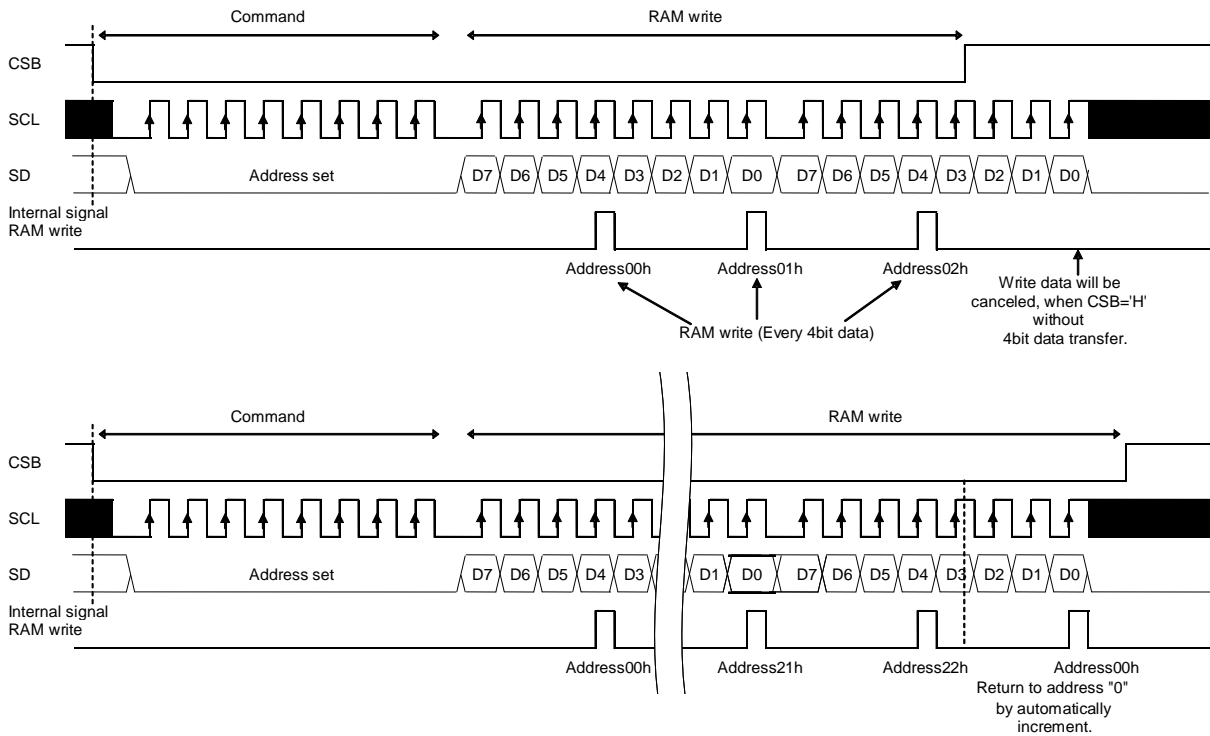


Figure 9. Data Transfer Format

○OSCILLATOR

There are two kinds of clock for logic and analog circuit; from internal oscillator circuit or external clock input. If internal oscillator circuit will be used, OSCIN must be connected to VSS.

*When you use external clock, execute ICSET command and connect OSCIN to external clock.

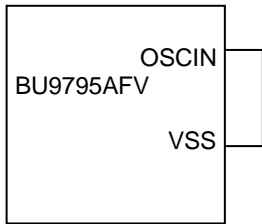


Figure 10. Internal oscillator circuit mode

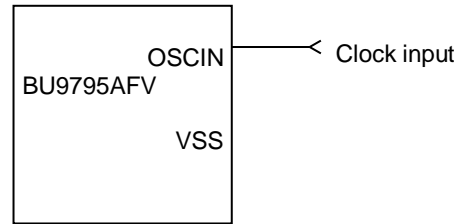


Figure 11. External clock mode

○LCD Driver Bias Circuit

This LSI generates LCD driving voltage with on-chip Buffer AMP.

And it can drive LCD at low power consumption.

*1/3 and 1/2Bias can be set in MODESET command.

*Line and frame inversion can be set in DISCTL command.

Refer to “LCD driving waveform” about each LCD driving waveform.

○Blink timing generator

This device has Blinking function.

*This LSI is able to set blink mode with BLKCTL command.

Blink frequency varies widely by characteristic of fCLK, when internal oscillation circuit.

Refer to Oscillation Characteristics for more details on fCLK.

○Reset (initial) condition

Initial condition after execute SOFTWARE RESET is as follows.

- Display is OFF.
- DDRAM address is initialized (DDRAM Data is not initialized).

Refer to Command Description about initialize value of register.

●Command / Function List

Description List of Command / Function

| No. | Command | Function |
|-----|---------------------------|------------------------|
| 1 | Mode Set (MODESET) | Set LCD drive mode |
| 2 | Address Set (ADSET) | Set LCD display mode 1 |
| 3 | Display Control (DISCTL) | Set LCD display mode 2 |
| 4 | Set IC Operation (ICSET) | Set IC operation |
| 5 | Blink Control (BLKCTL) | Set blink mode |
| 6 | All Pixel Control (APCTL) | Set pixel condition |

●Detailed Command Description

D7 (MSB) is bit for command or data judgment.
Refer to Command and data transfer method.

C : 0 : Next byte is RAM write data.
1 : Next byte is command.

○Mode Set (MODE SET)

| MSB | | | | LSB | | | |
|-----|----|----|----|-----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| C | 1 | 0 | * | P3 | P2 | * | * |

(* : Don't care)

Set display ON and OFF

| Setting | P3 | Reset initialize condition |
|----------------------|----|----------------------------|
| Display OFF(DISPOFF) | 0 | ○ |
| Display ON(DISPON) | 1 | |

Display OFF : Regardless of DDRAM data, all SEGMENT and COMMON output will be stopped after 1 frame of data write. Display OFF mode will be finished by Display ON.

Display ON : SEGMENT and COMMON output will be active and start to read the display data from DDRAM.

(Note) It is not synchronize with display frame, when it will be controlled display ON/OFF with INHb terminal.

Set bias level

| Setting | P2 | Reset initialize condition |
|----------|----|----------------------------|
| 1/3 Bias | 0 | ○ |
| 1/2 Bias | 1 | |

Refer to LCD driving waveform.

○Address set (ADSET)

| MSB | | | | LSB | | | |
|-----|----|----|----|-----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| C | 0 | 0 | P4 | P3 | P2 | P1 | P0 |

Address data is specified in P[4 : 0] and P2 (ICSET command) as follows.

| | MSB | | | LSB |
|---------------------|-------------|-------------|-------|-------------|
| Internal register | Address [5] | Address [4] | . . . | Address [0] |
| Bit of each command | ICSET [P2] | ADSET [P4] | . . . | ADSET [P0] |

The address is 00h in reset condition. The valid address is 00h to 22h.

Another address is invalid, (otherwise address will be set to 00h.)

P2 of ICSET command is only to define either MSB of address is "1" or "0".

Address counter will be set only when ADSET command is executed.

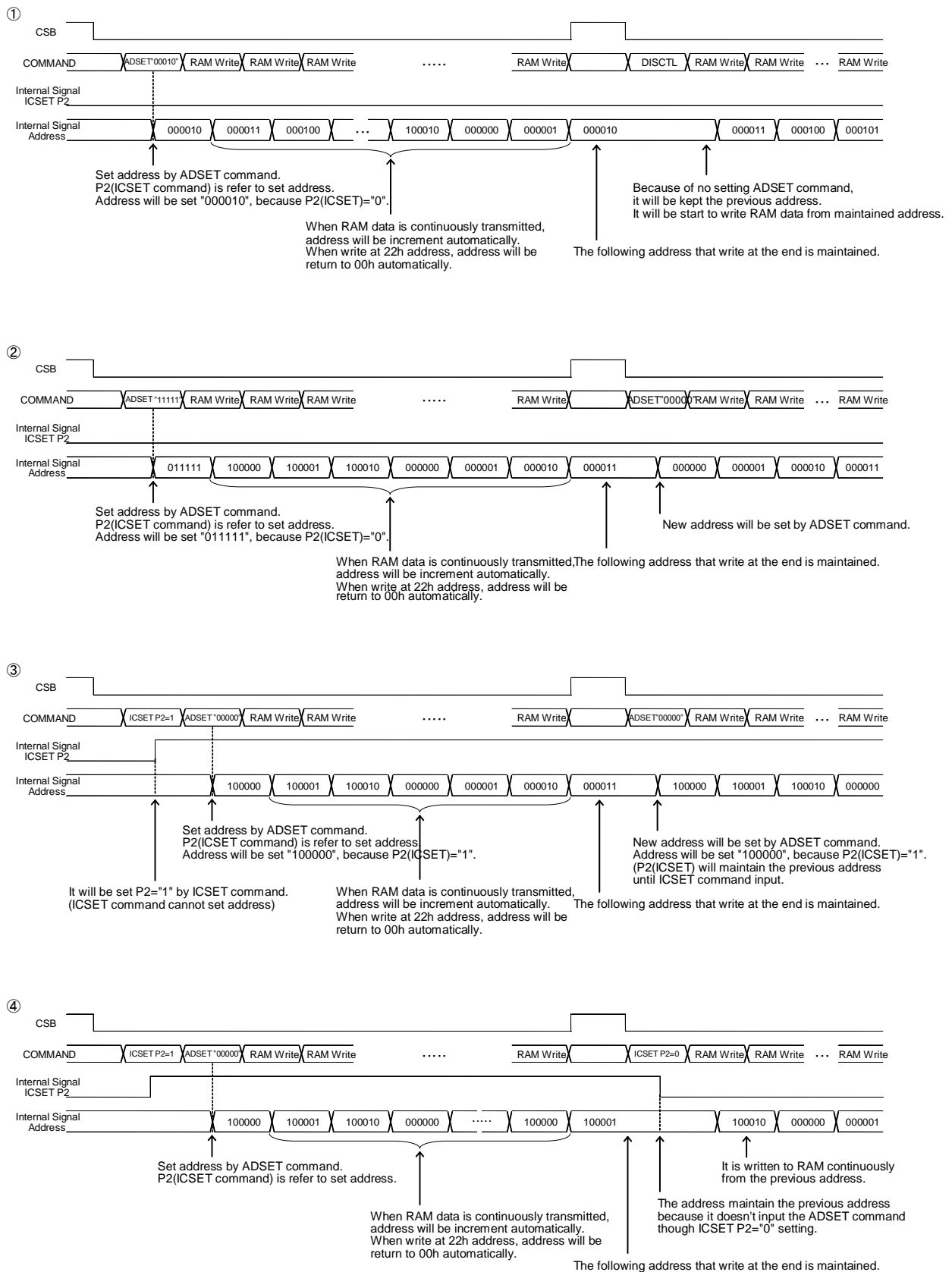


Figure 12. Address Set sequence

○Display control (DISCTL)

| | | | | | | | |
|-----|----|----|----|-----|----|----|----|
| MSB | | | | LSB | | | |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| C | 0 | 1 | P4 | P3 | P2 | P1 | P0 |

Set Frame frequency

| Setting | P4 | P3 | Reset initialize condition |
|---------|----|----|----------------------------|
| 80Hz | 0 | 0 | ○ |
| 71Hz | 0 | 1 | |
| 64Hz | 1 | 0 | |
| 53Hz | 1 | 1 | |

* About the characteristics of FR, refer to Oscillation characteristics.

Set LCD drive waveform

| Setting | P2 | Reset initialize condition |
|-----------------|----|----------------------------|
| Line inversion | 0 | ○ |
| Frame inversion | 1 | |

Set Power save mode

| Setting | P1 | P0 | Reset initialize condition |
|-------------------|----|----|----------------------------|
| Power save mode 1 | 0 | 0 | |
| Power save mode 2 | 0 | 1 | |
| Normal mode | 1 | 0 | ○ |
| High power mode | 1 | 1 | |

*VDD-VLCD≥3.0V is required for High power mode.

(Reference current consumption data)

| Setting | Reset initialize condition |
|-------------------|----------------------------|
| Power save mode 1 | ×0.5 |
| Power save mode 2 | ×0.67 |
| Normal mode | ×1.0 |
| High power mode | ×1.8 |

*Above current consumption data is reference value. It depends on panel load.

(Note) Frame rate FR / LCD drive waveform / Power save mode SR will effect display image.
Select the best value in point of current consumption and display image using LCD panel (under real application).

| Mode | Screen flicker | Display image / contrast |
|--------------------|----------------|--------------------------|
| Frame frequency | ○ | - |
| LCD drive waveform | ○ | ○ |
| Power save mode | - | ○ |

○Set IC Operation (ICSET)

| MSB | | | | LSB | | | |
|-----|----|----|----|-----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| C | 1 | 1 | 0 | 1 | P2 | P1 | P0 |

P2 : MSB data of DDRAM address. Please refer to “ADSET” command.

| Setting | P2 | Reset initialize condition |
|----------------|----|----------------------------|
| Address MSB'0' | 0 | ○ |
| Address MSB'1' | 1 | |

Set Software Reset condition

| Setting | P1 |
|----------------|----|
| No operation | 0 |
| Software Reset | 1 |

When “Software Reset” is executed, this LSI will be reset to initial condition.

If software reset is executed, the value of P2 and P1 will be ignored and they will be set initialized condition. (Refer to “Reset initial condition”)

Switch between internal clock and external clock.

| Setting | P0 | Reset initialize condition |
|----------------------|----|----------------------------|
| Internal clock | 0 | ○ |
| External clock input | 1 | |

For internal clock : OSCIN is connected to VSS.

For external clock input : Input external clock into OSCIN.

<external Clock Frame frequency calculation>

DISCTL 80Hz select : Frame frequency [Hz] = external clock[Hz] / 512

DISCTL 71Hz select : Frame frequency [Hz] = external clock[Hz] / 576

DISCTL 64Hz select : Frame frequency [Hz] = external clock[Hz] / 648

DISCTL 53Hz select : Frame frequency [Hz] = external clock[Hz] / 768

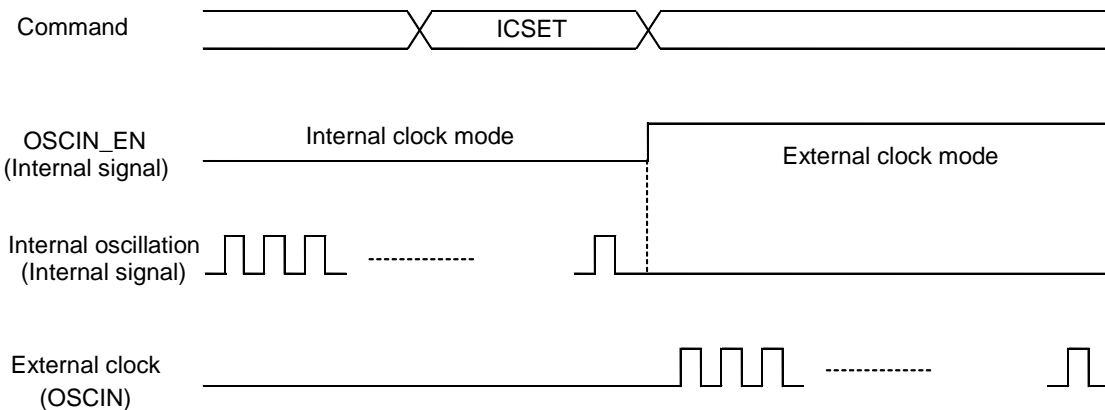


Figure 13. OSCMODE switching timing

○Blink control (BLKCTL)

| MSB | | | | LSB | | | |
|-----|----|----|----|-----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| C | 1 | 1 | 1 | 0 | * | P1 | P0 |

Set blink condition

| Setting (Hz) | P1 | P0 | Reset initialize condition |
|--------------|----|----|----------------------------|
| OFF | 0 | 0 | ○ |
| 0.5 | 0 | 1 | |
| 1 | 1 | 0 | |
| 2 | 1 | 1 | |

○All pixel control (APCTL)

| MSB | | | | LSB | | | |
|-----|----|----|----|-----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| C | 1 | 1 | 1 | 1 | 1 | P1 | P0 |

All display set ON. OFF

| Setting | P1 | Reset initialize condition |
|--------------|----|----------------------------|
| Normal | 0 | ○ |
| All pixel ON | 1 | |

| Setting | P0 | Reset initialize condition |
|---------------|----|----------------------------|
| Normal | 0 | ○ |
| All pixel OFF | 1 | |

All pixels ON : All pixels are ON regardless of DDRAM data.

All pixels OFF : All pixels are OFF regardless of DDRAM data.

(Note) All pixels ON/OFF is effective only at the time of "Display ON" status.

The data of DDRAM do not change with this command.

If both P1 and P0='1', APOFF is selected. APOFF has higher priority than APON.

●LCD driving waveform

(1/3bias)

Line inversion

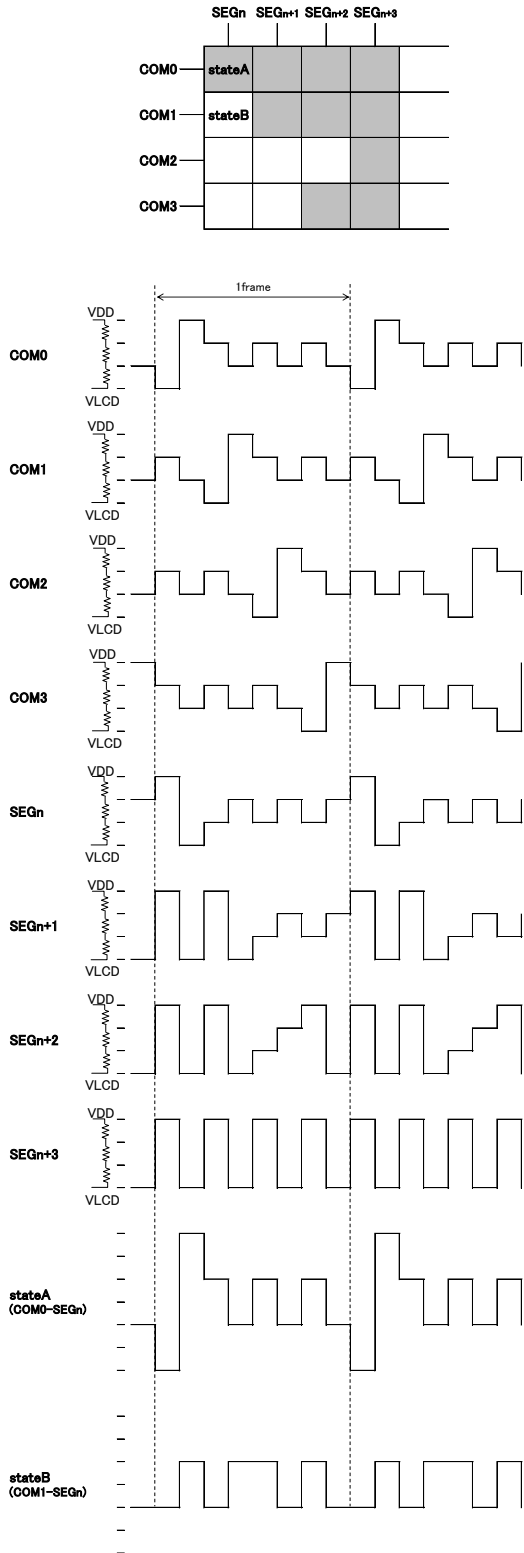


Figure 14. Line inversion waveform(1/3bias)

Frame inversion

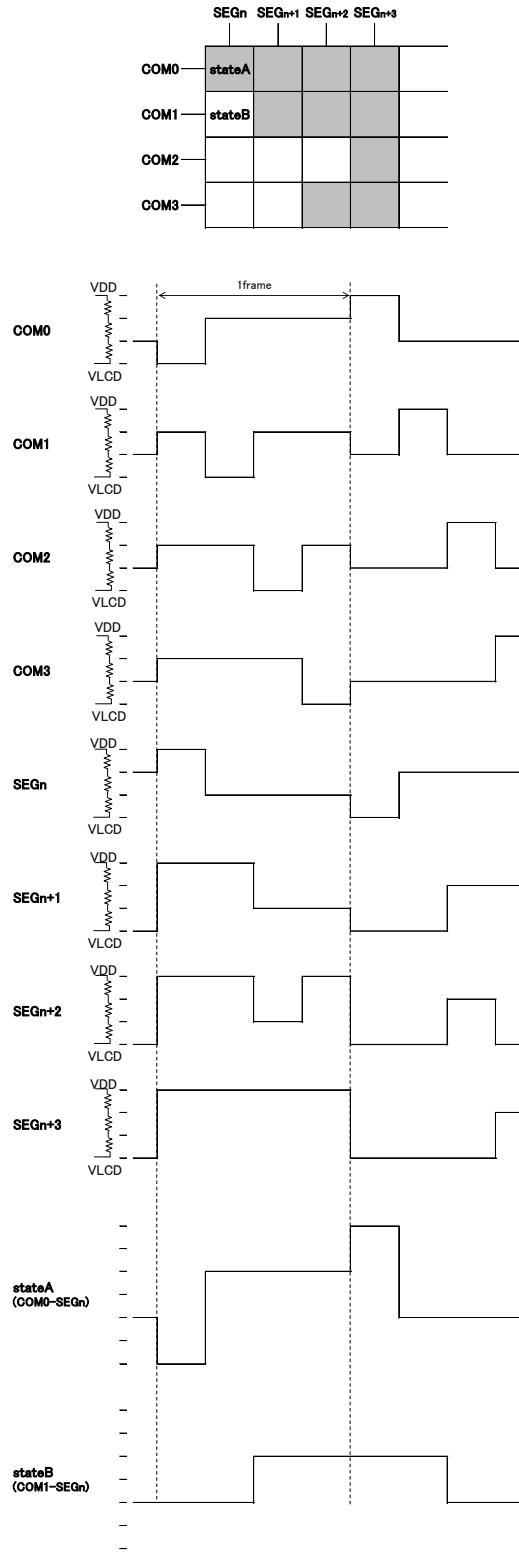


Figure 15. Frame inversion waveform(1/3bias)

(1/2bias)
Line inversion

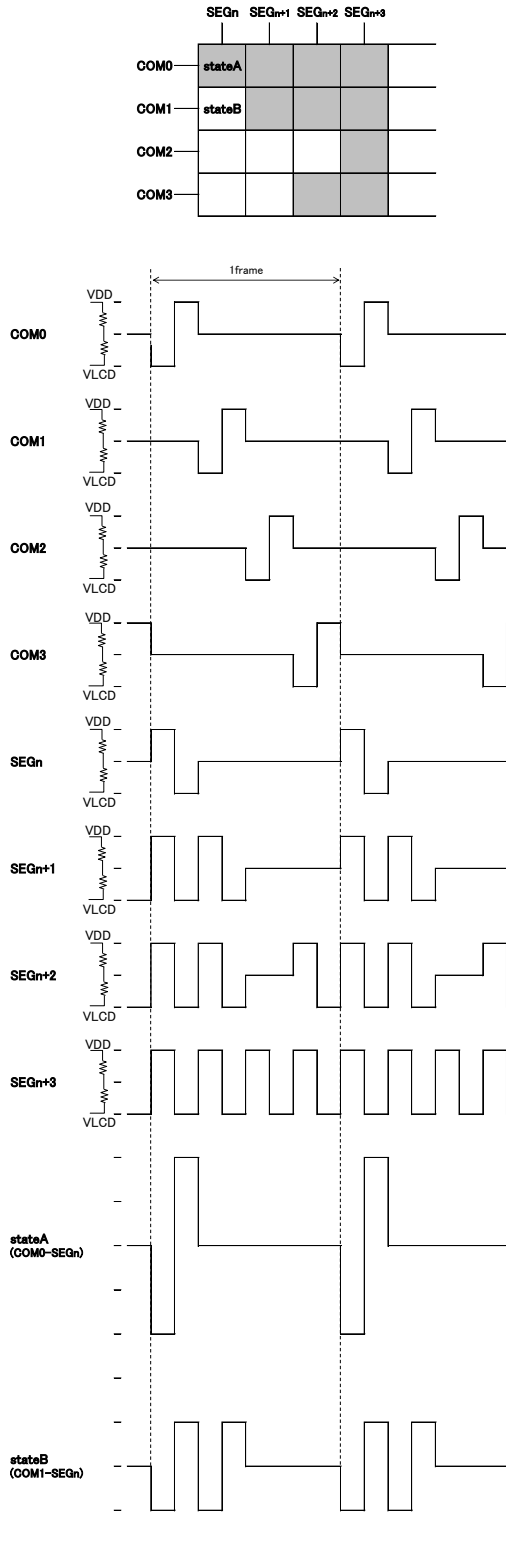


Figure 16. Line inversion waveform(1/2bias)

Frame inversion

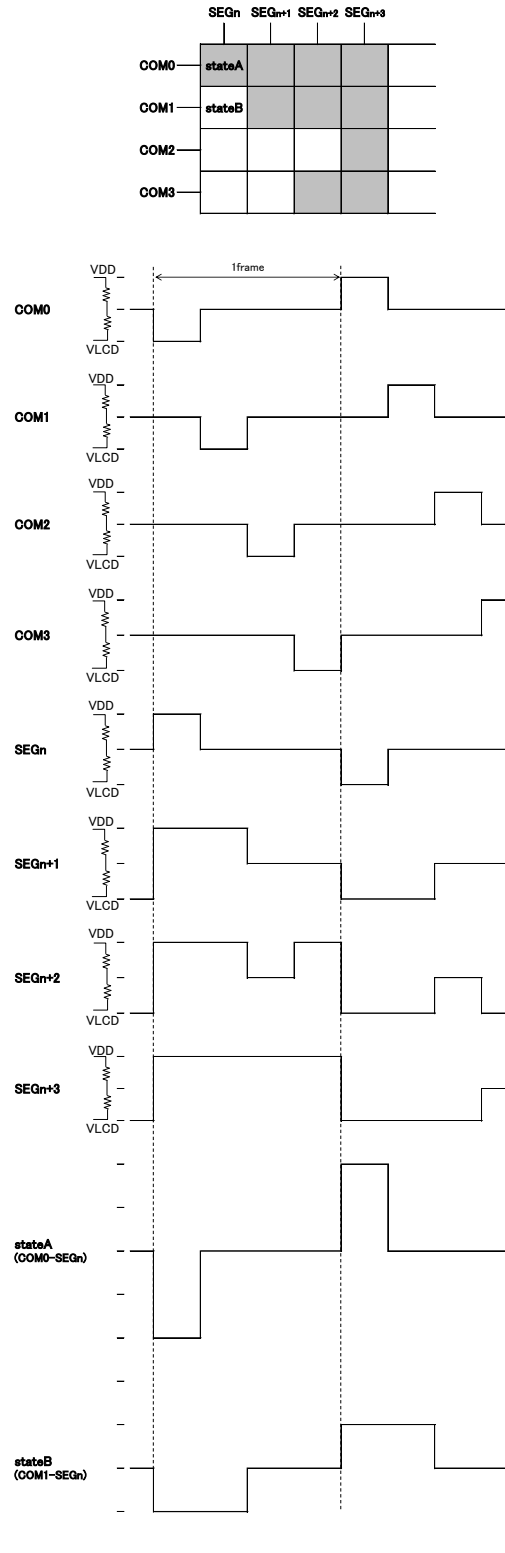


Figure 17. Frame inversion waveform(1/2bias)

●Example of display data

If LCD layout pattern is shown as in Figure18, Figure19 and DDRAM data is shown as in Table 2, display pattern will be shown as in Figure 20.

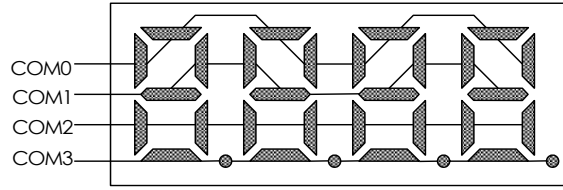


Figure 18. Example COM line pattern

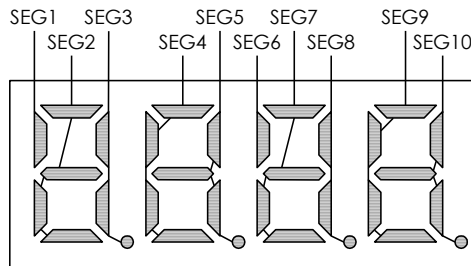


Figure 19. Example SEG line pattern



Figure 20. Example Display pattern

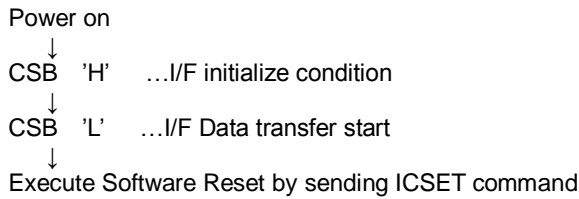
Table 2. DDRAM Data map

| | | Dummy data | | | | S | S | S | S | S | S | S | S | S | S | S | S | S | S | S | |
|---------|----|------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| | | S | S | S | S | S | S | S | S | S | S | S | S | S | S | S | S | S | S | S | |
| | | E | E | E | E | E | E | E | E | E | E | E | E | E | E | E | E | E | E | E | |
| | | G | G | G | G | G | G | G | G | G | G | G | G | G | G | G | G | G | G | G | |
| | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 |
| COM0 | D0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| COM1 | D1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| COM2 | D2 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| COM3 | D3 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Address | | 00h | 01h | 02h | 03h | 04h | 05h | 06h | 07h | 08h | 09h | 0Ah | 0Bh | 0Ch | 0Dh | 0Eh | 0Fh | 10h | 11h | 12h | 13h |

As SEG0, SEG1, SEG2, SEG3, SEG31, SEG32, SEG33, SEG34 are not output, 00h – 03h address will be dummy address.

●Initialize sequence

Please follow sequence below after Power-On to set this device to initial condition.



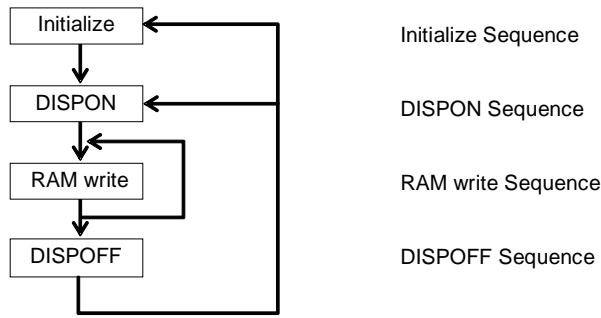
* Each register value and DDRAM address, DDRAM data are random condition after power on till initialize sequence is executed.

●Start sequence

○Start sequence example 1

| No. | Input | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Descriptions |
|-----|--------------|----|----|----|----|----|----|----|----|-------------------------|
| 1 | Power on | | | | | | | | | VDD=0 to 5V (Tr=0.1ms) |
| | ↓ | | | | | | | | | |
| 2 | wait 100μs | | | | | | | | | Initialize IC |
| | ↓ | | | | | | | | | |
| 3 | CSB 'H' | | | | | | | | | Initialize I/F data |
| | ↓ | | | | | | | | | |
| 4 | CSB 'L' | | | | | | | | | I/F Data transfer start |
| | ↓ | | | | | | | | | |
| 5 | ICSET | 1 | 1 | 1 | 0 | 1 | * | 1 | 0 | Software Reset |
| | ↓ | | | | | | | | | |
| 6 | BLKCTL | 1 | 1 | 1 | 1 | 0 | * | 0 | 1 | |
| | ↓ | | | | | | | | | |
| 7 | DISCTL | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | |
| | ↓ | | | | | | | | | |
| 8 | ICSET | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | RAM address MSB set |
| | ↓ | | | | | | | | | |
| 9 | ADSET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | RAM address set |
| | ↓ | | | | | | | | | |
| 10 | Display Data | * | * | * | * | * | * | * | * | address 00h to 01h |
| | Display Data | * | * | * | * | * | * | * | * | address 02h to 03h |
| | ⋮ | | | | | | | | | ⋮ |
| | Display Data | * | * | * | * | * | * | * | * | address 22h to 00h |
| | ↓ | | | | | | | | | |
| 11 | CSB 'H' | | | | | | | | | I/F Data transfer stop |
| | ↓ | | | | | | | | | |
| 12 | CSB 'L' | | | | | | | | | I/F Data transfer start |
| | ↓ | | | | | | | | | |
| 13 | MODESET | 1 | 1 | 0 | * | 1 | 0 | * | * | Display ON |
| | ↓ | | | | | | | | | |
| 14 | CSB 'H' | | | | | | | | | I/F Data transfer stop |

Start sequence example 2



This LSI is initialized with Initialize Sequence. And start to display with DISPON Sequence.
 This LSI will update display data with RAM write Sequence.
 And stop the display with DISPOFF sequence.
 If you want to restart to display, This LSI will restart to display with DISPON Sequence.

Initialize sequence

| Input | DATA | | | | | | | | Description |
|--|------|----|----|----|----|----|----|----|-----------------------------------|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| Power on wait 100µs CSB 'H' CSB 'L' | | | | | | | | | IC initialized I/F initialized |
| ICSET | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | Software Reset |
| MODESET | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | Display OFF |
| ADSET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | RAM address set |
| Display Data ... | * | * | * | * | * | * | * | * | Display data |
| CSB 'H' | | | | | | | | | |

DISPON sequence

| Input | DATA | | | | | | | | Description |
|---------|------|----|----|----|----|----|----|----|-----------------|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| CSB 'L' | | | | | | | | | |
| DISCTL | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | Display Control |
| BLKCTL | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | BLKCTL |
| APCTL | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | APCTL |
| MODESET | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | Display ON |
| CSB 'H' | | | | | | | | | |

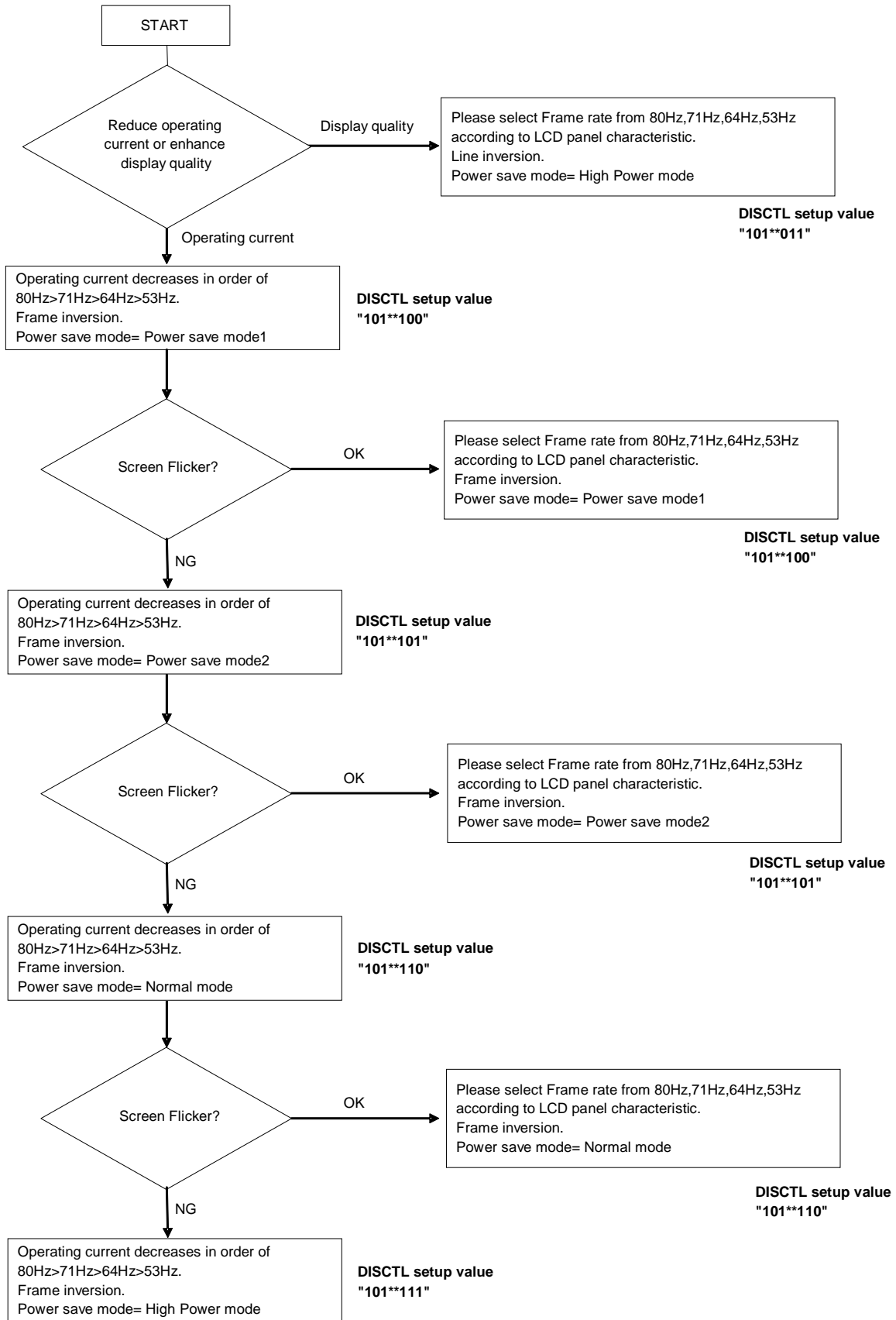
RAM write sequence

| Input | DATA | | | | | | | | Description |
|---------------------|------|----|----|----|----|----|----|----|-----------------|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| CSB 'L' | | | | | | | | | |
| DISCTL | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | Display Control |
| BLKCTL | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | BLKCTL |
| APCTL | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | APCTL |
| MODESET | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | Display ON |
| ADSET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | RAM address set |
| Display Data ... | * | * | * | * | * | * | * | * | Display data |
| CSB 'H' | | | | | | | | | |

DISPOFF sequence

| Input | DATA | | | | | | | | Description |
|---------|------|----|----|----|----|----|----|----|-------------|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| CSB 'L' | | | | | | | | | |
| MODESET | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | Display OFF |
| CSB 'H' | | | | | | | | | |

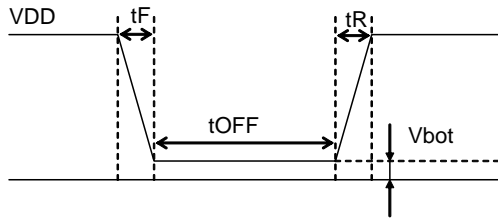
●Example of start sequence



●Cautions on Power ON condition

This LSI has "P.O.R" (Power-On Reset) circuit and Software Reset function.
Please keep the following recommended Power-On conditions in order to power up properly.

Please set power up conditions to meet the recommended t_R , t_F , t_{OFF} , and V_{bot} spec below in order to ensure P.O.R operation.



Recommended condition of t_R , t_F , t_{OFF} , V_{bot}

| t_R | t_F | t_{OFF} | V_{bot} |
|---------------|---------------|-----------------|----------------|
| Less than 1ms | Less than 1ms | More than 150ms | Less than 0.1V |

Figure 21. Power ON/OFF waveform

If it is difficult to meet above conditions, execute the following sequence after Power-On.
Command input is not accepted during power off. It has to take care that software reset is not a perfect substitute to POR function.

(1) CSB="L"→"H" condition

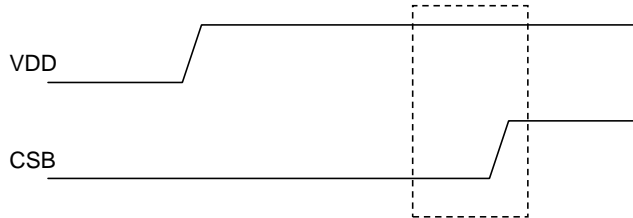


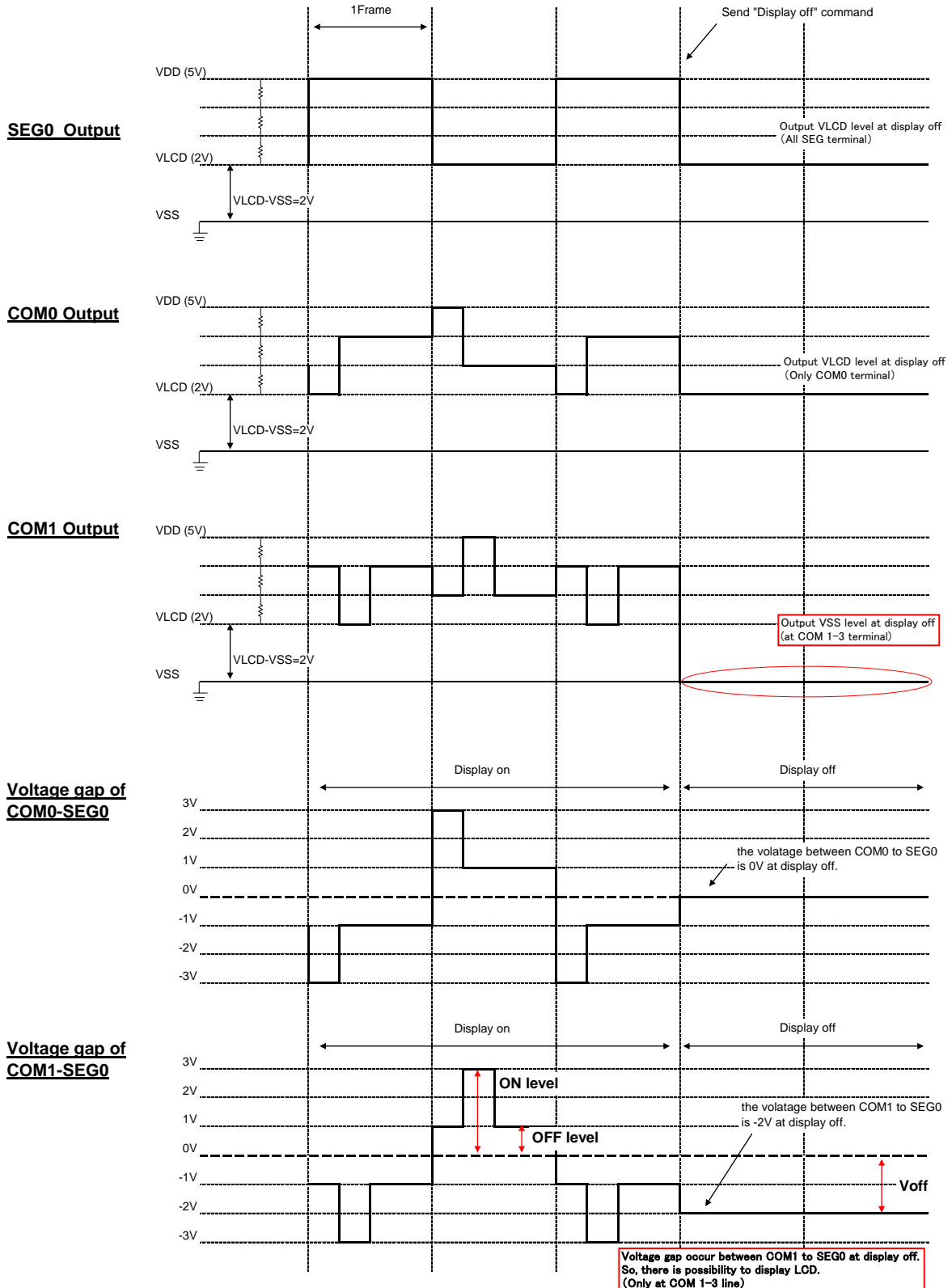
Figure 22. CSB Timing

(2) After CSB"H"→"L", execute Software Reset (ICSET command).

●Cautions on application

In case, BU9795AFV used at VLCD≠VSS, voltage gap occur between SEG line to COM1–3 line at Display off state. Because of this voltage gap, there is possibility to display LCD for a moment. To avoid this phenomenon, please decide VDD and VLCD level to satisfy Voff voltage lower than OFF level (OFF level = 1V at the example explained below).

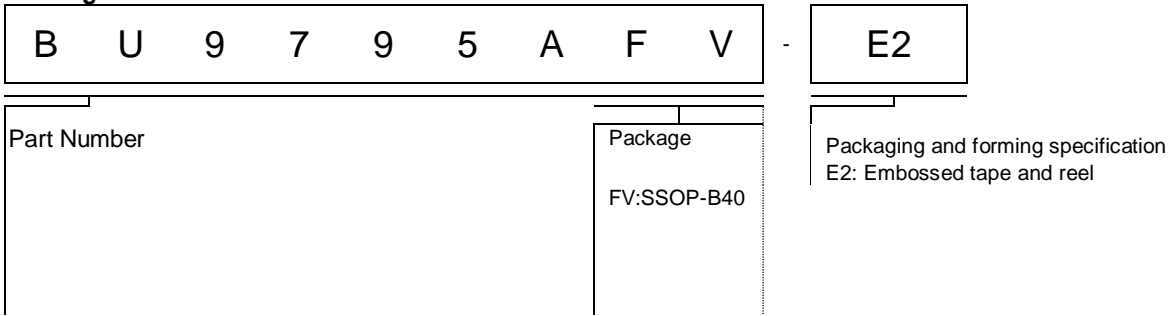
condition : VDD=5.0V
 VLCD=2.0V
 1/3bias
 DDRAM data ALL "H"
 Frame inversion



•Operational Notes

- (1) Absolute Maximum Ratings
Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.
- (2) Recommended Operating conditions
These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.
- (3) Reverse Connection of Power Supply
Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply terminals.
- (4) Power Supply Lines
Design the PCB layout pattern to provide low impedance ground and supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.
- (5) Ground Voltage
The voltage of the ground pin must be the lowest voltage of all pins of the IC at all operating conditions. Ensure that no pins are at a voltage below the ground pin at any time, even during transient condition.
- (6) Short between Pins and Mounting Errors
Be careful when mounting the IC on printed circuit boards. The IC may be damaged if it is mounted in a wrong orientation or if pins are shorted together. Short circuit may be caused by conductive particles caught between the pins.
- (7) Operation under Strong Electromagnetic Field
Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.
- (8) Testing on Application Boards
When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.
- (9) Regarding Input Pins of the IC
In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the GND voltage should be avoided. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input terminals have voltages within the values specified in the electrical characteristics of this IC.
- (10) GND Wiring Pattern
When using both small-signal and large-current GND traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the GND traces of external components do not cause variations on the GND voltage. The power supply and ground lines must be as short and thick as possible to reduce line impedance.
- (11) External Capacitor
When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.
- (12) Unused Input Terminals
Input terminals of an IC are often connected to the gate of a CMOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of IC. So unless otherwise specified, input terminals not being used should be connected to the power supply or ground line.
- (13) Rush current
When power is first supplied to the IC, rush current may flow instantaneously. It is possible that the charge current to the parasitic capacitance of internal photo diode or the internal logic may be unstable. Therefore, give special consideration to power coupling capacitance, power wiring, width of GND wiring, and routing of connections.

•Ordering Information

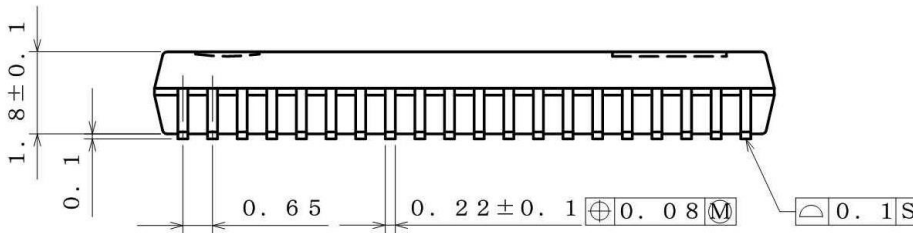
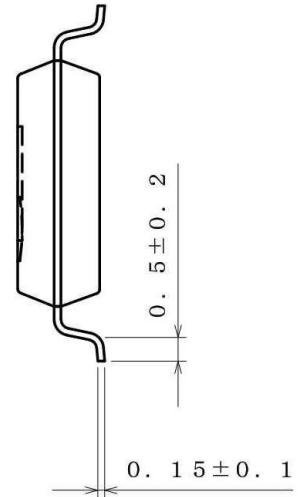
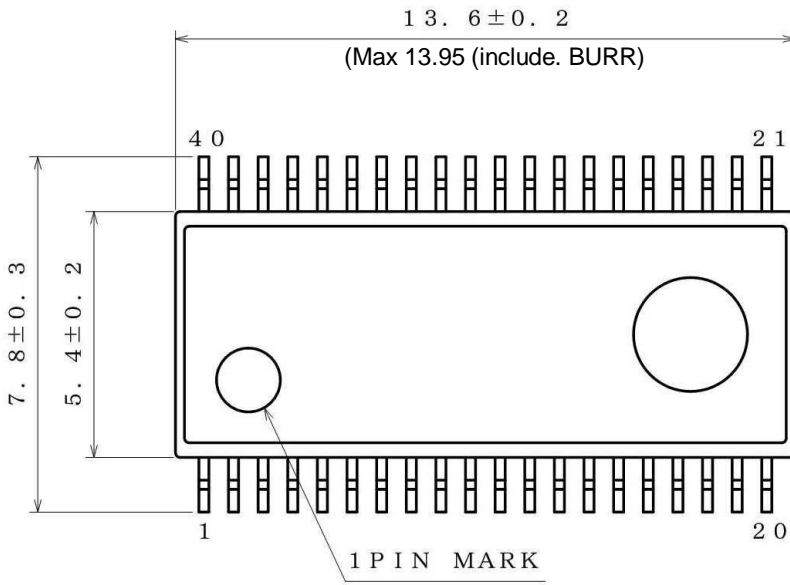


•Lineup

| Segment output | Common output | Package | | Orderable Part Number |
|----------------|---------------|----------|--------------|-----------------------|
| 27 | 4 | SSOP-B40 | Reel of 2000 | BU9795AFV-E2 |

●Physical Dimension Tape and Reel Information

| | |
|--------------|----------|
| Package Name | SSOP-B40 |
|--------------|----------|



(UNIT ; mm)

PKG : SSOP-B40

図番 ; EX157-5001

<Tape and Reel information>

| | |
|-------------------|---|
| Tape | Embossed carrier tape |
| Quantity | 2000pcs |
| Direction of feed | E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand) |

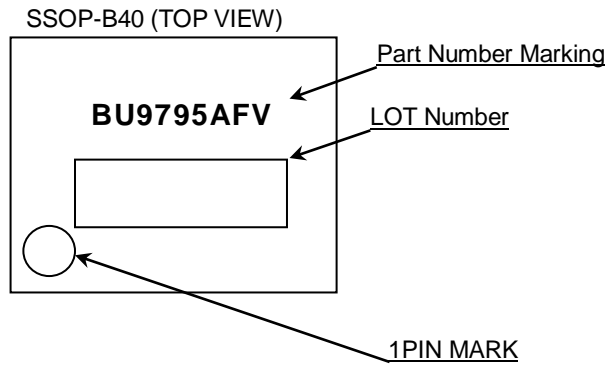
Reel

1pin

Direction of feed

*Order quantity needs to be multiple of the minimum quantity.

●Marking Diagrams



| Part Number | Package | Part Number Marking |
|-------------|----------|---------------------|
| BU9795AFV | SSOP-B40 | BU9795AFV |

●Revision History

| Date | Revision | Changes |
|--------------|----------|--|
| 14.Mar.2012 | 001 | New Release |
| 12.July.2012 | 002 | Add BU9795AKS2 |
| 8.Jan.2013 | 003 | Improved the statement in all pages. Deleted "Status of this document" in page 30. |
| 20.Mar.2019 | 004 | Remove BU9795AKV (VQFP48C) Remove BU9795AGUW (VBGA048W040) Remove BU9795AKS2 (SQFP-T52M) |

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| JAPAN | USA | EU | CHINA |
|-----------|-----------|------------|-----------|
| CLASS III | CLASS III | CLASS II b | CLASS III |
| CLASS IV | | CLASS III | |

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 - Installation of redundant circuits to reduce the impact of single or multiple circuit failure
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 - Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
 - Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
 - Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
 - Sealing or coating our Products with resin or other coating materials
 - Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.) ; or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - Use of the Products in places subject to dew condensation
- The Products are not subject to radiation-proof design.
- Please verify and confirm characteristics of the final or mounted products in using the Products.
- In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
- Confirm that operation temperature is within the specified range described in the product specification.
- ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

- When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
- In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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 - [b] the temperature or humidity exceeds those recommended by ROHM
 - [c] the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
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