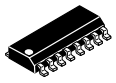
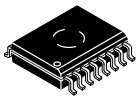
BCD-to-Seven Segment Latch/Decoder/Driver

MC14511B



SOIC−16
D SUFFIX
CASE 751B



SO−16 WB
DW SUFFIX
CASE 751G

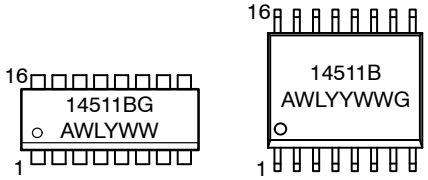
The MC14511B BCD−to−seven segment latch/decoder/driver is constructed with complementary MOS (CMOS) enhancement mode devices and NPN bipolar output drivers in a single monolithic structure. The circuit provides the functions of a 4−bit storage latch, an 8421 BCD−to−seven segment decoder, and an output drive capability. Lamp test ($\overline{LT}$), blanking ($\overline{BI}$), and latch enable (LE) inputs are used to test the display, to turn−off or pulse modulate the brightness of the display, and to store a BCD code, respectively. It can be used with seven−segment light−emitting diodes (LED), incandescent, fluorescent, gas discharge, or liquid crystal readouts either directly or indirectly.

Applications include instrument (e.g., counter, DVM, etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

Features

- Low Logic Circuit Power Dissipation
- High−Current Sourcing Outputs (Up to 25 mA)
- Latch Storage of Code
- Blanking Input
- Lamp Test Provision
- Readout Blanking on all Illegal Input Combinations
- Lamp Intensity Modulation Capability
- Time Share (Multiplexing) Facility
- Supply Voltage Range = 3.0 V to 18 V
- Capable of Driving Two Low−power TTL Loads, One Low−power Schottky TTL Load, or Two HTL Loads Over the Rated Temperature Range
- Chip Complexity: 216 FETs or 54 Equivalent Gates
- Triple Diode Protection on all Inputs
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

MARKING DIAGRAMS



SOIC−16 SO−16 WB

A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G = Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 1)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}	Input Voltage Range, All Inputs	−0.5 to V_{DD} + 0.5	V
I	DC Current Drain per Input Pin	10	mA
P_D	Power Dissipation, per Package (Note 2)	500	mW
T_A	Operating Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
I_{OHmax}	Maximum Output Drive Current (Source) per Output	25	mA
P_{OHmax}	Maximum Continuous Output Power (Source) per Output (Note 3)	50	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Temperature Derating: “D/DW” Packages: −7.0 mW/°C From 65°C to 125°C
3. $P_{OHmax} = I_{OH} (V_{DD} - V_{OH})$

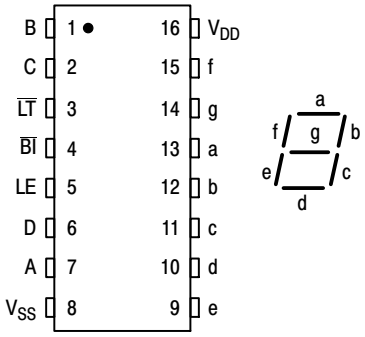
March, 2022 − Rev. 13
Publication Order Number:
MC14511B/D

This device contains protection circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high−impedance circuit. A destructive high current mode may occur if V_{in} and V_{out} are not constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

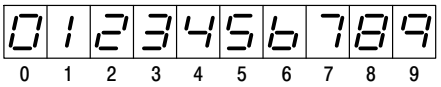
Due to the sourcing capability of this circuit, damage can occur to the device if V_{DD} is applied, and the outputs are shorted to V_{SS} and are at a logical 1 (See Maximum Ratings).

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

PIN ASSIGNMENT



DISPLAY



TRUTH TABLE

Inputs							Outputs							
LE	BI	LT	D	C	B	A	a	b	c	d	e	f	g	Display
X	X	0	X	X	X	X	1	1	1	1	1	1	1	8
X	0	1	X	X	X	X	0	0	0	0	0	0	0	Blank
0	1	1	0	0	0	0	1	1	1	1	1	1	0	0
0	1	1	0	0	0	1	0	1	1	0	0	0	0	1
0	1	1	0	0	1	0	1	1	0	1	1	0	1	2
0	1	1	0	0	1	1	1	1	1	1	0	0	1	3
0	1	1	0	1	0	0	0	1	1	0	0	1	1	4
0	1	1	0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	0	1	1	1	1	1	1	0	0	0	0	7
0	1	1	1	0	0	0	1	1	1	1	1	1	1	8
0	1	1	1	0	0	1	1	1	1	0	0	1	1	9
0	1	1	1	0	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	0	1	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	1	0	0	0	0	0	0	0	Blank
1	1	1	X	X	X	X				*				*

X = Don't Care

*Depends upon the BCD code previously applied when LE = 0

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	– 55°C Min	– 55°C Max	25°C Min	25°C Typ (Note 4)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage “0” Level V_{in} = V_{DD} or 0	V_{OL}	5.0 10 15	– – –	0.05 0.05 0.05	– – –	0 0 0	0.05 0.05 0.05	– – –	0.05 0.05 0.05	Vdc
“1” Level V_{in} = 0 or V_{DD}	V_{OH}	5.0 10 15	4.1 9.1 14.1	– – –	4.1 9.1 14.1	4.57 9.58 14.59	– – –	4.1 9.1 14.1	– – –	Vdc
Input Voltage # “0” Level (V_O = 3.8 or 0.5 Vdc) (V_O = 8.8 or 1.0 Vdc) (V_O = 13.8 or 1.5 Vdc)	V_{IL}	5.0 10 15	– – –	1.5 3.0 4.0	– – –	2.25 4.50 6.75	1.5 3.0 4.0	– – –	1.5 3.0 4.0	Vdc
“1” Level (V_O = 0.5 or 3.8 Vdc) (V_O = 1.0 or 8.8 Vdc) (V_O = 1.5 or 13.8 Vdc)	V_{IH}	5.0 10 15	3.5 7.0 11	– – –	3.5 7.0 11	2.75 5.50 8.25	– – –	3.5 7.0 11	– – –	Vdc
Output Drive Voltage (I_{OH} = 0 mA) Source	V_{OH}	5.0	4.1	–	4.1	4.57	–	4.1	–	Vdc
(I_{OH} = 5.0 mA)			–	–	–	4.24	–	–	–	
(I_{OH} = 10 mA)			3.9	–	3.9	4.12	–	3.5	–	
(I_{OH} = 15 mA)			–	–	–	3.94	–	–	–	
(I_{OH} = 20 mA)			3.4	–	3.4	3.70	–	3.0	–	
(I_{OH} = 25 mA)			–	–	–	3.54	–	–	–	
(I_{OH} = 0 mA)		10	9.1	–	9.1	9.58	–	9.1	–	Vdc
(I_{OH} = 5.0 mA)			–	–	–	9.26	–	–	–	
(I_{OH} = 10 mA)			9.0	–	9.0	9.17	–	8.6	–	
(I_{OH} = 15 mA)			–	–	–	9.04	–	–	–	
(I_{OH} = 20 mA)			8.6	–	8.6	8.90	–	8.2	–	
(I_{OH} = 25 mA)			–	–	–	8.70	–	–	–	
(I_{OH} = 0 mA)		15	14.1	–	14.1	14.59	–	14.1	–	Vdc
(I_{OH} = 5.0 mA)			–	–	–	14.27	–	–	–	
(I_{OH} = 10 mA)			14	–	14	14.18	–	13.6	–	
(I_{OH} = 15 mA)			–	–	–	14.07	–	–	–	
(I_{OH} = 20 mA)			13.6	–	13.6	13.95	–	13.2	–	
(I_{OH} = 25 mA)			–	–	–	13.70	–	–	–	
Output Drive Current (V_{OL} = 0.4 V) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 V)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 V)		15	4.2	–	3.4	8.8	–	2.4	–	
Input Current	I_{in}	15	–	± 0.1	–	±0.00001	± 0.1	–	± 1.0	μAdc
Input Capacitance	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (Per Package) V_{in} = 0 or V_{DD}, I_{out} = 0 μA	I_{DD}	5.0 10 15	– – –	5.0 10 20	– – –	0.005 0.010 0.015	5.0 10 20	– – –	150 300 600	μAdc
Total Supply Current (Notes 5 & 6) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0 10 15	I_T = (1.9 μA/kHz) f + I_{DD} I_T = (3.8 μA/kHz) f + I_{DD} I_T = (5.7 μA/kHz) f + I_{DD}							μAdc

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Noise immunity specified for worst−case input combination.
   Noise Margin for both “1” and “0” level =
   1.0 Vdc min @ V_{DD} = 5.0 Vdc
   2.0 Vdc min @ V_{DD} = 10 Vdc
   2.5 Vdc min @ V_{DD} = 15 Vdc
5. The formulas given are for the typical characteristics only at 25°C.
6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + 3.5 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

SWITCHING CHARACTERISTICS (Note 7) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time t_{TLH} = (0.40 ns/pF) C_L + 20 ns t_{TLH} = (0.25 ns/pF) C_L + 17.5 ns t_{TLH} = (0.20 ns/pF) C_L + 15 ns	t_{TLH}	5.0 10 15	– – –	40 30 25	80 60 50	ns
Output Fall Time t_{THL} = (1.5 ns/pF) C_L + 50 ns t_{THL} = (0.75 ns/pF) C_L + 37.5 ns t_{THL} = (0.55 ns/pF) C_L + 37.5 ns	t_{THL}	5.0 10 15	– – –	125 75 65	250 150 130	ns
Data Propagation Delay Time t_{PLH} = (0.40 ns/pF) C_L + 620 ns t_{PLH} = (0.25 ns/pF) C_L + 237.5 ns t_{PLH} = (0.20 ns/pF) C_L + 165 ns	t_{PLH}	5.0 10 15	– – –	640 250 175	1280 500 350	ns
t_{PHL} = (1.3 ns/pF) C_L + 655 ns t_{PHL} = (0.60 ns/pF) C_L + 260 ns t_{PHL} = (0.35 ns/pF) C_L + 182.5 ns	t_{PHL}	5.0 10 15	– – –	720 290 200	1440 580 400	
$\overline{\text{Blank}}$ Propagation Delay Time t_{PLH} = (0.30 ns/pF) C_L + 585 ns t_{PLH} = (0.25 ns/pF) C_L + 187.5 ns t_{PLH} = (0.15 ns/pF) C_L + 142.5 ns	t_{PLH}	5.0 10 15	– – –	600 200 150	750 300 220	ns
t_{PHL} = (0.85 ns/pF) C_L + 442.5 ns t_{PHL} = (0.45 ns/pF) C_L + 177.5 ns t_{PHL} = (0.35 ns/pF) C_L + 142.5 ns	t_{PHL}	5.0 10 15	– – –	485 200 160	970 400 320	
$\overline{\text{Lamp Test}}$ Propagation Delay Time t_{PLH} = (0.45 ns/pF) C_L + 290.5 ns t_{PLH} = (0.25 ns/pF) C_L + 112.5 ns t_{PLH} = (0.20 ns/pF) C_L + 80 ns	t_{PLH}	5.0 10 15	– – –	313 125 90	625 250 180	ns
t_{PHL} = (1.3 ns/pF) C_L + 248 ns t_{PHL} = (0.45 ns/pF) C_L + 102.5 ns t_{PHL} = (0.35 ns/pF) C_L + 72.5 ns	t_{PHL}	5.0 10 15	– – –	313 125 90	625 250 180	
Setup Time	t_{su}	5.0 10 15	100 40 30	– – –	– – –	ns
Hold Time	t_h	5.0 10 15	60 40 30	– – –	– – –	ns
Latch Enable Pulse Width	t_{WL}	5.0 10 15	520 220 130	260 110 65	– – –	ns

7. The formulas given are for the typical characteristics only.

Input LE low, and Inputs D, $\overline{BI}$ and $\overline{LT}$ high.
f in respect to a system clock.
All outputs connected to respective C_L loads.

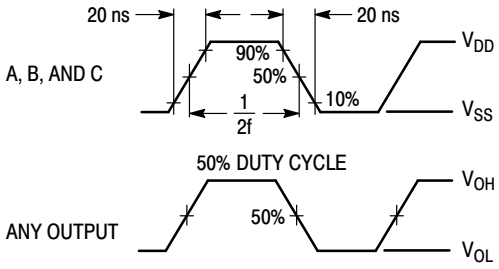
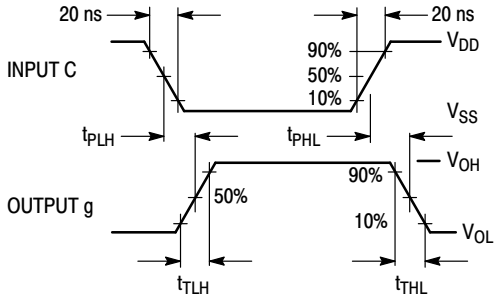
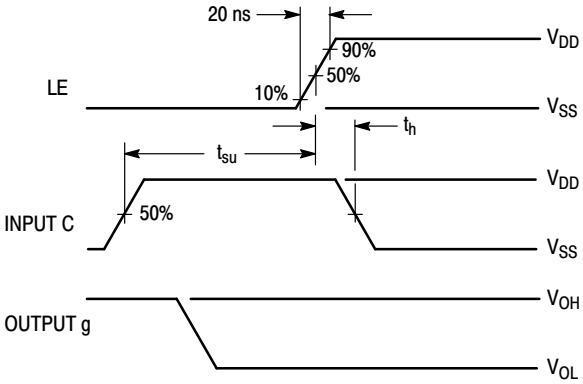


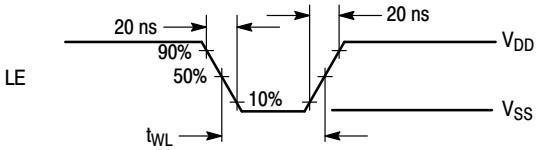
Figure 1. Dynamic Power Dissipation Signal Waveforms



(a) Inputs D and LE low, and Inputs A, B, $\overline{BI}$ and $\overline{LT}$ high.



(b) Input D low, Inputs A, B, $\overline{BI}$ and $\overline{LT}$ high.

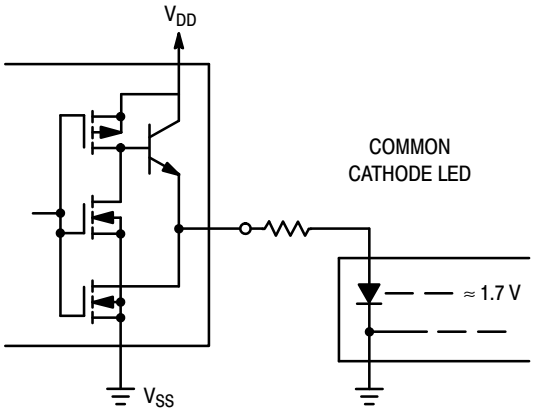


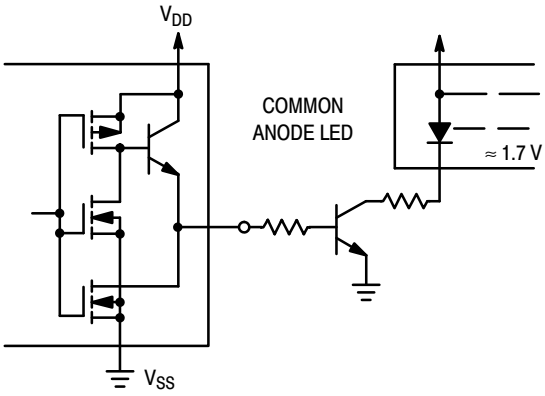
(c) Data DCBA strobed into latches.

Figure 2. Dynamic Signal Waveforms

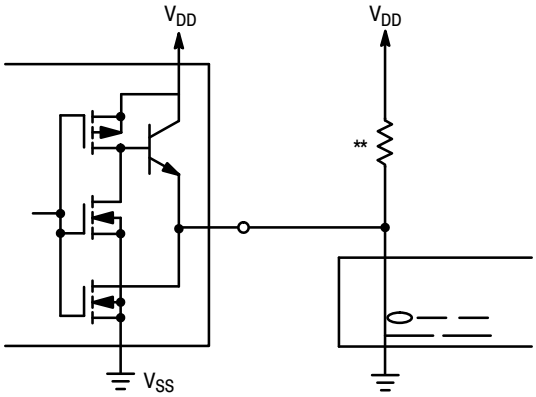
CONNECTIONS TO VARIOUS DISPLAY READOUTS

LIGHT EMITTING DIODE (LED) READOUT

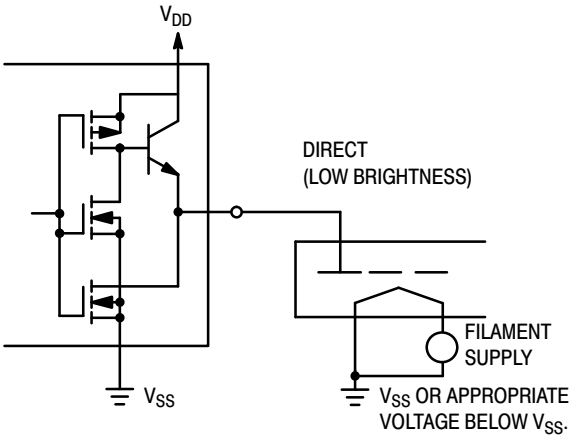




INCANDESCENT READOUT

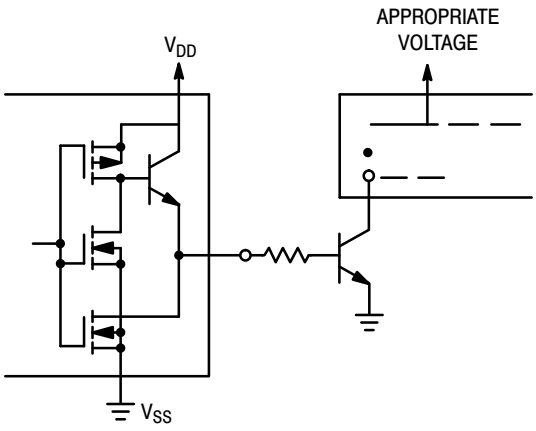


FLUORESCENT READOUT

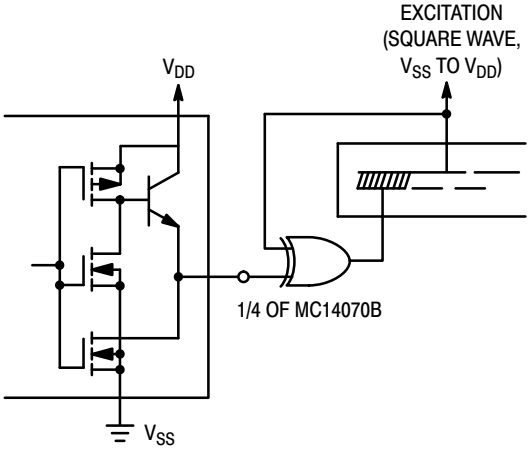


(CAUTION: Maximum working voltage = 18.0 V)

GAS DISCHARGE READOUT



LIQUID CRYSTAL (LCD) READOUT



** A filament pre−warm resistor is recommended to reduce filament thermal shock and increase the effective cold resistance of the filament.

Direct DC drive of LCD's not recommended for life of LCD readouts.

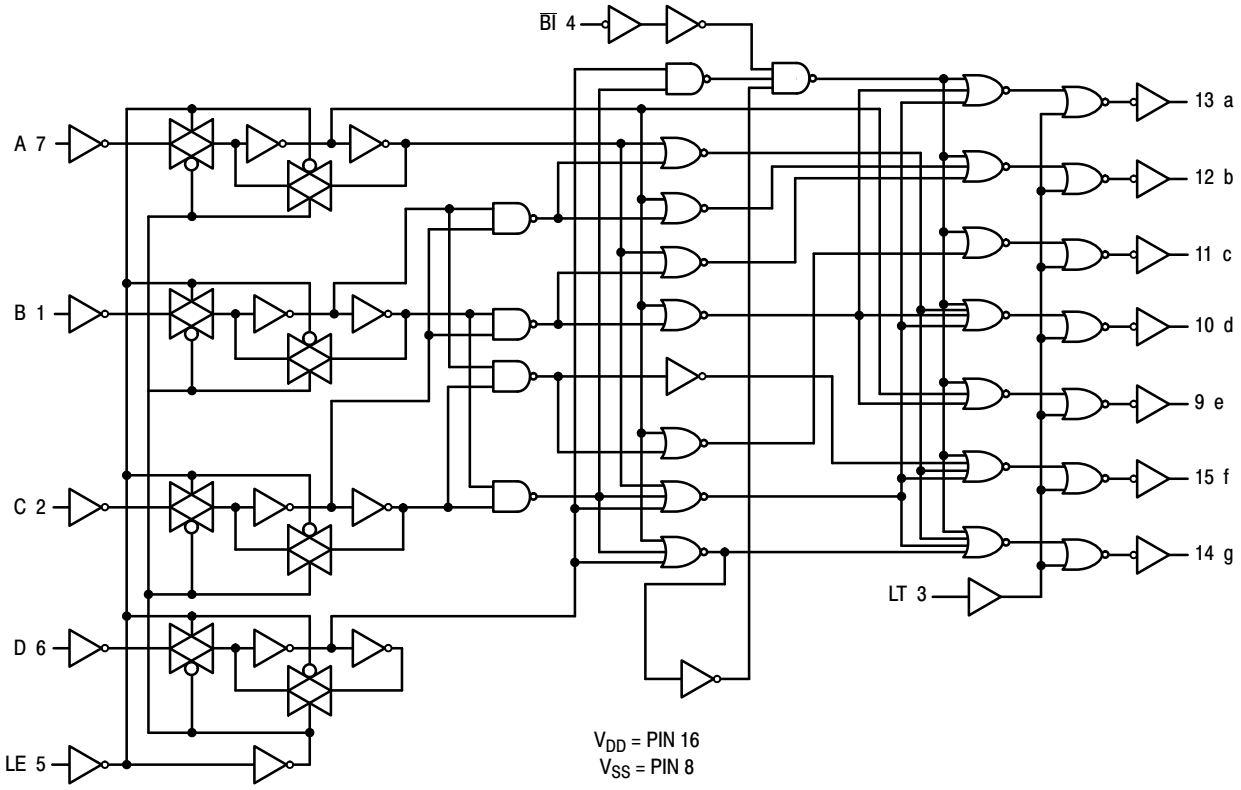


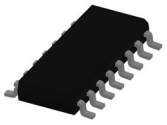
Figure 3. Logic Diagram

ORDERING INFORMATION

Device	Package	Shipping†
MC14511BDG	SOIC−16 (Pb−Free)	48 Units / Rail
MC14511BDR2G	SOIC−16 (Pb−Free)	2500 / Tape & Reel
MC14511BDWR2G	SO−16 WB (Pb−Free)	1000 / Tape & Reel
NLV14511BDWR2G*	SO−16 WB (Pb−Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

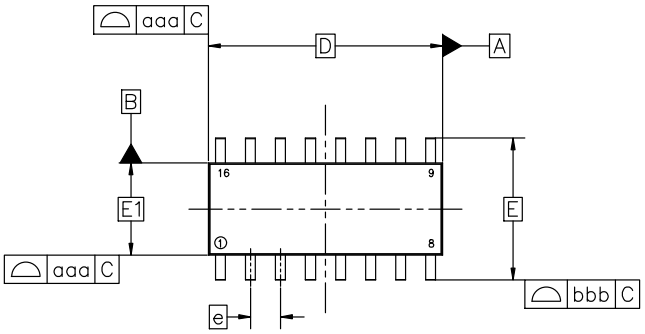
*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.



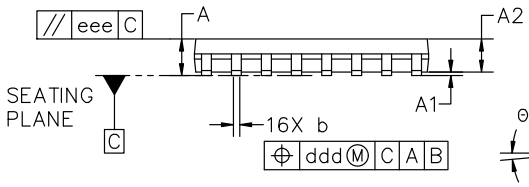
SOIC−16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

DATE 18 OCT 2024

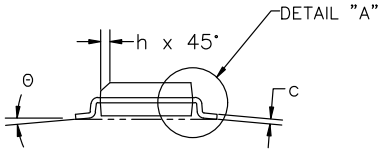
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



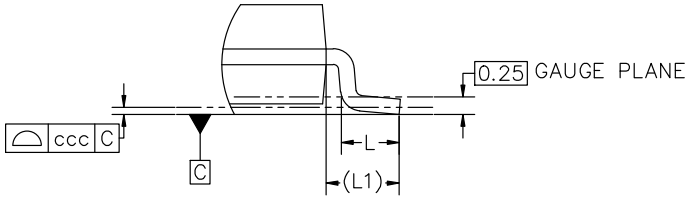
TOP VIEW



SIDE VIEW

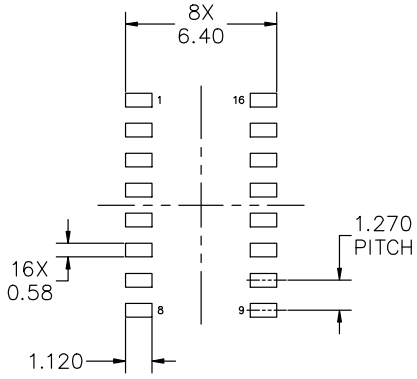


END VIEW



DETAIL "A"
Scale 3:1

MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.18	0.25
A2	1.25	1.37	1.50
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	−−−	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
Θ	0°	−−−	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



RECOMMENDED MOUNTING FOOTPRINT

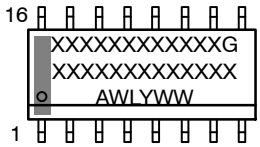
*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

DOCUMENT NUMBER:	**98ASB42566B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−16 9.90X3.90X1.37 1.27P**		**PAGE 1 OF 2**

SOIC−16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

DATE 18 OCT 2024

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:

PIN	
1.	COLLECTOR
2.	BASE
3.	EMITTER
4.	NO CONNECTION
5.	EMITTER
6.	BASE
7.	COLLECTOR
8.	COLLECTOR
9.	BASE
10.	EMITTER
11.	NO CONNECTION
12.	EMITTER
13.	BASE
14.	COLLECTOR
15.	EMITTER
16.	COLLECTOR

STYLE 2:

PIN	
1.	CATHODE
2.	ANODE
3.	NO CONNECTION
4.	CATHODE
5.	CATHODE
6.	NO CONNECTION
7.	ANODE
8.	CATHODE
9.	CATHODE
10.	ANODE
11.	NO CONNECTION
12.	CATHODE
13.	CATHODE
14.	NO CONNECTION
15.	ANODE
16.	CATHODE

STYLE 3:

PIN	
1.	COLLECTOR, DYE #1
2.	BASE, #1
3.	EMITTER, #1
4.	COLLECTOR, #1
5.	COLLECTOR, #2
6.	BASE, #2
7.	EMITTER, #2
8.	COLLECTOR, #2
9.	COLLECTOR, #3
10.	BASE, #3
11.	EMITTER, #3
12.	COLLECTOR, #3
13.	COLLECTOR, #4
14.	BASE, #4
15.	EMITTER, #4
16.	COLLECTOR, #4

STYLE 4:

PIN	
1.	COLLECTOR, DYE #1
2.	COLLECTOR, #1
3.	COLLECTOR, #2
4.	COLLECTOR, #2
5.	COLLECTOR, #3
6.	COLLECTOR, #3
7.	COLLECTOR, #4
8.	COLLECTOR, #4
9.	BASE, #4
10.	EMITTER, #4
11.	BASE, #3
12.	EMITTER, #3
13.	BASE, #2
14.	EMITTER, #2
15.	BASE, #1
16.	EMITTER, #1

STYLE 5:

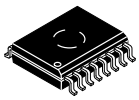
PIN	
1.	DRAIN, DYE #1
2.	DRAIN, #1
3.	DRAIN, #2
4.	DRAIN, #2
5.	DRAIN, #3
6.	DRAIN, #3
7.	DRAIN, #4
8.	DRAIN, #4
9.	GATE, #4
10.	SOURCE, #4
11.	GATE, #3
12.	SOURCE, #3
13.	GATE, #2
14.	SOURCE, #2
15.	GATE, #1
16.	SOURCE, #1

STYLE 6:

PIN	
1.	CATHODE
2.	CATHODE
3.	CATHODE
4.	CATHODE
5.	CATHODE
6.	CATHODE
7.	CATHODE
8.	CATHODE
9.	ANODE
10.	ANODE
11.	ANODE
12.	ANODE
13.	ANODE
14.	ANODE
15.	ANODE
16.	ANODE

STYLE 7:

PIN	
1.	SOURCE N-CH
2.	COMMON DRAIN (OUTPUT)
3.	COMMON DRAIN (OUTPUT)
4.	GATE P-CH
5.	COMMON DRAIN (OUTPUT)
6.	COMMON DRAIN (OUTPUT)
7.	COMMON DRAIN (OUTPUT)
8.	SOURCE P-CH
9.	SOURCE P-CH
10.	COMMON DRAIN (OUTPUT)
11.	COMMON DRAIN (OUTPUT)
12.	COMMON DRAIN (OUTPUT)
13.	GATE N-CH
14.	COMMON DRAIN (OUTPUT)
15.	COMMON DRAIN (OUTPUT)
16.	SOURCE N-CH

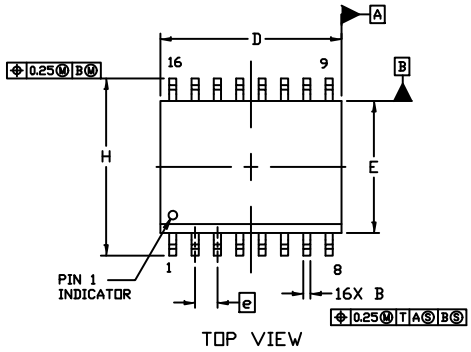


1

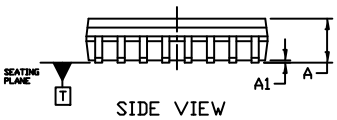
SCALE 1:1

SOIC−16 WB
CASE 751G
ISSUE E

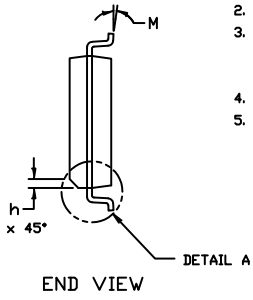
DATE 08 OCT 2021



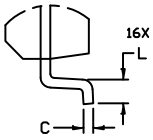
TOP VIEW



SIDE VIEW



END VIEW

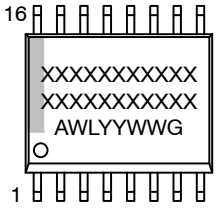


DETAIL A
2X SCALE

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION OR FLASH TO BE 0.15 PER SIDE.

	MILLIMETERS	
DIM	MIN.	MAX.
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.53 REF	
L	0.50	0.90
M	0°	7°

GENERIC MARKING DIAGRAM*



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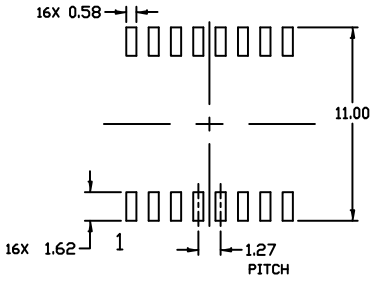

RECOMMENDED
MOUNTING FOOTPRINT

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DESCRIPTION:	**SOIC−16 WB**		**PAGE 1 OF 1**

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