NCP1565

Highly Integrated Dual-Mode Active Clamp PWM Controller

The NCP1565 is a highly integrated dual−mode active−clamp PWM controller targeting next−generation high−density, high−performance and small to medium power level isolated dc−dc converters for use in telecom and datacom industries. It can be configured in either voltage mode control with input voltage feed−forward or peak current mode control. Peak current mode control may be implemented with input voltage feed forward as well. Adjustable adaptive overlap time optimizes system efficiency based on input voltage and load conditions.

This controller integrates all the necessary control and protection functions to implement an isolated active clamp forward or asymmetric half−bridge converter. It integrates a high−voltage startup bias regulator. The NCP1565 has a line undervoltage detector, cycle−by−cycle current limiting, line voltage dependent maximum duty ratio limit, and programmable overtemperature protection using an external thermistor. It also includes a dual−function $\overline{\text{FLT/SD}}$ pin used for communicating the presence of a fault but also for shutting down the controller.

General Features

- Support Voltage Mode Control and Peak Current Mode Control
- Line Feedforward
- Adaptive Overlap time Control for Improved Efficiency
- Integrated 120 V High Voltage Startup Circuit
- Programmable Line Undervoltage Lockout (UVLO) with Adjustable Hysteresis
- Cycle by Cycle Peak Current Limiting
- Overcurrent Protection Based on Average Current
- Short Circuit Protection
- Programmable Duty Ratio Clamp
- Programmable Soft−Start
- Programmable Shutdown and Restart Delays
- Programmable External Overtemperature Protection Using Thermistor
- $\overline{\text{FLT/SD}}$ pin Used for Fault reporting and Shutdown Input
- Programmable Oscillator with 1.5 MHz Maximum Frequency
- 5 V/2% Voltage Reference
- Main Switch Drive Capability of −2 A/3 A
- Active Clamp Switch Drive Capability of −2 A/1 A
- V_{CC} Range: from 6.5 V to 20 V
- These Devices are Pb−Free, Halogen Free/BFR Free and RoHS Compliant

Typical Applications

- High Efficiency Isolated dc−dc Converters
- Server Power Supplies
- 24 V and 48 V Telecom systems
- 42 V Automotive Applications

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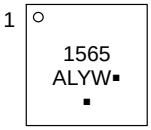
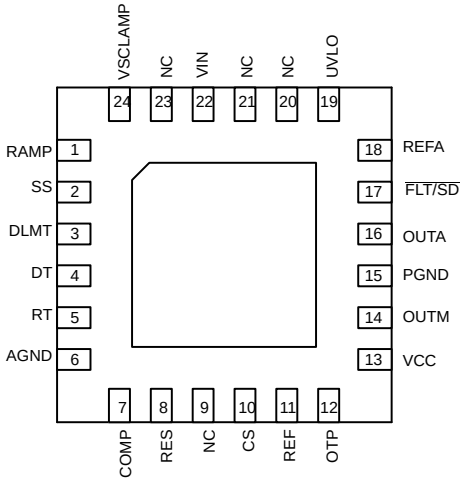
QFN24
MN SUFFIX
CASE 485CW

MARKING DIAGRAM



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 30 of this data sheet.

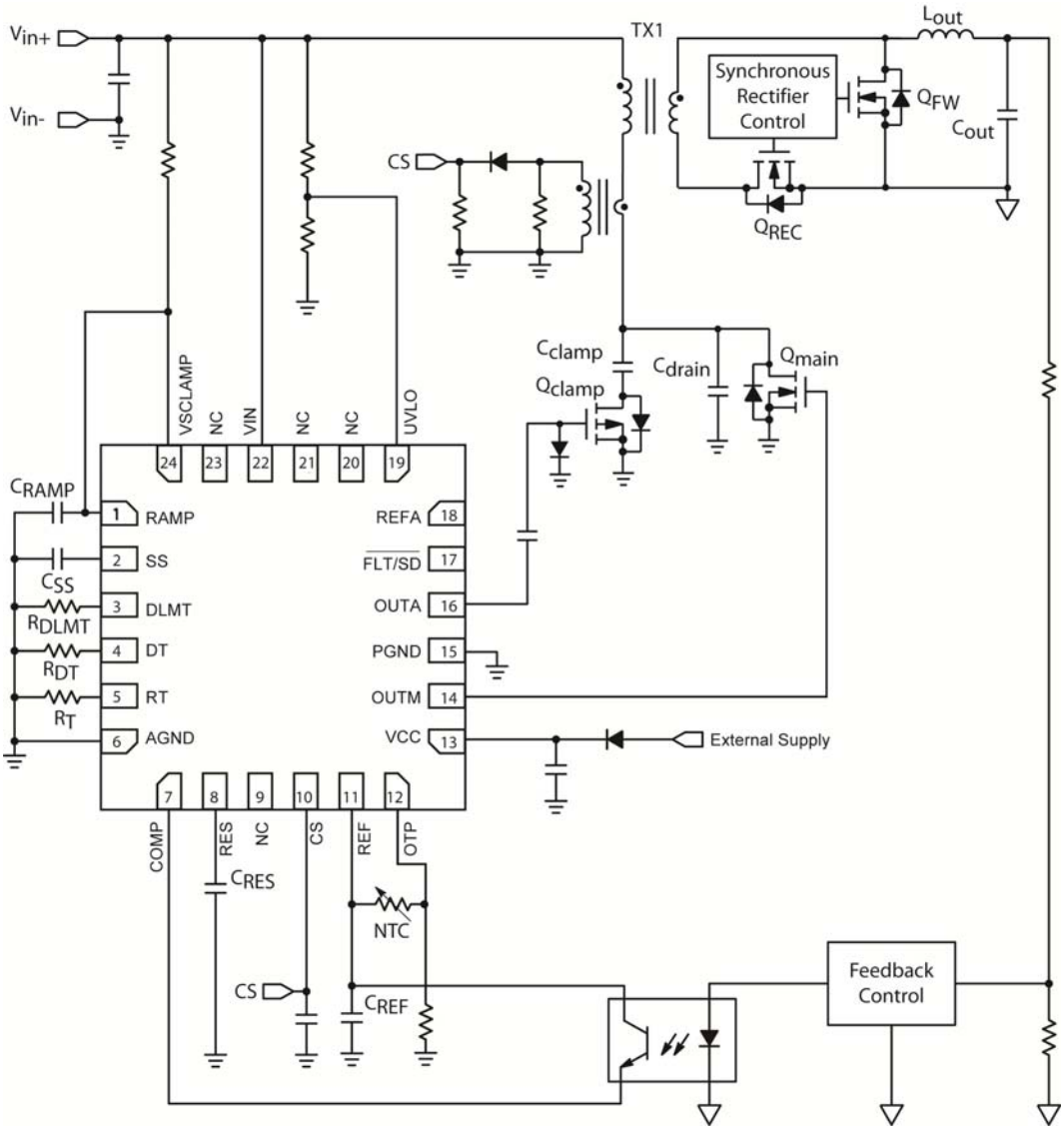


Figure 1. Typical Application Circuit in Voltage Mode Control

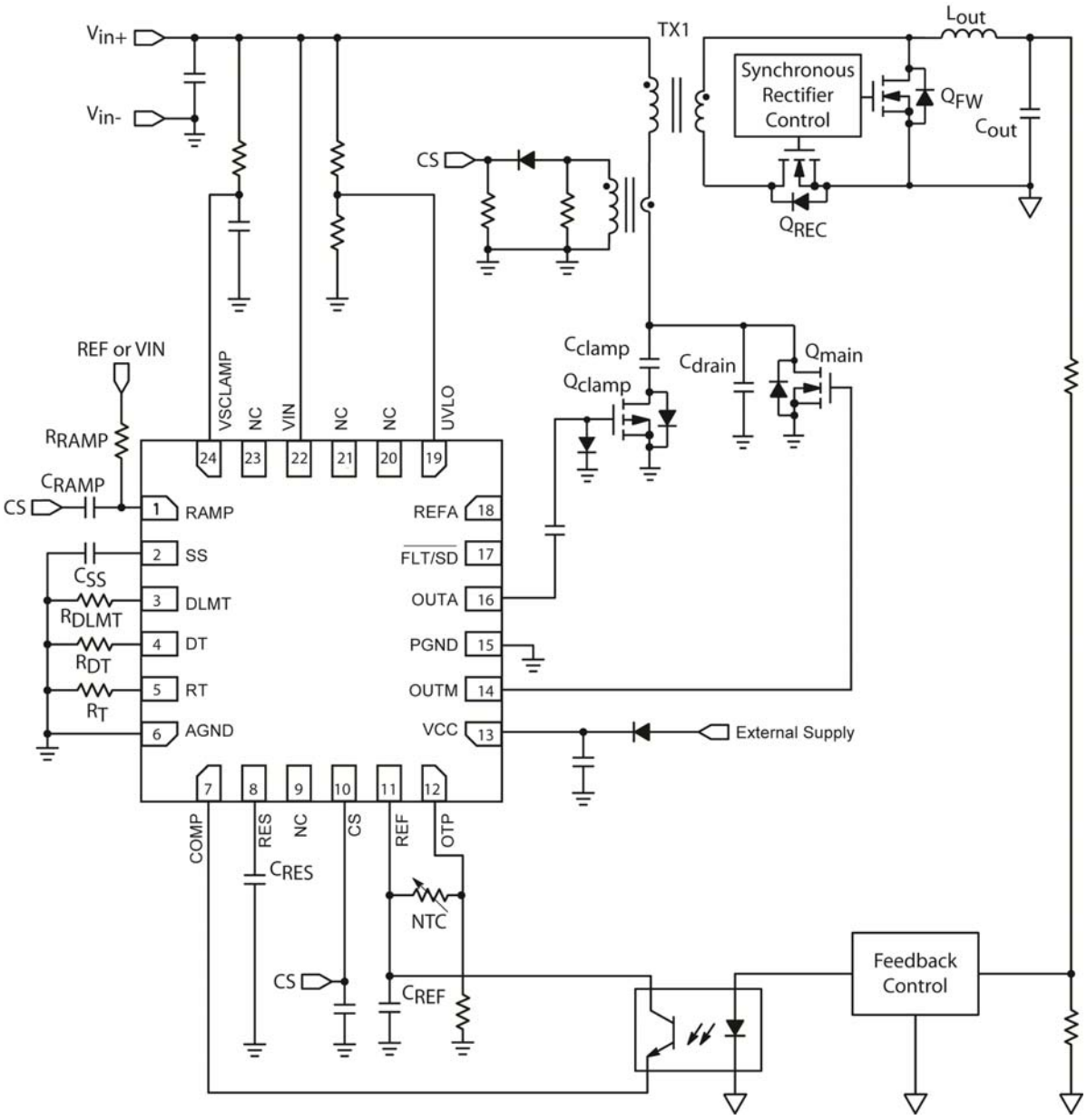


Figure 2. Typical Application Circuit in Current Mode Control

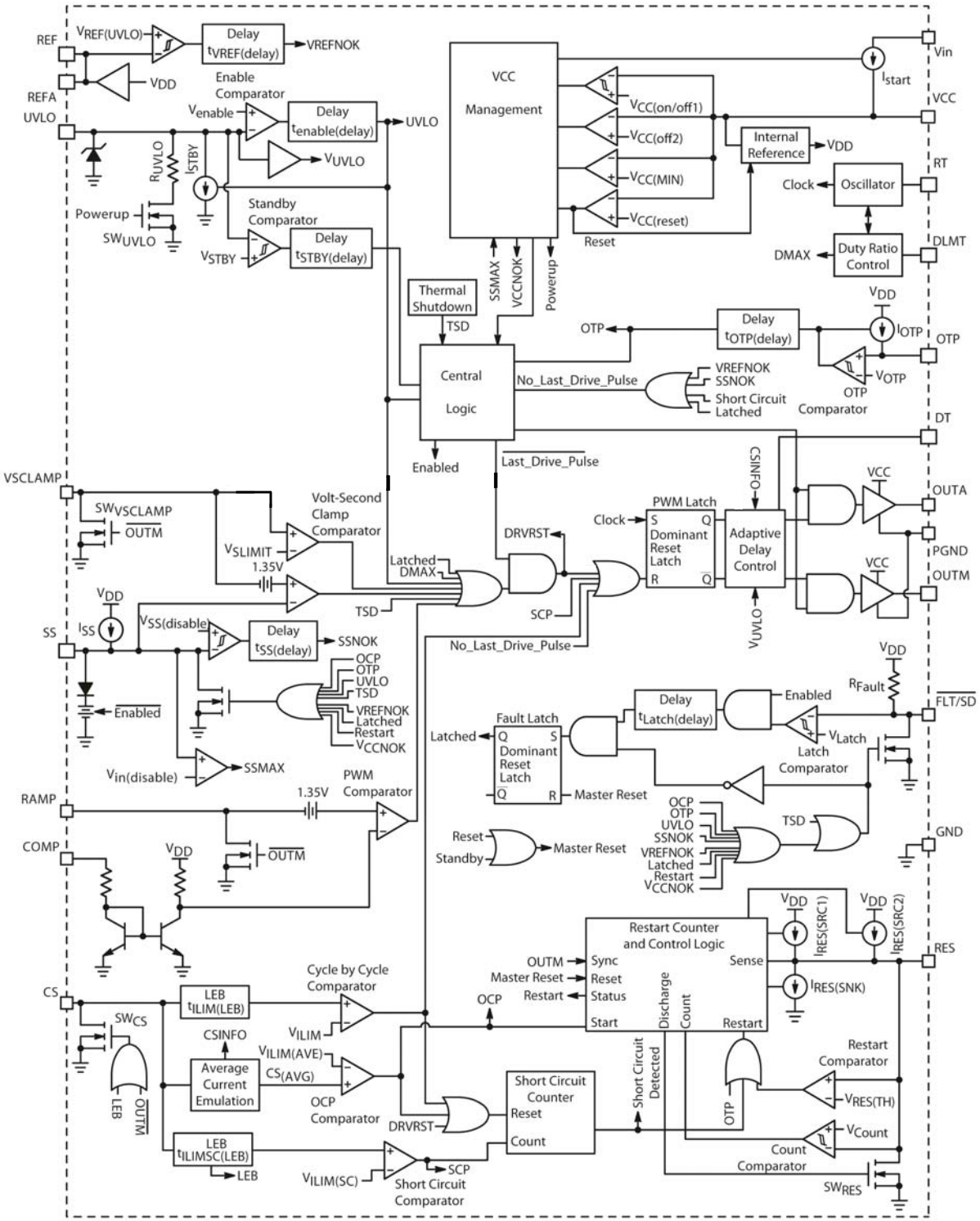


Figure 3. Functional Block Diagram

DETAILED PIN DESCRIPTION

Pin Number	Name	Function
1	RAMP	PWM modulator ramp. In voltage mode an external R−C circuit from V_{in} sets the PWM Ramp slope to implement feedforward. In current mode control, the resistor of the external R−C circuit connects to REF for ramp compensation.
2	SS	Soft−start control. A 20 μA current source charges the external capacitor connected to this pin. Duty ratio is limited during startup by comparing the voltage on this pin to a level−shifted VSCLAMP signal. Under steady state conditions, the SS voltage is approximately 4.5 V. Once a fault is detected the SS capacitor is discharged and the controller is disabled.
3	DLMT	Maximum duty ratio limit. A resistor between this pin and AGND sets the maximum duty ratio of the controller.
4	DT	Dead time control. An external resistor between this pin and AGND sets the overlap time delay between OUTM and OUTA.
5	RT	Oscillator frequency setting pin. The total external resistance connected between the RT and AGND pins sets the internal oscillator frequency.
6	AGND	Analog circuit ground reference. All control and timing components that connect to AGND should have the shortest loop possible to this pin to improve noise immunity. It should be tied to PGND at the return of the power stage.
7	COMP	Input to the pulse width modulator. An external optocoupler connected between the REF and COMP pin sources current into an internal NPN current mirror. The maximum duty ratio is achieved when no current is sourced by the optocoupler. The duty cycle reduces to zero once the source current exceeds 850 μA. The internal current mirror improves the frequency response by reducing the ac voltage across the optocoupler transistor.
8	RES	Restart time control. A capacitor between this pin and AGND set the shutdown delay and hiccup mode restart delay time. If a restart fault is detected, a pull−up current source, $I_{RES(SRC1)}$, typically 20 μA is enabled. If the RES pin voltage, V_{RES}, exceeds the restart threshold, $V_{RES(TH)}$, typically 1 V, the controller enters restart mode. $I_{RES(SRC1)}$ is disabled once in restart mode and a second pull up current source, $I_{RES(SRC2)}$, typically 5 μA enabled. $I_{RES(SRC2)}$ is disabled once V_{RES} reaches $V_{RES(peak)}$, typically 4 V. A pull−down current source, $I_{RES(SNK)}$, typically 5 μA, is enabled until VRES falls below $V_{RES(valley)}$ typically 2 V. The controller restarts after 32 V_{RES} charge/discharge cycles.
9	NC	No connect.
10	CS	Current sense input. The current sense signal is used for current−mode control, adaptive dead time control, cycle−by−cycle current limiting, over−current protection and short circuit protection, etc. If the CS voltage exceeds the cycle by cycle current limit threshold, V_{ILIM}, typically 0.45 V, the drive pulse is terminated. Internal leading edge blanking prevents triggering of the cycle by cycle current limit during normal operation. A short circuit condition exists if V_{CS} exceeds the short−circuit threshold, $V_{ILIM(SC)}$, typically set to 0.7 V, during two consecutive clock pulses.
11	REF	Precision 5 V reference. Maximum output current is 12 mA. It is required to bypass the reference with a capacitor. The recommended capacitance ranges between 0.1 to 0.47 μF.
12	OTP	Over−temperature protection. A voltage divider containing a NTC connects to this pin.
13	VCC	Positive input supply. This pin connects to an external capacitor for energy storage. An internal current source, I_{start}, supplies current from V_{in} to this pin. Once V_{CC} reaches $V_{CC(on)}$, typically 9.5 V, the startup current source is disabled. The current source is enabled once V_{CC} falls below $V_{CC(off1)}$, typically 9.4 V, while faults are present. Once faults are removed and the controller is operating, the startup current source turn−on threshold is reduced to $V_{CC(off2)}$, typically 7.5 V..
14	OUTM	Main switch gate control. OUTM can source 2 A and sink 3 A.
15	PGND	Ground connection for OUTM and OUTA. Tie to the power stage return with a short loop.
16	OUTA	Active clamp switch gate control. OUTA has an adjustable leading and trailing edge overlap delay against OUTM. OUTA can source 2 A and sink 1 A.
17	$\overline{\text{FLT/SD}}$	Fault report and shutdown control. This is a dual−function bi−directional pin. This pin is an open−collector output with a 10 kΩ internal pull−up resistance connected to REF.
18	REFA	Internally connected to REF.
19	UVLO	Input voltage undervoltage detector. The input voltage is scaled down and sampled by means of a resistor divider. The controller enters standby mode once the UVLO voltage, V_{UVLO}, exceeds the standby threshold, V_{STBY}, typically 0.4 V. The controller enters shutdown mode if V_{UVLO} falls below V_{STBY} by the shutdown hysteresis level. The controller is enabled once V_{UVLO} exceeds the enable threshold, V_{enable}, typically 1.25 V. Hysteresis is provided by an internal pull−down current source, I_{UVLO}, typically 20 μA. The current source is disabled once the controller is enabled.
20	NC	No connect (creepage distance).
21	NC	No connect (creepage distance).

DETAILED PIN DESCRIPTION

Pin Number	Name	Function
22	V_{in}	High voltage startup circuit input. Connect the input line voltage directly to this pin to enable the internal startup regulator. A constant current source supplies current from this pin to the capacitor connected to the VCC pin, eliminating the need for a startup resistor. The minimum charge current is 40 mA. The operating voltage range of the startup circuit is 13 V to 120 V.
23	NC	No connect (creepage distance).
24	VSCLAMP	Volt−second clamp. An external R−C divider from the input line generates a voltage ramp. This ramp is compared to a voltage reference, V_{SLIMIT}, typically 1.5 V. The OUTM pulse is terminated once the ramp voltage exceeds V_{SLIMIT}, thus limiting the maximum volt−second product of the main transformer. In voltage mode, VSCLAMP and RAMP pins can be tied together to share one external R−C circuit.

MAXIMUM RATINGS (Notes 1 through 3)

Rating	Symbol	Value	Unit
High Voltage Startup Circuit Input Voltage	V_{in}	−0.3 to 120	V
High Voltage Startup Circuit Input Current	I_{in}	70	mA
UVLO Input Voltage	V_{UVLO}	−0.3 to V_{CC}	V
OTP Input Voltage	V_{OTP}	−0.3 to 7	V
Ramp Input Voltage	V_{Ramp}	−0.3 to 7	V
Ramp Peak Input Current	I_{Ramp}	1	A
VSClamp Input Voltage	V_{SCLAMP}	−0.3 to 7	V
VSClamp Input Current	I_{SCLAMP}	0.5	mA
RT Input Voltage	V_{RT}	−0.3 to 7	V
RT Input Current	I_{RT}	2	mA
COMP Input Voltage	V_{COMP}	−0.3 to 5.5	V
COMP Input Current	I_{COMP}	1	mA
Reference Input Voltage	V_{REF}	−0.3 to 5.5	V
Reference Input Current	I_{REF}	20	mA
Supply Input Voltage	$V_{CC(MAX)}$	−0.3 to 20	V
Supply Input Current	$I_{CC(MAX)}$	70	mA
Main Driver Maximum Voltage	V_{OUTM}	−0.3 to V_{CC}	V
Main Driver Maximum Current	$I_{OUTM(SRC)}$ $I_{OUTM(SNK)}$	2 3	A
Active Clamp Driver Maximum Voltage	V_{OUTA}	−0.3 to V_{CC}	V
Active Clamp Driver Maximum Current	$I_{OUTA(SRC)}$ $I_{OUTA(SNK)}$	2 1	A
Current Sense Input Voltage	V_{CS}	−0.3 to 5.5	V
Current Sense Peak Input Current	I_{CS}	0.5	A
Soft−Start Input Voltage	V_{SS}	−0.3 to 5.5	V
Restart Input Voltage	V_{RES}	−0.3 to 5.5	V
Restart Peak Input Current	I_{RES}	0.1	A
$\overline{\text{FLT/SD}}$ Input Voltage	$V_{\overline{FLT/SD}}$	−0.3 to 7	V
$\overline{\text{FLT/SD}}$ Peak Input Current	$I_{\overline{FLT/SD}}$	0.1	A
Deadtime Input Voltage	V_{DT}	−0.3 to 5.5	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device contains Latch−Up protection and exceeds ± 100 mA per JEDEC Standard JESD78.
2. As specified for a JEDEC EIA/JESD 51.3 conductivity test. Test conditions were under natural convection of zero air flow.
3. V_{in} is the exception.

MAXIMUM RATINGS (Notes 1 through 3)

Rating	Symbol	Value	Unit
Maximum Duty Ratio Control Input Voltage	V_{DLMT}	−0.3 to 5.5	V
Maximum Duty Ratio Control Input Current	I_{DLMT}	2	mA
Maximum Operating Junction Temperature	T_J	−40 to 150	°C
Storage Temperature Range	T_{STG}	−60 to 150	°C
Lead Temperature (Soldering, 10 s)	$T_{L(MAX)}$	300	°C
Moisture Sensitivity Level	MSL	1	−
Power Dissipation (T_A = 25°C, 1 Oz Cu (35 μm), 0.155 Sq Inch (100 mm^2) Printed Circuit Copper Clad) MNTXG Suffix, Plastic Package (QFN−24)	P_D	760	mW
Thermal Resistance, Junction−to−Ambient 1 Oz Cu (35 μm) 2−Layer 100 mm^2 Printed Circuit Copper Clad (Note 3) MNTXG Suffix, Plastic Package (QFN−24)	$R_{\theta JA}$	131	°C/W
Thermal Resistance, Junction−to−Ambient 2 Oz Cu (70 μm) 2−Layer 100 mm^2 Printed Circuit Copper Clad (Note 3) MNTXG Suffix, Plastic Package (QFN−24)	$R_{\theta JA}$	115	°C/W
ESD Capability Human Body Model per JEDEC Standard JESD22−A114F. Machine Model per JEDEC Standard JESD22−A115C. Charge Device Model per JEDEC Standard JESD22−C101E.		 > 2000 > 200 > 1500	V

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2. As specified for a JEDEC EIA/JESD 51.3 conductivity test. Test conditions were under natural convection of zero air flow.
3. V_{in} is the exception.

ELECTRICAL CHARACTERISTICS: (C_{REF} = 0.1 μF, V_{in} = 48 V, V_{UVLO} = 2 V, V_{CC} = 10 V, V_{CS} = 0.25 V, R_{DLMT} = 49.9 kΩ, R_{DT} = 100 kΩ, R_T = 100 kΩ, for typical values T_J = 25°C, for min/max values, T_J is − 40°C to 125°C, unless otherwise noted)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
STARTUP AND SUPPLY CIRCUITS						
Supply Voltage Upper Regulation Level Lower Regulation While Disabled Lower Regulation While Enabled Minimum Operating Voltage Reset Voltage	 V_{CC} increasing V_{CC} decreasing V_{CC} decreasing V_{CC} decreasing V_{CC} decreasing	 $V_{CC(on)}$ $V_{CC(off1)}$ $V_{CC(off2)}$ $V_{CC(MIN)}$ $V_{CC(reset)}$	 9.1 9.0 7.3 6.2 6.1	 9.5 9.4 7.5 6.5 6.4	 9.9 9.8 7.7 6.8 6.7	V
Startup Delay	Delay from $V_{CC(on)}$ to Enable	$t_{delay(start)}$	30	−	125	μs
Delay in turning start−up source off	V_{CC} > $V_{CC(off2)}$	$t_{Vcc(off2)}$		3	10	μs
Delay in turning start−up source on	V_{CC} < $V_{CC(off2)}$	$t_{Vcc(on2)}$		15	30	μs
Startup Current	V_{CC} = $V_{CC(on)}$ − 0.2 V, V_{in} = 48 V	I_{start}	40	55	−	mA
Startup Circuit Off−State Leakage Current	V_{in} = 120 V	$I_{Vin(off)}$	−	−	100	μA
Minimum Startup Voltage	I_{start} = 15 mA, V_{CC} = $V_{CC(on)}$ − 0.2 V	$V_{in(MIN)}$	−	−	15	V
Supply Current Disabled mode current Standby No Switching Operating Current	 UVLO below 0.4 V V_{CC} = 10 V, V_{UVLO} = 1 V V_{CC} = 10 V, I_{COMP} = 850 μA f = 200 kHz, C_{OUTM} = C_{OUTA} = open	 I_{CC1} I_{CC2} I_{CC3} I_{CC4}	 − − −	 − − − −	 2 2 4 5	mA
REFERENCE						
Reference Voltage	I_{REF} = 0 mA	V_{REF}	4.9	5.0	5.1	V
Load Regulation	I_{REF} = 0 to 10 mA	$V_{REF(load−reg)}$	4.85	5.00	5.15	V
Step Load Response	I_{REF} = 5 to 10 mA, di/dt = 100 mA/μs	$V_{REF(step−reg)}$	4.85	5.00	5.15	V
Source Current	V_{REF} = 4.75 V	$I_{REF(MAX)}$	12	−	−	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Guaranteed by Design. Not Tested.
5. Guaranteed by Design.

ELECTRICAL CHARACTERISTICS: (C_{REF} = 0.1 μF, V_{in} = 48 V, V_{UVLO} = 2 V, V_{CC} = 10 V, V_{CS} = 0.25 V, R_{DLMT} = 49.9 kΩ, R_{DT} = 100 kΩ, R_T = 100 kΩ, for typical values T_J = 25°C, for min/max values, T_J is − 40°C to 125°C, unless otherwise noted)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
REFERENCE						
Minimum Capacitance (Note 4)		$C_{REF(range)}$	0.1	−	−	μF
Reference Undervoltage Threshold	V_{REF} increasing	$V_{REF(UVLO)}$		4.5	4.75	V
Reference Undervoltage Hysteresis	V_{REF} decreasing	$V_{REF(HYS)}$		200		mV
LINE VOLTAGE UVLO						
Standby Threshold	V_{UVLO} increasing	V_{STBY}	0.35	0.40	0.45	V
Standby Hysteresis	V_{UVLO} decreasing	$V_{STBY(HYS)}$	0.05	0.10	0.15	V
Enable Threshold	V_{UVLO} increasing	V_{enable}	1.23	1.25	1.27	V
Disable Filter Delay	$V_{UVLO} = V_{enable}$ − 400 mV	$t_{enable(delay2)}$	0.5	−	1	μs
Pull−Down Current in Standby Mode	$V_{UVLO} = V_{enable}$ - 0.1 V $V_{SHDN} < V_{UVLO} < V_{enable}$	I_{STBY}	18	20	22	μA
Pull−Down Current Enable Threshold		$I_{STBY(THD)}$	−	$V_{CC(off2)}$	−	V
Pull−Down Resistor while I_{STBY} is Disabled	V_{UVLO} = 1.25 V	R_{UVLO}	22.4	32.0	41.6	kΩ
MAIN GATE DRIVE						
Rise Time (10−90%)	from 10% to 90% of V_{OUTM}, C_{OUTM} = 2.2 nF	$t_{OUTM(rise)}$	−	8.8	17.6	ns
Fall Time (90−10%)	90% to 10% of V_{OUTM}, C_{OUTM} = 2.2 nF	$t_{OUTM(fall)}$	−	6.0	12	ns
Current Capability Source Sink	 V_{OUTM} = 4 V V_{OUTM} = 4 V, V_{CC} = 7.5 V, I_{COMP} = 850 μA	 $I_{OUTM(SRC)}$ $I_{OUTM(SNK)}$	 2 3		 − −	A
High State Voltage Offset	$V_{CC} - V_{OUTM}$, V_{CC} = 8 V, C_{OUTM} = 2.2 nF	$V_{OUTM(offset)}$	−	−	0.2	V
Low Stage Voltage	V_{UVLO} = 1 V	$V_{OUTM(low)}$	−	−	0.2	V
ACTIVE CLAMP GATE DRIVE						
Rise Time (10−90%)	from 10 to 90% of V_{OUTA}, C_{OUTA} = 2.2 nF	$t_{OUTM(rise)}$	−	8.8	17.6	ns
Fall Time (90−10%)	90 to 10% of V_{OUTA}, C_{OUTA} = 2.2 nF	$t_{OUTM(fall)}$	−	17.6	35.2	ns
Current Capability Source Sink	 V_{OUTA} = 4 V V_{OUTA} = 4 V, V_{CC} = 7.5 V	 $I_{OUTA(SRC)}$ $I_{OUTA(SNK)}$	 2 1		 − −	A
High State Voltage Offset	$V_{CC} - V_{OUTA}$, V_{CC} = 8 V, C_{OUTA} = 2.2 nF	$V_{OUTA(offset)}$	−	−	0.2	V
Low Stage Voltage	V_{UVLO} = 1 V	$V_{OUTA(low)}$	−	−	0.2	V
CURRENT SENSE						
Average Current Limit Threshold		$V_{ILIM(ave)}$	288	300	312	mV
Average Current Limit Leading Edge Blanking Duration (Note 4)		$t_{ILIMAVE(LEB)}$	23	30	37	ns
Average Current Limit Propagation Delay (Note 4)		$t_{ILIMAVE(delay)}$	−	40	−	ns
Cycle by Cycle Current Limit Threshold		V_{ILIM}	432	450	468	mV
Cycle by Cycle Current Limit Leading Edge Blanking Duration		$t_{ILIM(LEB)}$	42	55	68	ns
Cycle by Cycle Current Limit Propagation Delay	Step V_{CS} to 0.7 V to OUTM falling edge, dV/dt = 20 V/μs	$t_{ILIM(delay)}$	−	40	56	ns
Short Circuit Current Limit Threshold		$V_{ILIM(SC)}$	672	700	728	mV
Short Circuit Current Limit Leading Edge Blanking Duration		$t_{ILIMSC(LEB)}$	23	30	37	ns
Short−Circuit Current Limit Propagation Delay	Step V_{CS} to 0.9 V to OUTM falling edge, dV/dt = 10 V/μs	$t_{ILIMSC(delay)}$	−	40	56	ns
Short Circuit Counter	Step V_{CS} to $V_{ILIM(SC)}$ + 0.2 V	n_{ILIMSC}	−	2	−	−
Discharge Switch On Resistance	V_{SCLAMP} = 2 V, V_{CS} = 100 mV	$R_{CSswitch(on)}$	−	−	35	Ω

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Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
OVERTEMPERATURE PROTECTION (OTP)						
Overtemperature Detect Threshold	V_{OTP} increasing	$V_{OTP(TH)}$	1.23	1.25	1.27	V
Overtemperature Detect Delay	V_{OTP} = $V_{OTP(TH)}$ − 20 mV	$t_{OTP(delay)}$	10	20	30	μs
Pull−up Current in OTP Mode	V_{OTP} = $V_{OTP(TH)}$ + 0.1 V	I_{OTP}	18	20	22	μA
SOFT−START						
Soft−Start Charge Current	V_{SS} = 1.5 V to 3 V	I_{SS}	18	20	22	μA
Soft−Start Onset Threshold		$V_{SS(offset)}$		1.35		V
Clamp Voltage		$V_{SS(clamp)}$		0.85		V
Discharge Switch On Resistance	V_{SS} = 100 mV	$R_{SSswitch(on)}$	−	−	30	Ω
Disable Threshold	V_{SS} decreasing	$V_{SS(disable)}$	0.4	0.5	0.6	V
RESTART						
Restart Delay Threshold	V_{RES} increasing	$V_{RES(TH)}$	0.96	1.00	1.04	V
Peak Voltage	V_{CS} > $V_{ILIMAVE}$, V_{RES} increasing	$V_{RES(peak)}$	3.8	4.0	4.2	V
Valley Voltage	V_{CS} > $V_{ILIMAVE}$, V_{RES} decreasing	$V_{RES(valley)}$	1.9	2.0	2.1	V
Discharge Current	V_{CS} < $V_{ILIMAVE}$, V_{RES} = 100 mV	$I_{RES(SNK)}$	4	5	6	μA
Charge Current	V_{CS} > $V_{ILIMAVE}$, V_{RES} = $V_{RES(valley)}$ − 50 mV V_{CS} > $V_{ILIMAVE}$, V_{RES} = $V_{RES(valley)}$ + 50 mV	$I_{RES(SRC1)}$ $I_{RES(SRC2)}$	18 4	20 5	22 6	μA
Restart Counter	V_{OTP} > $V_{OTP(TH)}$	n_{RES}		32		
Discharge Voltage		$V_{RES(DIS)}$	50	100	150	mV
Discharge Switch On Resistance	V_{RES} = 200 mV	$R_{ESswitch(on)}$	−	−	110	Ω
FAULT REPORT and REMOTE SHUTDOWN						
Enable Threshold	$V_{\overline{FLT/SD}}$ = increasing	$V_{FLT(enable)}$	1.37	1.45	1.53	V
Fault Threshold	$V_{\overline{FLT/SD}}$ = decreasing	$V_{fault\overline{FLT/SD}}$	1.23	1.25	1.27	V
Internal Pull−Up Resistor	$V_{\overline{FLT/SD}}$ = 3 V	$R_{FAULT/SD}$	8.5	10.0	11.5	kΩ
Discharge Switch On Resistance	$V_{\overline{FLT/SD}}$ = 100 V	$R_{FAULTswitch(on)}$	−	−	120	Ω
OSCILLATOR						
Operating Frequency Range (Note 5)		f_{range}	100	−	1500	kHz
Oscillator Frequency t_{D1} ≈ 100 ns t_{D1} ≈ 75 ns	 R_T = 49.9 kΩ, R_{DT} = 69.8 kΩ, R_{DLMT} = 26.7 kΩ R_T = 16.2 kΩ, R_{DT} = 52.3 kΩ, R_{DLMT} = 9.09 kΩ	 f_{OSC1} f_{OSC2}	 180 540	 200 600	 220 660	kHz
MAXIMUM DUTY RATIO						
Maximum Duty Ratio F_{sw} = 200 kHz F_{sw} = 600 kHz	Internal spec is ± 3%, V_{UVLO} = 1.4 V R_T = 49.9 kΩ, R_{DT} = 69.8 kΩ, R_{DLMT} = 41.2 kΩ R_T = 49.9 kΩ, R_{DT} = 69.8 kΩ, R_{DLMT} = 34.0 kΩ R_T = 49.9 kΩ, R_{DT} = 69.8 kΩ, R_{DLMT} = 26.7 kΩ R_T = 16.2 kΩ, R_{DT} = 52.3 kΩ, R_{DLMT} = 14.0 kΩ R_T = 16.2 kΩ, R_{DT} = 52.3 kΩ, R_{DLMT} = 11.5 kΩ R_T = 16.2 kΩ, R_{DT} = 52.3 kΩ, R_{DLMT} = 9.09 kΩ	 $D_{(MAX1a)}$ $D_{(MAX2a)}$ $D_{(MAX3a)}$ $D_{(MAX1b)}$ $D_{(MAX2b)}$ $D_{(MAX3b)}$	 76.5 62.8 48.8 76.2 62.1 47.8	 80.5 66.1 50.3 80.2 65.4 49.3	 84.5 69.4 53.8 84.2 68.7 52.8	%
Minimum Duty Ratio	I_{COMP} = 850 μA	$D_{(MIN)}$	−	−	0	%
VOLT−SECOND CLAMP						
Volt Second Limit Voltage Threshold	I_{COMP} = 0 μA	V_{SLIMIT}	1.44	1.50	1.56	V
Volt−Second Propagation Delay	Step V_{SCLAMP} to 2 V to OUTM falling edge, dV/dt = 10 V/μs	$t_{VSCLAMP}$		40	60	ns
VSCLAMP Switch On Resistance	V_{SCLAMP} = 100 mV	$R_{VSCLAMPswitch(on)}$	−	−	45	Ω
VSCLAMP Input Leakage Current	V_{SCLAMP} = 1.4 V	$I_{VSCLAMP(leak)}$	−	−	100	nA
OVERLAP TIME DELAY						
Overlap Delay Range (Note 5)	Include UVLO Adjustment. But not CS.	$t_{D(range)}$	20	−	500	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Guaranteed by Design. Not Tested.
5. Guaranteed by Design.

ELECTRICAL CHARACTERISTICS: (C_{REF} = 0.1 μF, V_{in} = 48 V, V_{UVLO} = 2 V, V_{CC} = 10 V, V_{CS} = 0.25 V, R_{DLMT} = 49.9 kΩ, R_{DT} = 100 kΩ, R_T = 100 kΩ, for typical values T_J = 25°C, for min/max values, T_J is − 40°C to 125°C, unless otherwise noted)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
OVERLAP TIME DELAY						
Overlap Delay from OUTA to OUTM rising Edges	R_{DT} = 52.3 kΩ, V_{UVLO} = 2.5 V, V_{CS} = 0.4 V R_{DT} = 52.3 kΩ, V_{UVLO} = 2.5 V, V_{CS} = 0.05 V R_{DT} = 69.8 kΩ, V_{UVLO} = 2.5 V, V_{CS} = 0.4 V R_{DT} = 69.8 kΩ, V_{UVLO} = 1.5 V, V_{CS} = 0.05 V R_{DT} = 274 kΩ, V_{UVLO} = 3 V, V_{CS} = 0.4 V R_{DT} = 274 kΩ, V_{UVLO} = 3 V, V_{CS} = 0.05 V	t_{D1a} t_{D1b} t_{D1c} t_{D1d} t_{D1e} t_{D1f}	47.3 56.8 63.1 107.1 206.5 259.9	63 95 84 179 275 433	78.8 132.6 105.2 250 344.2 606.4	ns
Overlap Delay from OUTM to OUTA Falling Edges	R_{DT} = 52.3 kΩ, V_{UVLO} = 2.5 V, V_{CS} = 0.4 V R_{DT} = 52.3 kΩ, V_{UVLO} = 2.5 V, V_{CS} = 0.05 V R_{DT} = 69.8 kΩ, V_{UVLO} = 2.5 V, V_{CS} = 0.4 V R_{DT} = 69.8 kΩ, V_{UVLO} = 1.5 V, V_{CS} = 0.05 V R_{DT} = 274 kΩ, V_{UVLO} = 3 V, V_{CS} = 0.4 V R_{DT} = 274 kΩ, V_{UVLO} = 3 V, V_{CS} = 0.05 V	t_{D2a} t_{D2b} t_{D2c} t_{D2d} t_{D2e} t_{D2f}	31.2 37.5 41.6 70.7 136.3 171.5	42 63 56 118 182 286	52 87.5 69.4 165 227.2 400.2	ns
Ratio from t_{D1} to t_{D2}			–	0.66	–	
RAMP						
PWM Propagation Delay	Step V_{RAMP} to 2 V to OUTM falling edge, dV/dt = 10 V/μs	t_{PWM}		40	60	ns
PWM Offset Voltage		$V_{PWM(offset)}$		1.35		V
Discharge Switch On Resistance	V_{RAMP} = 100 mV	$R_{AMPswitch(on)}$	–	–	25	Ω
RAMP Input Leakage Current	V_{RAMP} = 1.8 V	$I_{RAMP(leak)}$	–	–	100	nA
THERMAL SHUTDOWN						
Thermal Shutdown	Temperature increasing	T_{SHDN}	150	165	–	°C
Thermal Shutdown Hysteresis	Temperature decreasing	$T_{SHDN(HYS)}$	–	20	–	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Guaranteed by Design. Not Tested.
5. Guaranteed by Design.

TYPICAL OPERATING CHARACTERISTICS

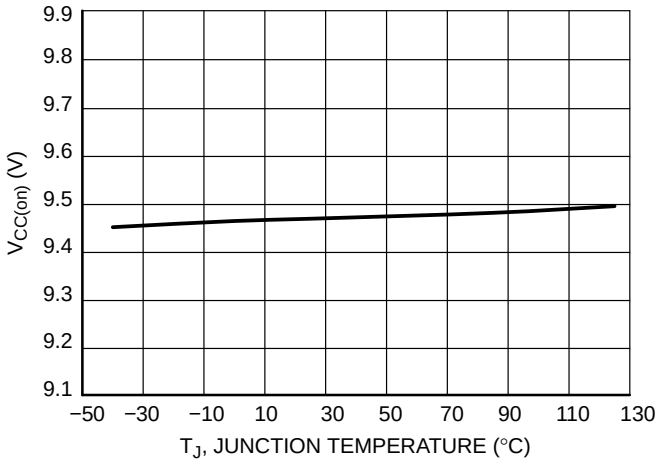


Figure 4. Turn−on Voltage Variation vs. Junction Temperature

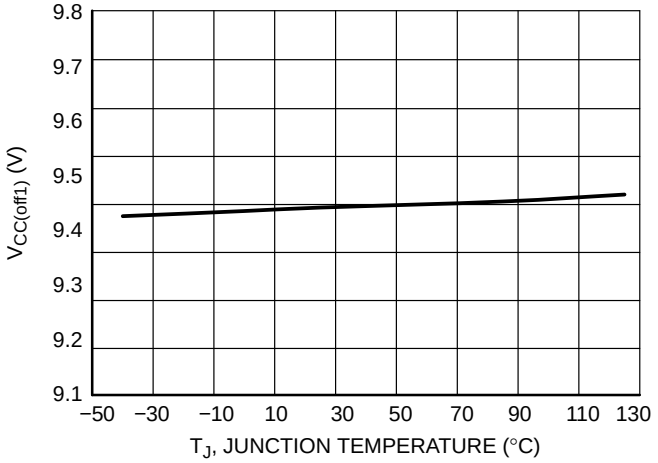


Figure 5. Turn−off Voltage 1 Variation vs. Junction Temperature

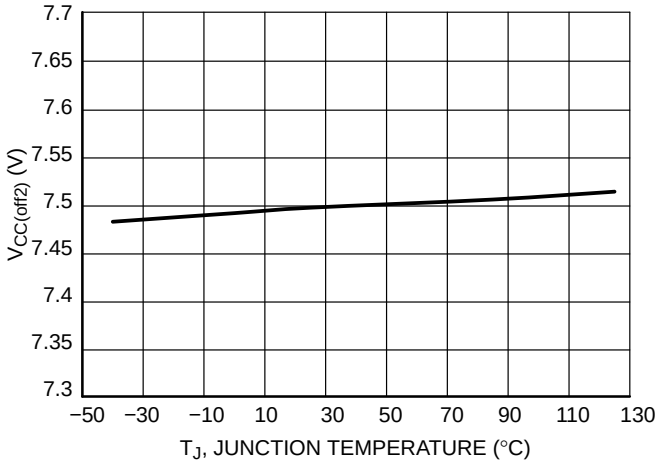


Figure 6. Turn−off Voltage 2 Variation vs. Junction Temperature

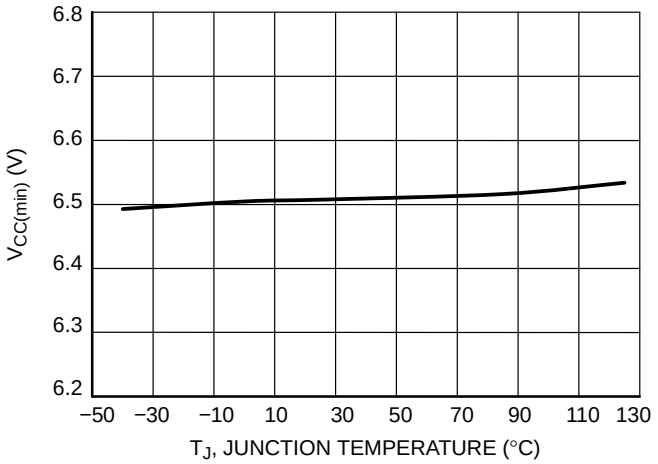


Figure 7. Minimum Operating Voltage Variation vs. Junction Temperature

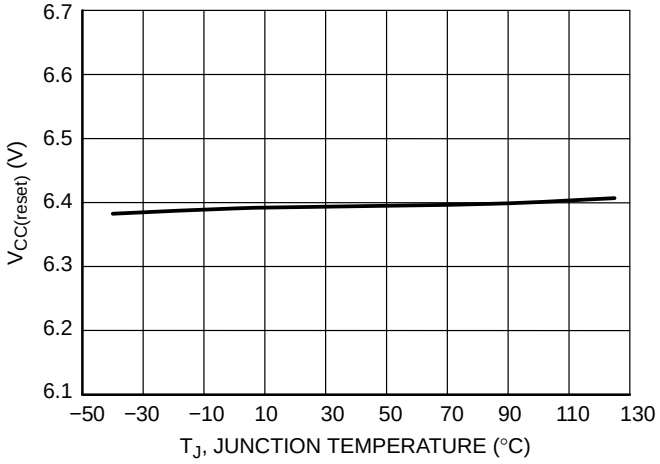


Figure 8. Reset Voltage Variation vs. Junction Temperature

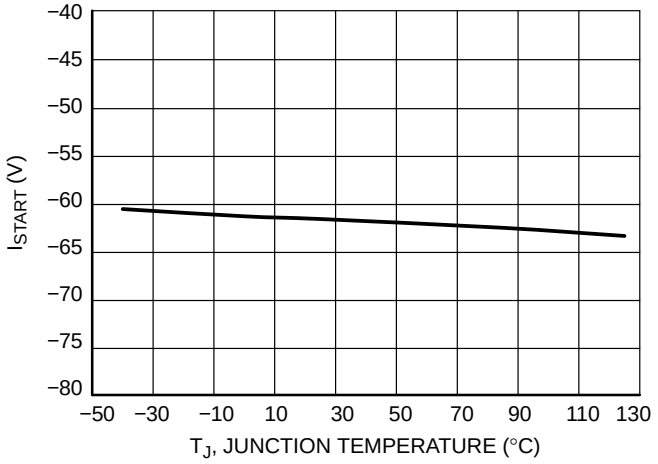


Figure 9. Start−up Current Variation vs. Junction Temperature

TYPICAL OPERATING CHARACTERISTICS

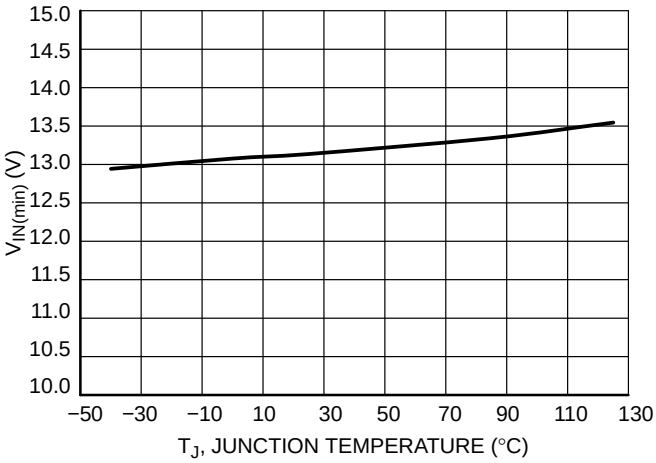


Figure 10. Minimum Startup Voltage on the HV Pin Variation vs. Junction Temperature

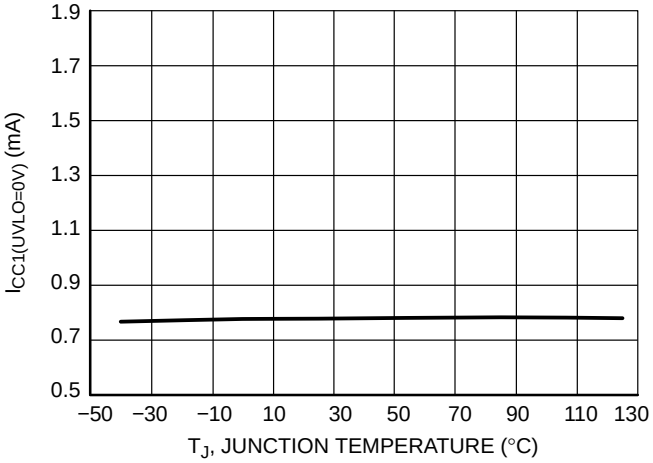


Figure 11. Operating Current in Disabled Mode vs. Junction Temperature

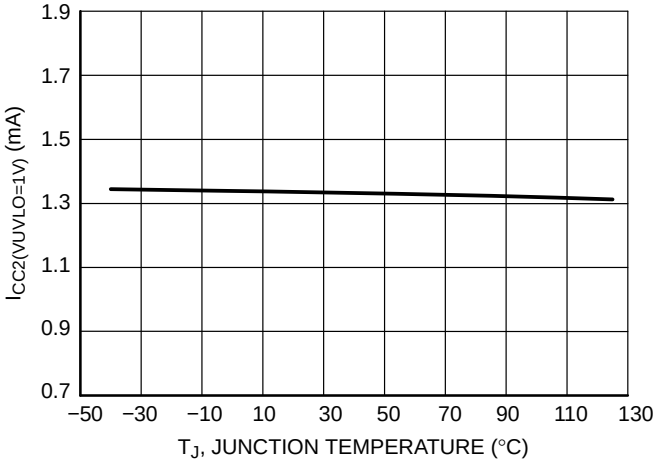


Figure 12. Operating Current in Standby Mode vs. Junction Temperature

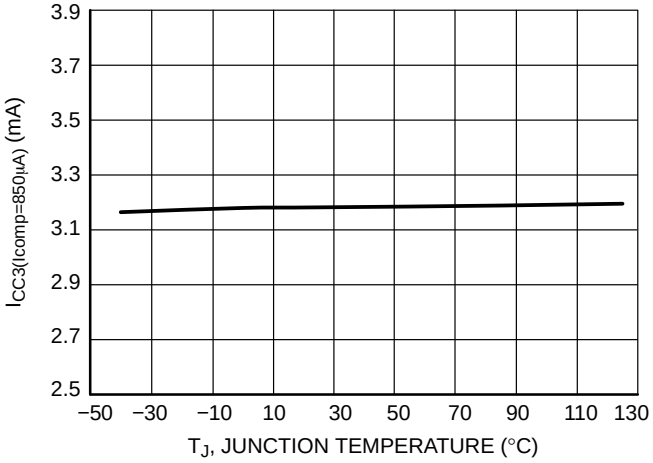


Figure 13. Operating Current in Active Mode but Without Switching vs. Junction Temperature

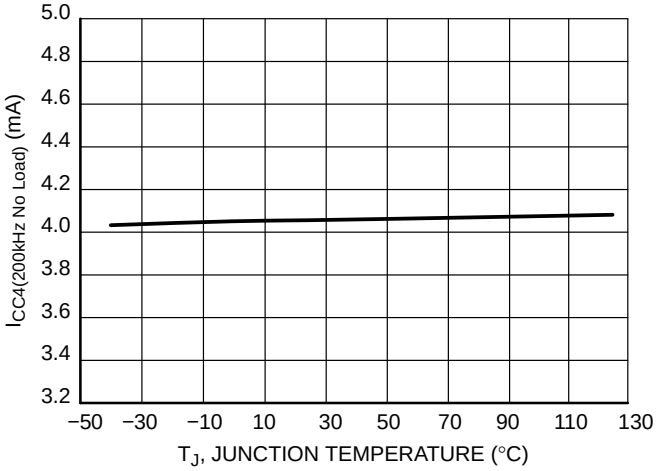


Figure 14. Operating Current While Switching Without Load on Driver Outputs vs. Junction Temperature

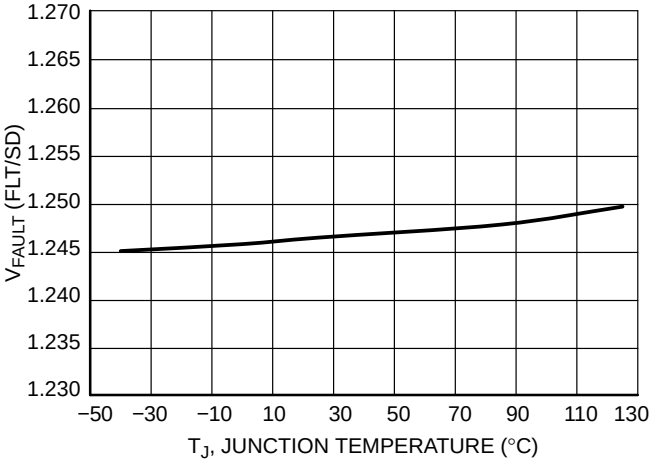


Figure 15. Fault Pin Activation Level vs. Junction Temperature

TYPICAL OPERATING CHARACTERISTICS

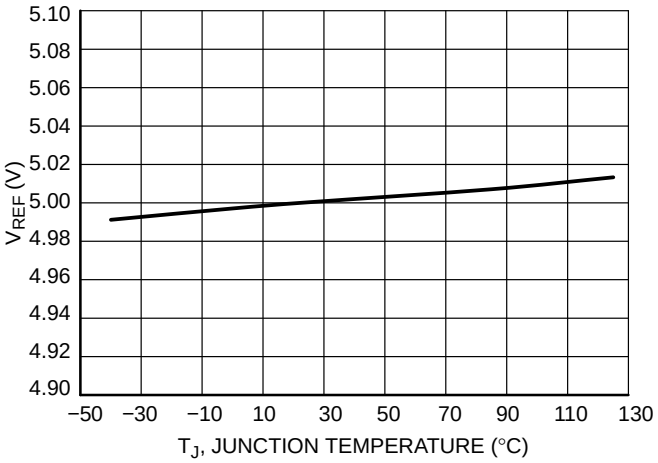


Figure 16. Reference Voltage Variation vs. Junction Temperature

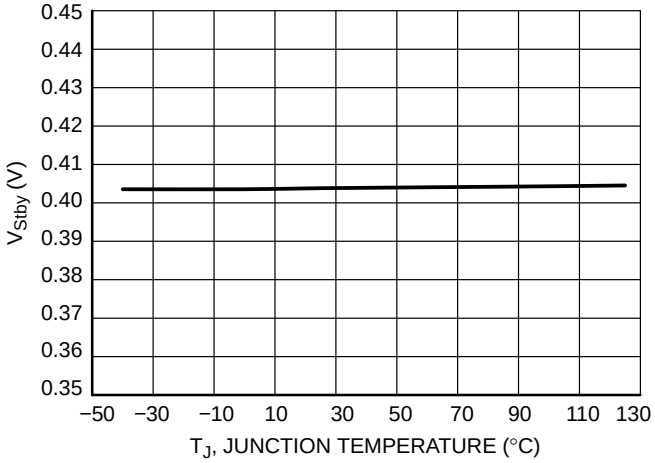


Figure 17. Standby Threshold Variation vs. Junction Temperature

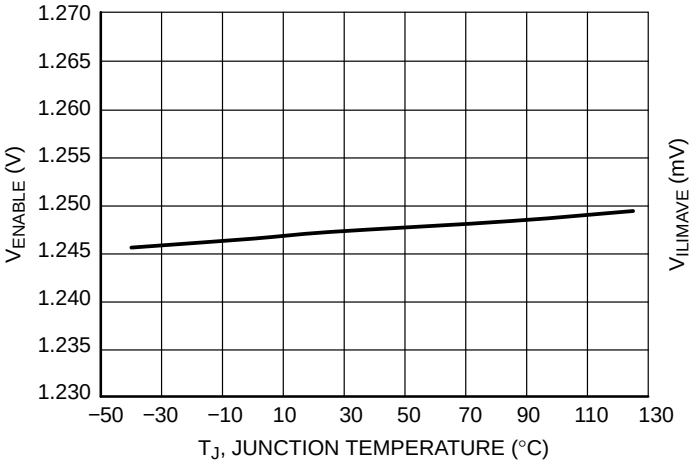


Figure 18. Enable Voltage Variation vs. Junction Temperature

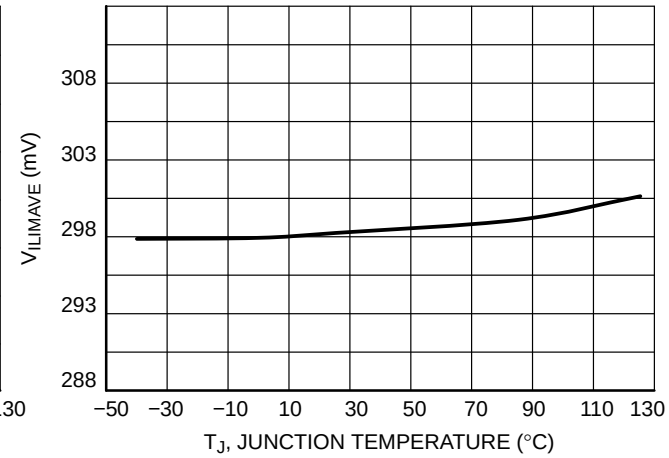


Figure 19. Average Current Limit Threshold Variation vs. Junction Temperature

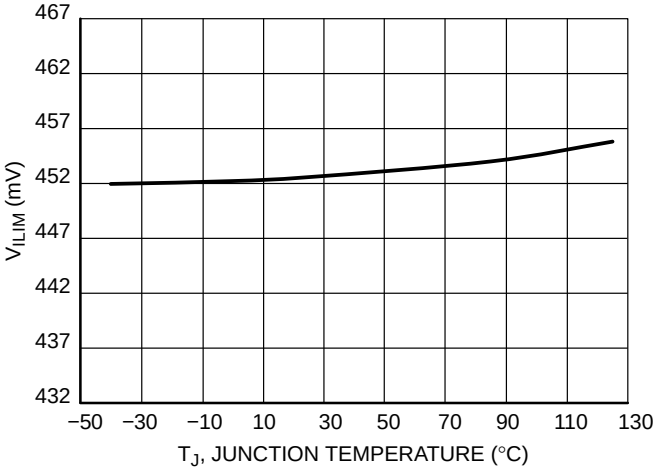


Figure 20. Cycle by Cycle Current Limit Threshold Variation vs. Junction Temperature

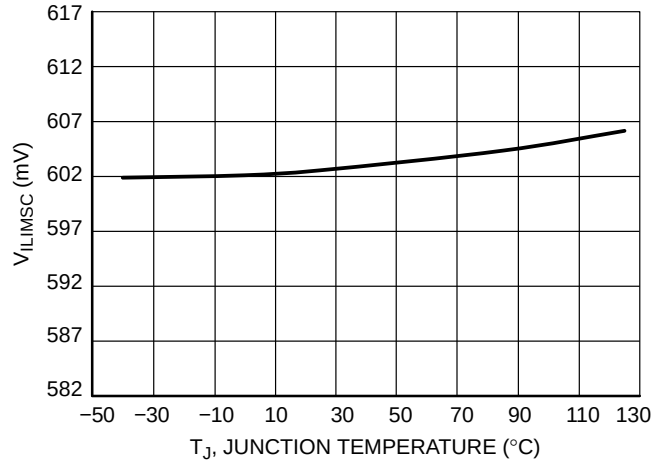


Figure 21. Short−Circuit Current Limit Threshold Variation vs. Junction Temperature

TYPICAL OPERATING CHARACTERISTICS

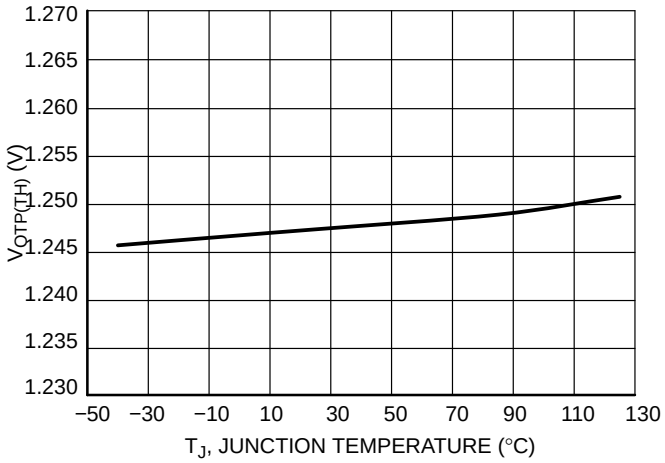


Figure 22. OTP Threshold Variation vs. Junction Temperature

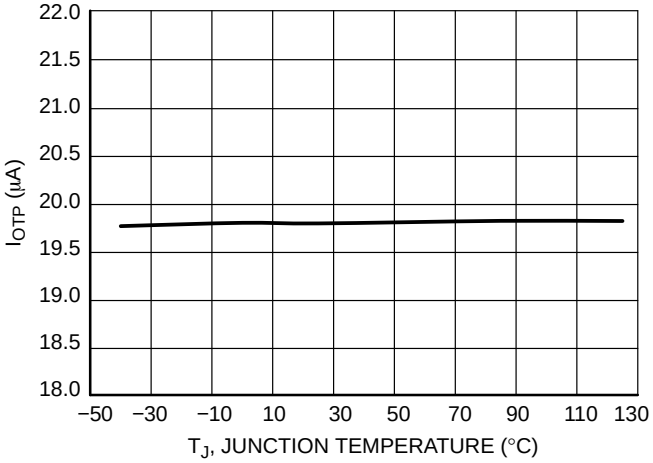


Figure 23. OTP Current Variation vs. Junction Temperature

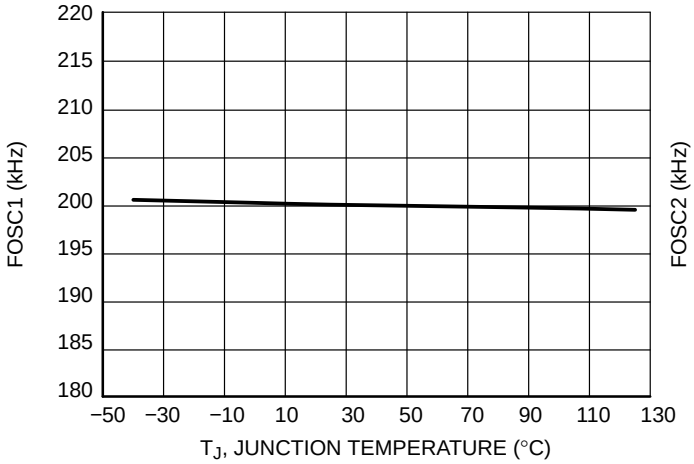


Figure 24. Oscillator Frequency Variation vs. Junction Temperature (F_{SW} = 200 kHz)

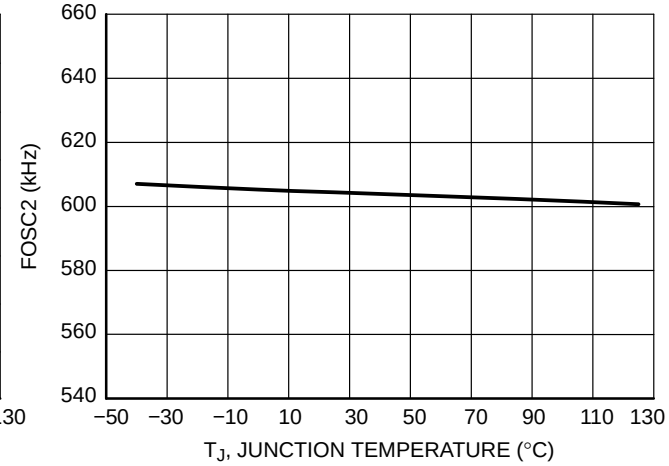


Figure 25. Oscillator Frequency Variation vs. Junction Temperature (F_{SW} = 600 kHz)

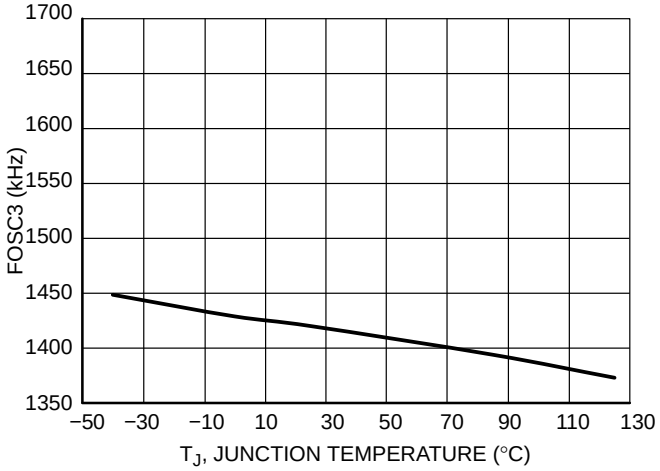


Figure 26. Oscillator Frequency Variation vs. Junction Temperature (F_{SW} = 1.5 MHz)

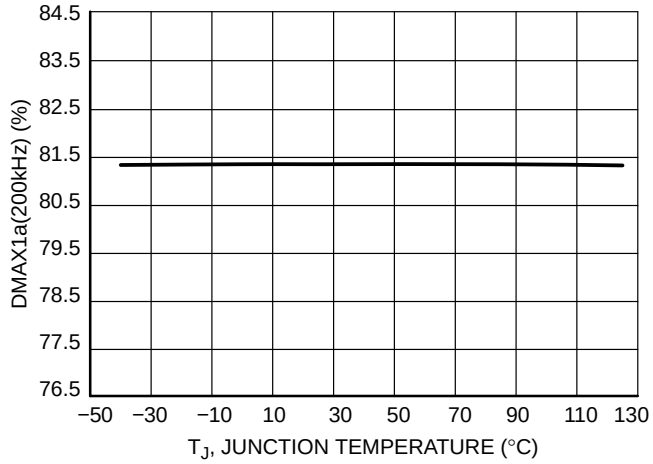


Figure 27. Maximum Duty Ratio Variation vs. Junction Temperature (F_{SW} = 200 kHz)

TYPICAL OPERATING CHARACTERISTICS

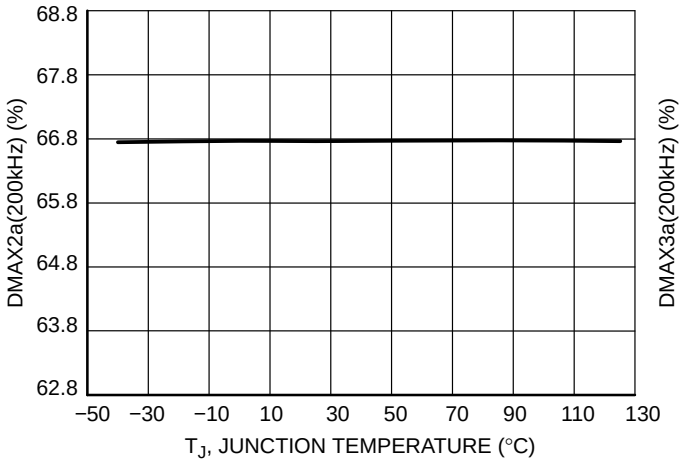


Figure 28. Maximum Duty Ratio Variation vs. Junction Temperature (F_{SW} = 200 kHz)

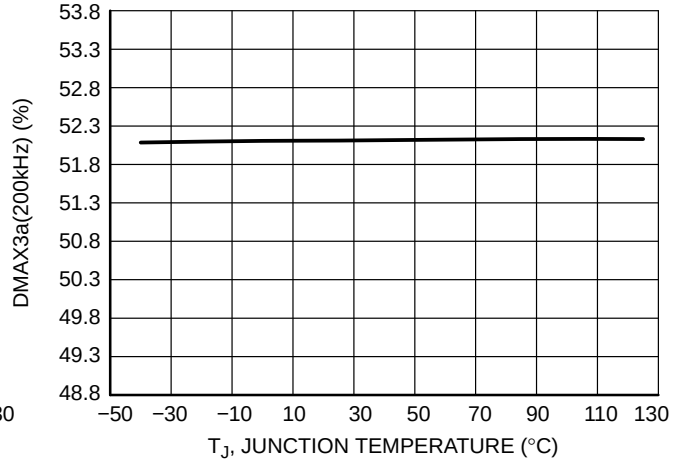


Figure 29. Maximum Duty Ratio Variation vs. Junction Temperature (F_{SW} = 200 kHz)

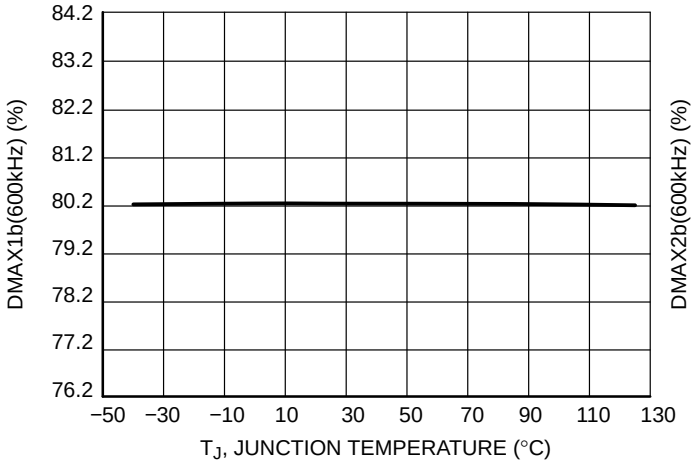


Figure 30. Maximum Duty Ratio Variation vs. Junction Temperature (F_{SW} = 600 kHz)

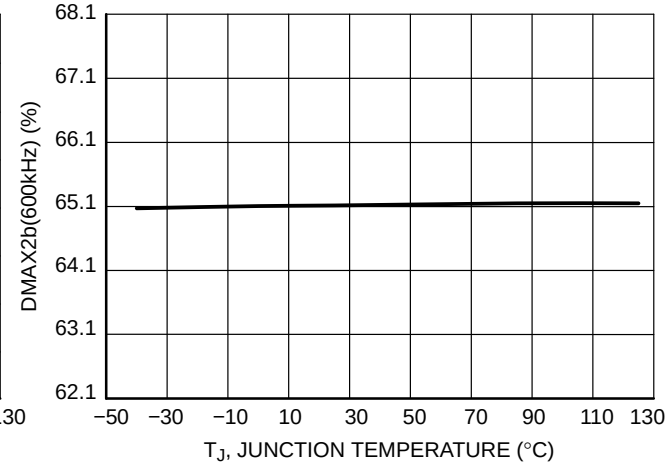


Figure 31. Maximum Duty Ratio Variation vs. Junction Temperature (F_{SW} = 600 kHz)

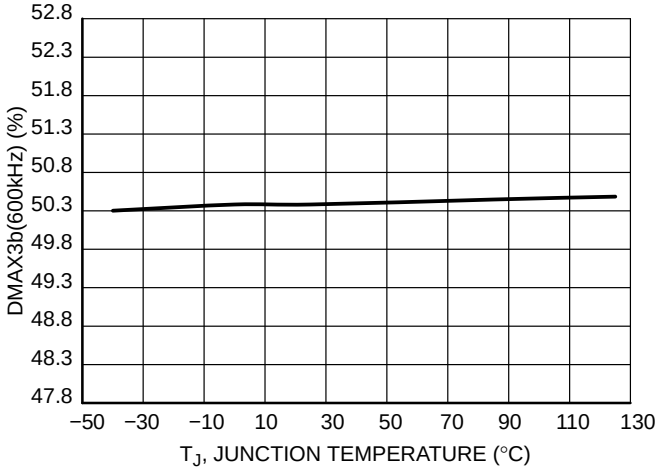


Figure 32. Maximum Duty Ratio Variation vs. Junction Temperature (F_{SW} = 600 kHz)

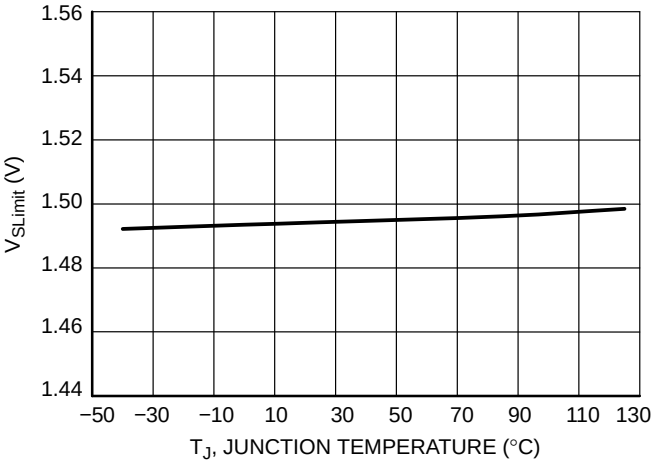


Figure 33. Volt−Second Limit vs. Junction Temperature

TYPICAL OPERATING CHARACTERISTICS

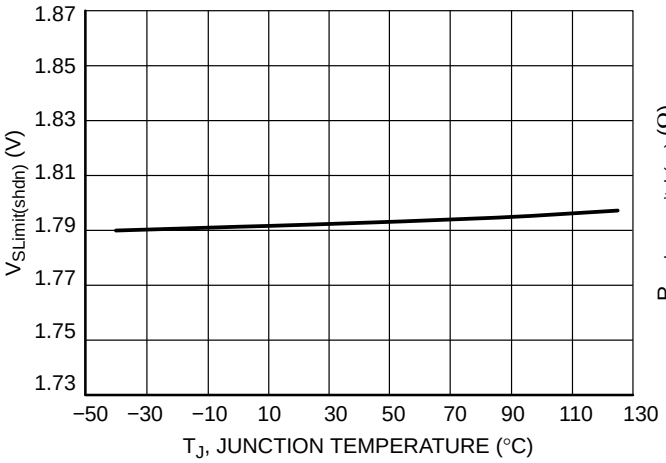


Figure 34. Shutdown Pulse Volt−Second Limit vs. Junction Temperature

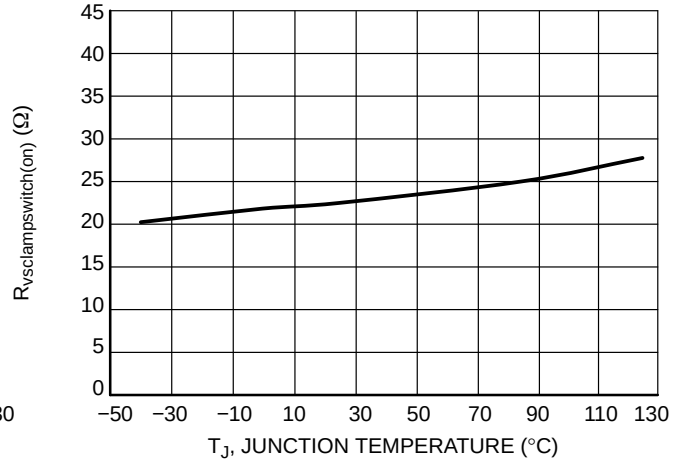


Figure 35. Volt−Second Switch−On Resistance Variation vs. Junction Temperature

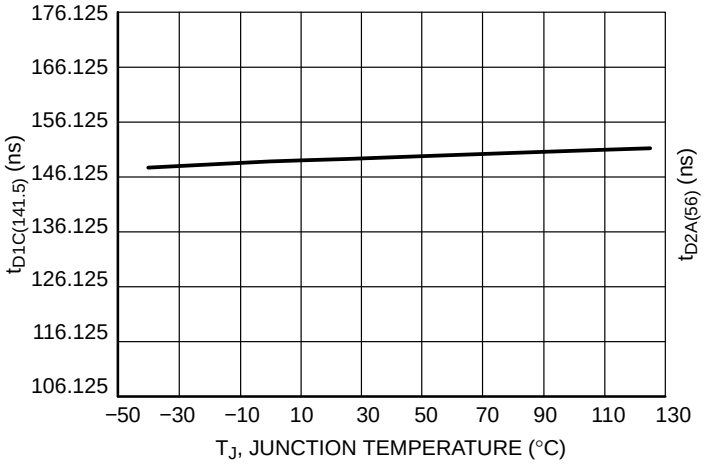


Figure 36. Overlap Delay OUTA to OUTM Variation vs. Junction Temperature

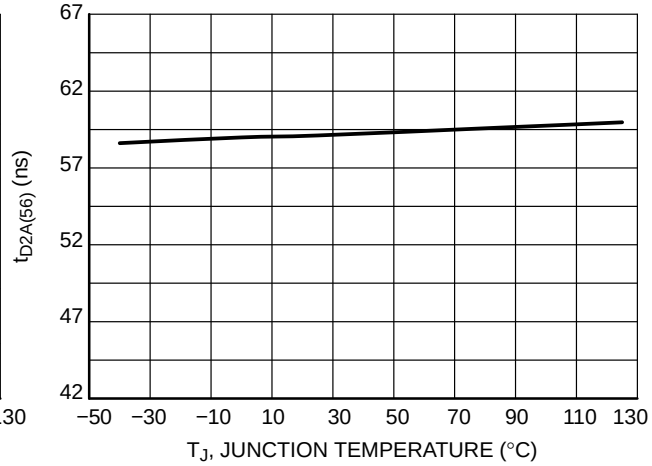


Figure 37. Overlap Delay OUTM to OUTA Variation vs. Junction Temperature

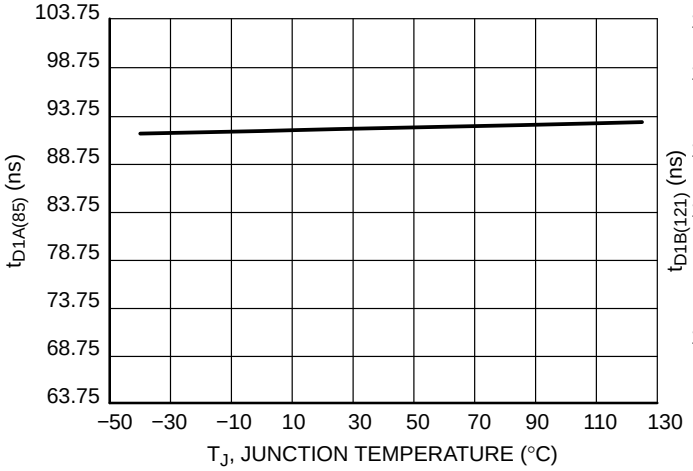


Figure 38. Overlap Delay OUTA to OUTM Variation vs. Junction Temperature

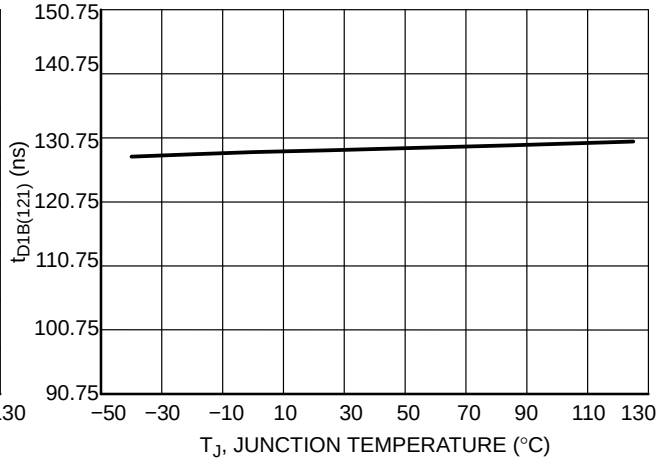


Figure 39. Overlap Delay OUTA to OUTM Variation vs. Junction Temperature

TYPICAL OPERATING CHARACTERISTICS

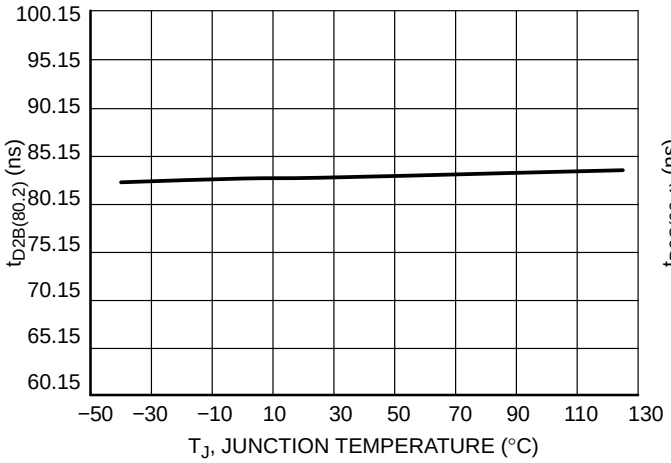


Figure 40. Overlap Delay OUTM to OUTA Variation vs. Junction Temperature

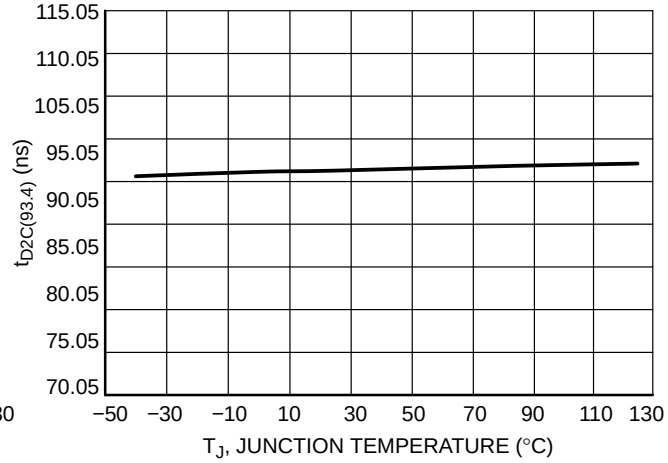


Figure 41. Overlap Delay OUTM to OUTA Variation vs. Junction Temperature

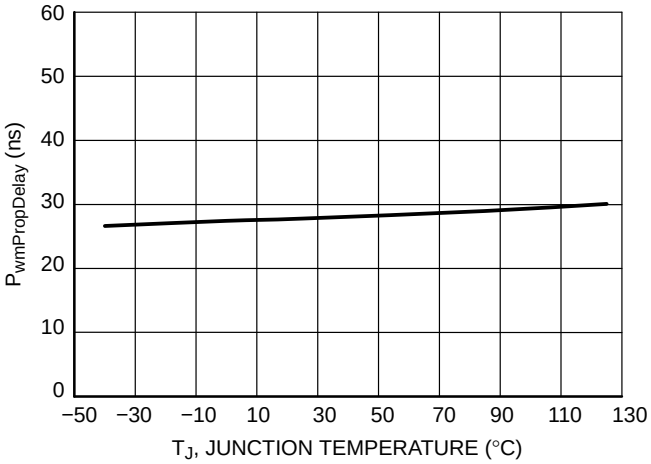


Figure 42. Pulse Width Modulator Delay Variation vs. Junction Temperature

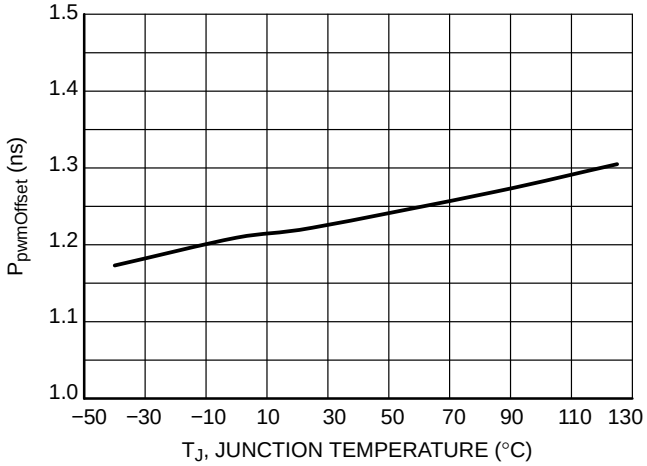


Figure 43. Pulse Width Modulator Offset Variation vs. Junction Temperature

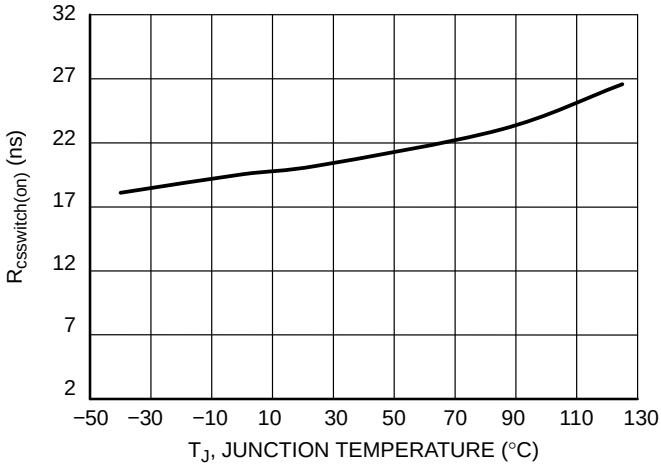


Figure 44. Current Sense Pin Discharge Switch $r_{DS(on)}$ Variation vs. Junction Temperature

APPLICATION INFORMATION

The NCP1565 is a highly−integrated dual−mode active clamp PWM controller targeting next−generation high−density, high−performance and small to medium power level isolated dc−dc converters for use in telecom and datacom applications. Operating up to 1.5 MHz, the part can be configured in either voltage mode control with input voltage feedforward or peak−current mode control. An adjustable adaptive overlap time between the main power and the active clamp MOSFETs optimizes system efficiency based on input voltage and load conditions enabling higher efficiency and greater power density solutions.

This controller integrates all the necessary control and protection functions to implement an isolated active−clamp forward or asymmetric half−bridge converter with synchronous rectification. It integrates a high−voltage startup bias regulator directly connected to the dc input, up to 120 V. The NCP1565 protection features include:

- A line undervoltage detector to stop operation in case the input rail collapses below a programmable level
- A two−threshold cycle−by−cycle current limit which allows to detect short circuit situations but also overload conditions on the dc−dc converter output
- A line voltage−dependent maximum duty ratio limit to safely operate the forward transformer
- A programmable over temperature protection using an external NTC sensor
- An adjustable re−start time to force an auto−recovery hiccup mode in presence of the above faults

The part includes a dedicated pin $\overline{\text{FLT/SD}}$ for signaling the presence of a fault condition. The pin can be used as an input to shutdown the controller using an external signal. The controller also features an adjustable restart time.

High−Voltage Startup Circuit

The NCP1565 integrates a high voltage startup circuit accessible by the V_{in} pin. The startup circuit is rated up to a maximum voltage of 120 V. The startup regulator consists of a constant current source that supplies current from a high−voltage rail to the supply capacitor on the V_{CC} pin (CV_{CC}). The startup circuit current (I_{start}) is 40 mA minimum. The internal high voltage startup circuit eliminates the need for external startup components. In addition, this regulator reduces no−load power and increases the system efficiency as it uses negligible power in the normal operation mode.

The startup circuit is configured to operate in the so−called Dynamic Self−Supply (DSS) mode in certain conditions. In this DSS mode, V_{CC} hiccups between two levels (9.5 V and 9.4 V typically) and self supplies the IC in lack of auxiliary supply. This mode can be briefly entered at startup (fault clearance delay) but it is mainly activated in a fault state or in lack of auxiliary V_{CC}: in this mode, as no external supply is present, the DSS block permanently maintains the controller supply until the auxiliary V_{CC} comes back. This is the case for instance in deep DCM mode when the part skips cycle. V_{CC} can no longer be maintained (pulses are too narrow) and V_{CC} collapses until it hits 7.5 V. At this point, the DSS takes over. Please make sure power dissipation in this mode respects the maximum power dissipation capability of the controller.

A typical startup sequence commences with the charge of the V_{CC} capacitor up to the startup threshold $V_{CC(on)}$, 9.5 V typically. Once this threshold is reached, the current source turns off and the part starts its own internal initialization: it resets all registers, charges the soft−start capacitor above 0.5 V, makes sure all the fault inputs are cleared ($\overline{\text{FLT/SD}}$ is high, the OverTemperature Protection (OTP) input is low and the input voltage sensed by the UVLO input is within acceptable limits). As the V_{CC} capacitor is alone to supply the controller during this startup time, the level across its terminals falls and eventually reaches $V_{CC(off1)}$, typically 9.4 V, especially if some faults are still present at startup. At this point, the current source turns back on until V_{CC} reaches $V_{CC(on)}$, again: a hiccup takes place and lasts until the part is ready to switch, i.e. all faults are cleared. Once internal flags are ready, an extra delay is added, $t_{delay(start)}$, before the part is actually enabled and switches. After the enable signal has been asserted, the V_{CC} UVLO level drops to $V_{CC(off2)}$, typically 7.5 V

During the initialization sequence, the main power MOSFET is not switching, OUTM is low. On the opposite, to allow the immediate availability of the low−side P−channel active clamp switch, its dedicated output OUTA is raised to V_{CC} when the 9.5 V threshold is reached. This is to allow the pre−charge of the P−channel charge pump capacitor and makes it ready for operation.

While the part is enabled, the voltage on the soft−start (SS) capacitor is slowly rising up and when it crosses the internal 1.35 V offset, OUTM starts to produce low duty ratio pulses, driving the forward converter main power MOSFET. Please note that while the internal enable flag is not asserted (during the initialization sequence or during a fault), the voltage on the SS pin is clamped to 0.85 V, naturally putting the part in ready−to−pulse mode whenever enable gets asserted.

At the end of the initialization sequence, the controller stops the high−voltage startup source and V_{CC} drops as the auxiliary voltage did not build up yet. Before reaching the lower regulation threshold, $V_{CC(off2)}$, typically 7.5 V, the auxiliary winding must have appeared to take over the controller supply. You will size the V_{CC} capacitor in that way. If for any reason the auxiliary winding did not build up before V_{CC} reaches 7.5 V, the current source turns back on again to maintain the controller supply in a kind of non−regulated hysteretic mode... In this DSS mode, the current capability is 40 mA at minimum and you have to make sure the internal IC consumption (including driving current) is well below 40 mA. During this mode, the average current absorbed by the V_{in} pin is roughly the average

current consumed by the part. Care must be taken to ensure that a low current is absorbed while in the upper input voltage range. Failure to respect this fact will damage the controller by overheat.

In case an accidental overload of the DSS would occur (you consume too much on the V_{cc} pin and the DSS cannot maintain V_{CC}), the voltage would drop to $V_{CC(MIN)}$, typically 6.5 V. In this mode, the part restarts after a start−up sequence. A typical successful start−up sequence appears in Figure 45 while it fails in Figure 46 as the current absorbed from the V_{CC} is too high. In this case, the part restarts again for another attempt.

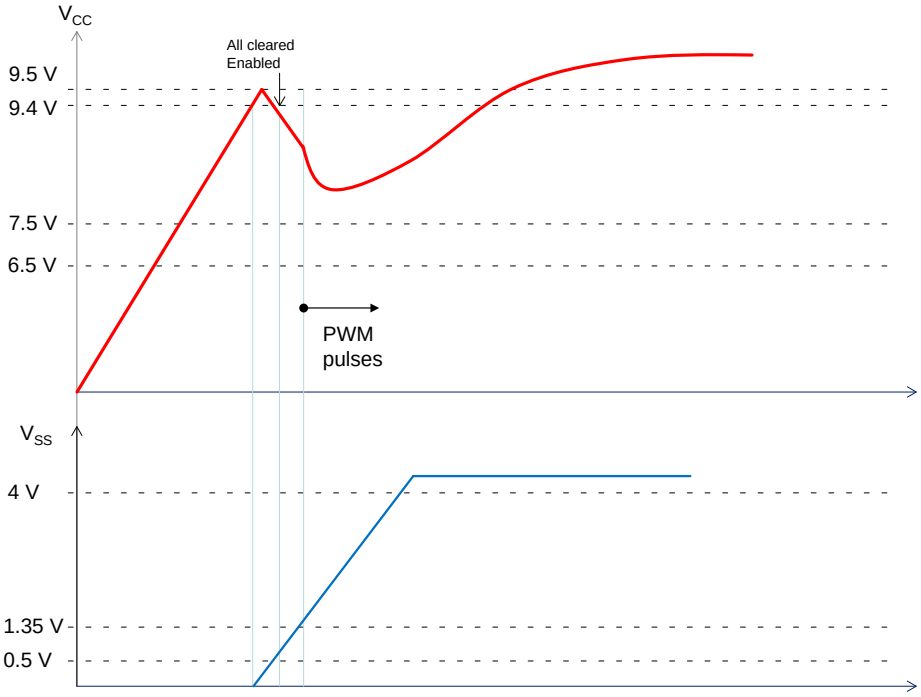


Figure 45. A Typical Startup Sequence in Which the Auxiliary Voltage Builds Up in Time

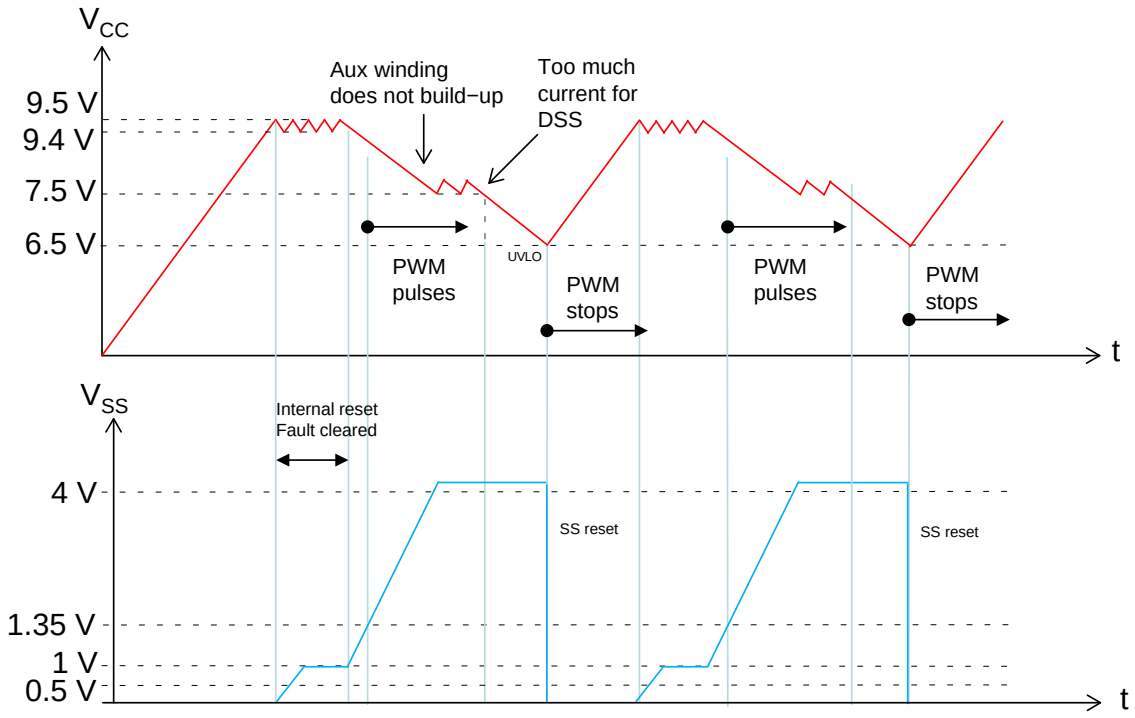


Figure 46. In this Figure, the Auxiliary Voltage did not Build up in Time, Aborting the Startup Sequence

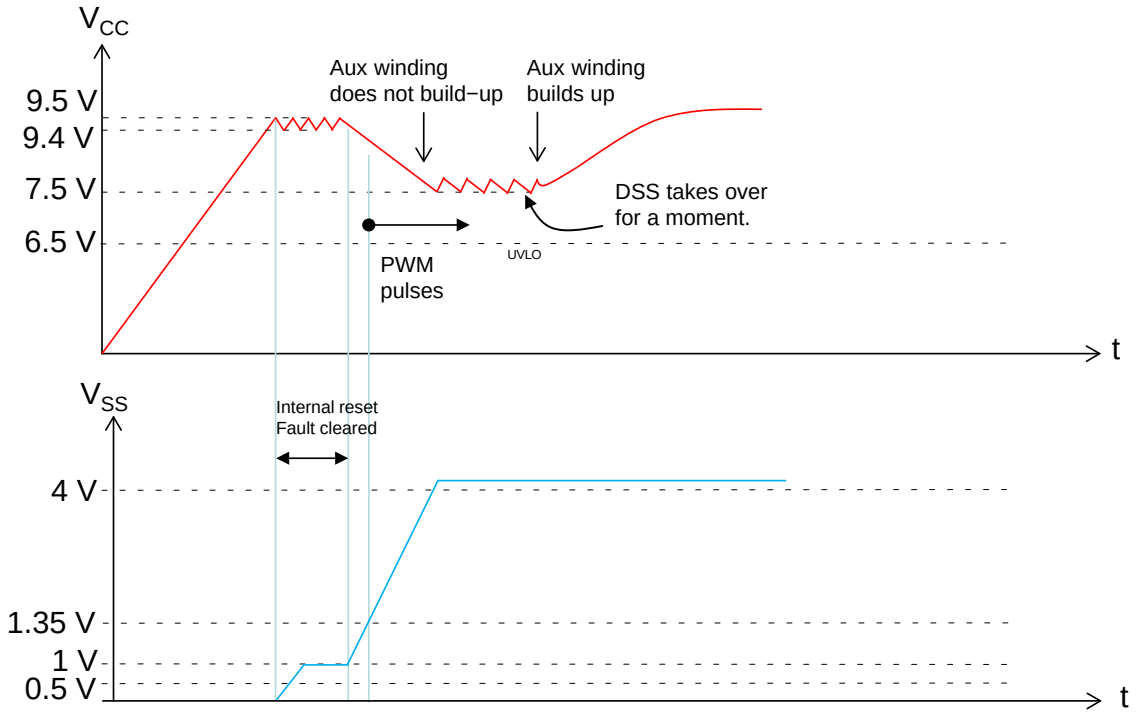


Figure 47. In this Figure, the VCC Capacitor is Small and is Getting Help from the DSS Until the Auxiliary Voltage Eventually Takes Off

The V_{CC} capacitor must be sized such that a V_{CC} voltage greater than $V_{CC(off2)}$ is maintained while the auxiliary supply voltage is building up. However, if the capacitance has adversely dropped because of extreme temperatures conditions for instance, it can happen that V_{CC} drops too fast and the DSS is activated. This is what Figure 47 shows. DSS takes over until V_{CC} aux builds up. Again, care must be taken to ensure that part power dissipation remains within acceptable limits.

The operating IC bias current, I_{CC4}, and gate charge load at the drive outputs must be considered to correctly size CV_{CC}. To size this capacitor, you must account for the MOSFET drive current. The average current absorbed from the V_{CC} capacitor at startup depends on the switching frequency F_{sw} and the total gate charge Q_G as follows:

$$I_{DRV} = F_{sw}Q_G \qquad \text{(eq. 1)}$$

Assume we picked a 40 nC gate−charge MOSFET operated at 200 kHz. The average current absorbed by the driver will be:

$$I_{DRV} = 200k \times 40n = 8\ mA \qquad \text{(eq. 2)}$$

The capacitor value depends on several parameters:

- The allowed voltage drop before the controller activates the DSS at 7.5 V. This drop is 2 V, from 9.5 V to 7.5 V.
- The current sourced by the capacitor while the auxiliary winding is building up. It is made of Equation 1 plus the internal controller consumption, I_{CC4} (4 mA at 200 kHz).
- The time taken by the auxiliary winding to build up is more difficult to assess given the numerous parameters at play: primary−side current limit, soft−start duration, output capacitance and so on. Simulations in worst−case give us an estimated time of 5 ms for the auxiliary supply to reach 8 V.

With these parameters on hand, the V_{CC} capacitor can be evaluated:

$$CV_{CC} \geq \frac{(I_{DRV} + I_{CCR})t_{startup}}{\Delta V} = \frac{12m \times 5m}{2} = 30\ \mu F \qquad \text{(eq. 3)}$$

A 47 μF capacitor is a possible choice. Figure 47 illustrates a typical start−up sequence.

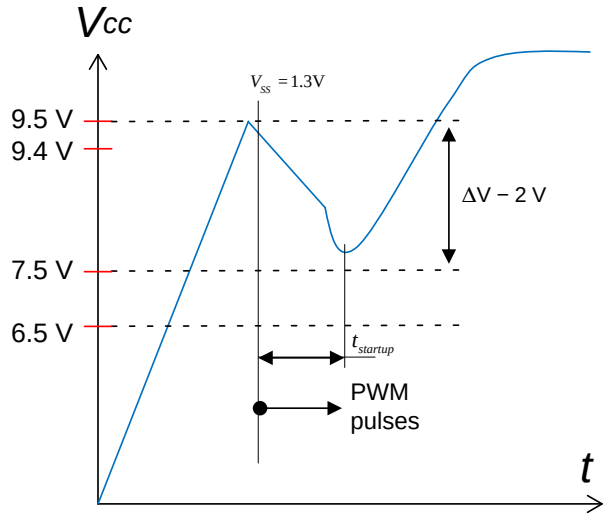


Figure 48. This Sketch Shows how the VCC Capacitor can be Sized to Avoid Tripping the DSS Circuit at Start−up

If power dissipation is under control during start up, you can reduce the capacitor value given by Equation 3 and implement the start−up scheme shown in Figure 46. Demonstration boards with 1−2 μF V_{CC} capacitors have shown proper operation with these values.

Line Undervoltage Detector

The NCP1565 monitors the line voltage and enables the controller when the input voltage is within the required range. The input voltage is also used for modulating the drivers overlap time as we will see later. The input voltage is sampled using a resistor divider and applied to the UVLO pin. A small bypass capacitor is recommended for noise filtering. The UVLO input can be used as an enable/disable function. Figure 49 shows the UVLO detector architecture.

By monitoring the voltage on the UVLO pin, the controller can be put in three different modes: disable, standby and enable. The controller enters standby mode once the UVLO voltage, V_{UVLO}, exceeds the standby threshold, V_{STBY}, typically 0.4 V. The standby mode features a 100 mV hysteresis, $V_{STBY(HYS)}$, which, added to a 1.5 μs delay, provides adequate noise immunity. In standby mode, V_{CC} hiccups between 9.5 and 9.4 V, the reference voltage is maintained. The $\overline{FLT/SD}$ pin is pulled low to signal the UVLO. Figure 49 illustrates an input voltage drop that keeps V_{UVLO} above 0.4 V, putting the part into standby mode.

The controller transitions into the enable mode once V_{UVLO} exceeds V_{enable}, typically 1.25 V. Once in enable mode, the controller is allowed to start if no other faults are present. An internal pull−down current source, I_{STBY}, provides hysteresis. It is typically 20 μA. I_{STBY} turns off once the controller is enabled, allowing V_{UVLO} to rise above V_{enable} by the hysteresis level set by R_1. The controller is disabled if V_{UVLO} falls below V_{enable}, at which point I_{STBY} is re−enabled creating a voltage drop on the UVLO pin. A maximum delay of 1 μs, $t_{enable(delay)}$, on the Enable Comparator provides noise immunity. I_{STBY} is disabled while V_{CC} is below $V_{CC(off2)}$ during power up or if V_{CC} falls below $V_{CC(reset)}$ after I_{STBY} has been enabled.

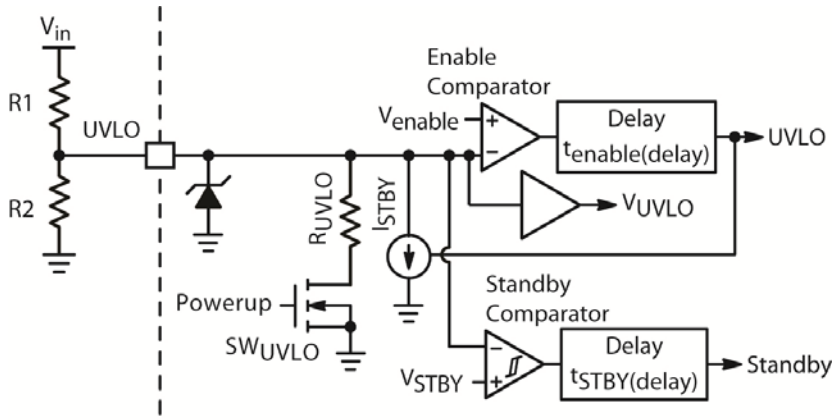


Figure 49. UVLO Block Diagram

The resistor divider is selected such that V_{UVLO} exceeds V_{enable} at the desired input voltage. Equation 4 is used to calculate the startup voltage level, $V_{in(start)}$. Equation 5 is used to calculate the minimum operating voltage, $V_{in(min)}$.

$$V_{in(start)} = V_{enable}\left(\frac{R_1 + R_2}{R_2}\right) + R_1 I_{STBY} \quad \text{(eq. 4)}$$

$$V_{in(min)} = V_{enable}\left(\frac{R_1 + R_2}{R_2}\right) \quad \text{(eq. 5)}$$

A pull−down transistor and resistor combination, SW_{UVLO} and R_{UVLO}, ensure V_{UVLO} is below V_{enable} while I_{STBY} is disabled. This prevents the controller from incorrectly turning on while V_{UVLO} settles.

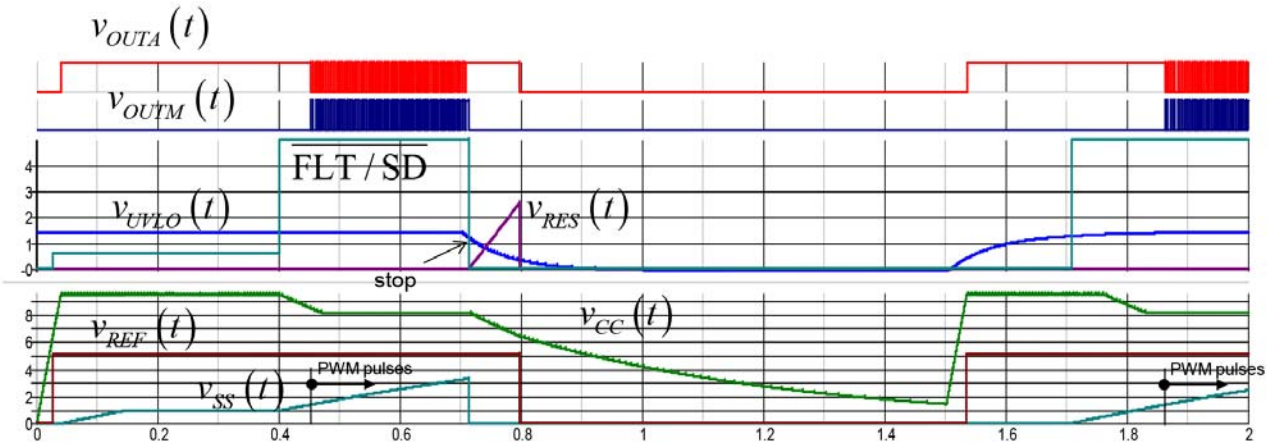


Figure 50. The Part Starts up while V_{in} is ok. V_{in} now decreases to 0, shutting off the part. V_{in} is back again shortly after, restarting the part.

Soft−start

Soft−start slowly increases the duty ratio during power up, allowing the controller to gradually reach steady−state operation by slowly increasing the output voltage while reducing startup circuit stress. The duty ratio is controlled by comparing the SS pin voltage, V_{SS}, to the VSCLAMP pin voltage, V_{SCLAMP}. V_{SCLAMP} is level−shifted by 1.35 V before comparing it to V_{SS}. This ensures a minimum duty ratio of 0%.

V_{SS} is slowly increased by charging the soft−start capacitor with a fixed current source, I_{SS}, typically 20 μA. OUTM is disabled once the peak voltage of V_{SCLAMP} exceeds V_{SS}. The soft−start pin is internally grounded while a fault is present.

Current Sense

A signal proportional to the current across the main switch is applied to the CS pin. The current sense information is used to calculate the average primary current to modulate the drivers overlap time and implement overcurrent protection (OCP). It is also used for cycle by cycle peak current limit control and detecting a short circuit condition. Figure 50 shows the block diagram of the current limit circuitry.

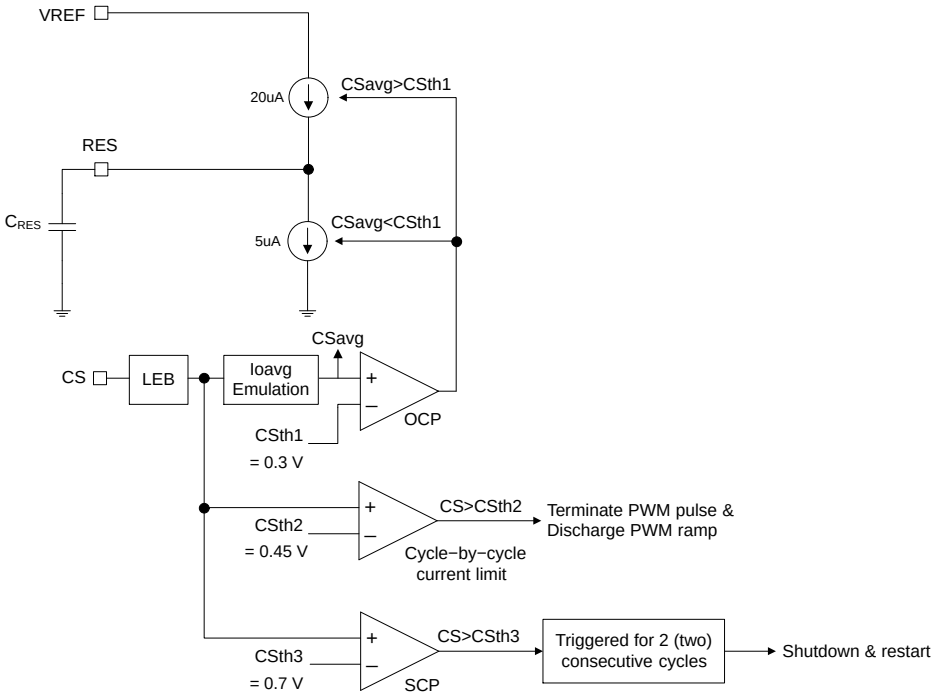


Figure 51. The Current Limit Circuitry Implements Three Distinct Comparators

The controller can identify three different types of overcurrent conditions:

- Regular current pulse: in a forward converter normal operation, the primary current is made of the reflected inductor current to which adds the primary magnetizing current. When the voltage image of this current exceeds the feedback setpoint (in current mode) or the maximum sense voltage (0.45 V typical in voltage mode), the current pulse is terminated.
- Short−circuit pulse: if an abnormally−high current pulse is detected (0.7 V) for two consecutive clock pulses, the part shuts off and goes into restart mode. This can happen during a winding short circuit or in presence of a defective component in the secondary side.
- Overcurrent condition: in case the converter's output is overloaded, the average input current will increase, reflecting the average input power increase. The NCP1565 averages the primary−side current sense information and when it exceeds a certain value, a shutdown delay starts. When this delay elapses, the part shuts off and goes into restart mode.

An Internal leading edge blanking (LEB) circuitry masks the current sense information before applying it to the current monitoring circuitry. LEB prevents unwanted noise from terminating the drive pulses prematurely. It is recommended to place a small *RC* filter close to the CS pin to suppress noise. The LEB period begins once V_{OUTM} reaches approximately 2 V. To improve the pin noise immunity, an internal switch, $R_{CS(switch)}$, discharges and holds the CS pin low at the conclusion of every cycle. The switch is enabled while the main driver is low. The maximum impedance of the switch, is 20 Ω.

The average information is reconstructed from the CS information and used to determine the OCP shutdown delay. Once the average current information, $C_{S(AVG)}$, exceeds $V_{ILIM(AVE)}$, typically 0.3 V, the 5 μA pull−down current source, $I_{RES(SNK)}$, is disabled and the 20 μA pull−up current source, $I_{RES(SRC1)}$, is enabled to charge the RES capacitor. The average current information is blanked by the $t_{ILIMAVE(LEB)}$ timer, typically 30 ns. As long as an overcurrent is sensed, the capacitor connected to the RES pin continues its charge. If the overcurrent disappears, the 20 μA source stops and the capacitor discharges with the 5 μA pull−down source. If the overcurrent comes back again, the 20 μA source takes over and lifts the capacitor voltage towards the 1 V threshold. When it is reached, the part stops all operations and goes into restart mode: 32 up/down voltage cycles between 2/4 V are counted on the RES pin before an attempt to restart occurs.

Cycle by cycle peak current limit protection is implemented using the cycle−by−cycle comparator. It terminates the drive pulse if the CS voltage exceeds V_{ILIM}, typically 0.45 V. The cycle−by−cycle current information is blanked by the $t_{ILIM(LEB)}$ timer, typically 55 ns. The cycle−by−cycle comparator propagation delay, $t_{ILIM(delay)}$, is typically 40 ns. Cycle−by−cycle peak current limit protection is available in all operating modes.

The short circuit comparator protects the controller during a winding short circuit condition for instance. The comparator terminates the drive pulse if the CS voltage exceeds $V_{ILIM(SC)}$, typically 0.7 V. The short circuit current information is blanked by the $t_{ILIMSC(LEB)}$ timer, typically 30 ns. The short circuit comparator propagation delay, $t_{ILIMSC(delay)}$, is typically 40 ns. Two consecutive short circuit conditions cause the controller to enter restart mode without a shutdown delay.

Figure 52 shows simulation waveforms during a short circuit fault. Once the overcurrent fault is detected the main driver operates at minimum on time. At the third internal clock cycle, the short circuit condition is confirmed and a restart sequence is initiated. In restart mode, V_{CC} is hiccupping between $V_{CC(on)}$ and $V_{CC(off1)}$ and the soft−start capacitor is discharged.

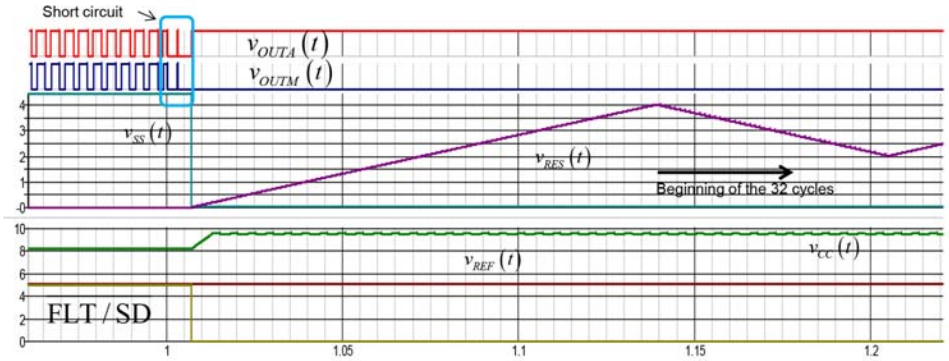


Figure 52. A Short Circuit Occurs and Shuts Down the Part After Two Consecutive Pulses

The current sense signal is generated using either a current sense resistor or current sense transformer. In both instances, good PCB layout practices are required to ensure correct operation of the current sense detection circuitry. A few are listed below:

1. The current sense filter capacitor must be placed as close as possible to the IC and referenced to the AGND pin.
2. When using a current sense transformer both leads of the transformer secondary should be routed to the filter network located very close to the IC.
3. Low current signals should all be connected to the AGND net. AGND should connect to the power ground at the return terminal of the input capacitor.
4. If using a current sense resistor, the return path should be connected to PGND and not AGND.

Volt−Second Clamp

A volt−second clamp is an important safety feature in any forward converter, especially active clamp type where the duty ratio excursion can easily exceed 50%. A clamp helps to prevent magnetizing current runaway and transformer saturation in faulty situations. An external *RC* divider ($R_{VSCLAMP}$−$C_{VSCLAMP}$) from the input line generates the VSCLAMP ramp to control the volt−second limit of the converter. The slope of the ramp is proportional to the input voltage and controls the maximum on−time during a line voltage transition. The ramp prevents from exceeding the maximum volt−second of the transformer by clamping the duty ratio excursion during the transient input. As NCP1565 can be configured to operate in both voltage mode and peak current mode control, Figures 53 and 54 respectively show the recommended clamp configuration for these operating modes.

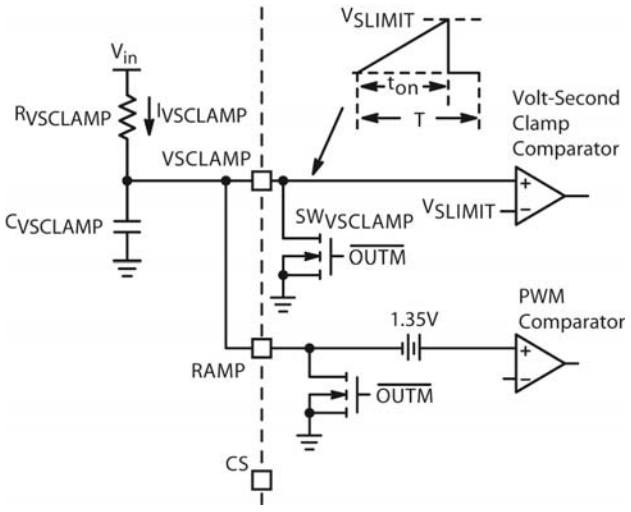


Figure 53. The VSCLAMP Configuration in Voltage−mode Control

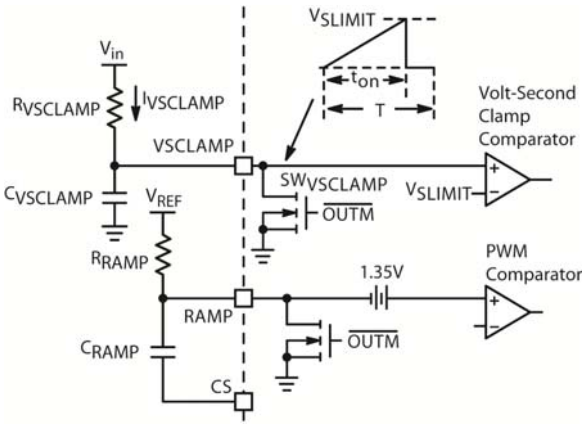


Figure 54. The VSCLAMP Configuration in Peak Current−mode Control

The PWM drive pulse terminates once the VSCLAMP ramp reaches V_{SLIMIT}, typically 1.5 V. The *RC* divider is selected such that the VSCLAMP ramp peak voltage reaches V_{SLIMIT} at the desired maximum volt−second limit. The VSCLAMP pin is pulled down by $SW_{VSCLAMP}$ at the end of every cycle and is held low until the next drive pulse.

The volt−second limit depends on the transformer you have. Assume the transformer specification allows a maximum volt−second product of 111.6 V−μs for a 200 kHz operation (62% duty ratio max at a 36 V input voltage). It means that maximum on−times at low and high line cannot respectively exceed:

$$t_{on,maxLL} < \frac{V{-}\mu s_{max}}{V_{in,min}} = \frac{111.6}{36} = 3.1\ \mu s \quad \text{(eq. 6)}$$

$$t_{on,maxHL} < \frac{V{-}\mu s}{V_{in,max}} = \frac{111.6}{76} = 1.47\ \mu s \quad \text{(eq. 7)}$$

The *RC* network is thus dimensioned so that the ramp hits the 1.5−V limit in less than 1.47 μs when the input voltage is 76 V or 3.1 μs when the input is 36 V. Let us select a normalized capacitor value of 1 nF for instance. In this case, if we consider a near−linear charging current (the series resistor is of high value), then the necessary current will be:

$$I_{charge} > \frac{V_{limit}C_{VSclamp}}{t_{on,maxHL}} = \frac{1.5 \times 1n}{1.47\mu} = 1.02\ mA \quad \text{(eq. 8)}$$

A 1 mA current provides adequate noise immunity. In this case, $R_{VSclamp}$ is simply obtained by:

$$R_{VSclamp} = \frac{t_{on,max}}{C_{VSclamp} \ln\left(1 - \frac{V_{Slimit}}{V_{in,max}}\right)} \quad \text{(eq. 9)}$$

$$= \frac{1.47\mu}{\ln \times \ln\left(1 - \frac{1.5}{76}\right)} = 73.74\ k\Omega$$

It is recommended to keep $R_{VSCLAMP}$ and $C_{VSCLAMP}$ close to the controller and away from high dv/dt signals such as drive outputs or swinging high−voltage nodes. $C_{VSCLAMP}$ must be connected to AGND for a reliable operation.

Comp Input

The PWM Comparator modulates the duty ratio to regulate the output voltage. A signal proportional to the loop error signal is applied to this pin using an optocoupler. A voltage proportional to the error signal, V_{error}, is internally generated and compared to a regulation ramp. The on−time terminates once the ramp exceeds the internal error voltage. In voltage−mode control the VSCLAMP ramp signal is used for regulation (see Figure 53). In current mode control the sum of the current sense ramp and the voltage compensation ramp is used for regulation.

The internal error voltage is generated by applying a current into the COMP pin as shown in Figure 55. The COMP current is internally mirrored with a 10−to−1 ratio. The mirrored current pulls down on a 50 kΩ pull−up resistor from V_{REF}.

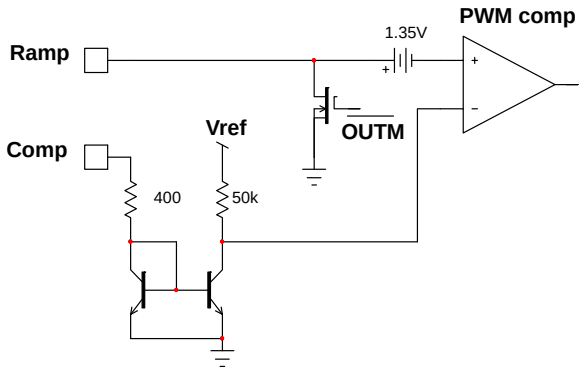


Figure 55. COMP Input Architecture

An almost constant voltage across the optocoupler is achieved when using a current−based feedback input. This results in a faster system response because duty ratio adjusts without the need to charge/discharge the large optocoupler parasitic capacitance. In the frequency domain, the optocoupler pole is moved to a higher frequency allowing the system to operate at a higher crossover frequency. The COMP pin dynamic resistance is 400 Ω. This resistance does not play a role in the loop gain but enters the picture if you plan to place a capacitor across the COMP pin to ground.

Maximum duty ratio is achieved when the COMP current is 0 A or when the pin is left open. A duty ratio of 0% is achieved when the COMP current is approximately 850 μA.

Frequency

The oscillator frequency, F_{sw}, is set by placing a resistor, R_T, between the RT and AGND pins. The NCP1565 is optimized for operation between 200 kHz and 1.5 MHz. Equation 10 shows the relationship between F_{sw} and R_T.

$$R_T = \left(\frac{1}{F_{sw}} - 20\ ns\right) \cdot 10^{10} \quad \text{(eq. 10)}$$

R_T should be placed directly across the RT and AGND pins. Assuming a 200 kHz switching frequency, then R_T should be:

$$R_T = \left(\frac{1}{200k} - 20\ ns\right) \cdot 10^{10} = 49.8\ k\Omega \quad \text{(eq. 11)}$$

Maximum Duty Ratio

The maximum duty ratio of the oscillator is set by placing a resistor, R_{DLMT}, between the DLMT and AGND pins. The adjustable duty ratio range is between 50% and 80%. The maximum duty ratio accuracy is ±3%. The resistor that sets the maximum duty ratio depends on the timing resistance calculated in Equation 10. It depends on the timing resistance but also on an overlap delay, t_{D1}. The overlap time (t_{D1}) between OUTA and OUTM reduces the effective duty ratio of OUTM. Please look in the electrical characteristics table to know what overlap value to use.

$$R_{DLMT} = \left(\frac{D_{max}}{F_{sw}} + t_{D1} - 20\ ns\right) R_T F_{sw} \quad \text{(eq. 12)}$$

Assume our transformer specification states a maximum duty ratio of 62%. Our circuit operates at a 200 kHz frequency and the overlap time is set to 75 ns. We should place a resistance of the following value:

$$R_{DLMT} = \left(\frac{0.62}{200k} + 75n - 20\ ns\right) \times 49.8k \times 200k \quad \text{(eq. 13)}$$

$$= 31.4\ k\Omega$$

R_{DLMT} should be placed directly across the DLMT and AGND pins.

Fault Reporting and Shutdown Input

The $\overline{FLT/SD}$ pin reports the presence of a fault to an external supervisory circuitry. It also can be used to shutdown the controller if externally brought down. This pin has an open collector output with a 10 kΩ internal pull−up resistor ($R_{\overline{FLT/SD}}$) connected to the 5 V reference. The $\overline{FLT/SD}$ pin is internally pulled low (to indicate a fault) by an internal transistor, , when an overcurrent, short circuit, $V_{CC(UVLO)}$, OVP, OTP or low input voltage fault is detected. The pin is also pulled low when the controller is in restart mode.

During the initialization sequence, the shutdown detection pin is released once V_{REF} reaches its regulation level. The controller considered that the $\overline{FLT/SD}$ pin is cleared from a fault when the pin voltage, $V_{\overline{FLT/SD}}$, exceeds the enable threshold, $V_{FLT(enable)}$, typically 1.45 V, and V_{SS} exceeds $V_{SS(disable)}$, typically 0.5 V. The controller is disabled once $V_{\overline{FLT/SD}}$, falls below the shutdown threshold,

V_{fault}, typically 1.25 V. While the controller is in shutdown state, V_{CC} is hiccupping between 9.5/9.4 V typically and V_{REF} is kept high. When the $\overline{FLT/SD}$ pin is brought low, the part activates the restart delay (RES is cycled up and down 32 times) before a new restart is authorized when the $\overline{FLT/SD}$ pin is released.

Restart Mode

The NCP1565 incorporates a restart timer to disable the controller for a certain amount of time and initiate a hiccup mode operation if a fault is detected. In short circuit operations, this technique limits the overall dissipated power. Once the fault is gone, the controller automatically resumes operations. A restart event occurs if one of the following faults is detected:

- Overcurrent fault (OCP)
- Two consecutive short−circuit pulses (SCP)
- Overtemperature fault detected on OTP pin
- Internal thermal shutdown fault
- The pin has been externally pulled low

Please note that the pin is internally held low during the duration of the restart timer. The simplified architecture of the restart timer is shown in Figure 56.

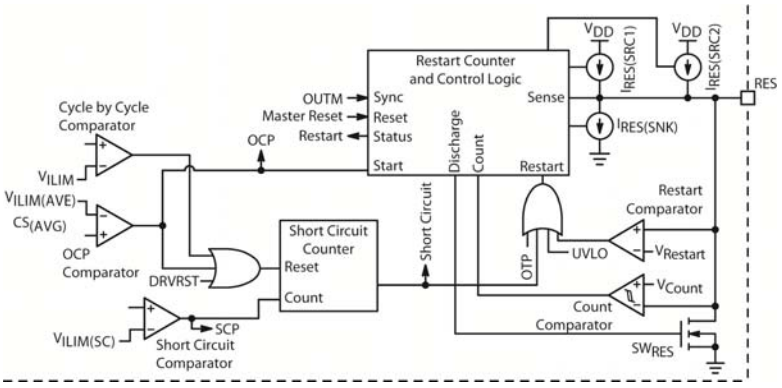


Figure 56. Restart Timer Architecture

A pull−down current source, $I_{RES(SNK)}$, typically 5 μA, holds the RES pin at a low level when no faults are present. The restart timer sequentially charges and discharges 32 times the capacitor on the RES pin, C_{RES}, between 2 V and 4 V to set the restart or hiccup duration. A fault triggers a restart or hiccup delay with the exception of an overcurrent fault. An overcurrent fault starts the shutdown delay timer before drive pulses are cut. A restart sequence initiates once the shutdown delay expires.

The RES pin combines two functions: the restart delay and the shutdown delay. As explained, the restart delay is made of 32 up/down cycles between 2/4 V on the RES pin. The shutdown delay is actually the time taken by the RES pin to charge from 0 to 1 V. This charge is initiated by the average input current reconstruction. When this internal averaged current exceeds 0.3 V, the capacitor on the RES pin is charged by the 20 μA source. If the overcurrent goes away, the capacitor slowly discharges by a 5 μA pull−down current sink. If the fault comes back, the 5 μA sink turns off and the 20 μA is reactivated. When the capacitor voltage eventually reaches 1 V, all pulses are stopped and the part enters auto−recovery hiccup mode via the restart delay.

Figure 57 shows operating waveforms during an overload condition. The controller is disabled once V_{RES} exceeds 1 V.

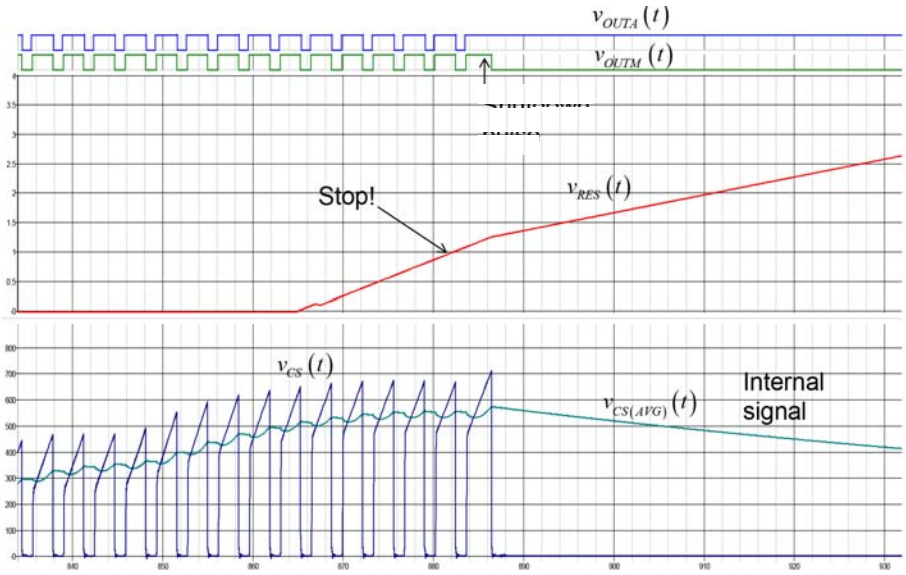


Figure 57. Overload Condition Operating Waveforms

Hiccup is ensured by charging and discharging the capacitor connected to the RES pin C_{RES} between 2 and 4 V. Charge and discharge currents are equal to 5 μA and respectively correspond to parameters $I_{RES(SRC2)}$ and $I_{RES(SNK)}$. The restart mode ends after 32 consecutive charge/discharge cycles. C_{RES} is then pulled low using an internal pull down transistor, SW_{RES}. The transistor is disabled once V_{RES} falls below the discharge level, $V_{RES(DIS)}$, typically 100 mV. Once C_{RES} is fully discharged a new startup sequence commences and soft−start is released.

During the restart delay, the VCC pin is maintained by the controller operating the high−voltage current source in the DSS mode: the voltage hiccups between 9.4 V and 9.5 V.

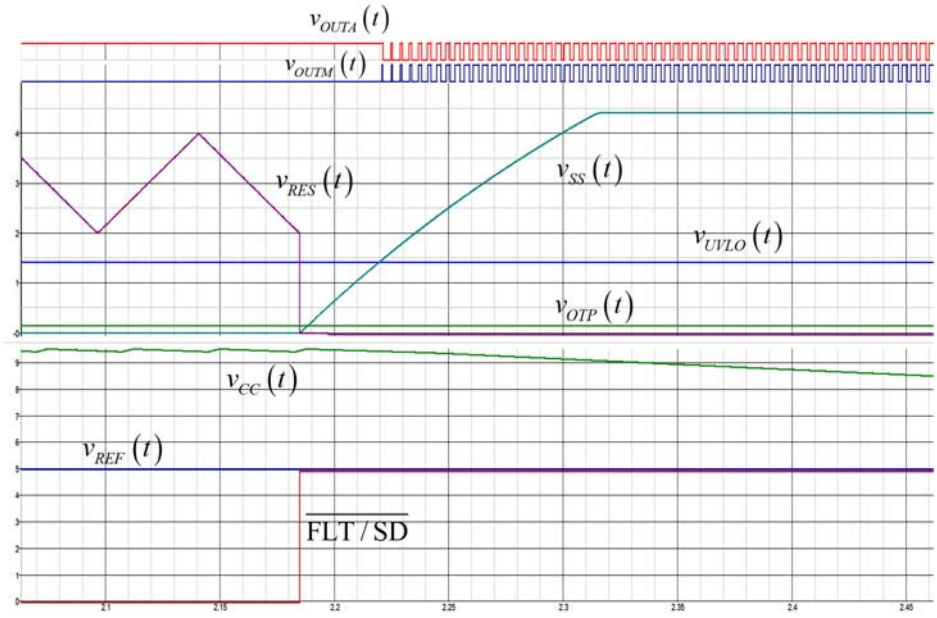


Figure 58. Timing Diagram Exiting Restart

Gate Drive Outputs

The NCP1565 has two in−phase output drivers with an adaptive overlap delay (t_D). The main output, OUTM, can sink a minimum of 3 A and source a minimum of 2 A. The secondary output, OUTA, can sink a minimum of 1 A and source a minimum of 2 A.

OUTM is configured to drive an N−channel MOSFET as the main switch. OUTA is configured to drive a P−channel MOSFET which source is grounded. OUTA is purposely sized smaller than OUTM because the active clamp MOSFET only sees the magnetizing current in an active clamp forward topology. Therefore, a smaller active clamp

MOSFET with less input capacitance is used compared to the main switch. Also, on−losses associated with this P−channel have a beneficial damping effect on the $L_{mag}C_{clamp}$ resonating network.

Once V_{CC} reaches $V_{CC(on)}$, the internal startup circuit is disabled and OUTA goes high to pre−charge the P−channel charge pump capacitor. OUTA goes low following OUTM after the overlap delay expires. OUTA remains high while the controller is disabled or until V_{CC} falls below $V_{CC(reset)}$.

The outputs are biased directly from V_{CC} and their high state voltage is approximately V_{CC}. Therefore, the auxiliary supply voltage should not exceed the maximum gate voltage of the main and active clamp MOSFETs.

The inductance between the drivers and its load should be kept to a minimum to minimize current induced voltage spikes. This can be achieved by reducing the connection length between the drivers and their loads and using wide traces for connections.

Adaptive Overlap Time

In an active clamp forward converter, there are two delays involved in the driving signals. Both deal with Zero Voltage Switching (ZVS) operations. When the main N−channel MOSFET turns off, the magnetizing current finds an immediate path in the P−channel body diode. The conduction of this diode forces a low voltage across the drain−source terminals of the considered MOSFET. Once this condition is obtained, the P−channel can be turned on. This delay ensures ZVS is present for the P−channel. To limit switching losses on the main N−channel MOSFET, you also want to ensure quasi or full ZVS operation. To meet this requirement, the P−channel will be turned off slightly before turning on the N−channel so that the drain−source voltage can swing down to ground or approach it: this is the second delay.

A simplified block diagram and waveforms of an active clamp forward converter with a low side active clamp switch are shown in Figure 59. Driver OUTM drives the main switch where as OUTAC drives the active clamp switch. Overlap time between the drive signals is required to achieve zero or near zero volts switching (ZVS) on the switches.

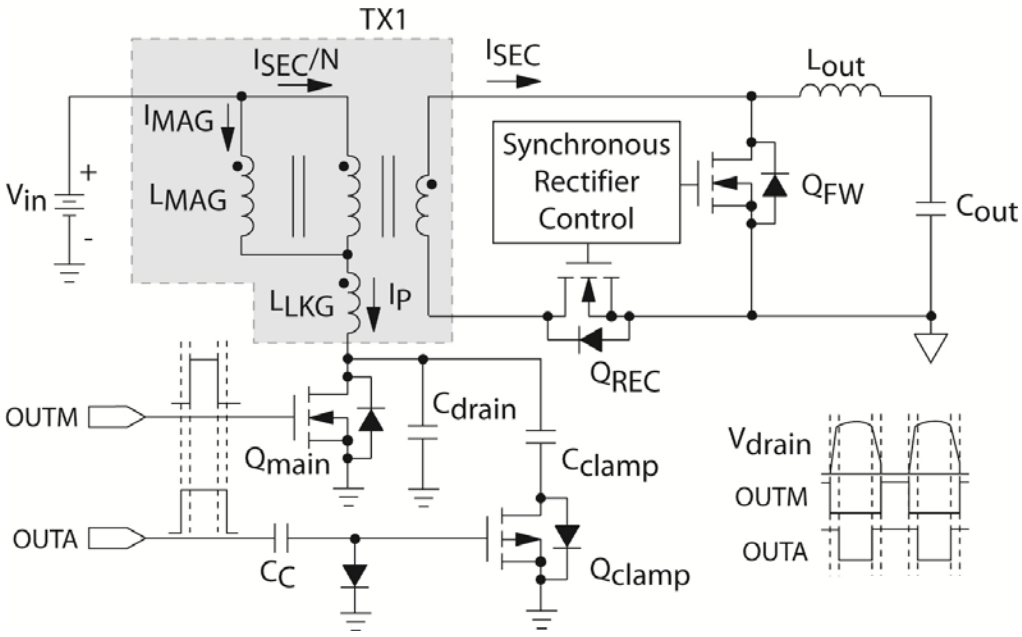


Figure 59. Active−clamp Forward Topology

OUTA leads OUTM during a low to high transition by a time duration given by t_{D1}. OUTA trails OUTM during a high to low transition by a time duration given by t_{D2}. Figure 60 shows the overlap time delays between the OUTA and OUTM drive signals.

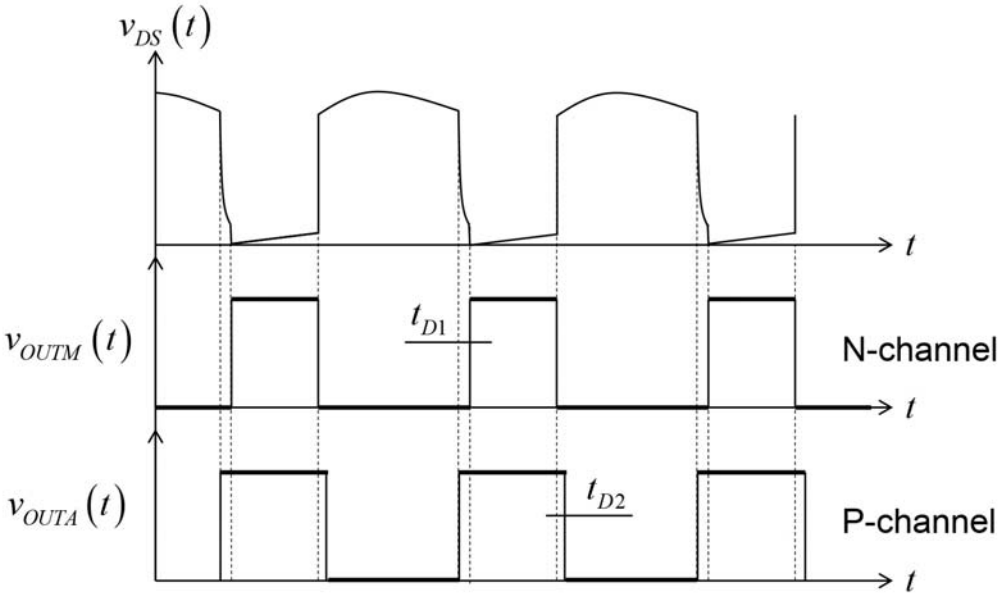


Figure 60. Overlap Time Waveforms

The overlap time is usually optimized for full−load efficiency. However, the optimum overlap time required to achieve ZVS varies with line and load conditions. In light load, the magnetizing energy is reduced slowing down the drain voltage transitions. Keeping the same overlap regardless of loading conditions can affect the converter's efficiency along its operating range. NCP1565 adaptively adjusts the overlap times to optimize the system efficiency across operating conditions. The current sense information (representative of load) and the UVLO voltage (representative of input voltage) are used to adjust the overlap times. The overlap times are essentially constant at mid to high load. In light load conditions, overlap times are inversely proportional to load and input voltage. The adaptive overlap time adjustment becomes active around 30% of the maximum load. The input voltage stops modulating the adaptive overlap timer once V_{UVLO} exceeds approximately 3.5 V.

A resistor, R_{DT}, between the DT and AGND pins adjusts the overlap time. The minimum trailing delay is 20 ns. Equations 14 and 15 show the relationship between overlap delays and R_{DT}, the scaled−down input voltage and the current sense voltage.

$$t_{D2} = \frac{R_{DT} \cdot 1.1 \times 10^{-16}}{\frac{V_{UVLO}}{37.06k} + \text{minimum}\left(\frac{V_{CS}}{2k}, \frac{V_{UVLO}}{35k}\right)} \quad \text{(eq. 14)}$$

$$t_{D1} = \frac{t_{D2}}{0.66} \quad \text{(eq. 15)}$$

For our 200 kHz dc−dc converter, we scaled down the input voltage by a ratio of 0.0365 before reaching the UVLO pin. For a 36 V input, we have 1.31 V on the UVLO pin. The dead−time resistance R_{DT} has been selected to 65 kΩ. If we plot Equation 15 using Mathcad® as V_{CS} varies from 0 to 0.45 V, we obtain Figure 61 graph for three different input voltages (t_{1LL} for 36 V, t_{1NL} for 48 V and t_{1HL} for 76 V):

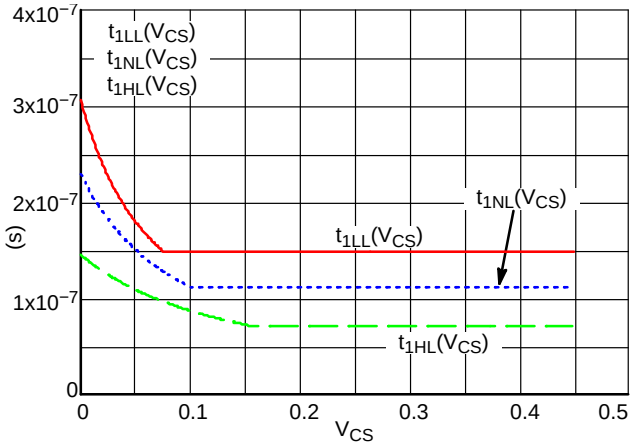


Figure 61. The Dead Time Evolution with Input Voltage and the Sensed Current

The trailing delay, t_{D2}, is 66% of the leading delay, t_{D1}. This allows the user to optimize the delay for the main switch optimum turn−on transition while ensuring the active clamp switch always exhibit ZVS. The active clamp switch only sees the magnetizing current. Therefore, having the body diode conduct for a small time period does not significantly impact the system efficiency.

Reference Voltage

A 5.0 V ±2% reference is provided on the REF pin. It provides a minimum current of 12 mA. This reference can be used for biasing external circuitry. An external bypass capacitor is required for stability. The recommended minimum capacitance is 0.1 μF. The reference is enabled once V_{UVLO} exceeds V_{STBY} and V_{CC} exceeds $V_{CC(min)}$,

typically 6.5 V. It is disabled once V_{CC} falls below $V_{CC(reset)}$, typically 6.4 V. The reference pin incorporates an undervoltage detector. The reference is disabled if it falls below its undervoltage lockout threshold, $V_{REF(UVLO)}$, typically 4.5 V. The reference undervoltage lockout has hysteresis, $V_{REF(HYS)}$, typically 200 mV. The controller is immediately disabled if a V_{REF} undervoltage lockout fault is detected. A 1.5 μs filter delay provides noise immunity.

V_{REF} is biased directly from V_{CC}. Therefore, if a load is applied to V_{CC} while V_{REF} is charging, chances exist to prevent the auxiliary voltage from properly building up, aborting the startup sequence. V_{CC} and V_{REF} capacitors should be sized such that the charging of V_{REF} does not cause V_{CC} to fall below $V_{CC(reset)}$. Otherwise, the reference will be disabled.

If too much current is drawn from the REF pin, V_{CC} will collapse. Once V_{CC} falls $V_{CC(min)}$ OUTA is forced high. Once OUTM goes low, the controller is disabled resulting in a discharge of the soft−start capacitor. V_{REF} and OUTA are disabled once V_{CC} falls below $V_{CC(reset)}$. Once V_{REF} is disabled, the overload condition is removed allowing V_{CC} to charge back up.

Power Dissipation

The controller junction−to−ambient thermal resistance $R_{\theta JA}$ depends on the available copper surface it is soldered upon. Below are characterization data that link R_{J-A} with copper surface and number of layers. 1 oz and 2 oz copper respectively correspond to 35 μm and 70 μm PCB copper thickness.

QFN package
2 layer JEDEC EIA/JESD 51.3

Cu Area mm²	1.0 oz	2.0 oz
100	131	115
125	122	107
150	115	101
200	105	93
300	93	82
400	85	75
500	79	69
600	74	66

QFN package
4 layer JEDEC EIA/JESD 51.7

Cu Area mm²	1.0 oz	2.0 oz
100	48	46
125	48	46
150	48	46
200	48	46
300	48	46
400	47	46
500	47	45
600	47	45

Copper area	$R_{\theta JA}$ 35 μm	$R_{\theta JA}$ 70 μm

Temperature Shutdown

An internal thermal shutdown circuit monitors the junction temperature of the integrated circuit. The controller is disabled if the junction temperature exceeds the thermal shutdown threshold, T_{SHDN}, typically 165°C. The controller restarts once the IC temperature drops below T_{SHDN} by the thermal shutdown hysteresis, $T_{SHDN(HYS)}$, typically 20°C and V_{CC} has charged to $V_{CC(on)}$ at least once while in thermal shutdown mode.

A thermal shutdown fault is cleared if V_{CC} drops below $V_{CC(reset)}$, or if V_{UVLO} falls below V_{STBY} by its hysteresis level. A power−up sequence commences at the next $V_{CC(on)}$ if all faults are removed.

ORDERING INFORMATION

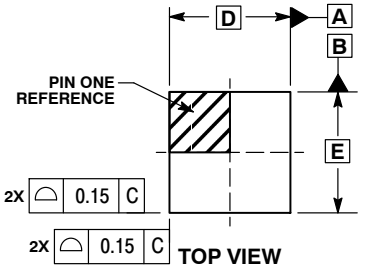
Device	Package	Shipping†
NCP1565MNTXG	QFN24 (Pb−Free)	4000 / Tape & Reel

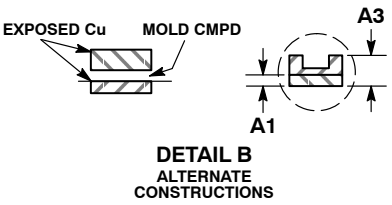
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

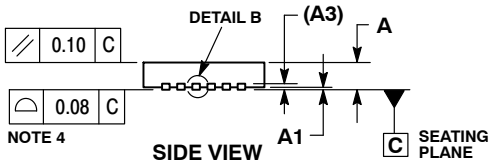
SCALE 2:1

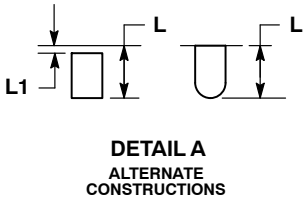
QFN24, 4x4, 0.5P
CASE 485CW
ISSUE O

DATE 15 NOV 2012



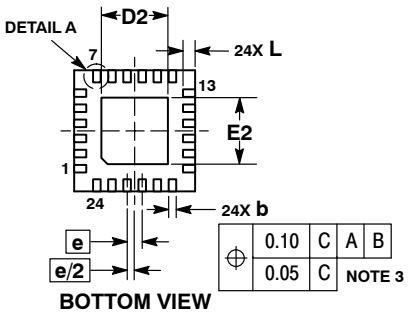




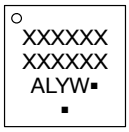


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.21	0.31
D	4.00 BSC	
D2	2.10	2.30
E	4.00 BSC	
E2	2.10	2.30
e	0.50 BSC	
L	0.30	0.50
L1	---	0.15



GENERIC MARKING DIAGRAM*

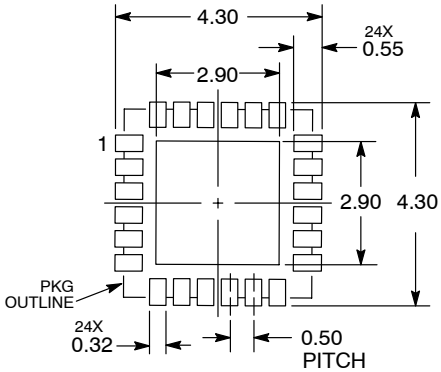


XXXXXX= Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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