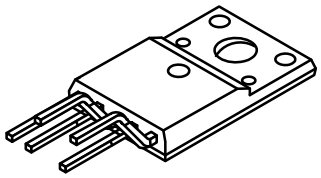
Green Mode Fairchild Power Switch (FPS™)

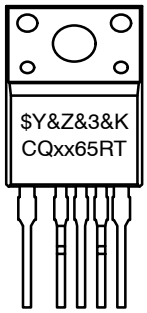
FSCQ Series

FSCQ0765RT / FSCQ0965RT / FSCQ1265RT / FSCQ1565RT



TO−220−5
CASE 340BH

MARKING DIAGRAM



$Y	= **onsemi** Logo
&Z	= Assembly Plant Code
&3	= Date Code (Year & Week)
&K	= Lot Code
CQXX65RT	= Specific Device Code
XX	= 07, 09, 12, 15

ORDERING INFORMATION

See detailed ordering and shipping information on page 31 of this data sheet.

Description

A Quasi−Resonant Converter (QRC) typically shows lower EMI and higher power conversion efficiency compared to a conventional hard−switched converter with a fixed switching frequency. Therefore, a QRC is well suited for noise−sensitive applications, such as color TV and audio. Each product in the FSCQ series contains an integrated Pulse Width Modulation (PWM) controller and a SENSEFET®. This series is specifically designed for quasi−resonant off−line Switch Mode Power Supplies (SMPS) with minimal external components. The PWM controller includes an integrated fixed frequency oscillator, under−voltage lockout, leading−edge blanking (LEB), optimized gate driver, internal soft−start, temperature−compensated precise current sources for loop compensation, and self−protection circuitry. Compared with a discrete MOSFET and PWM controller solution, the FSCQ series can reduce total cost, component count, size, and weight; while increasing efficiency, productivity, and system reliability. These devices provide a basic platform for cost−effective designs of quasi−resonant switching flyback converters.

Features

- Optimized for Quasi−Resonant Converter (QRC)
- Advanced Burst−Mode Operation for under 1 W Standby Power Consumption
- Pulse−by−Pulse Current Limit
- Overload Protection (OLP) – Auto Restart
- Over−Voltage Protection (OVP) – Auto Restart
- Abnormal Over−Current Protection (AOCP) – Latch
- Internal Thermal Shutdown (TSD) – Latch
- Under−Voltage Lockout (UVLO) with Hysteresis
- Low Startup Current (Typical: 25 μA)
- Internal High Voltage SENSEFET
- Built−in Soft−Start (20 ms)
- Extended Quasi−Resonant Switching
- This is a Pb−Free and Halid−Free Device

Applications

- CTV
- Audio Amplifier

Related Resources

- https://www.onsemi.com/pub/Collateral/AN−4146.pdf
- https://www.onsemi.com/pub/Collateral/AN−4140.pdf

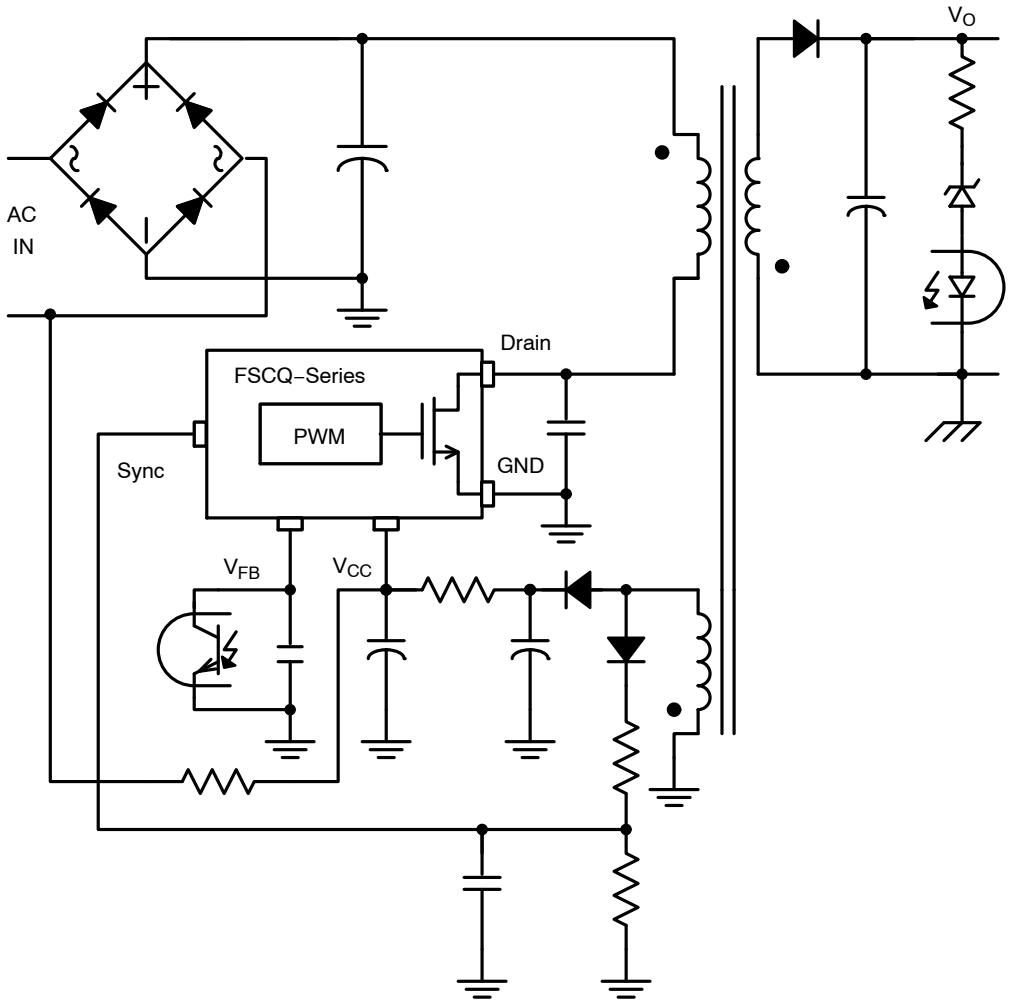


Figure 1. Typical Flyback Application

Table 1. MAXIMUM OUTPUT POWER (Note 1)

	230 V_{AC} ±15% (Note 2)	**85−265 V_{AC}**
Product	**Open Frame** (Note 3)	**Open Frame** (Note 3)
FSCQ0765RT	100 W	85 W
FSCQ0965RT	130 W	110 W
FSCQ1265RT	170 W	140 W
FSCQ1565RT	210 W	170 W

1. The junction temperature can limit the maximum output power.
2. 230 V_{AC} or 100/115 V_{AC} with doubler.
3. Maximum practical continuous power in an open frame design at 50°C ambient.

Internal Block Diagram

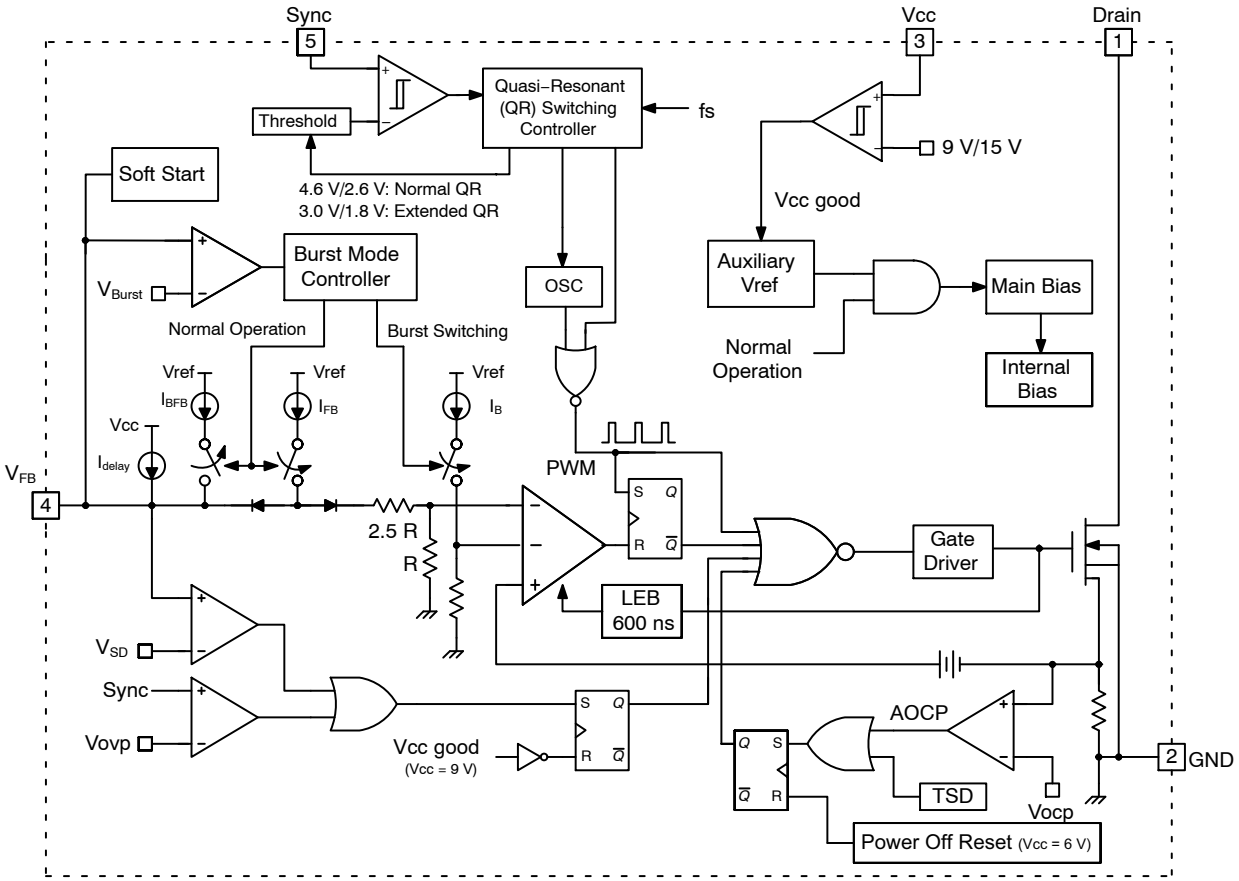


Figure 2. Functional Block Diagram

Pin Configuration

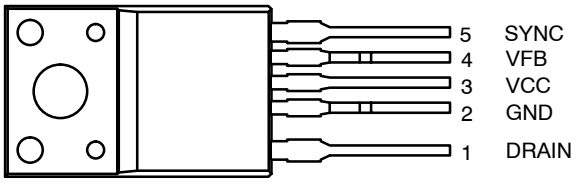


Figure 3. Pin Assignments (Top View)

PIN DESCRIPTION

Pin No.	Symbol	Description
1	DRAIN	This pin is the high−voltage power SENSEFET drain connection.
2	GND	This pin is the control ground and the SENSEFET source.
3	VCC	This pin is the positive supply input. This pin provides internal operating current for both startup and steady−state operation.
4	VFB	This pin is internally connected to the inverting input of the PWM comparator. The collector of an opto−coupler is typically tied to this pin. For stable operation, a capacitor should be placed between this pin and GND. If the voltage of this pin reaches 7.5 V, the overload protection triggers, which results in the FPS] shutting down.
5	SYNC	This pin is internally connected to the sync detect comparator for quasi−resonant switching. In normal quasi−resonant operation, the threshold of the sync comparator is 4.6 V / 2.6 V. Whereas, the sync threshold is changed to 3.0 V / 1.8 V in an extended quasi−resonant operation.

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise specified)

Parameter		Symbol	Value	Unit
Drain Pin Voltage		V_{DS}	650	V
Supply Voltage		V_{CC}	20	V
Analog Input Voltage Range		V_{sync}	−0.3 to 13	V
		V_{FB}	−0.3 to V_{CC}	
Drain Current Pulsed (Note 4)	FSCQ0765RT	I_{DM}	15.2	A
	FSCQ0965RT		16.4	
	FSCQ1265RT		21.2	
	FSCQ1565RT		26.4	
Continuous Drain Current (T_C = 25°C) (T_C: Case Back Surface Temperature)	FSCQ0765RT	I_D	3.8	$A_{(rms)}$
	FSCQ0965RT		4.1	
	FSCQ1265RT		5.3	
	FSCQ1565RT		6.6	
Continuous Drain Current* (T_{DL} = 25°C) (T_{DL}: Case Back Surface Temperature)	FSCQ0765RT	I_D*	7.0	$A_{(rms)}$
	FSCQ0965RT		7.6	
	FSCQ1265RT		11.0	
	FSCQ1565RT		13.3	
Continuous Drain Current (T_C = 100°C)	FSCQ0765RT	I_D	2.4	$A_{(rms)}$
	FSCQ0965RT		2.6	
	FSCQ1265RT		3.4	
	FSCQ1565RT		4.4	

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise specified) (continued)

Parameter		Symbol	Value	Unit
Single−Pulsed Avalanche Energy (Note 5)	FSCQ0765RT	E_{AS}	570	mJ
	FSCQ0965RT		630	
	FSCQ1265RT		950	
	FSCQ1565RT		1050	
Total Power Dissipation (T_C = 25°C with Infinite Heat Sink)	FSCQ0765RT	P_D	45	W
	FSCQ0965RT		49	
	FSCQ1265RT		50	
	FSCQ1565RT		75	
Operating Junction Temperature		T_J	150	°C
Operating Ambient Temperature		T_A	−25 to +85	°C
Storage Temperature Range		T_{STG}	−55 to +150	°C
Human Body Model (All Pins Except V_{FB})	(GND − V_{FB} = 1.7 kV)	ESD	2.0	kV
Machine Model (All Pins Except V_{FB})	(GND − V_{FB} = 170 V)		300	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

4. Repetitive rating: pulse width limited by maximum junction temperature.
5. L = 15 mH, starting T_J = 25°C. These parameters, although guaranteed by design, are not tested in production.

THERMAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Characteristic	Characteristic	Symbol	Value	Unit
Junction−to Case Thermal Impedance	FSCQ0765RT	J_C	2.60	°C/W
	FSCQ0965RT		2.55	
	FSCQ1265RT		2.50	
	FSCQ1565RT		2.00	

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Symbol	Parameter		Test Condition	Min	Typ	Max	Unit
SENSEFET PART							
BV_{DSS}	Drain−Source Breakdown Voltage		V_{GS} = 0 V, I_D = 250 μA	650	–	–	V
I_{DSS}	Zero Gate Voltage Drain Current		V_{DS} = 650 V, V_{GS} = 0 V	–	–	250	μA
$R_{DS(ON)}$	Drain−Source On−State Resistance	FSCQ0765RT	V_{GS} = 10 V, I_D = 1 A	–	1.40	1.60	Ω
		FSCQ0965RT	V_{GS} = 10 V, I_D = 1 A	–	1.00	1.20	
		FSCQ1265RT	V_{GS} = 10 V, I_D = 1 A	–	0.75	0.90	
		FSCQ1565RT	V_{GS} = 10 V, I_D = 1 A	–	0.53	0.70	
C_{ISS}	Input Capacitance	FSCQ0765RT	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	–	1415	–	pF
		FSCQ0965RT		–	1750	–	
		FSCQ1265RT		–	2400	–	
		FSCQ1565RT		–	3050	–	
C_{OSS}	Output Capacitance	FSCQ0765RT	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	–	100	–	pF
		FSCQ0965RT		–	130	–	
		FSCQ1265RT		–	175	–	
		FSCQ1565RT		–	220	–	
CONTROL SECTION							
f_{OSC}	Switching Frequency		V_{FB} = 5 V, V_{CC} = 18 V	18	20	22	kHz
Δf_{OSC}	Switching Frequency Variation (Note 7)		−25°C ≤ T_A ≤ 85°C	0	±5	±10	%
I_{FB}	Feedback Source Current		V_{FB} = 0.8 V, V_{CC} = 18 V	0.50	0.65	0.80	mA
D_{MAX}	Maximum Duty Cycle		V_{FB} = 5 V, V_{CC} = 18 V	92	95	98	%
D_{MIN}	Minimum Duty Cycle		V_{FB} = 0 V, V_{CC} = 18 V	–	0	–	%
V_{START}	UVLO Threshold Voltage		V_{FB} = 1 V	14	15	16	V
V_{STOP}				8	9	10	
t_{SS}	Soft−Start Time (Note 6)			18	20	22	ms
BURST MODE SECTION							
V_{BEN}	Burst Mode Enable Feedback Voltage			0.25	0.40	0.55	V
I_{BFB}	Burst Mode Feedback Source Current		V_{FB} = 0 V	60	100	140	μA
t_{BS}	Burst Mode Switching Time		V_{FB} = 0.9 V, Duty = 50%	1.2	1.4	1.6	ms
t_{BH}	Burst Mode Hold Time		V_{FB} = 0.9 V → 0 V	1.2	1.4	1.6	ms
PROTECTION SECTION							
V_{SD}	Shutdown Feedback Voltage		V_{CC} = 18 V	7.0	7.5	8.0	V
I_{DELAY}	Shutdown Delay Current		V_{FB} = 5 V, V_{CC} = 18 V	4	5	6	μA
V_{OVP}	Over−Voltage Protection		V_{FB} = 3 V	11	12	13	V
V_{OCL}	Over−Current Latch Voltage (Note 6)		V_{CC} = 18 V	0.9	1.0	1.1	V
TSD	Thermal Shutdown Temperature (Note 7)			140	–	–	°C
SYNC SECTION							
V_{SH1}	Sync Threshold in Normal QR (H)		V_{CC} = 18 V, V_{FB} = 5 V	4.2	4.6	5.0	V
V_{SL1}	Sync Threshold in Normal QR (L)			2.3	2.6	2.9	V
V_{SH2}	Sync Threshold in Extended QR (H)			2.7	3.0	3.3	V
V_{SL2}	Sync Threshold in Extended QR (L)			1.6	1.8	2.0	V
f_{SYH}	Extended QR Enable Frequency			–	90	–	kHz
f_{SYL}	Extended QR Disable Frequency			–	45	–	kHz

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) (continued)

Symbol	Parameter		Test Condition	Min	Typ	Max	Unit
TOTAL DEVICE SECTION							
I_{OP}	Operating Supply Current in Normal Operation (Note 8)	FSCQ0765RT	V_{FB} = 5 V	–	4	6	mA
		FSCQ0965RT		–	6	8	
		FSCQ1265RT		–	6	8	
		FSCQ1565RT		–	7	9	
I_{OB}	Operating Supply Current in Burst Mode (Non−Switching) (Note 8)		V_{FB} = GND	–	0.25	0.50	mA
I_{START}	Startup Current		V_{CC} = V_{START} − 0.1 V	–	25	50	μA
I_{SN}	Sustain Latch Current (Note 6)		V_{CC} = V_{STOP} − 0.1 V	–	50	100	μA
CURRENT SENSE SECTION							
I_{LIM}	Maximum Current Limit (Note 9)	FSCQ0765RT	V_{CC} = 18 V, V_{FB} = 5 V	4.40	5.00	5.60	A
		FSCQ0965RT		5.28	6.00	6.72	
		FSCQ1265RT		6.16	7.00	7.84	
		FSCQ1565RT		7.04	8.00	8.96	
$I_{BUR(pk)}$	Burst Peak Current	FSCQ0765RT	V_{CC} = 18 V, V_{FB} = Pulse	0.65	0.90	1.15	A
		FSCQ0965RT		0.60	0.90	1.20	
		FSCQ1265RT		0.80	1.20	1.60	
		FSCQ1565RT		–	1.00	–	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. These parameters, although guaranteed, are tested only in wafer test process.
7. These parameters, although guaranteed by design, are not tested in production.
8. This parameter is the current flowing in the control IC.
9. These parameters indicate inductor current.
10. These parameters, although guaranteed, are tested only in wafer test process.

TYPICAL PERFORMANCE CHARACTERISTICS

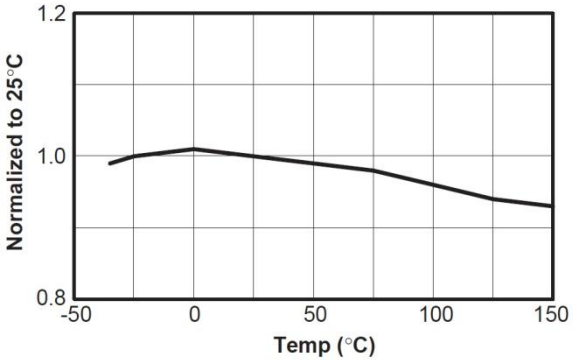


Figure 4. Operating Supply Current

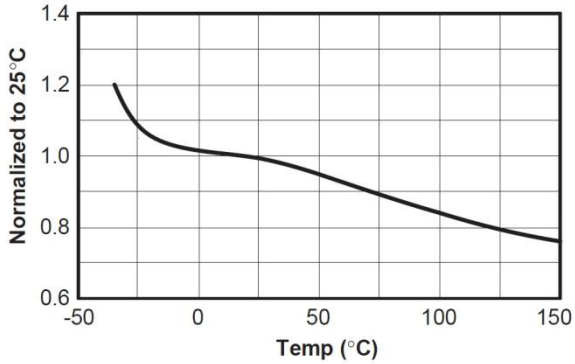


Figure 5. Burst Mode Supply Current (Non−Switching)

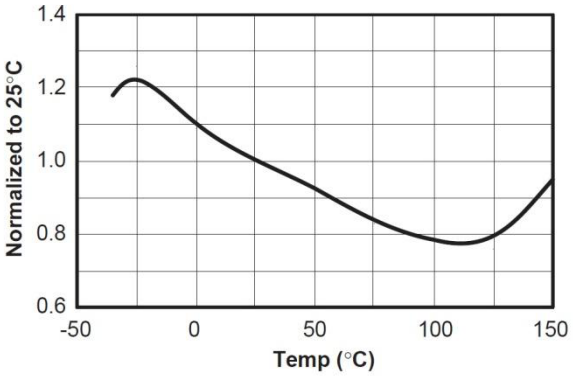


Figure 6. Startup Current

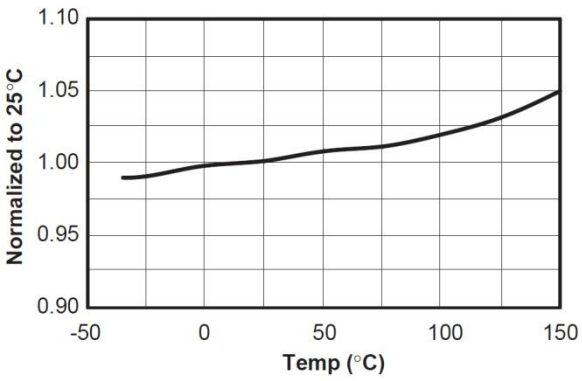


Figure 7. Start Threshold Voltage

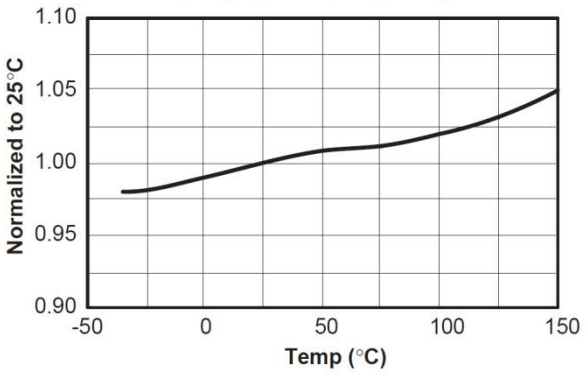


Figure 8. Stop Threshold Voltage

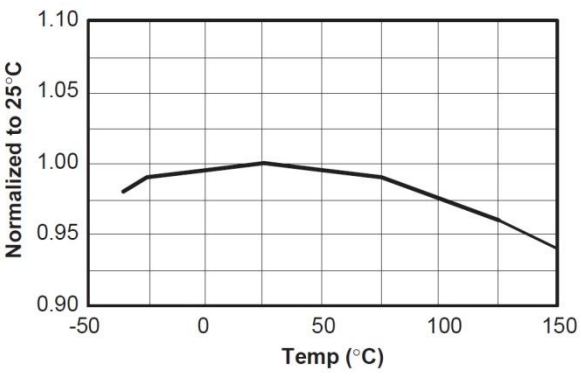


Figure 9. Initial Frequency

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

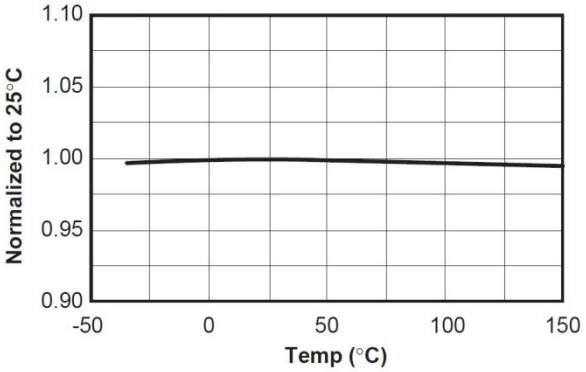


Figure 10. Maximum Duty Cycle

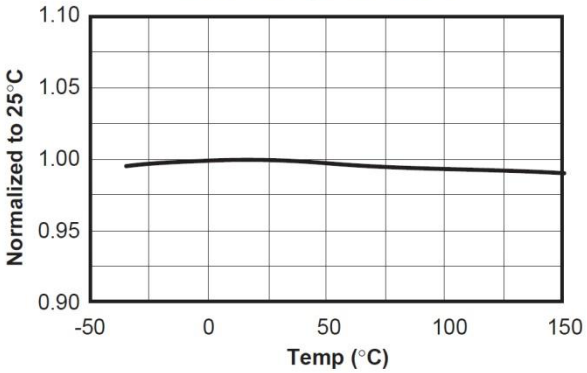


Figure 11. Over−Voltage Protection

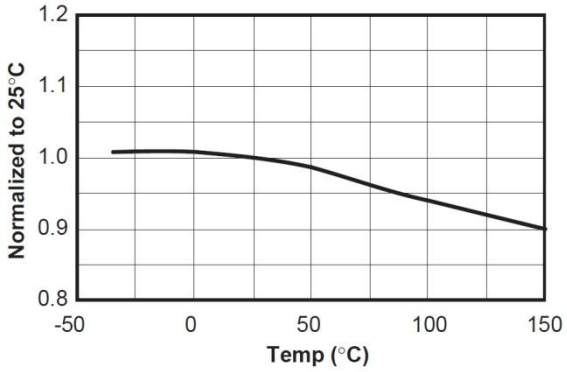


Figure 12. Shutdown Delay Current

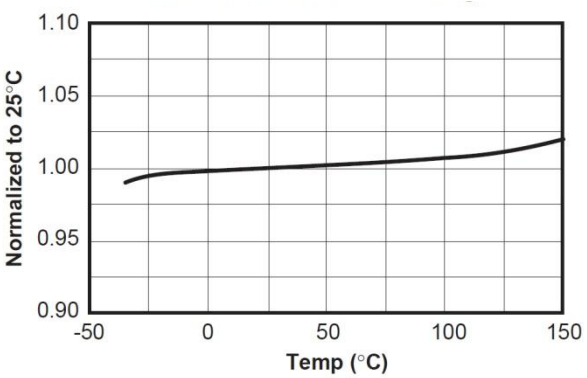


Figure 13. Shutdown Feedback Voltage

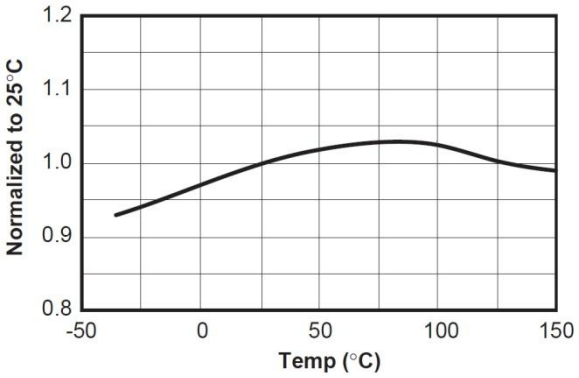


Figure 14. Feedback Source Current

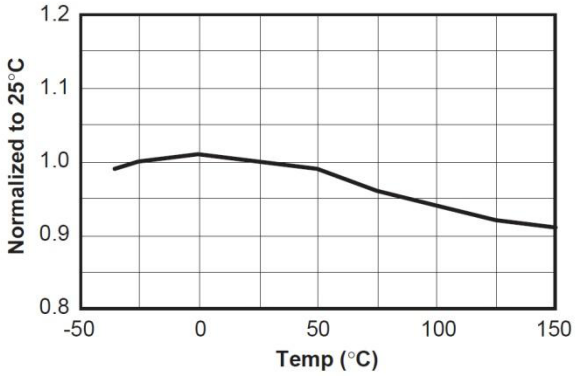


Figure 15. Burst Mode Feedback Source Current

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

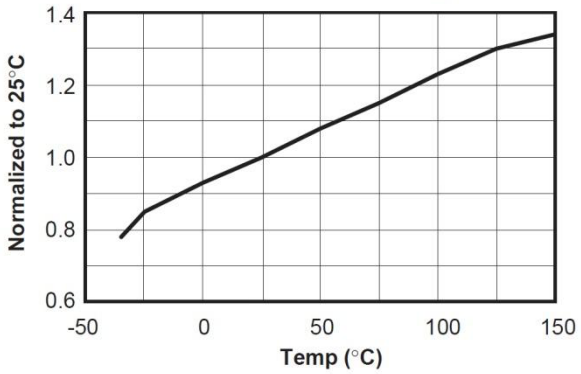


Figure 16. Feedback Offset Voltage

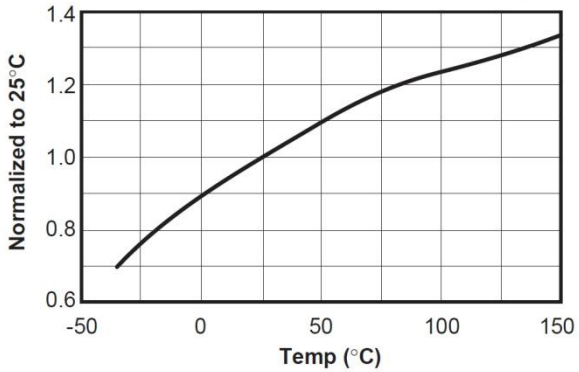


Figure 17. Burst Mode Enable Feedback Voltage

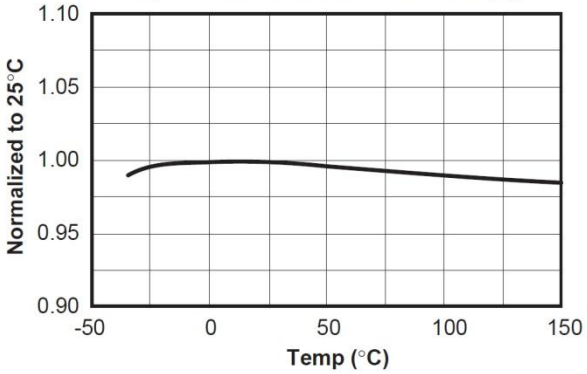


Figure 18. Sync. Threshold in Normal QR(H)

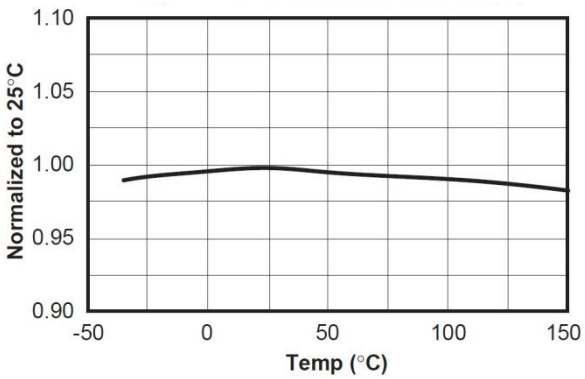


Figure 19. Sync. Threshold in Normal QR(L)

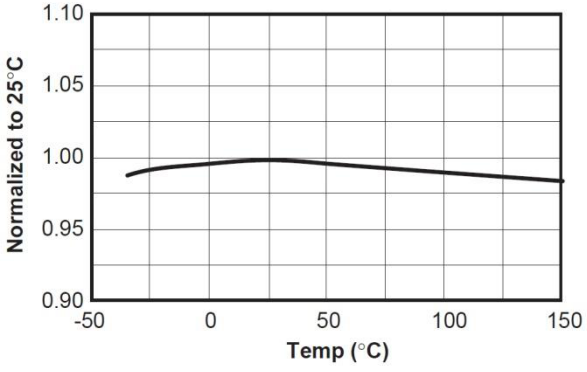


Figure 20. Sync. Threshold in Extended QR(H)

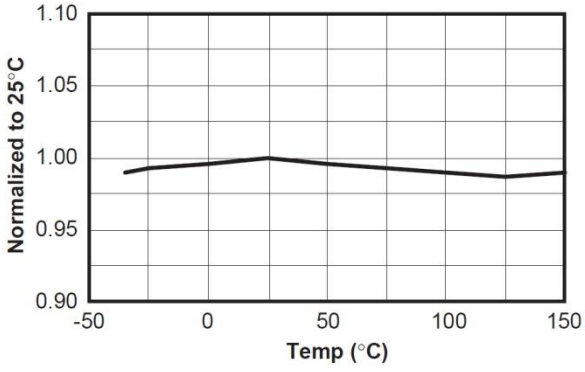


Figure 21. Sync. Threshold in Extended QR(L)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

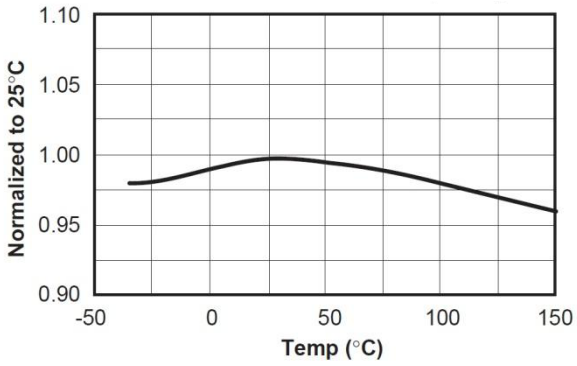


Figure 22. Extended QR Enable Frequency

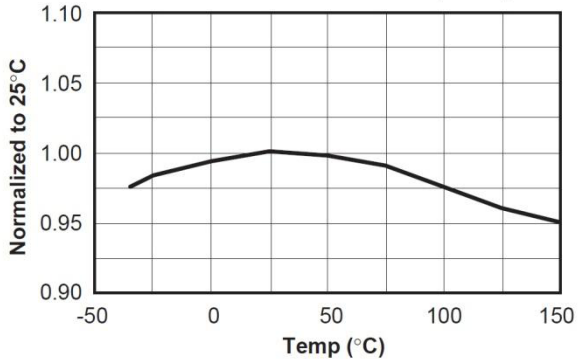


Figure 23. Extended QR Disable Frequency

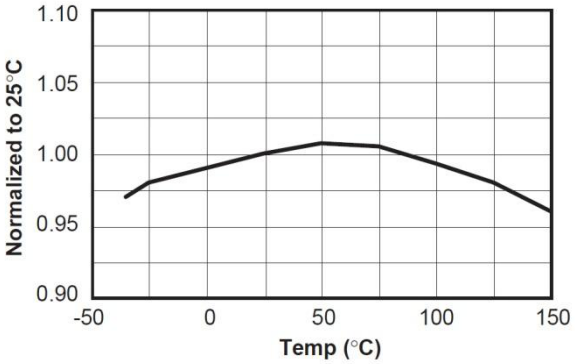


Figure 24. Pulse−by−Pulse Current Limit

Functional Description

Startup

Figure 25 shows the typical startup circuit and the transformer auxiliary winding for the FSCQ series. Before the FSCQ series begins switching, it consumes only startup current (typically 25 μA). The current supplied from the AC line charges the external capacitor (C_{a1}) that is connected to the V_{CC} pin. When V_{CC} reaches the start voltage of 15 V (V_{START}), the FSCQ series begins switching and its current consumption increases to IOP. Then, the FSCQ series continues normal switching operation and the power required is supplied from the transformer auxiliary winding, unless V_{CC} drops below the stop voltage of 9 V (V_{STOP}). To guarantee stable operation of the control IC, V_{CC} has under−voltage lockout (UVLO) with 6 V hysteresis. Figure 26 shows the relationship between the operating supply current of the FSCQ series and the supply voltage (V_{CC}).

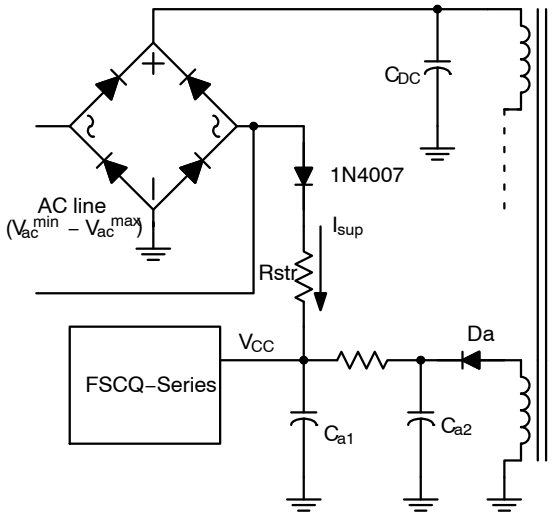


Figure 25. Startup Circuit

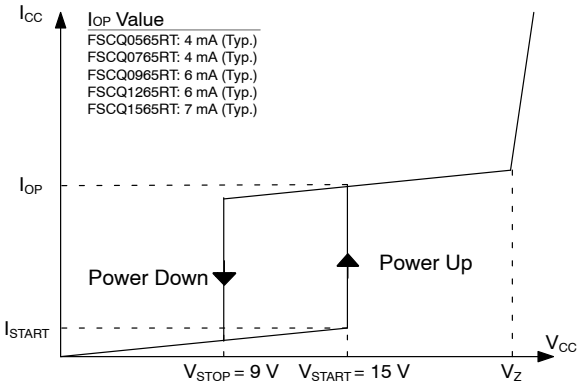


Figure 26. Relationship between Operating Supply Current and V_{CC} Voltage

The minimum average of the current supplied from the AC is given by:

$$I_{SUP}{}^{AVG} = \left(\frac{\sqrt{2 \cdot V_{AC}{}^{MIN}}}{\pi} - \frac{V_{START}}{2} \right) \cdot \frac{1}{R_{STR}} \quad \text{(eq. 1)}$$

where $V_{ac}{}^{min}$ is the minimum input voltage, V_{START} is the FSCQ series' start voltage (15 V), and R_{str} is the startup resistor. The startup resistor should be chosen so that $I_{sup}{}^{avg}$ is larger than the maximum startup current (50 mA).

Once the resistor value is determined, the maximum loss in the startup resistor is obtained as:

$$\text{Loss} = \frac{1}{R_{STR}} \cdot \left[\frac{\left(V_{AC}{}^{MAX}\right)^2 + V_{START}{}^2}{2} - \frac{2\sqrt{2} \cdot V_{START} \cdot V_{AC}{}^{MAX}}{\pi} \right] \quad \text{(eq. 2)}$$

where $V_{ac}{}^{max}$ is the maximum input voltage.

The startup resistor should have properly rated dissipation wattage.

Synchronization

The FSCQ series employs a quasi−resonant switching technique to minimize the switching noise and loss. In this technique, a capacitor (Cr) is added between the MOSFET drain and the source, as shown in Figure 27. The basic waveforms of the quasi−resonant converter are shown in Figure 28. The external capacitor lowers the rising slope of the drain voltage to reduce the EMI caused when the MOSFET turns off. To minimize the MOSFET's switching loss, the MOSFET should be turned on when the drain voltage reaches its minimum value, as shown in Figure 28.

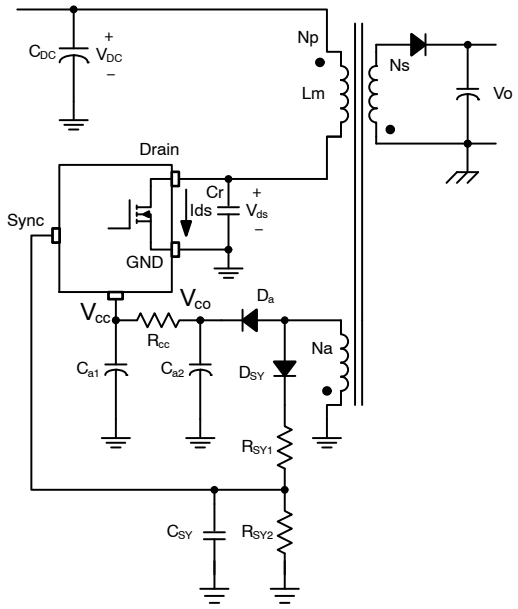


Figure 27. Synchronization Circuit

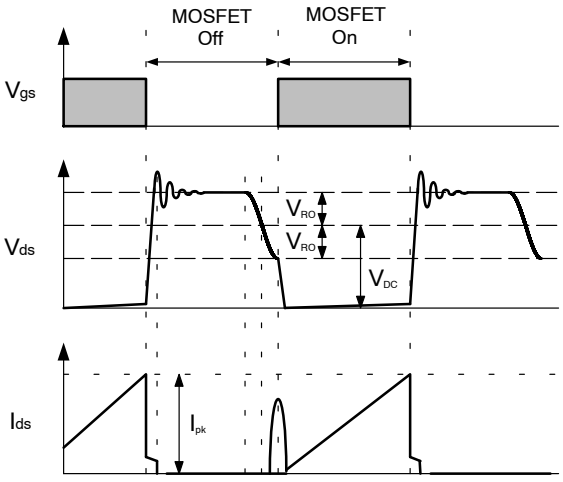


Figure 28. Quasi−Resonant Operation Waveforms

The minimum drain voltage is indirectly detected by monitoring the V_{CC} winding voltage, as shown in Figure 27 and Figure 29. Choose voltage dividers, R_{SY1} and R_{SY2}, so that the peak voltage of the sync signal (V_{sypk}) is lower than the OVP voltage (12 V) to avoid triggering OVP in normal operation. It is typical to set V_{sypk} to be lower than OVP voltage by 3–4 V. To detect the optimum time to turn on MOSFET, the sync capacitor (CSY) should be determined so that t_R is the same with t_Q, as shown in Figure 29. The t_R and t_Q are given as:

$$t_R = R_{SY2} \cdot C_{SY} \cdot \ln\left(\frac{V_{CO}}{2.6} \cdot \frac{R_{SY2}}{R_{SY1} + R_{SY2}}\right) \quad \text{(eq. 3)}$$

$$t_Q = \pi \cdot \sqrt{L_m \cdot C_{eo}} \quad \text{(eq. 4)}$$

$$V_{CO} = \frac{N_a \cdot (V_O + V_{FO})}{N_s} - V_{Fa} \quad \text{(eq. 5)}$$

where:

- L_m is the primary side inductance of the transformer,
- N_s is the number of turns for the output winding,
- N_a is the number of turns for the V_{CC} winding,
- V_{Fo} is the diode forward−voltage drop of the output winding,
- V_{Fa} is the diode forward−voltage drop of the V_{CC} winding; and
- C_{eo} is the sum of the output capacitance of the MOSFET and the external capacitor, C_r.

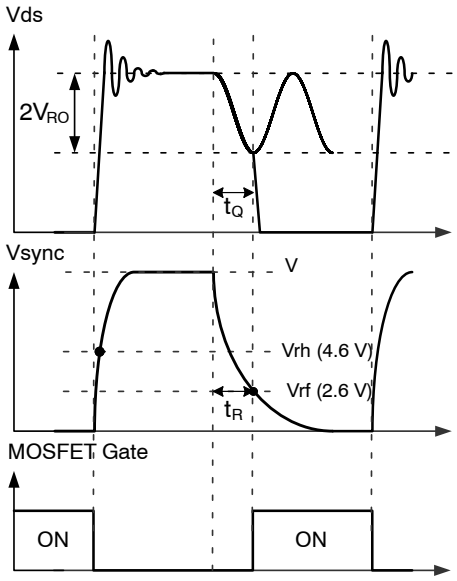


Figure 29. Normal QR Operation Waveforms

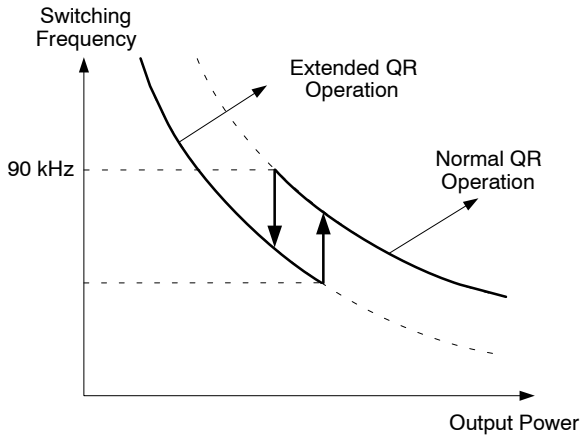


Figure 30. Extended Quasi−Resonant Operation

In general, the QRC has a limitation in a wide load range application, since the switching frequency increases as the output load decreases, resulting in a severe switching loss in the light load condition. To overcome this limitation, the FSCQ series employs an extended quasi−resonant switching operation. Figure 30 shows the mode change between normal and extended quasi−resonant operations. In the normal quasi−resonant operation, the FSCQ series enters into the extended quasi−resonant operation when the switching frequency exceeds 90 kHz as the load reduces. To reduce the switching frequency, the MOSFET is turned on when the drain voltage reaches the second minimum level,

as shown in Figure 31. Once the FSCQ series enters into the extended quasi−resonant operation, the first sync signal is ignored. After the first sync signal is applied, the sync threshold levels are changed from 4.6 V and 2.6 V to 3 V and 1.8 V, respectively, and the MOSFET turn−on time is synchronized to the second sync signal. The FSCQ series returns to its normal quasi−resonant operation when the switching frequency reaches 45 kHz as the load increases.

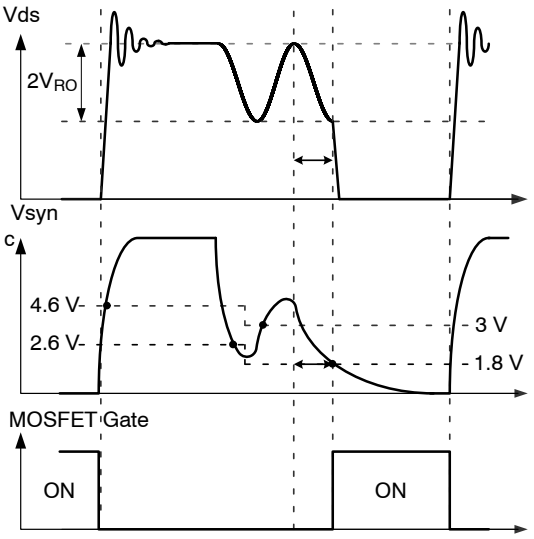


Figure 31. Extended QR Operation Waveforms

Feedback Control

The FSCQ series employs current mode control, as shown in Figure 32. An optocoupler (such as **onsemi's** H11A817A) and shunt regulator (such as **onsemi's** KA431) are typically used to implement the feedback network. Comparing the feedback voltage with the voltage across the R_{sense} resistor, plus an offset voltage, makes it possible to control the switching duty cycle. When the reference pin voltage of the shunt regulator exceeds the internal reference voltage of 2.5 V, the opto−coupler LED current increases, pulling down the feedback voltage and reducing the duty cycle. This typically occurs when input voltage is increased or output load is decreased.

Pulse−by−Pulse Current Limit

Because current mode control is employed, the peak current through the SENSEFET is limited by the inverting input of the PWM comparator (V_{fb}*) as shown in Figure 32. The feedback current (I_{FB}) and internal resistors are designed so that the maximum cathode voltage of diode D_2 is about 2.8 V, which occurs when all IFB flows through the internal resistors. Since D_1 is blocked when the feedback voltage (V_{fb}) exceeds 2.8 V, the maximum voltage of the cathode of D_2 is clamped at this voltage, thus clamping V_{fb}*. Therefore, the peak value of the current through the SENSEFET is limited.

Leading Edge Blanking (LEB)

At the instant the internal SENSEFET is turned on, there is usually a high current spike through the SENSEFET, caused by the external resonant capacitor across the MOSFET and secondary−side rectifier reverse recovery. Excessive voltage across the R_{sense} resistor can lead to incorrect feedback operation in the current mode PWM control. To counter this effect, the FSCQ series employs a leading edge blanking (LEB) circuit. This circuit inhibits the PWM comparator for a short time (t_{LEB}) after the Sense FET is turned on.

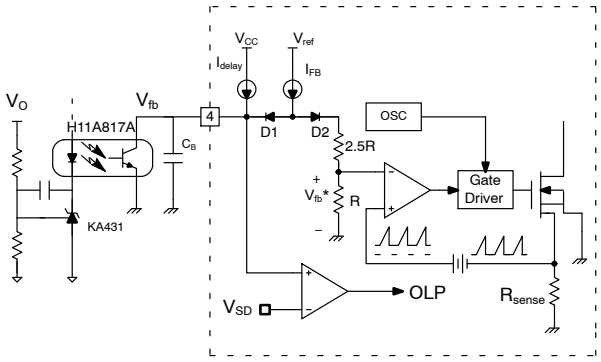


Figure 32. Pulse Width Modulation (PWM) Circuit

Protection Circuits

The FSCQ series has several self−protective functions such as overload protection (OLP), abnormal over−current protection (AOCP), overvoltage protection (OVP), and thermal shutdown (TSD). OLP and OVP are auto−restart mode protections, while TSD and AOCP are latch mode protections. Because these protection circuits are fully integrated into the IC without external components, the reliability can be improved without increasing cost.

- *Auto− Restart Mode Protection:* Once the fault condition is detected, switching is terminated and the SENSEFET remains off. This causes V_{CC} to fall. When V_{CC} falls to the under voltage lockout (UVLO) stop voltage of 9 V, the protection is reset and the FSCQ series consumes only startup current (25 mA). Then, the V_{CC} capacitor is charged up, since the current supplied through the startup resistor is larger than the current that the FPS consumes. When V_{CC} reaches the start voltage of 15 V, the FSCQ series resumes its normal operation. If the fault condition is not removed, the SENSEFET remains off and V_{CC} drops to stop voltage again. In this manner, the auto−restart can alternately enable and disable the switching of the power SENSEFET until the fault condition is eliminated (see Figure 33).
- *Latch Mode Protection:* Once this protection is triggered, switching is terminated and the SENSEFET remains off until the AC power line is unplugged. Then, V_{CC} continues charging and discharging between 9 V and 15 V. The latch is reset only when V_{CC} is discharged to 6 V by unplugging the AC power line.

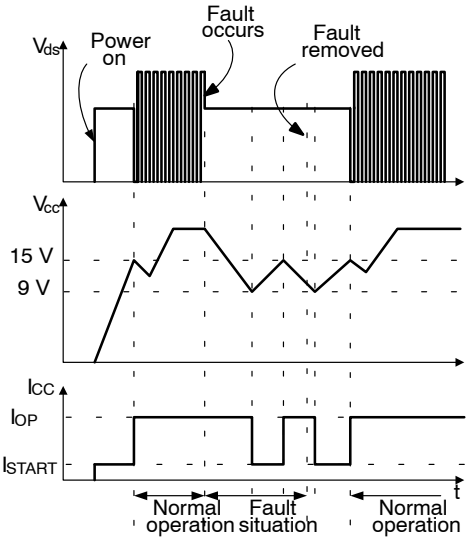


Figure 33. Auto Restart Mode Protection

Overload Protection (OLP)

Overload is defined as the load current exceeding its normal level due to an unexpected abnormal event. In this situation, the protection circuit should trigger to protect the SMPS. However, even when the SMPS is in the normal operation, the over load protection circuit can be triggered during the load transition. To avoid this undesired operation, the overload protection circuit is designed to trigger after a specified time to determine whether it is a transient situation or an overload situation. Because of the pulse−by−pulse current limit capability, the maximum peak current through the SENSEFET is limited, and therefore the maximum input power is restricted with a given input voltage. If the output consumes more than this maximum power, the output voltage (Vo) decreases below the set voltage. This reduces the current through the opto−coupler LED, which also reduces the opto−coupler transistor current, thus increasing the feedback voltage (V_{fb}). If V_{fb} exceeds 2.8 V, D_1 is blocked, and the 5 μA current source starts to charge C_B slowly up to V_{CC}. In this condition, Vfb continues increasing until it reaches 7.5 V, then the switching operation is terminated as shown in Figure 34. The delay for shutdown is the time required to charge CB from 2.8 V to 7.5 V with 5 μA. In general, a 20~50 ms delay is typical for most applications. OLP is implemented in auto restart mode.

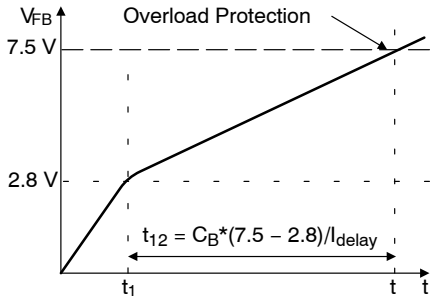


Figure 34. Overload Protection

Abnormal Over Current Protection (AOCP)

When the secondary rectifier diodes or the transformer pins are shorted, a steep current with extremely high di/dt can flow through the SENSEFET during the LEB time. Even though the FSCQ series has OLP (Overload Protection), it is not enough to protect the FSCQ series in that abnormal case, since severe current stress will be imposed on the SENSEFET until the OLP triggers. The FSCQ series has an internal AOCP (Abnormal Over−Current Protection) circuit as shown in Figure 35. When the gate turn−on signal is applied to the power SENSEFET, the AOCP block is enabled and monitors the current through the sensing resistor. The voltage across the resistor is then compared with a preset AOCP level. If the sensing resistor voltage is greater than the AOCP level, the set signal is applied to the latch, resulting in the shutdown of SMPS. This protection is implemented in the latch mode.

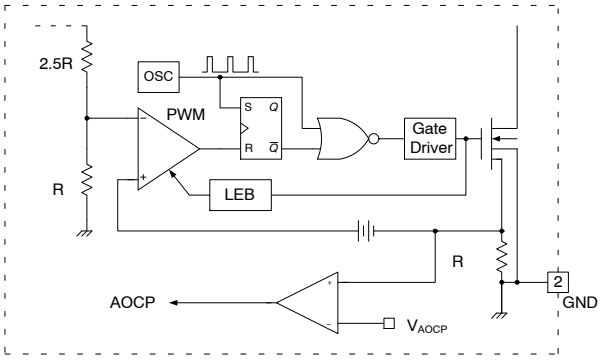


Figure 35. AOCP Block

Over−Voltage Protection (OVP)

If the secondary side feedback circuit malfunctions or a solder defect causes an open in the feedback path, the current through the opto−coupler transistor becomes almost zero. Then, V_{fb} climbs up in a similar manner to the over load situation, forcing the preset maximum current to be supplied to the SMPS until the over load protection triggers. Because more energy than required is provided to the output, the output voltage may exceed the rated voltage before the overload protection triggers, resulting in the breakdown of the devices in the secondary side. In order to prevent this situation, an over voltage protection (OVP) circuit is employed. In general, the peak voltage of the sync signal is proportional to the output voltage and the FSCQ series uses a sync signal instead of directly monitoring the output voltage. If the sync signal exceeds 12 V, an OVP is triggered resulting in a shutdown of SMPS. In order to avoid undesired triggering of OVP during normal operation, the peak voltage of the sync signal should be designed to be below 12 V. This protection is implemented in the auto restart mode.

Thermal Shutdown (TSD)

The SENSEFET and the control IC are built in one package. This makes it easy for the control IC to detect abnormal over temperature of the SENSEFET. When the temperature exceeds approximately 150°C, the thermal shutdown triggers. This protection is implemented in the latch mode.

Soft Start

The FSCQ series has an internal soft−start circuit that increases PWM comparator's inverting input voltage together with the SENSEFET current slowly after it starts up. The typical soft start time is 20 ms. The pulse width to the power switching device is progressively increased to establish the correct working conditions for transformers, inductors, and capacitors. Increasing the pulse width to the power switching device also helps prevent transformer saturation and reduces the stress on the secondary diode during startup. For a fast build up of the output voltage, an offset is introduced in the soft−start reference current.

Burst Operation

To minimize the power consumption in the standby mode, the FSCQ series employs burst operation. Once FSCQ series enters burst mode, FSCQ series allows all output voltages and effective switching frequency to be reduced. Figure 36 shows the typical feedback circuit for C−TV applications. In normal operation, the picture on signal is applied and the transistor Q_1 is turned on, which decouples R_3, D_Z and D_1 from the feedback network. Therefore, only V_{O1} is regulated by the feedback circuit in normal operation and determined by R_1 and R_2 as:

$$V_{O1}^{NORM} = 2.5 \cdot \left(\frac{R_1 + R_2}{R_2}\right) \qquad \text{(eq. 6)}$$

In standby mode, the picture ON signal is disabled and the transistor Q_1 is turned off, which couples R_3, D_Z, and D_1 to the reference pin of KA431. Then, V_{O2} is determined by the Zener diode breakdown voltage. Assuming that the forward voltage drop of D_1 is 0.7 V, V_{O2} in standby mode is approximately given by:

$$V_{O2}^{STBY} = V_Z + 0.7 + 2.5 \qquad \text{(eq. 7)}$$

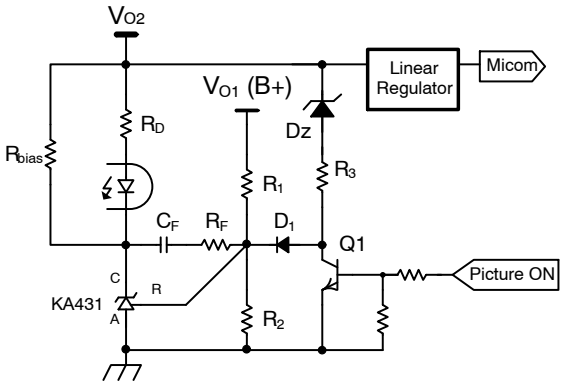


Figure 36. Typical Feedback Circuit to Drop Output Voltage in Standby Mode

Figure 38 shows the burst mode operation waveforms. When the picture ON signal is disabled, Q_1 is turned off and R_3 and Dz are connected to the reference pin of KA431 through D_1. Before Vo2 drops to V_{o2}^{stby}, the voltage on the reference pin of KA431 is higher than 2.5 V, which increases the current through the opto LED. This pulls down the feedback voltage (V_{FB}) of FSCQ series and forces FSCQ series to stop switching. If the switching is disabled longer than 1.4 ms, FSCQ series enters into burst operation and the operating current is reduced from I_{OP} to 0.25 mA (IOB). Since there is no switching, V_{o2} decreases until it reaches V_{o2}^{stby}. As V_{o2} reaches V_{o2}^{stby}, the current through the opto LED decreases allowing the feedback voltage to rise. When the feedback voltage reaches 0.4 V, FSCQ series resumes switching with a predetermined peak drain current of 0.9 A. After burst switching for 1.4 ms, FSCQ series stops switching and checks the feedback voltage. If the feedback voltage is below 0.4 V, FSCQ series stops switching until the feedback voltage increases to 0.4 V. If the feedback voltage is above 0.4 V, FSCQ series goes back to the normal operation. The output voltage drop circuit can be implemented alternatively, as shown in Figure 37. In the circuit, the FSCQ series goes into burst mode, when picture off signal is applied to Q_1. Then, V_{o2} is determined by the Zener diode breakdown voltage. Assuming that the forward voltage drop of opto LED is 1 V, the approximate value of V_{o2} in standby mode is given by:

$$V_{O2}^{STBY} = V_Z + 1 \qquad \text{(eq. 8)}$$

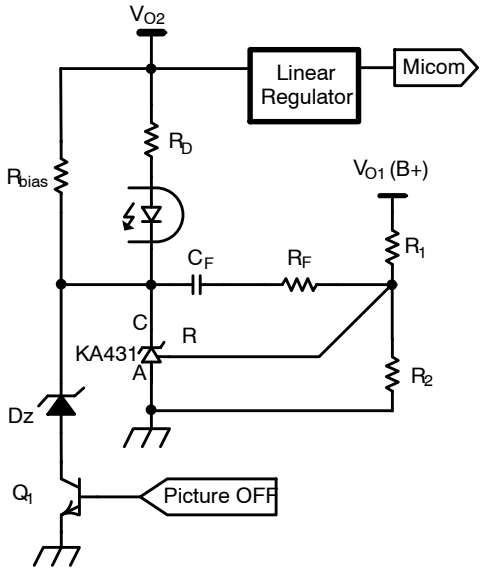


Figure 37. Feedback Circuit to Drop Output Voltage in Standby Mode

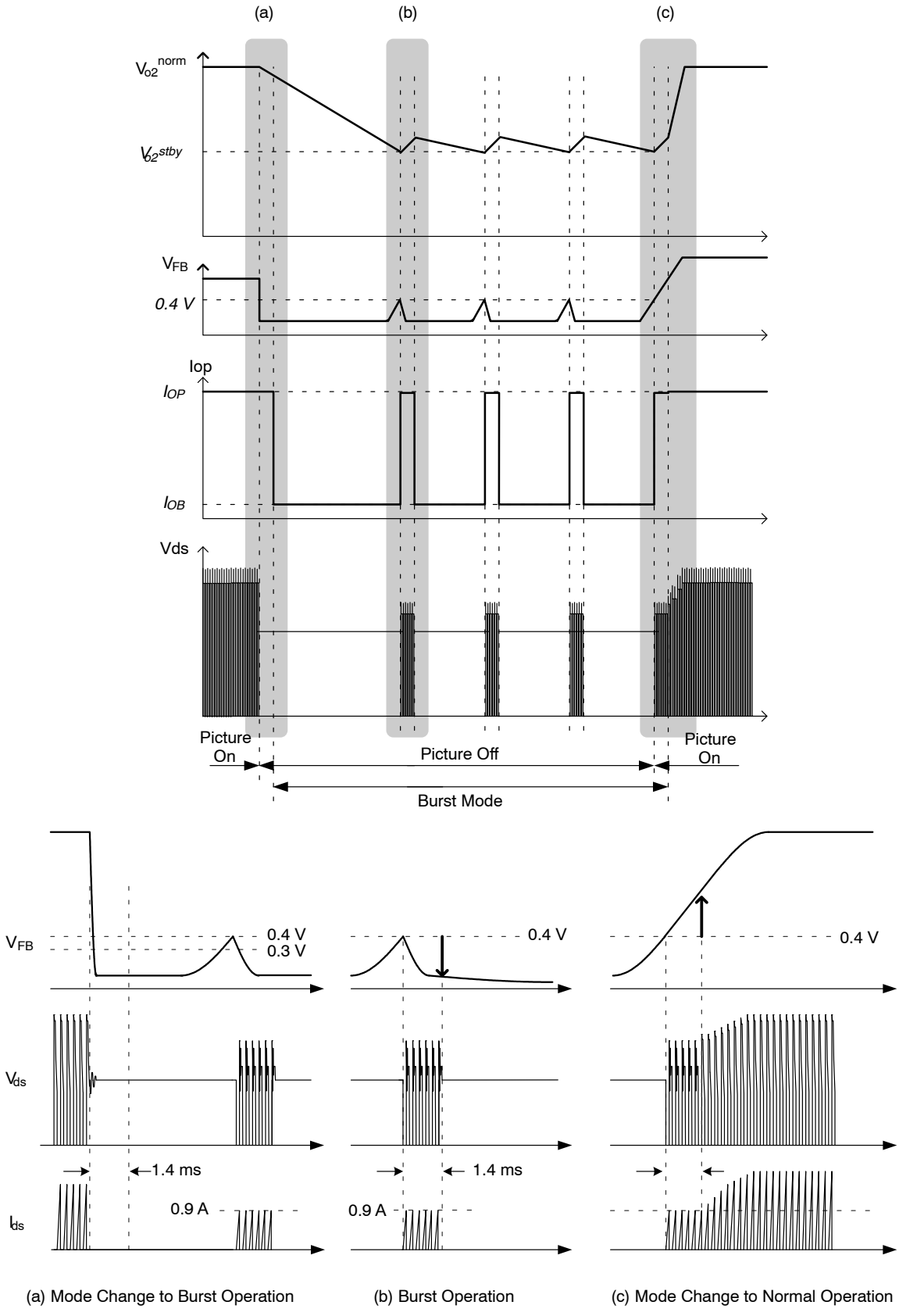


Figure 38. Burst Operation Waveforms

FSCQ0765RT Typical Application Circuit

FSCQ0765RT TYPICAL APPLICATION CIRCUIT

Application	Output Power	Input Voltage	Output Voltage (Max. Current)
C−TV	83 W	Universal Input (90−270 V_{ac})	12 V (1 A)
			18 V (0.5 A)
			125 V (0.4 A)
			24 V (0.5 A)

Features

- High Efficiency (>83% at 90 V_{ac} Input)
- Wider Load Range through the Extended Quasi−Resonant Operation
- Low Standby Mode Power Consumption (<1 W)
- Low Component Count
- Enhanced System Reliability Through Various Protection Functions
- Internal Soft−Start (20 ms)

Key Design Notes

- 24 V Output Designed to Drop to 8 V in Standby Mode

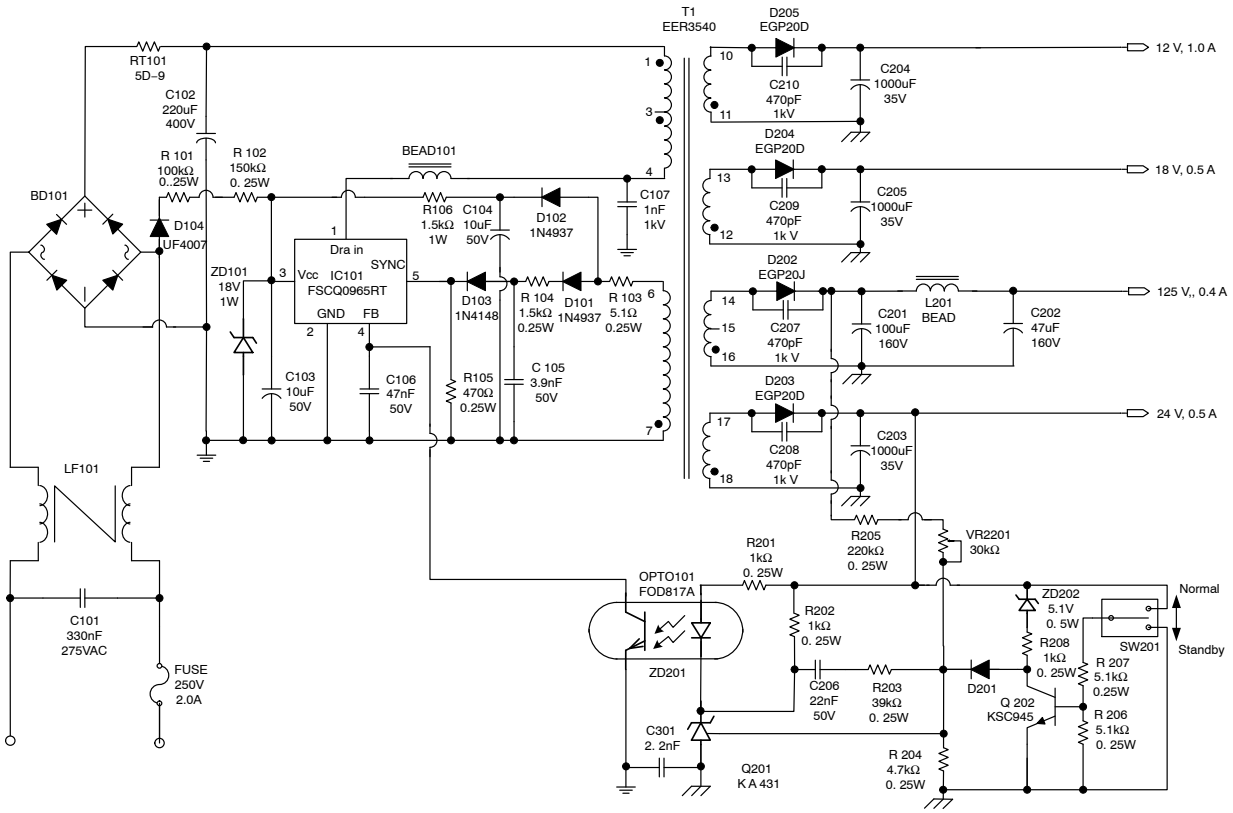


Figure 39. FSCQ0765RT Typical Application Circuit Schematic

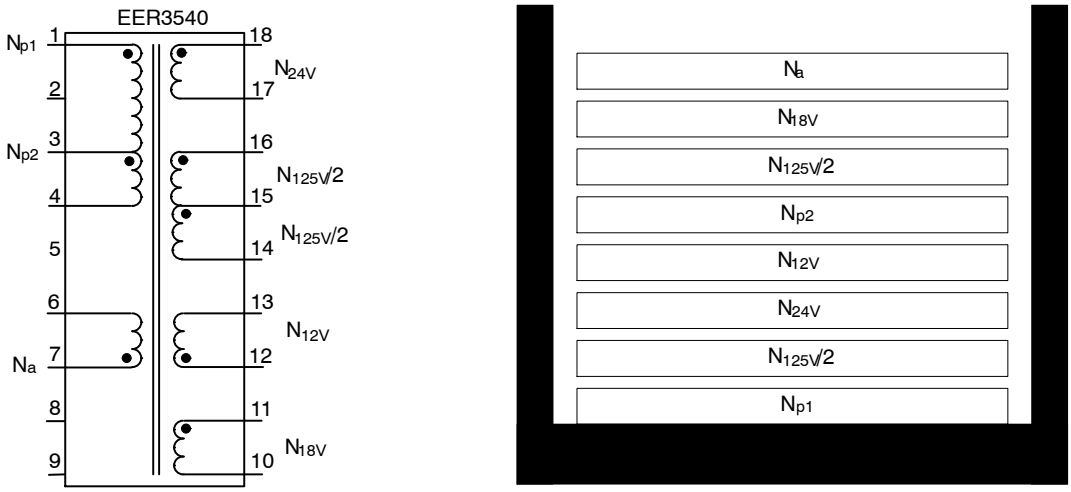


Figure 40. Transformer Schematic Diagram

WINDING SPECIFICATION

No	Pin (s → f)	Wire	Turns	Winding Method
N_{p1}	1–3	0.5φ x 1	32	Center Winding
$N_{125V}/2$	16–15	0.5φ x 1	32	
N_{24V}	18–17	0.4φ x 2	13	
N_{12V}	12–13	0.5φ x 2	7	
N_{p2}	3–4	0.5φ x 1	32	
$N_{125V}/2$	15–14	0.5φ x 1	32	
N_{18V}	11–10	0.4φ x 2	10	
N_a	7–6	0.3φ x 1	20	

ELECTRICAL CHARACTERISTICS

	Pin	Specification	Remarks
Inductance	1–3	515 μH ±5%	1 kHz, 1 V
Leakage Inductance	1–3	10 μH Max.	2nd all short

Core & Bobbin

- Core: EER3540
- Bobbin: EER3540
- Ae: 107 mm^2

BILL OF MATERIALS

Part	Value	Note
Fuse		
FUSE	250 V / 2 A	
NTC		
RT101	5D−9	
Resistor		
R101	100 kΩ	0.25 W
R102	150 kΩ	0.25 W
R103	5.1 Ω	0.25 W
R104	1.5 kΩ	0.25 W
R105	470 Ω	0.25 W
R106	1.5 kΩ	1 W
R107	Open	
R201	1 kΩ	0.25 W
R202	1 kΩ	0.25 W
R203	39 kΩ	0.25 W
R204	4.7 kΩ	0.25 W, 1%
R205	220 kΩ	0.25 W, 1%
R206	5.1 kΩ	0.25 W
R207	5.1 kΩ	0.25 W
R208	1 kΩ	0.25 W
VR201	30 kΩ	
Capacitor		
C101	330 nF / 275 V_{AC}	
C102	220 μF / 400 V	Box Capacitor
C103	10 μF / 50 V	Electrolytic
C104	10 μF / 50 V	Electrolytic
C105	3.9 nF / 50 V	Electrolytic
C106	47 nF / 50 V	Film Capacitor
C107	680 pF / 1 kV	Film Capacitor
C108	Open	
C201	100 μF / 160 V	Electrolytic
C202	47 μF / 160 V	Electrolytic
C203	1000 μF / 35 V	Electrolytic
C204	1000 μF / 35 V	Electrolytic
C205	1000 μF / 35 V	Electrolytic
C206	22 nF / 50 V	Film Capacitor

BILL OF MATERIALS (continued)

Part	Value	Note
C207	470 pF / 1 kV	Ceramic Capacitor
C208	470 pF / 1 kV	Ceramic Capacitor
C209	470 pF / 1 kV	Ceramic Capacitor
C210	470 pF / 1 kV	Ceramic Capacitor
C301	2.2 nF / 1 kV	AC Ceramic Capacitor
Inductor		
BEAD101	BEAD	
BEAD201	5 μH	3 A
Diode		
D101	1N4937	1 A, 600 V
D102	1N4937	1 A, 600 V
D103	1N4148	0.15 A, 50 V
D104	Short	
D105	Open	
ZD101	1N4746	18 V, 1 W
ZD102	Open	
ZD201	1N5231	5.1 V, 0.5 W
D201	1N4148	0.15 A, 50 V
D202	EGP20J	2 A, 600 V
D203	EGP20D	2 A, 200 V
D204	EGP20D	2 A, 200 V
D205	EGP20D	2 A, 200 V
Bridge Diode		
BD101	GSIB660	6 A, 600 V
Line Filter		
LF101		14 mH
Transformer		
T101	EER3540	
Switch		
SW201	ON/OFF	For MCU Signal
IC		
IC101	FSCQ0765RT	TO−220F−5L
OPT101	FOD817A	
Q201	KA431LZ	TO−92
Q202	KSC945	

FSCQ0965RT Typical Application Circuit

FSCQ0965RT TYPICAL APPLICATION CIRCUIT

Application	Output Power	Input Voltage	Output Voltage (Max. Current)
C−TV	102 W	Universal Input (90−270 V_{ac})	12 V (0.5 A)
			18 V (0.5 A)
			125 V (0.5 A)
			24 V (1.0 A)

Features

- High Efficiency (>83% at 90 V_{ac} Input)
- Wider Load Range through the Extended Quasi−Resonant Operation
- Low Standby Mode Power Consumption (<1 W)
- Low Component Count
- Enhanced System Reliability Through Various Protection Functions
- Internal Soft−Start (20 ms)

Key Design Notes

- 24 V Output Designed to Drop to 8 V in Standby Mode

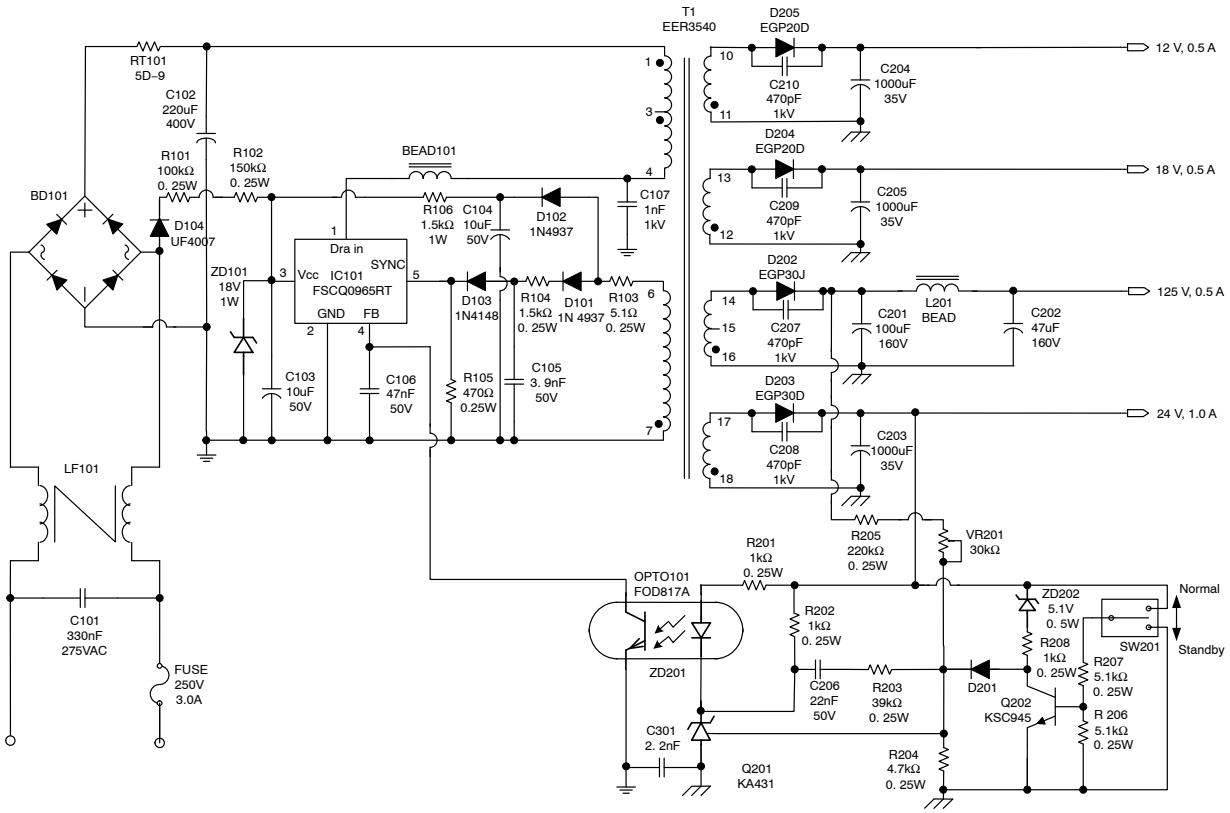


Figure 41. FSCQ0965RT Typical Application Circuit Schematic

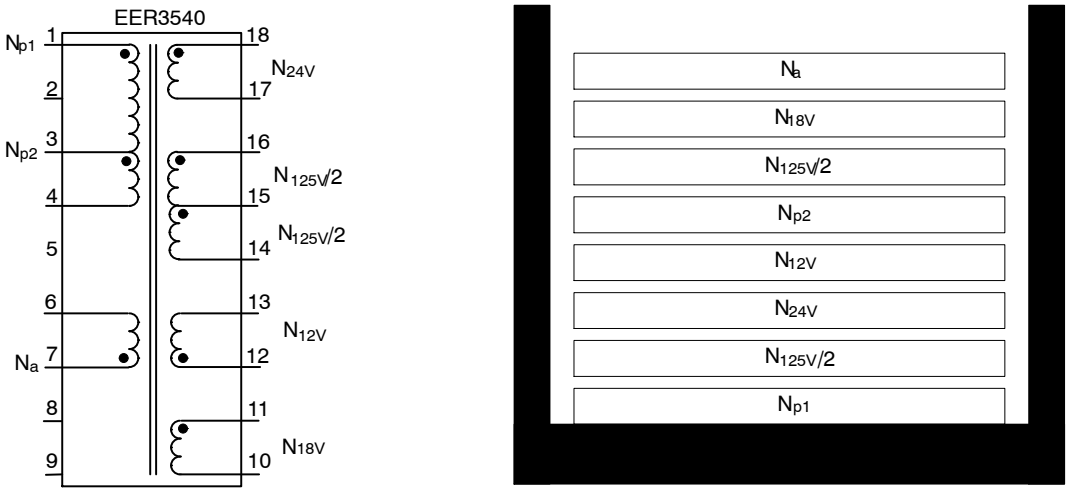


Figure 42. Transformer Schematic Diagram

WINDING SPECIFICATION

No	Pin (s → f)	Wire	Turns	Winding Method
N_{p1}	1–3	0.5φ x 1	32	Center Winding
$N_{125V}/2$	16–15	0.5φ x 1	32	
N_{24V}	18–17	0.4φ x 2	13	
N_{12V}	12–13	0.5φ x 2	7	
N_{p2}	3–4	0.5φ x 1	32	
$N_{125V}/2$	15–14	0.5φ x 1	32	
N_{18V}	11–10	0.4φ x 2	10	
N_a	7–6	0.3φ x 1	20	

ELECTRICAL CHARACTERISTICS

	Pin	Specification	Remarks
Inductance	1–3	410 μH ±5%	1 kHz, 1 V
Leakage Inductance	1–3	10 μH Max.	2nd all short

Core & Bobbin

- Core: EER3540
- Bobbin: EER3540
- Ae: 107 mm^2

BILL OF MATERIALS

Part	Value	Note
Fuse		
FUSE	250 V / 3 A	
NTC		
RT101	5D−9	
Resistor		
R101	100 kΩ	0.25 W
R102	150 kΩ	0.25 W
R103	5.1 Ω	0.25 W
R104	1.5 kΩ	0.25 W
R105	470 Ω	0.25 W
R106	1.5 kΩ	1 W
R107	Open	
R201	1 kΩ	0.25 W
R202	1 kΩ	0.25 W
R203	39 kΩ	0.25 W
R204	4.7 kΩ	0.25 W, 1%
R205	220 kΩ	0.25 W, 1%
R206	5.1 kΩ	0.25 W
R207	5.1 kΩ	0.25 W
R208	1 kΩ	0.25 W
VR201	30 kΩ	
Capacitor		
C101	330 nF / 275 V_{AC}	
C102	220 μF / 400 V	Box Capacitor
C103	10 μF / 50 V	Electrolytic
C104	10 μF / 50 V	Electrolytic
C105	3.9 nF / 50 V	Electrolytic
C106	47 nF / 50 V	Film Capacitor
C107	1 nF / 1 kV	Film Capacitor
C108	Open	
C201	100 μF / 160 V	Electrolytic
C202	47 μF / 160 V	Electrolytic
C203	1000 μF / 35 V	Electrolytic
C204	1000 μF / 35 V	Electrolytic
C205	1000 μF / 35 V	Electrolytic
C206	22 nF / 50 V	Film Capacitor

BILL OF MATERIALS (continued)

Part	Value	Note
C207	470 pF / 1 kV	Ceramic Capacitor
C208	470 pF / 1 kV	Ceramic Capacitor
C209	470 pF / 1 kV	Ceramic Capacitor
C210	470 pF / 1 kV	Ceramic Capacitor
C301	2.2 nF / 1 kV	AC Ceramic Capacitor
Inductor		
BEAD101	BEAD	
BEAD201	5 μH	3 A
Diode		
D101	1N4937	1 A, 600 V
D102	1N4937	1 A, 600 V
D103	1N4148	0.15 A, 50 V
D104	Short	
D105	Open	
ZD101	1N4746	18 V, 1 W
ZD102	Open	
ZD201	1N5231	5.1 V, 0.5 W
D201	1N4148	0.15 A, 50 V
D202	EGP30J	3 A, 600 V
D203	EGP30D	3 A, 200 V
D204	EGP20D	2 A, 200 V
D205	EGP20D	2 A, 200 V
Bridge Diode		
BD101	GSIB660	6 A, 600 V
Line Filter		
LF101		14 mH
Transformer		
T101	EER3540	
Switch		
SW201	ON/OFF	For MCU Signal
IC		
IC101	FSCQ0965RT	TO−220F−5L
OPT101	FOD817A	
Q201	KA431LZ	TO−92
Q202	KSC945	

FSCQ1265RT Typical Application Circuit

FSCQ1265RT TYPICAL APPLICATION CIRCUIT

Application	Output Power	Input Voltage	Output Voltage (Max. Current)
C−TV	132 W	Universal Input (90−270 V_{ac})	8.5 V (0.5 A)
			15 V (0.5 A)
			140 V (0.6 A)
			24 V (1.5 A)

Features

- High Efficiency (>83% at 90 V_{ac} Input)
- Wider Load Range through the Extended Quasi−Resonant Operation
- Low Standby Mode Power Consumption (<1 W)
- Low Component Count
- Enhanced System Reliability Through Various Protection Functions
- Internal Soft−Start (20 ms)

Key Design Notes

- 24 V Output Designed to Drop to 8 V in Standby Mode

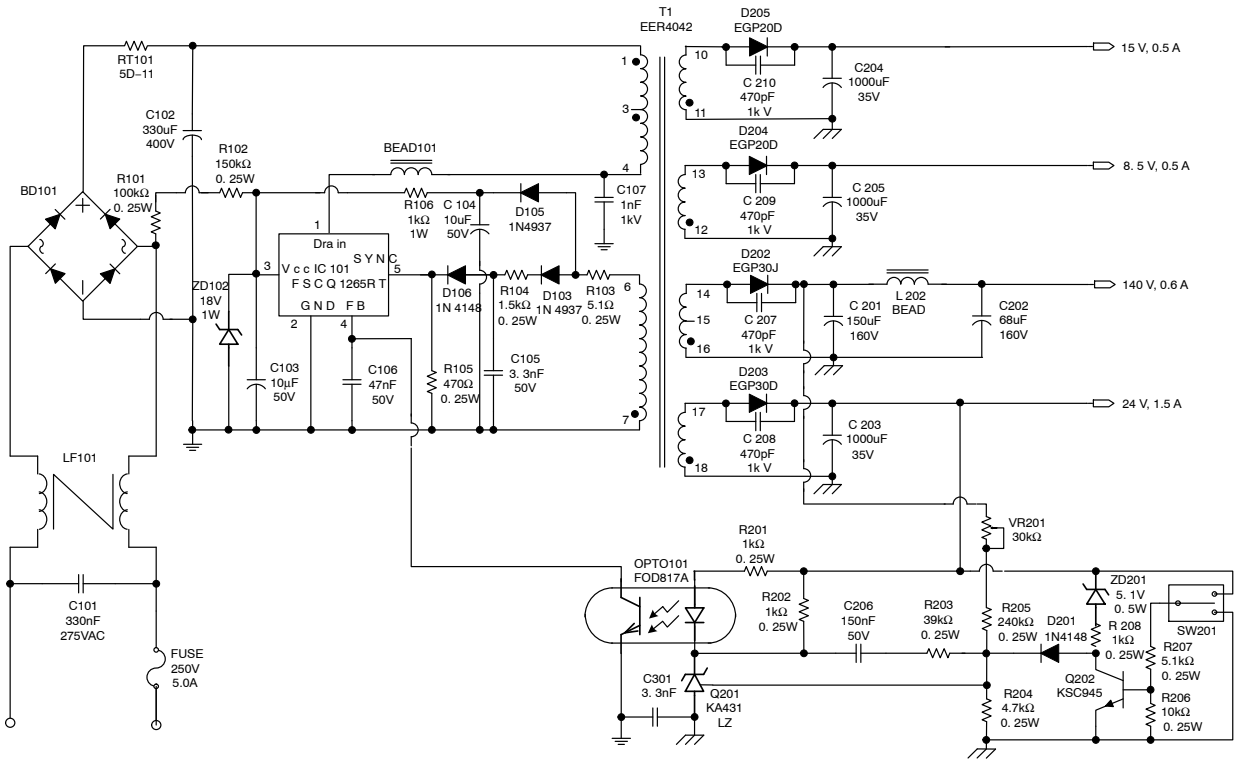


Figure 43. FSCQ1265RT Typical Application Circuit Schematic

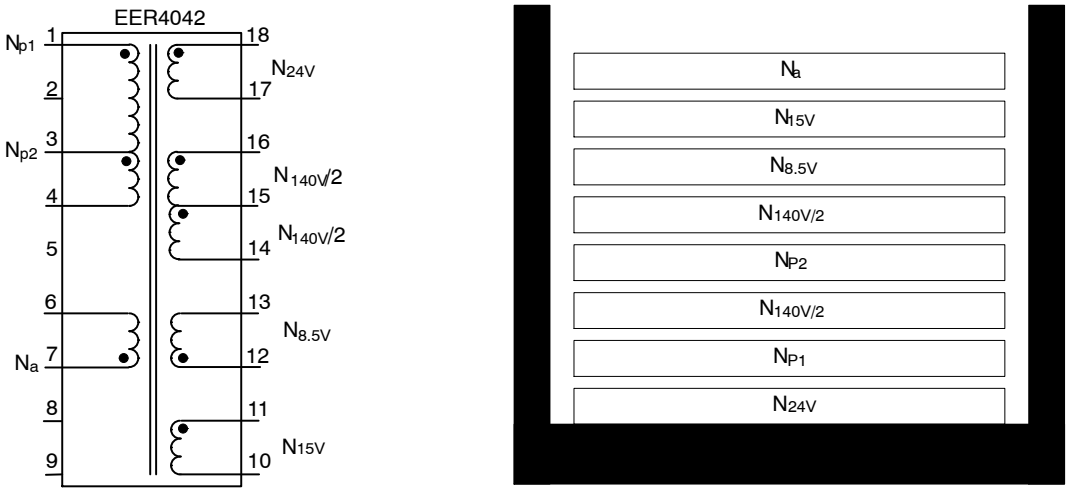


Figure 44. Transformer Schematic Diagram

WINDING SPECIFICATION

No	Pin (s → f)	Wire	Turns	Winding Method
N_{24}	18–17	0.65φ x 2	8	Space Winding
N_{P1}	1–3	0.1φ x 10 x 2	20	Center Winding
$N_{140V}/2$	16–15	0.1φ x 10 x 2	23	Center Winding
N_{p2}	3–4	0.1φ x 10 x 2	20	Center Winding
$N_{140V}/2$	15–14	0.1φ x 10 x 2	22	Center Winding
$N_{8.5V}$	12–13	0.6φ x 1	3	Space Winding
N_{15V}	11–10	0.6φ x 1	6	Space Winding
N_a	7–6	0.3φ x 1	13	Space Winding

ELECTRICAL CHARACTERISTICS

	Pin	Specification	Remarks
Inductance	1–4	315 μH ±5%	1 kHz, 1 V
Leakage Inductance	1–4	10 μH Max.	2nd all short

Core & Bobbin

- Core: EER4042
- Bobbin: EER4042 (18 Pin)
- Ae: 153 mm^2

BILL OF MATERIALS

Part	Value	Note
Fuse		
FUSE	250 V / 5 A	
NTC		
RT101	5D−11	
Resistor		
R101	100 kΩ	0.25 W
R102	150 kΩ	0.25 W
R103	5.1 Ω	0.25 W
R104	1.5 kΩ	0.25 W
R105	470 Ω	0.25 W
R106	1 kΩ	1 W
R107	Open	
R201	1 kΩ	0.25 W
R202	1 kΩ	0.25 W
R203	39 kΩ	0.25 W
R204	4.7 kΩ	0.25 W, 1%
R205	240 kΩ	0.25 W, 1%
R206	10 kΩ	0.25 W
R207	5.1 kΩ	0.25 W
R208	1 kΩ	0.25 W
VR201	30 kΩ	
Capacitor		
C101	330 nF / 275 V_{AC}	
C102	330 μF / 400 V	Box Capacitor
C103	10 μF / 50 V	Electrolytic
C104	10 μF / 50 V	Electrolytic
C105	3.3 nF / 50 V	Electrolytic
C106	47 nF / 50 V	Film Capacitor
C107	1 nF / 1 kV	Film Capacitor
C108	Open	
C201	100 μF / 160 V	Electrolytic
C202	68 μF / 160 V	Electrolytic
C203	1000 μF / 35 V	Electrolytic
C204	1000 μF / 35 V	Electrolytic
C205	1000 μF / 35 V	Electrolytic
C206	150 nF / 50 V	Film Capacitor

BILL OF MATERIALS (continued)

Part	Value	Note
C207	470 pF / 1 kV	Ceramic Capacitor
C208	470 pF / 1 kV	Ceramic Capacitor
C209	470 pF / 1 kV	Ceramic Capacitor
C210	470 pF / 1 kV	Ceramic Capacitor
C301	3.3 nF / 1 kV	AC Ceramic Capacitor
Inductor		
BEAD101	BEAD	
BEAD201	5 μH	3 A
Diode		
D101	1N4937	1 A, 600 V
D102	1N4937	1 A, 600 V
D103	1N4148	0.15 A, 50 V
D104	Short	
D105	Open	
ZD101	1N4746	18 V, 1 W
ZD102	Open	
ZD201	1N5231	5.1 V, 0.5 W
D201	1N4148	0.15 A, 50 V
D202	EGP30J	3 A, 600 V
D203	EGP30D	3 A, 200 V
D204	EGP20D	2 A, 200 V
D205	EGP20D	2 A, 200 V
Bridge Diode		
BD101	GSIB660	6 A, 600 V
Line Filter		
LF101		14 mH
Transformer		
T101	EER4042	
Switch		
SW201	ON/OFF	For MCU Signal
IC		
IC101	FSCQ1265RT	TO−220F−5L
OPT101	FOD817A	
Q201	KA431LZ	TO−92
Q202	KSC945	

FSCQ1565RT Typical Application Circuit

FSCQ1565RT TYPICAL APPLICATION CIRCUIT

Application	Output Power	Input Voltage	Output Voltage (Max. Current)
C−TV	160 W	Universal Input (90−270 V_{ac})	8.5 V (0.5 A)
			15 V (0.5 A)
			140 V (0.8 A)
			24 V (1.5 A)

Features

- High Efficiency (>83% at 90 V_{ac} Input)
- Wider Load Range through the Extended Quasi−Resonant Operation
- Low Standby Mode Power Consumption (<1 W)
- Low Component Count
- Enhanced System Reliability Through Various Protection Functions
- Internal Soft−Start (20 ms)

Key Design Notes

- 24 V Output Designed to Drop to 8 V in Standby Mode

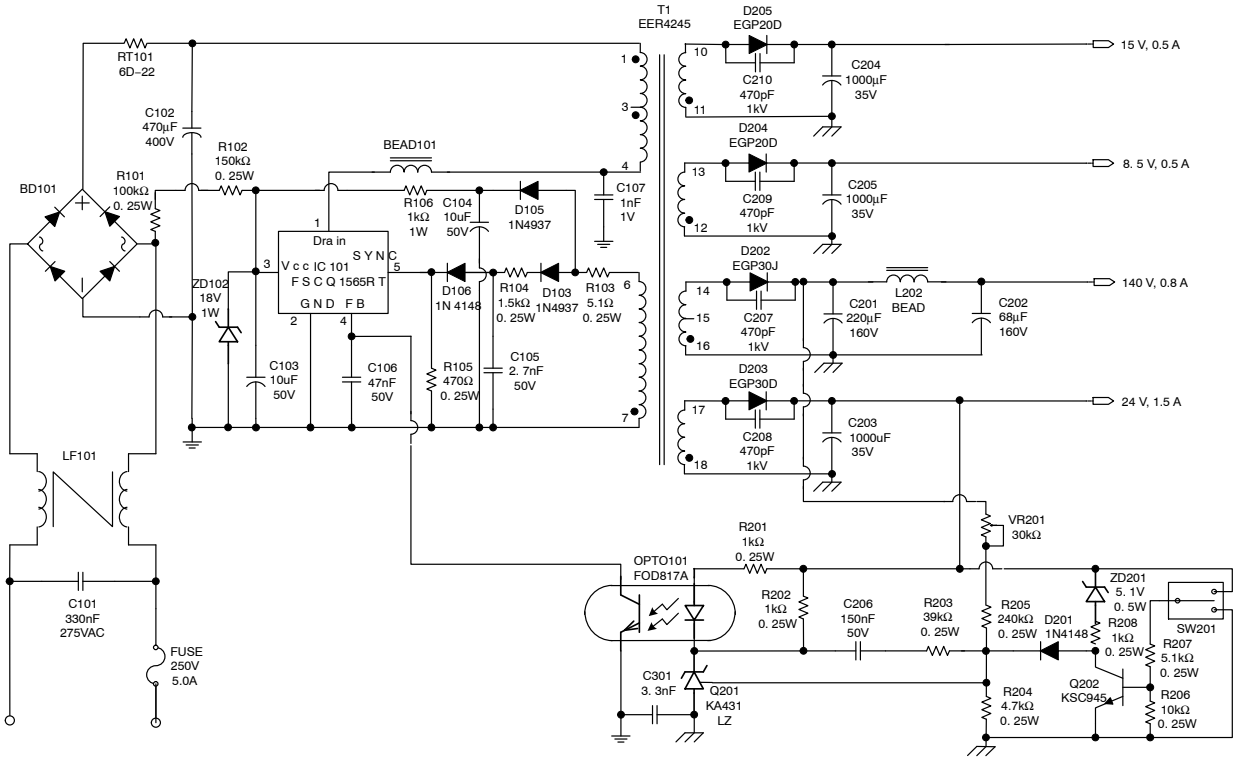


Figure 45. FSCQ1565RT Typical Application Circuit Schematic

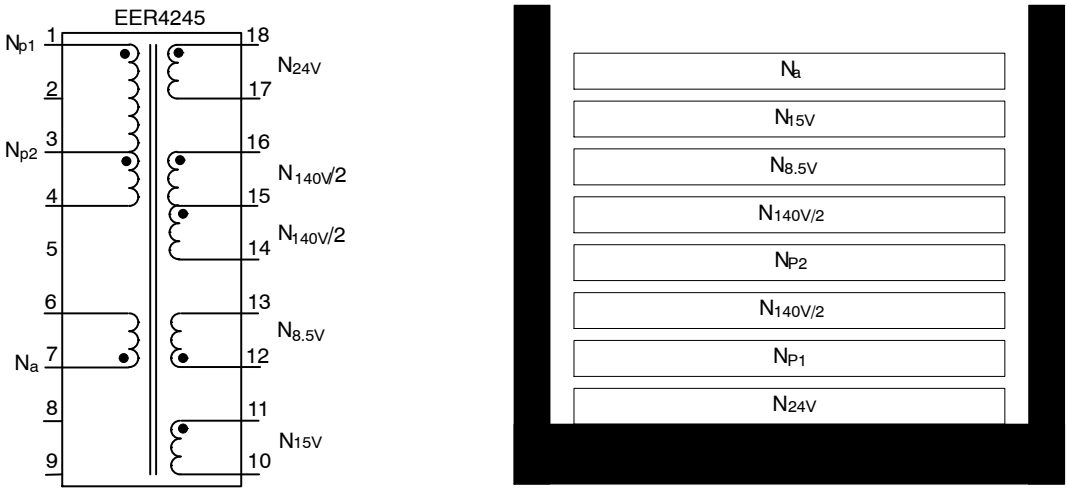


Figure 46. Transformer Schematic Diagram

WINDING SPECIFICATION

No	Pin (s → f)	Wire	Turns	Winding Method
N_{24V}	18–17	0.65φ x 2	5	Space Winding
N_{P1}	1–3	0.08φ x 20 x 2	13	Center Winding
$N_{140V}/2$	16–15	0.08φ x 20 x 2	15	Center Winding
N_{p2}	3–4	0.08φ x 20 x 2	13	Center Winding
$N_{140V}/2$	15–14	0.08φ x 20 x 2	14	Center Winding
$N_{8.5V}$	12–13	0.6φ x 1	2	Space Winding
N_{15V}	11–10	0.6φ x 1	3	Space Winding
N_a	7–6	0.3φ x 1	8	Space Winding

ELECTRICAL CHARACTERISTICS

	Pin	Specification	Remarks
Inductance	1–4	220 μH ±5%	1 kHz, 1 V
Leakage Inductance	1–4	10 μH Max.	2nd all short

Core & Bobbin

- Core: EER4245
- Bobbin: EER4245 (18 Pin)
- Ae: 201.8 mm^2

BILL OF MATERIALS

Part	Value	Note
Fuse		
FUSE	250 V / 5 A	
NTC		
RT101	6D−22	
Resistor		
R101	100 kΩ	0.25 W
R102	150 kΩ	0.25 W
R103	5.1 Ω	0.25 W
R104	1.5 kΩ	0.25 W
R105	470 Ω	0.25 W
R106	1.5 kΩ	1 W
R107	Open	
R201	1 kΩ	0.25 W
R202	1 kΩ	0.25 W
R203	39 kΩ	0.25 W
R204	4.7 kΩ	0.25 W, 1%
R205	240 kΩ	0.25 W, 1%
R206	10 kΩ	0.25 W
R207	5.1 kΩ	0.25 W
R208	1 kΩ	0.25 W
VR201	30 kΩ	
Capacitor		
C101	330 nF / 275 V_{AC}	
C102	470 μF / 400 V	Box Capacitor
C103	10 μF / 50 V	Electrolytic
C104	10 μF / 50 V	Electrolytic
C105	2.7 nF / 50 V	Electrolytic
C106	47 nF / 50 V	Film Capacitor
C107	1 nF / 1 kV	Film Capacitor
C108	Open	
C201	220 μF / 160 V	Electrolytic
C202	68 μF / 160 V	Electrolytic
C203	1000 μF / 35 V	Electrolytic
C204	1000 μF / 35 V	Electrolytic
C205	1000 μF / 35 V	Electrolytic
C206	150 nF / 50 V	Film Capacitor

BILL OF MATERIALS (continued)

Part	Value	Note
C207	470 pF / 1 kV	Ceramic Capacitor
C208	470 pF / 1 kV	Ceramic Capacitor
C209	470 pF / 1 kV	Ceramic Capacitor
C210	470 pF / 1 kV	Ceramic Capacitor
C301	3.3 nF / 1 kV	AC Ceramic Capacitor
Inductor		
BEAD101	BEAD	
BEAD201	5 μH	3 A
Diode		
D101	1N4937	1 A, 600 V
D102	1N4937	1 A, 600 V
D103	1N4148	0.15 A, 50 V
D104	Short	
D105	Open	
ZD101	1N4746	18 V, 1 W
ZD102	Open	
ZD201	1N5231	5.1 V, 0.5 W
D201	1N4148	0.15 A, 50 V
D202	EGP30J	3 A, 600 V
D203	EGP30D	3 A, 200 V
D204	EGP20D	2 A, 200 V
D205	EGP20D	2 A, 200 V
Bridge Diode		
BD101	GSIB660	6 A, 600 V
Line Filter		
LF101		14 mH
Transformer		
T101	EER4245	
Switch		
SW201	ON/OFF	For MCU Signal
IC		
IC101	FSCQ1565RT	TO−220F−5L
OPT101	FOD817A	
Q201	KA431LZ	TO−92
Q202	KSC945	

PCB Layout

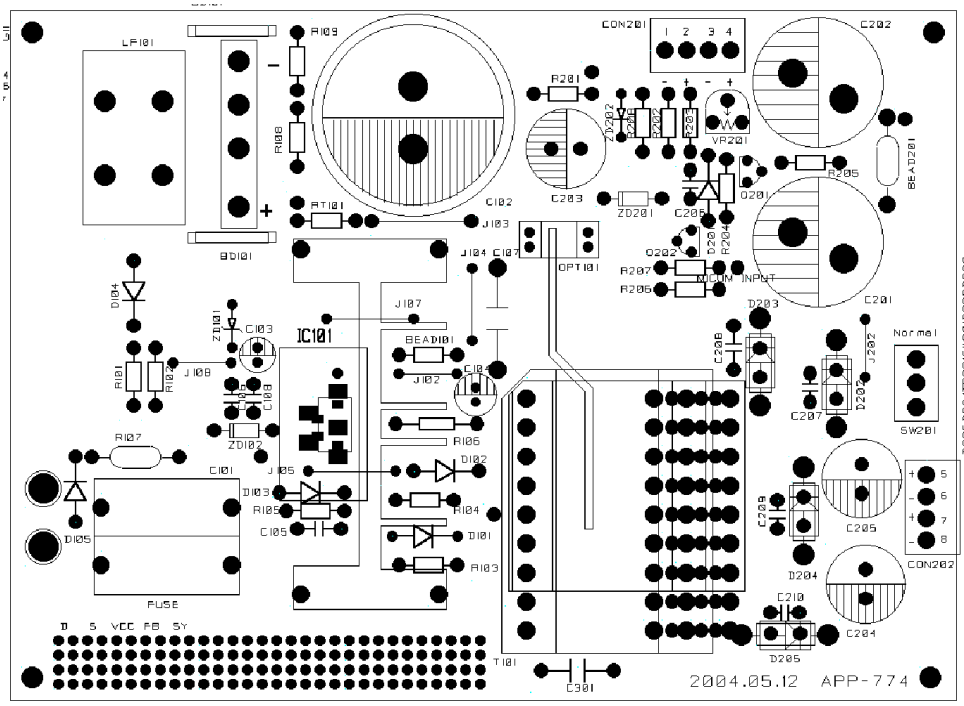


Figure 47. Top View

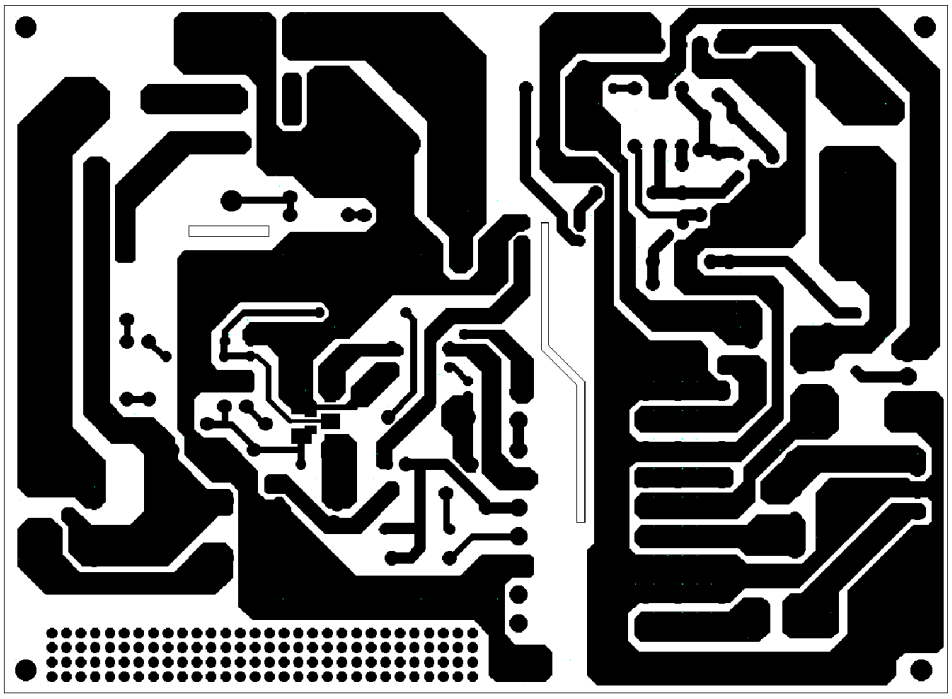
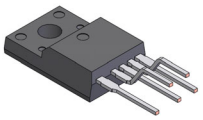


Figure 48. Bottom View

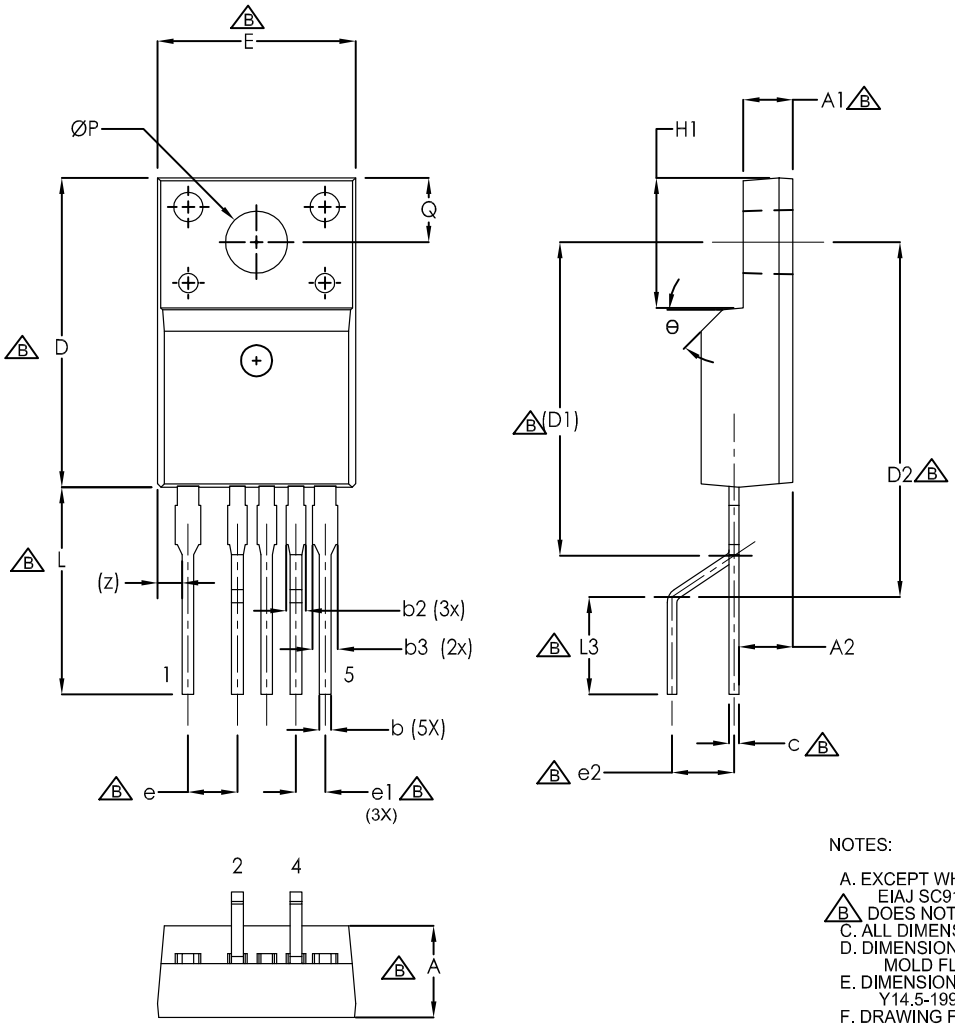
ORDERING INFORMATION TABLE

Part Number	Package	Marking Code	BV_{DSS} (V)	R_{DSON} Max. (Ω)
FSCQ0765RTYDTU	TO−220F−5L (Forming)	CQ0765RT	650	1.6
FSCQ0965RTYDTU		CQ0965RT		1.2
FSCQ1265RTYDTU		CQ1265RT		0.9
FSCQ1565RTYDTU		CQ1565RT		0.7



TO−220− FULLPAK 5LD LF
CASE 340BH
ISSUE A

DATE 22 JUL 2021



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	4.50	4.70	4.90
A1	2.34	2.54	2.74
A2	2.56	2.76	2.96
b	0.50	0.60	0.70
b2	--	–	1.00
b3	--	–	1.30
c	0.45	0.53	0.60
D	15.67	15.87	16.07
D1	16.08 REF		
D2	17.70	18.20	18.70
E	9.96	10.16	10.36
e	2.54 BSC		
e1	1.50 BSC		
e2	2.88	3.18	3.48
H1	6.48	6.68	6.88
L	10.13	10.63	11.13
L3	4.50	5.00	5.50
P	3.08	3.18	3.28
Q	3.20	3.30	3.40
z	1.50 BSC		
θ	–	--	45°

NOTES:

A. EXCEPT WHERE NOTED CONFORMS TO EIAJ SC91A.
B. DOES NOT COMPLY EIAJ STD. VALUE.
C. ALL DIMENSIONS ARE IN MILLIMETERS.
D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
E. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.
F. DRAWING FILE NAME: TO220C05REV2

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales