TXS0102 2-Bit Bidirectional Voltage-Level Translator for Open-Drain and Push-Pull Applications

1 Features

- No direction-control signal needed
- Maximum data rates:
  - 24 Mbps (push pull)
  - 2 Mbps (open drain)
- Available in the Texas Instruments NanoStar™ integrated circuit package
- 1.65 V to 3.6 V on A port and 2.3 V to 5.5 V on B port ($V_{CCA} \leq V_{CCB}$)
- V_{CC} isolation feature: if either V_{CC} input is at GND, both ports are in the High-Impedance state
- No power-supply sequencing required: either V_{CCA} or V_{CCB} can be ramped first
- I_{off} supports partial-power-down mode operation
- Latch-up performance exceeds 100 mA per JESD 78, Class II
- ESD protection exceeds JESD 22:
  - A port:
    - 2500-V Human-Body Model (A114-B)
    - 250-V Machine Model (A115-A)
    - 1500-V Charged-Device Model (C101)
  - B port:
    - 8-kV Human-Body Model (A114-B)
    - 250-V Machine Model (A115-A)
    - 1500-V Charged-Device Model (C101)

2 Applications

- I^2C / SMBus
- UART
- GPIO

3 Description

This two-bit non-inverting translator is a bidirectional voltage-level translator and can be used to establish digital switching compatibility between mixed-voltage systems. It uses two separate configurable power-supply rails, with the A ports supporting operating voltages from 1.65 V to 3.6 V while it tracks the V_{CCA} supply, and the B ports supporting operating voltages from 2.3 V to 5.5 V while it tracks the V_{CCB} supply. This allows the support of both lower and higher logic signal levels while providing bidirectional translation capabilities between any of the 1.8-V, 2.5-V, 3.3-V, and 5-V voltage nodes.

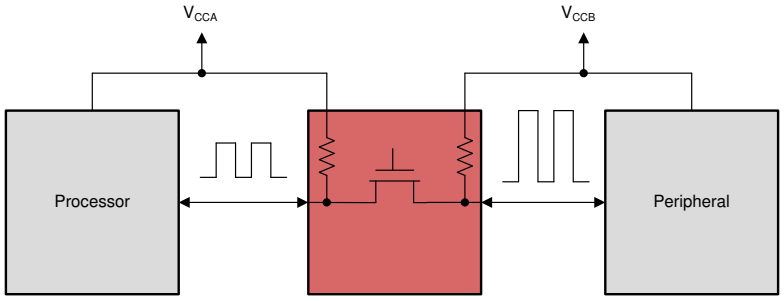
When the output-enable (OE) input is low, all I/Os are placed in the high-impedance state, which significantly reduces the power-supply quiescent current consumption.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Package Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TXS0102	DCT (SSOP, 8)	2.95 mm × 2.80 mm
	DCU (VSSOP, 8)	2.30 mm × 2.00 mm
	DQE (X2SON, 8)	1.40 mm × 1.00 mm
	DQM (X2SON, 8)	1.80 mm × 1.20 mm
	YZP (DSBGA, 8)	1.90 mm × 0.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Application Block Diagram for TXS0102

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision I (August 2018) to Revision J (July 2023)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1

Changes from Revision H (April 2018) to Revision I (August 2018)	Page
• Updated the V_{IH} A-port I/O V_{CCA} value in the Recommended Operating Conditions table from: *1.65 V to 3.6 V*, to: *1.65 V to 1.95 V*	5

Changes from Revision G (January 2018) to Revision H (April 2018)	Page
• Updated *TXS0102 Layout Example* diagram	19

5 Pin Configuration and Functions

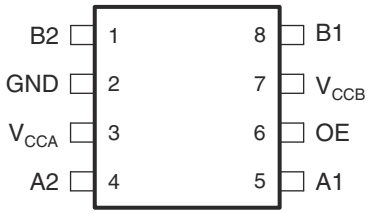


Figure 5-1. DCT or DCU Package, 8-Pin SSOP and VSSOP (Top View)

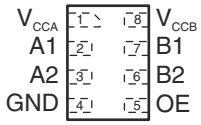


Figure 5-2. DQE or DQM Package, 8-Pin X2SON (Top View)

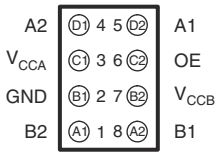


Figure 5-3. YZP Package, 8-Pin DSBGA (Bottom View)

Table 5-1. Pin Functions

PIN				TYPE[1]	DESCRIPTION
NAME	NO.				
	DCT, DCU	DQE, DQM	YZP		
A1	5	2	D2	I/O	Input/output A. Referenced to V_{CCA}.
A2	4	3	D1	I/O	Input/output A. Referenced to V_{CCA}.
B1	8	7	A2	I/O	Input/output B. Referenced to V_{CCB}.
B2	1	6	A1	I/O	Input/output B. Referenced to V_{CCB}.
GND	2	4	B1	—	Ground
OE	6	5	C2	I	Output enable (active High). Pull OE low to place all outputs in 3-state mode. Referenced to V_{CCA}.
V_{CCA}	3	1	C1	P	A-port supply voltage. 1.65 V ≤ V_{CCA} ≤ 3.6 V and V_{CCA} ≤ V_{CCB}
V_{CCB}	7	8	B2	P	B-port supply voltage. 2.3 V ≤ V_{CCB} ≤ 5.5 V

(1) I = input, O = output, I/O = input and output, P = power

6 Specifications

6.1 Absolute Maximum Ratings

over recommended operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply voltage range, V_{CCA}		–0.5	4.6	V
Supply voltage range, V_{CCB}		–0.5	6.5	V
Input voltage range, V_I (2)	A port	–0.5	4.6	V
	B port	–0.5	6.5	
Voltage range applied to any output in the high-impedance or power-off state, V_O (2)	A port	–0.5	4.6	V
	B port	–0.5	6.5	
Voltage range applied to any output in the high or low state, V_O (2) (3)	A port	–0.5	V_{CCA} + 0.5	V
	B port	–0.5	V_{CCB} + 0.5	
Input clamp current, I_{IK}	V_I < 0		–50	mA
Output clamp current, I_{OK}	V_O < 0		–50	mA
Continuous output current, I_O			±50	mA
Continuous current through V_{CCA}, V_{CCB}, or GND			±100	mA
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CCA} and V_{CCB} are provided in the recommended operating conditions table.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins, A Port(1)	±2500	V
		Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins, B Port(1)	±8000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	V
		250-V Machine Model (A115-A), all pins	±250	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

V_{CCI} is the supply voltage associated with the input port. V_{CCO} is the supply voltage associated with the output port.

				MIN	MAX	UNIT
V_{CCA}	Supply voltage(1)			1.65	3.6	V
V_{CCB}	Supply voltage			2.3	5.5	V
V_{IH}	High-level input voltage	A-port I/Os	V_{CCA} = 1.65 V to 1.95 V V_{CCB} = 2.3 V to 5.5 V	V_{CCI} – 0.2	V_{CCI}	V
			V_{CCA} = 1.65 V to 3.6 V V_{CCB} = 2.3 V to 5.5 V	V_{CCI} – 0.4	V_{CCI}	
		B-port I/Os	V_{CCA} = 1.65 V to 3.6 V V_{CCB} = 2.3 V to 5.5 V	V_{CCI} – 0.4	V_{CCI}	V
		OE input	V_{CCA} = 1.65 V to 3.6 V V_{CCB} = 2.3 V to 5.5 V	V_{CCA} × 0.65	5.5	V
V_{IL} (2)	Low-level input voltage	A-port I/Os	V_{CCA} = 1.65 V to 3.6 V V_{CCB} = 2.3 V to 5.5 V	0	0.15	V
		B-port I/Os	V_{CCA} = 1.65 V to 3.6 V V_{CCB} = 2.3 V to 5.5 V	0	0.15	V
		OE input	V_{CCA} = 1.65 V to 3.6 V V_{CCB} = 2.3 V to 5.5 V	0	V_{CCA} × 0.35	V
Δt/Δv	Input transition rise or fall rate	A-port I/Os push-pull driving	V_{CCA} = 1.65 V to 3.6 V V_{CCB} = 2.3 V to 5.5 V		10	ns/V
		B-port I/Os push-pull driving	V_{CCA} = 1.65 V to 3.6 V V_{CCB} = 2.3 V to 5.5 V		10	ns/V
		Control input	V_{CCA} = 1.65 V to 3.6 V V_{CCB} = 2.3 V to 5.5 V		10	ns/V
T_A	Operating free-air temperature			–40	85	°C

(1) V_{CCA} must be less than or equal to V_{CCB}, and V_{CCA} must not exceed 3.6 V.
(2) The maximum V_{IL} value is provided to ensure that a valid V_{OL} is maintained. The V_{OL} value is V_{IL} plus the voltage drop across the pass-gate transistor.

6.4 Thermal Information

THERMAL METRIC(1)		TXS0102					UNIT
		DCT	DCU	DQE	DQM	YZP	
		8 PINS	8 PINS	8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	182.6	199.1	199.3	239.3	105.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	113.3	72.4	26.4	106.7	1.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	94.9	77.8	78.6	130.4	10.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	39.4	6.2	5.9	8.2	3.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	93.9	77.4	78.0	130.2	10.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)(1) (2) (3)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	T_A = 25°C			T_A = –40°C to +85°C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{OHA}	Port A output high voltage	I_{OH} = –20 µA $V_{IB} \geq V_{CCB}$ – 0.4 V	1.65 V to 3.6 V	2.3 V to 5.5 V				V_{CCA} × 0.67			V
V_{OLA}	Port A output low voltage	I_{OL} = 1 mA $V_{IB} \leq$ 0.15 V	1.65 V to 3.6 V	2.3 V to 5.5 V						0.4	V
V_{OHB}	Port B output high voltage		1.65 V to 3.6 V	2.3 V to 5.5 V				V_{CCB} × 0.67			V
V_{OLB}	Port B output low voltage		1.65 V to 3.6 V	2.3 V to 5.5 V						0.4	V
I_I	Input leakage current	OE	1.65 V to 3.6 V	2.3 V to 5.5 V			±1			±2	µA
I_{off}	Partial power down current	A port	0 V	0 V to 5.5 V			±1			±2	µA
		B port	0 V to 3.6 V	0 V			±1			±2	µA
I_{OZ}	High-impedance state output current	A or B port	1.65 V to 3.6 V	2.3 V to 5.5 V			±1			±2	µA
I_{CCA}	V_{CCA} supply current	V_I = V_O = open I_O = 0	1.65 V to V_{CCB}	2.3 V to 5.5 V						2.4	µA
			3.6 V	0 V						2.2	µA
			0 V	5.5 V						–1	µA
I_{CCB}	V_{CCB} supply current	V_I = V_O = open I_O = 0	1.65 V to V_{CCB}	2.3 V to 5.5 V						12	µA
			3.6 V	0 V						–1	µA
			0 V	5.5 V						1	µA
I_{CCA} + I_{CCB}	Combined supply current	V_I = V_{CCI} or GND I_O = 0	1.65 V to V_{CCB}	2.3 V to 5.5 V						14.4	µA
C_I	Input capacitance	OE	3.3 V	3.3 V		2.5				3.5	pF
C_{io}	Input-to-output internal capacitance	A or B port	3.3 V	3.3 V		10					pF
		A port				5			6		pF
		B port				6			7.5		pF

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port
(3) V_{CCA} must be less than or equal to V_{CCB}, and V_{CCA} must not exceed 3.6 V.

6.6 Timing Requirements: V_{CCA} = 1.8 V ±0.15 V

		V_{CCB} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Data rate	Push-pull driving		21		22		24	Mbps
	Open-drain driving		2		2		2	
t_w Pulse duration	Push-pull driving (data inputs)	47		45		41		ns
	Open-drain driving (data inputs)	500		500		500		

6.7 Timing Requirements: V_{CCA} = 2.5 V ± 0.2 V

		V_{CCB} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Data rate	Push-pull driving		20		22		24	Mbps
	Open-drain driving		2		2		2	
t_w Pulse duration	Push-pull driving (data inputs)	50		45		41		ns
	Open-drain driving (data inputs)	500		500		500		

6.8 Timing Requirements: V_{CCA} = 3.3 V ± 0.3 V

		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		UNIT
		MIN	MAX	MIN	MAX	
Data rate	Push-pull driving		23		24	Mbps
	Open-drain driving		2		2	
t_w Pulse duration	Push-pull driving (data inputs)	43		41		ns
	Open-drain driving (data inputs)	500		500		

6.9 Switching Characteristics: V_{CCA} = 1.8 V ± 0.15 V

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CCB} = 2.5 V ±0.2 V		V_{CCB} = 3.3 V ±0.2 V		V_{CCB} = 3.3 V ±0.2 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
t_{PHL}	Propagation delay time high-to-low output	A-to-B	Push-pull driving		5.3		5.4		6.8	ns
			Open-drain driving	2.3	8.8	2.4	9.6	2.6	10	
t_{PLH}	Propagation delay time low-to-high output	A-to-B	Push-pull driving		6.8		7.1		7.5	ns
			Open-drain driving	45	260	36	208	27	198	
t_{PHL}	Propagation delay time high-to-low output	B-to-A	Push-pull driving		4.4		4.5		4.7	ns
			Open-drain driving	1.9	5.3	1.1	4.4	1.2	4	
t_{PLH}	Propagation delay time low-to-high output	B-to-A	Push-pull driving		5.3		4.5		0.5	ns
			Open-drain driving	45	175	36	140	27	102	
t_{en}	Enable time	OE-to-A or B			200		200		200	ns
t_{dis}	Disable time	OE-to-A or B			50		40		35	ns
t_{rA}	Input rise time	A port rise time	Push-pull driving	3.2	9.5	2.3	9.3	2	7.6	ns
			Open-drain driving	38	165	30	132	22	95	
t_{rB}	Input rise time	B port rise time	Push-pull driving	4	10.8	2.7	9.1	2.7	7.6	ns
			Open-drain driving	34	145	23	106	10	58	
t_{fA}	Input fall time	A port fall time	Push-pull driving	2	5.9	1.9	6	1.7	13.3	ns
			Open-drain driving	4.4	6.9	4.3	6.4	4.2	6.1	
t_{fB}	Input fall time	B port fall time	Push-pull driving	2.9	13.8	2.8	16.2	2.8	16.2	ns
			Open-drain driving	6.9	13.8	7.5	16.2	7	16.2	
$t_{SK(O)}$	Skew (time), output	Channel -to- channel skew			0.7		0.7		0.7	ns
	Maximum data rate		Push-pull driving	21		22		24		Mbps
			Open-drain driving	2		2		2		

6.10 Switching Characteristics: V_{CCA} = 2.5 V ± 0.2 V

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CCB} = 2.5 V ±0.2 V		V_{CCB} = 3.3 V ±0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
t_{PHL}	Propagation delay time high-to-low output	A-to-B	Push-pull driving		3.2		3.7		3.8	ns
			Open-drain driving	1.7	6.3	2	6	2.1	5.8	
t_{PLH}	Propagation delay time low-to-high output	A-to-B	Push-pull driving		3.5		4.1		4.4	ns
			Open-drain driving	43	250	36	206	27	190	
t_{PHL}	Propagation delay time high-to-low output	B-to-A	Push-pull driving		3		3.6		4.3	ns
			Open-drain driving	1.8	4.7	2.6	4.2	1.2	4	
t_{PLH}	Propagation delay time low-to-high output	B-to-A	Push-pull driving		2.5		1.6		1	ns
			Open-drain driving	44	170	37	140	27	103	
t_{en}	Enable time	OE-to-A or B			200		200		200	ns
t_{dis}	Disable time	OE-to-A or B			50		40		35	ns
t_{rA}	Input rise time	A port rise time	Push-pull driving	2.8	7.4	2.6	6.6	1.8	5.6	ns
			Open-drain driving	3	149	28	121	24	89	
t_{rB}	Input rise time	B port rise time	Push-pull driving	3.2	8.3	2.9	7.2	2.4	6.1	ns
			Open-drain driving	35	151	24	112	12	64	
t_{fA}	Input fall time	A port fall time	Push-pull driving	1.9	5.7	1.9	5.5	1.8	5.3	ns
			Open-drain driving	4.4	6.9	4.3	6.2	4.2	5.8	
t_{fB}	Input fall time	B port fall time	Push-pull driving	2.2	7.8	2.4	6.7	2.6	6.6	ns
			Open-drain driving	5.1	8.8	5.4	9.4	5.4	10.4	
$t_{SK(O)}$	Skew (time), output	Channel-to-channel skew			0.7		0.7		0.7	ns
	Maximum data rate		Push-pull driving	20		22		24		Mbps
			Open-drain driving	2		2		2		

6.11 Switching Characteristics: V_{CCA} = 3.3 V ± 0.3 V

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CCB} = 3.3 V ±0.2 V		V_{CCB} = 5 V ± 0.5 V		UNIT
				MIN	MAX	MIN	MAX	
t_{PHL}	Propagation delay time high-to-low output	A-to-B	Push-pull driving		2.4		3.1	ns
			Open-drain driving	1.3	4.2	1.4	4.6	
t_{PLH}	Propagation delay time low-to-high output	A-to-B	Push-pull driving		4.2		4.4	ns
			Open-drain driving	36	204	28	165	
t_{PHL}	Propagation delay time high-to-low output	B-to-A	Push-pull driving		2.5		3.3	ns
			Open-drain driving	1	124	1	97	
t_{PLH}	Propagation delay time low-to-high output	B-to-A	Push-pull driving		2.5		2.6	ns
			Open-drain driving	3	139	3	105	
t_{en}	Enable time	OE-to-A or B			200		200	ns
t_{dis}	Disable time	OE-to-A or B			40		35	ns
t_{rA}	Input rise time	A port rise time	Push-pull driving	2.3	5.6	1.9	4.8	ns
			Open-drain driving	25	116	19	85	
t_{rB}	Input rise time	B port rise time	Push-pull driving	2.5	6.4	2.1	7.4	ns
			Open-drain driving	26	116	14	72	
t_{fA}	Input fall time	A port fall time	Push-pull driving	2	5.4	1.9	5	ns
			Open-drain driving	4.3	6.1	4.2	5.7	
t_{fB}	Input fall time	B port fall time	Push-pull driving	2.3	7.4	2.4	7.6	ns
			Open-drain driving	5	7.6	4.8	8.3	
$t_{SK(O)}$	Skew (time), output	Channel-to-channel skew			0.7		0.7	ns
	Maximum data rate		Push-pull driving	23		24		Mbps
			Open-drain driving	2		2		

6.12 Typical Characteristics

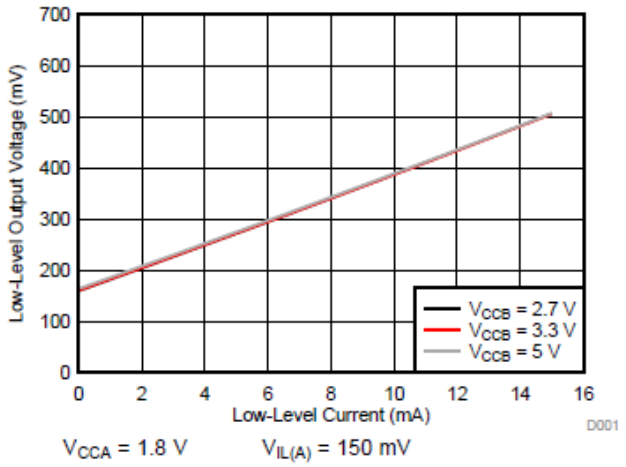


Figure 6-1. Low-Level Output Voltage ($V_{OL(Bx)}$) vs Low-Level Current ($I_{OL(Bx)}$)

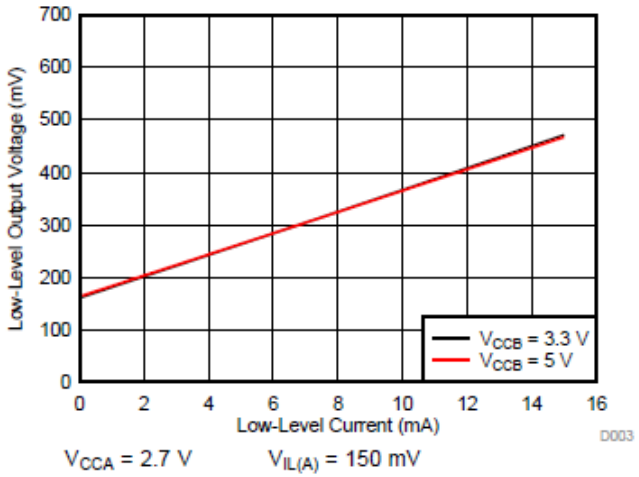


Figure 6-2. Low-Level Output Voltage ($V_{OL(Bx)}$) vs Low-Level Current ($I_{OL(Bx)}$)

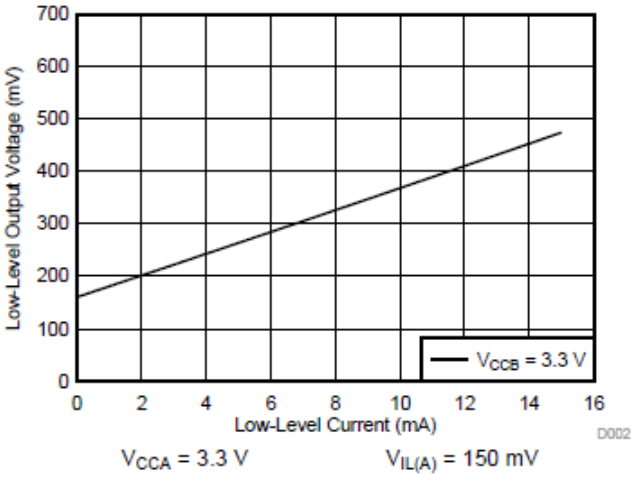


Figure 6-3. Low-Level Output Voltage ($V_{OL(Bx)}$) vs Low-Level Current ($I_{OL(Bx)}$)

7 Parameter Measurement Information

Unless otherwise noted, all input pulses are supplied by generators having the following characteristics:

- PRR 10 MHz
- Z_O = 50 W
- dv/dt ≥ 1 V/ns

Note

All parameters and waveforms are not applicable to all devices.

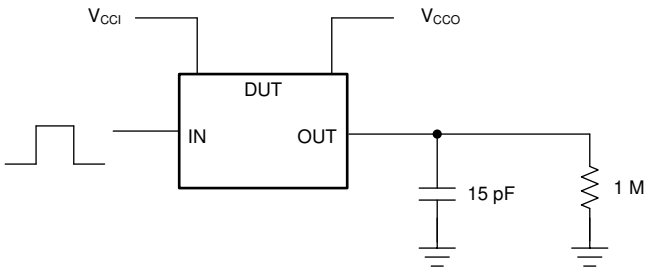


Figure 7-1. Data Rate, Pulse Duration, Propagation Delay, Output Rise And Fall Time Measurement Using A Push-Pull Driver

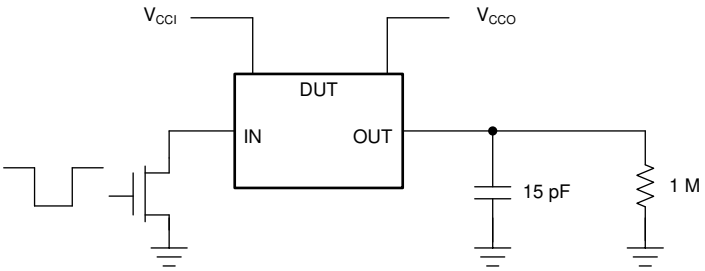


Figure 7-2. Data Rate, Pulse Duration, Propagation Delay, Output Rise And Fall Time Measurement Using An Open-Drain Driver

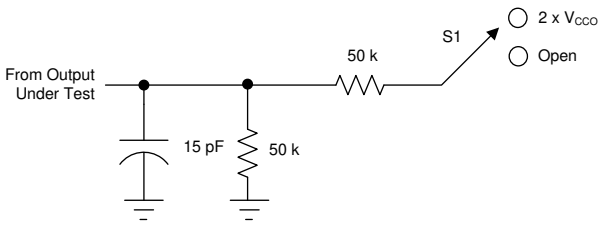
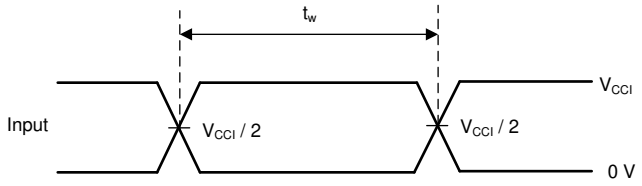


Figure 7-3. Load Circuit For Enable / Disable Time Measurement

Table 7-1. Switch Configuration For Enable / Disable Timing

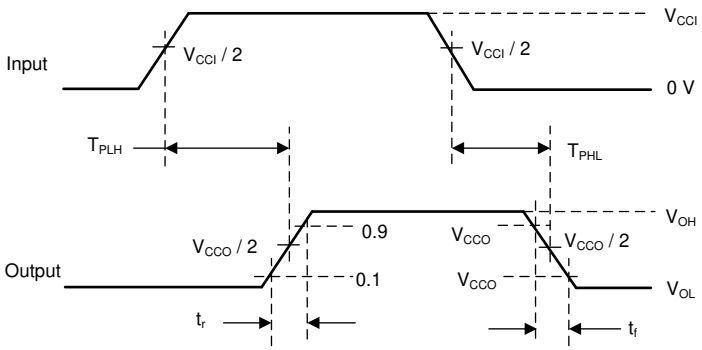
TEST	S1
t_{PZL} (2), t_{PLZ} (1)	2 × V_{CCO}
t_{PHZ} (1), t_{PZH} (2)	Open

(1) t_{PLZ} and t_{PHZ} are the same as t_{dis}.
(2) t_{PZL} and t_{PZH} are the same as t_{en}.



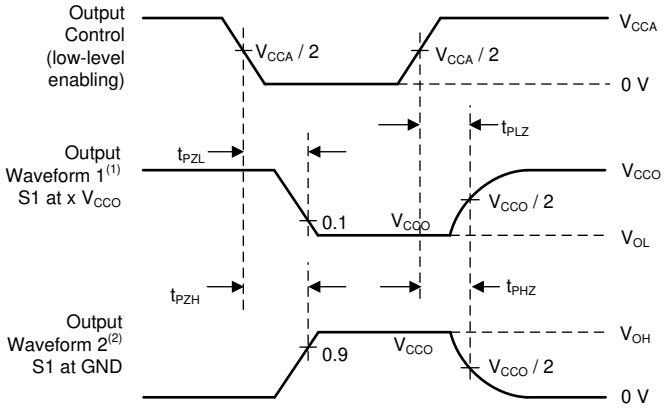
(1) All input pulses are measured one at a time, with one transition per measurement.

Figure 7-4. Voltage Waveforms Pulse Duration



(1) All input pulses are measured one at a time, with one transition per measurement.

Figure 7-5. Voltage Waveforms Propagation Delay Times



(1) Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
(2) Waveform 2 is for an output with internal conditions such that the ouput is high, except when disabled by the output control.

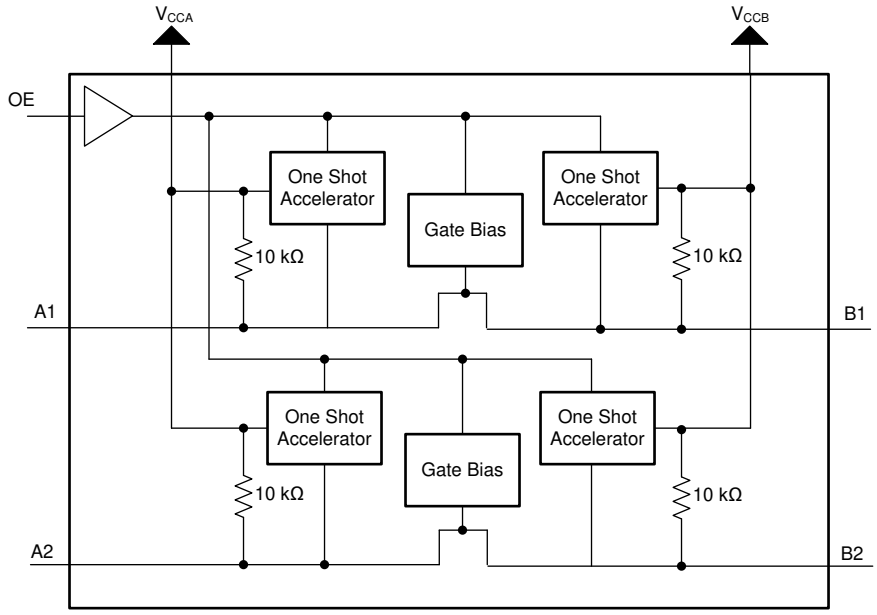
Figure 7-6. Voltage Waveforms Enable And Disable Times

8 Detailed Description

8.1 Overview

The TXS0102 device is a directionless voltage-level translator specifically designed for translating logic voltage levels. The A port is able to accept I/O voltages ranging from 1.65 V to 3.6 V, while the B port can accept I/O voltages from 2.3 V to 5.5 V. The device is a pass-gate architecture with edge-rate accelerators (one-shots) to improve the overall data rate. 10-kΩ pullup resistors, commonly used in open-drain applications, have been conveniently integrated so that an external resistor is not needed. While this device is designed for open-drain applications, the device can also translate push-pull CMOS logic outputs.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Architecture

The TXS0102 architecture (see Figure 8-1) is an auto-direction-sensing based translator that does not require a direction-control signal to control the direction of data flow from A to B or from B to A.

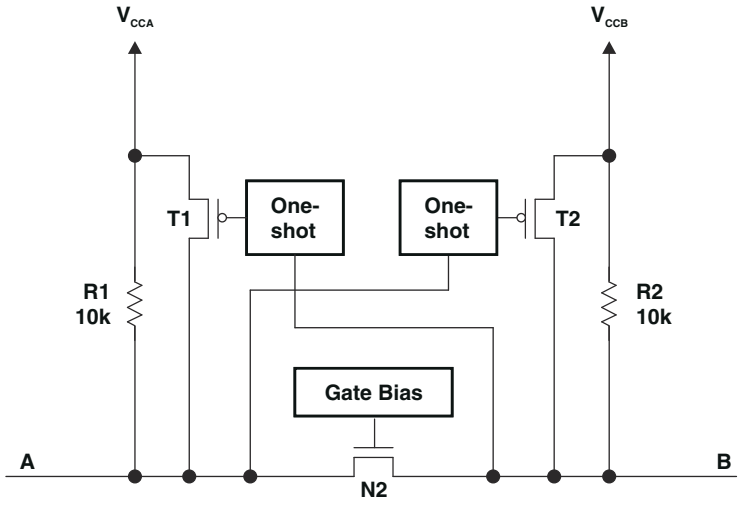


Figure 8-1. Architecture of a TXS0102 Cell

These two bidirectional channels independently determine the direction of data flow without a direction-control signal. Each I/O pin can be automatically reconfigured as either an input or an output, which is how this auto-direction feature is realized.

The TXS0102 device is part of TI's "Switch" type voltage translator family and employs two key circuits to enable this voltage translation:

1. An N-channel pass-gate transistor topology that ties the A-port to the B-port

   and
2. Output one-shot (O.S.) edge-rate accelerator circuitry to detect and accelerate rising edges on the A or B ports

For bidirectional voltage translation, pull-up resistors are included on the device for dc current sourcing capability. The V_{GATE} gate bias of the N-channel pass transistor is set at approximately one threshold voltage (V_T) above the V_{CC} level of the low-voltage side. Data can flow in either direction without guidance from a control signal.

The O.S. rising-edge rate accelerator circuitry speeds up the output slew rate by monitoring the input edge for transitions, helping maintain the data rate through the device. During a low-to-high signal rising edge, the O.S. circuits turn on the PMOS transistors (T1, T2) to increase the current drive capability of the driver for approximately 30 ns or 95% of the input edge, whichever occurs first. This edge-rate acceleration provides high ac drive by bypassing the internal 10-kΩ pull-up resistors during the low-to-high transition to speed up the signal. The output resistance of the driver is decreased to approximately 50 Ω to 70 Ω during this acceleration phase. To minimize dynamic I_{CC} and the possibility of signal contention, the user should wait for the O.S. circuit to turn off before applying a signal in the opposite direction. The worst-case duration is equal to the minimum pulse-width number provided in the *Timing Requirements* section of this data sheet.

8.3.2 Input Driver Requirements

The continuous dc-current *sinking* capability is determined by the external system-level open-drain (or push-pull) drivers that are interfaced to the TXS0102 I/O pins. Since the high bandwidth of these bidirectional I/O circuits is used to facilitate this fast change from an input to an output and an output to an input, they have a modest dc-current *sourcing* capability of hundreds of micro-Amps, as determined by the internal 10-kΩ pullup resistors.

The fall time (t_{fA}, t_{fB}) of a signal depends on the edge-rate and output impedance of the external device driving TXS0102 data I/Os, as well as the capacitive loading on the data lines.

Similarly, the t_{PHL} and max data rates also depend on the output impedance of the external driver. The values for t_{fA}, t_{fB}, t_{PHL}, and maximum data rates in the data sheet assume that the output impedance of the external driver is less than 50 Ω.

8.3.3 Output Load Considerations

TI recommends careful PCB layout practices with short PCB trace lengths to avoid excessive capacitive loading and to ensure that proper O.S. triggering takes place. PCB signal trace-lengths should be kept short enough such that the round trip delay of any reflection is less than the one-shot duration. This improves signal integrity by ensuring that any reflection sees a low impedance at the driver. The O.S. circuits have been designed to stay on for approximately 30 ns. The maximum capacitance of the lumped load that can be driven also depends directly on the one-shot duration. With very heavy capacitive loads, the one-shot can time-out before the signal is driven fully to the positive rail. The O.S. duration has been set to best optimize trade-offs between dynamic ICC, load driving capability, and maximum bit-rate considerations. Both PCB trace length and connectors add to the capacitance that the TXS0102 device output sees, so it is recommended that this lumped-load capacitance be considered to avoid O.S. retriggering, bus contention, output signal oscillations, or other adverse system-level affects.

8.3.4 Enable and Disable

The TXS0102 device has an OE input that is used to disable the device by setting OE low, which places all I/Os in the Hi-Z state. The disable time (t_{dis}) indicates the delay between the time when OE goes low and when the outputs are disabled (Hi-Z). The enable time (t_{en}) indicates the amount of time the user must allow for the one-shot circuitry to become operational after OE is taken high.

8.3.5 Pullup or Pulldown Resistors on I/O Lines

Each A-port I/O has an internal 10-kΩ pullup resistor to V_{CCA}, and each B-port I/O has an internal 10-kΩ pullup resistor to V_{CCB}. If a smaller value of pullup resistor is required, an external resistor must be added from the I/O to V_{CCA} or V_{CCB} (in parallel with the internal 10-kΩ resistors). Adding lower value pull-up resistors will effect V_{OL} levels, however. The internal pull-ups of the TXS0102 are disabled when the OE pin is low.

8.4 Device Functional Modes

The device has two functional modes, enabled and disabled. To disable the device set the OE input low, which places all I/Os in a high impedance state. Setting the OE input high will enable the device.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TXS0102 device can be used to bridge the digital-switching compatibility gap between two voltage nodes to successfully interface logic threshold levels found in electronic systems. It should be used in a point-to-point topology for interfacing devices or systems operating at different interface voltages with one another. Its primary target application use is for interfacing with open-drain drivers on the data I/Os such as I^2C or 1-wire, where the data is bidirectional and no control signal is available. The device can also be used in applications where a push-pull driver is connected to the data I/Os, but the TXB0102 might be a better option for such push-pull applications.

9.2 Typical Application

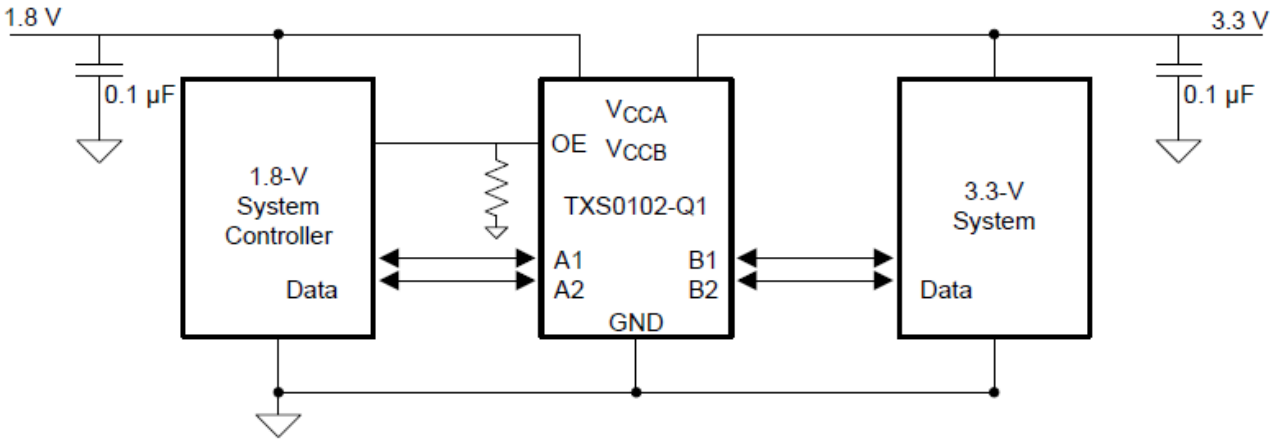


Figure 9-1. Typical Application Circuit

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 9-1. And make sure the $V_{CCA} \leq V_{CCB}$.

Table 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	1.65 to 3.6 V
Output voltage range	2.3 to 5.5 V

9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

• Input voltage range

- Use the supply voltage of the device that is driving the TXS0102 device to determine the input voltage range. For a valid logic high the value must exceed the VIH of the input port. For a valid logic low the value must be less than the VIL of the input port.

• Output voltage range

- Use the supply voltage of the device that the TXS0102 device is driving to determine the output voltage range.

- The TXS0102 device has 10-kΩ internal pullup resistors. External pullup resistors can be added to reduce the total RC of a signal trace if necessary.

• An external pull down resistor decreases the output VOH and VOL. Use Equation 1 to calculate the VOH as a result of an external pull down resistor.

$V_{OH} = V_{CCx} \times R_{PD} / (R_{PD} + 10\ k\Omega)$

Where:

• V_{CCx} is the supply voltage on either V_{CCA} or V_{CCB}

• R_{PD} is the value of the external pull down resistor

9.2.3 Application Curves

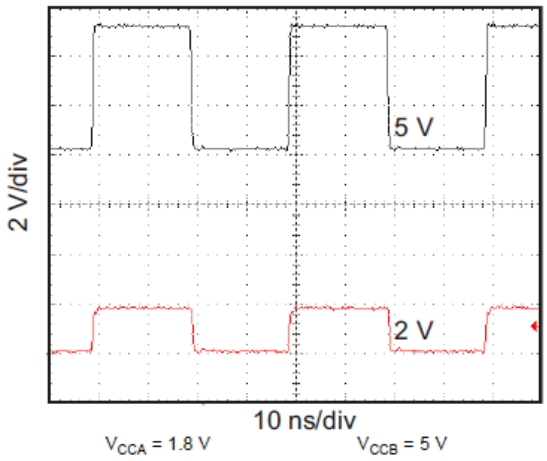


Figure 9-2. Level-Translation of a 2.5-MHz Signal

9.3 Power Supply Recommendations

During operation, ensure that $V_{CCA} \leq V_{CCB}$ at all times. The sequencing of each power supply will not damage the device during the power up operation, so either power supply can be ramped up first. The output-enable (OE) input circuit is designed so that it is supplied by V_{CCA} and when the (OE) input is low, all outputs are placed in the high-impedance state. To ensure the high-impedance state of the outputs during power up or power down, the OE input pin must be tied to GND through a pulldown resistor and must not be enabled until V_{CCA} and V_{CCB} are fully ramped and stable. The minimum value of the pulldown resistor to ground is determined by the current-sourcing capability of the driver.

9.4 Layout

9.4.1 Layout Guidelines

To ensure reliability of the device, the following common printed-circuit board layout guidelines are recommended:

- Bypass capacitors should be used on power supplies and should be placed as close as possible to the V_{CCA}, V_{CCB} pin, and G_{ND} pin.
- Short trace lengths should be used to avoid excessive loading.
- PCB signal trace-lengths must be kept short enough so that the round-trip delay of any reflection is less than the one-shot duration, approximately 30 ns, ensuring that any reflection encounters low impedance at the source driver.

9.4.2 Layout Example

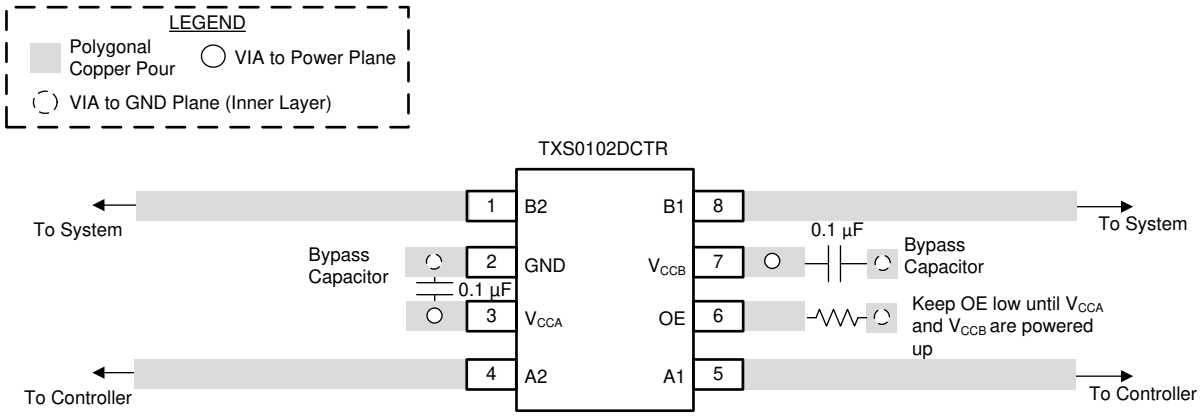


Figure 9-3. TXS0102 Layout Example

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *A Guide to Voltage Translation With TXS-Type Translators* application note
- Texas Instruments, *Factors Affecting VOL for TXS and LSF Auto-bidirectional Translation Devices* application note
- Texas Instruments, *Biasing Requirements for TXS, TXB, and LSF Auto-Bidirectional Translators* application note
- Texas Instruments, *Effects of pullup and pulldown resistors on TXS and TXB devices* application note
- Texas Instruments, *Introduction to logic* application note
- Texas Instruments, *TI Logic and Linear Products Guide* selection and solution guides
- Texas Instruments, *Washing Machine Solutions Guide* selection and solution guides
- Texas Instruments, *TI Smartphone Solutions Guide* selection and solution guides

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

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TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TXS0102DCTR	ACTIVE	SM8	DCT	8	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(35UT, NFE) (R, Z)	Samples
TXS0102DCTRE4	ACTIVE	SM8	DCT	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(35UT, NFE) (R, Z)	Samples
TXS0102DCTT	ACTIVE	SM8	DCT	8	250	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(35UT, NFE) (R, Z)	Samples
TXS0102DCTTE4	ACTIVE	SM8	DCT	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(35UT, NFE) (R, Z)	Samples
TXS0102DCTTG4	ACTIVE	SM8	DCT	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(35UT, NFE) (R, Z)	Samples
TXS0102DCUR	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(FE, NFEQ, NFER) NZ	Samples
TXS0102DCURG4	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NFER	Samples
TXS0102DCUT	ACTIVE	VSSOP	DCU	8	250	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(FE, NFEQ, NFER) NZ	Samples
TXS0102DCUTG4	ACTIVE	VSSOP	DCU	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NFER	Samples
TXS0102DQER	ACTIVE	X2SON	DQE	8	5000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	2H	Samples
TXS0102DQMR	ACTIVE	X2SON	DQM	8	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	2H (2H7, 2HR) (2HG, 2HH)	Samples
TXS0102YZPR	ACTIVE	DSBGA	YZP	8	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(2H, 2HN)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TXS0102 :

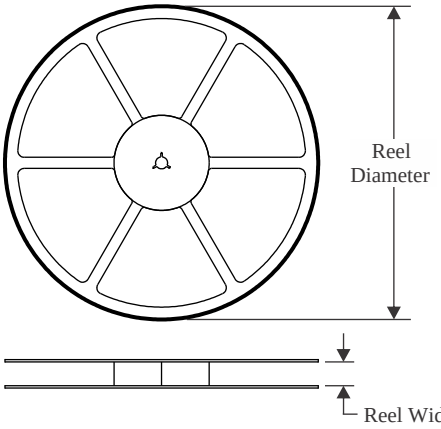
- Automotive : TXS0102-Q1

NOTE: Qualified Version Definitions:

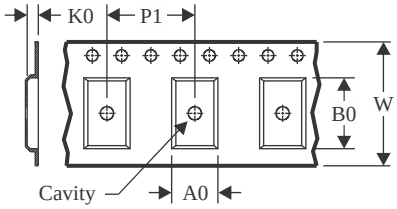
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

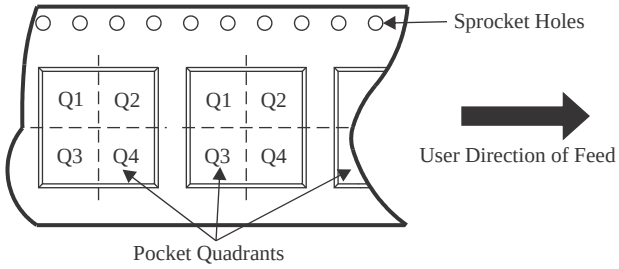


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

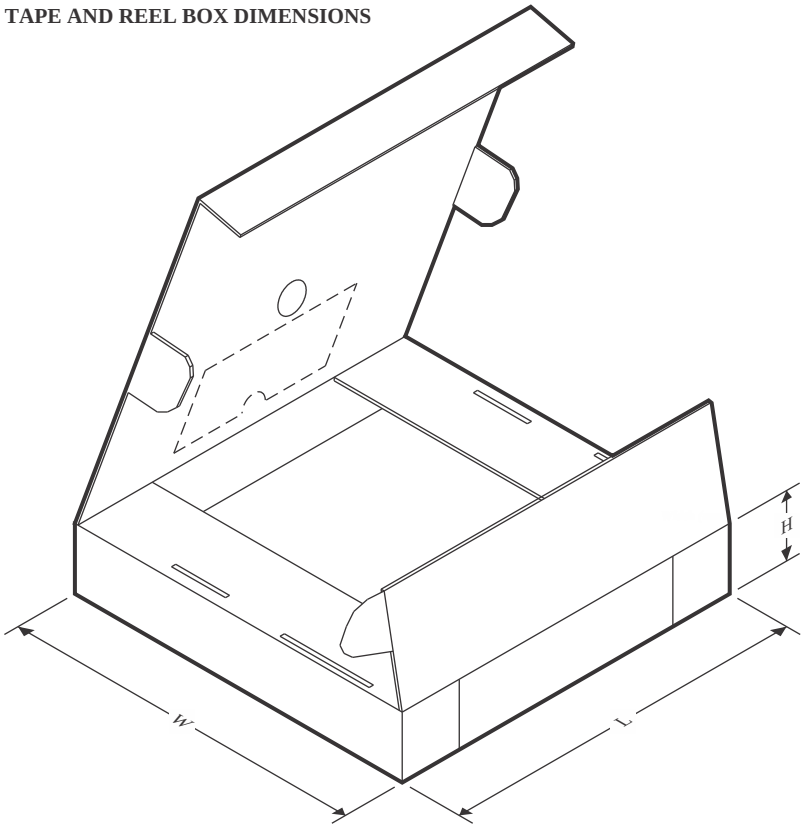
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXS0102DCTR	SM8	DCT	8	3000	180.0	12.4	3.15	4.35	1.55	4.0	12.0	Q3
TXS0102DCTRE4	SM8	DCT	8	3000	177.8	12.4	3.45	4.4	1.45	4.0	12.0	Q3
TXS0102DCTT	SM8	DCT	8	250	180.0	12.4	3.15	4.35	1.55	4.0	12.0	Q3
TXS0102DCUR	VSSOP	DCU	8	3000	180.0	9.0	2.25	3.4	1.0	4.0	8.0	Q3
TXS0102DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
TXS0102DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
TXS0102DCUTG4	VSSOP	DCU	8	250	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
TXS0102DQER	X2SON	DQE	8	5000	180.0	8.4	1.2	1.6	0.55	4.0	8.0	Q1
TXS0102DQMR	X2SON	DQM	8	3000	180.0	9.5	1.4	2.0	0.5	4.0	8.0	Q1
TXS0102DQMR	X2SON	DQM	8	3000	180.0	8.4	1.57	2.21	0.59	4.0	8.0	Q1
TXS0102YZPR	DSBGA	YZP	8	3000	180.0	8.4	1.02	2.02	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

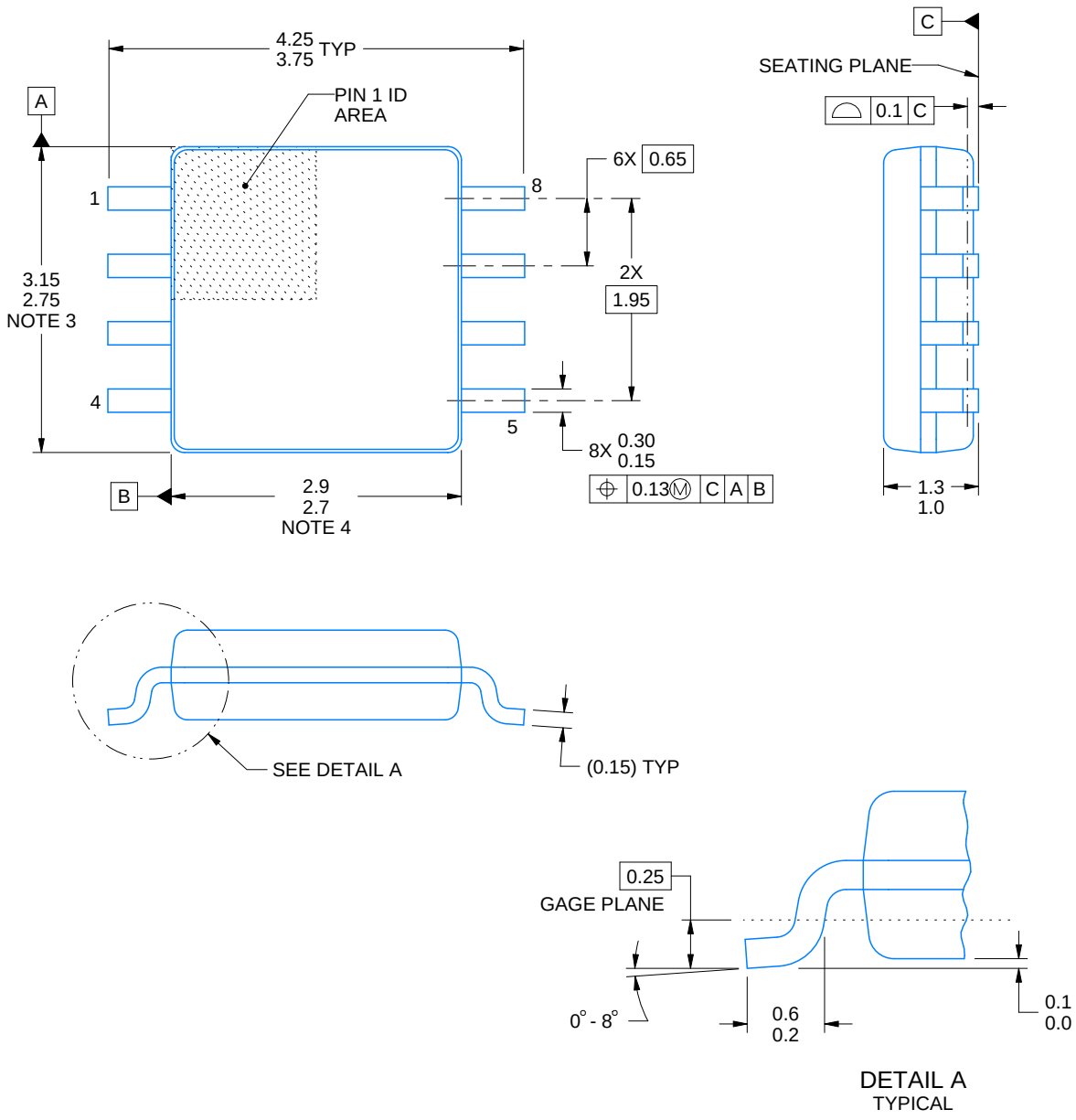
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXS0102DCTR	SM8	DCT	8	3000	190.0	190.0	30.0
TXS0102DCTRE4	SM8	DCT	8	3000	183.0	183.0	20.0
TXS0102DCTT	SM8	DCT	8	250	190.0	190.0	30.0
TXS0102DCUR	VSSOP	DCU	8	3000	182.0	182.0	20.0
TXS0102DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
TXS0102DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0
TXS0102DCUTG4	VSSOP	DCU	8	250	202.0	201.0	28.0
TXS0102DQER	X2SON	DQE	8	5000	202.0	201.0	28.0
TXS0102DQMR	X2SON	DQM	8	3000	184.0	184.0	19.0
TXS0102DQMR	X2SON	DQM	8	3000	202.0	201.0	28.0
TXS0102YZPR	DSBGA	YZP	8	3000	182.0	182.0	20.0

PACKAGE OUTLINE

DCT0008A

SSOP - 1.3 mm max height

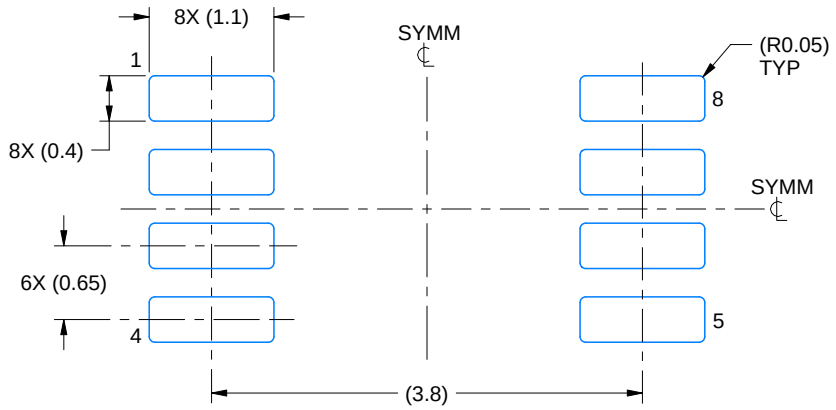
SMALL OUTLINE PACKAGE



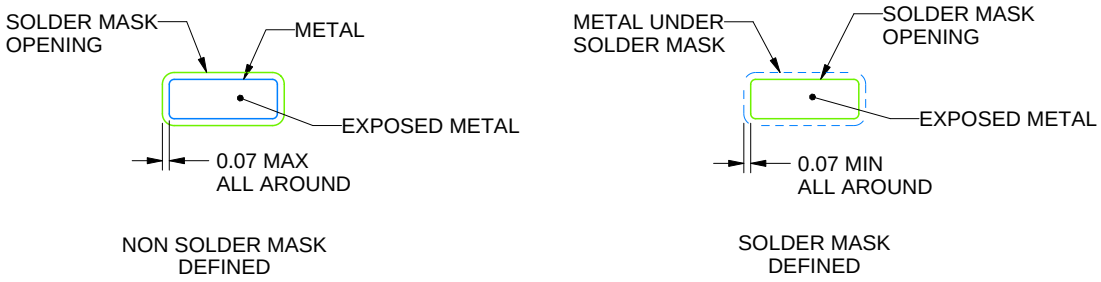
4220784/C 06/2021

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

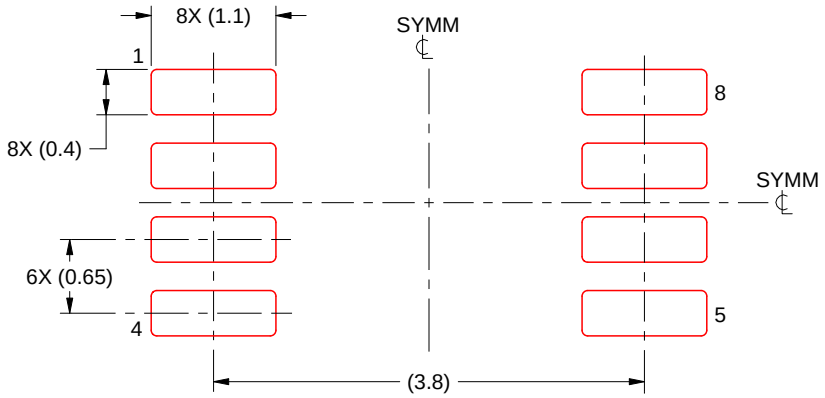


SOLDER MASK DETAILS

4220784/C 06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



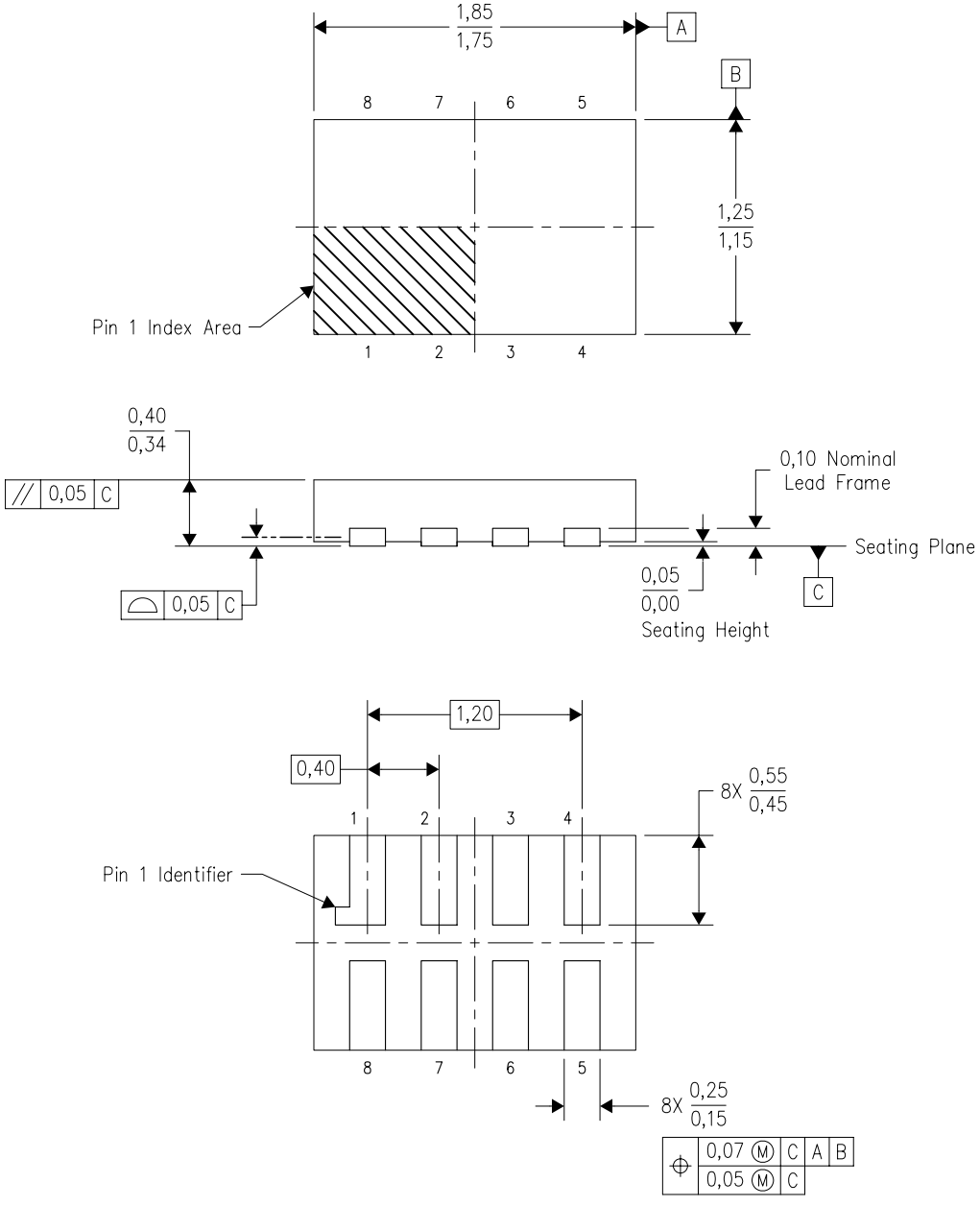
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4220784/C 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DQM (R–PX2SON–N8) PLASTIC SMALL OUTLINE NO–LEAD

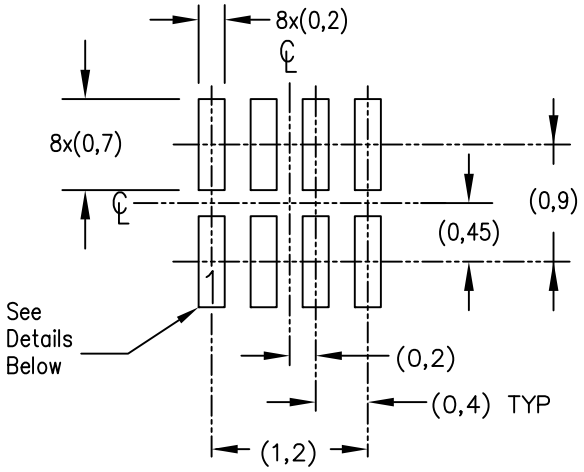


4210302/A 06/2009

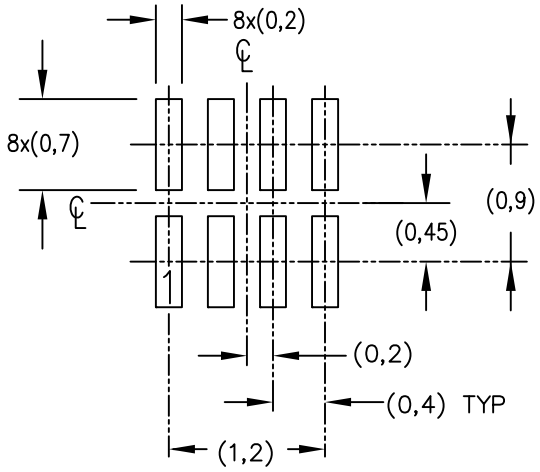
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.

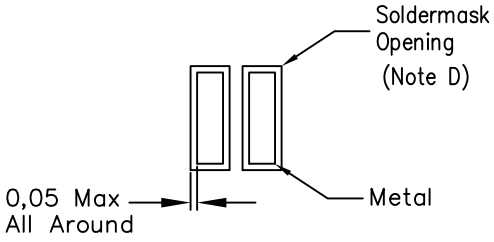
DQM (R–PX2SON–N8) PLASTIC SMALL OUTLINE NO–LEAD

Example Board Layout

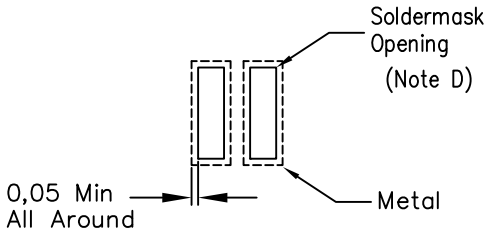


Example Stencil Design
0.1mm Thick Stencil
(Note C)





Non Solder Mask Defined Pad



Solder Mask Defined Pad

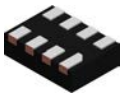
Solder Mask Details

4218746/A 07/13

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
D. Customers should contact their board fabrication site for recommended solder mask tolerances.

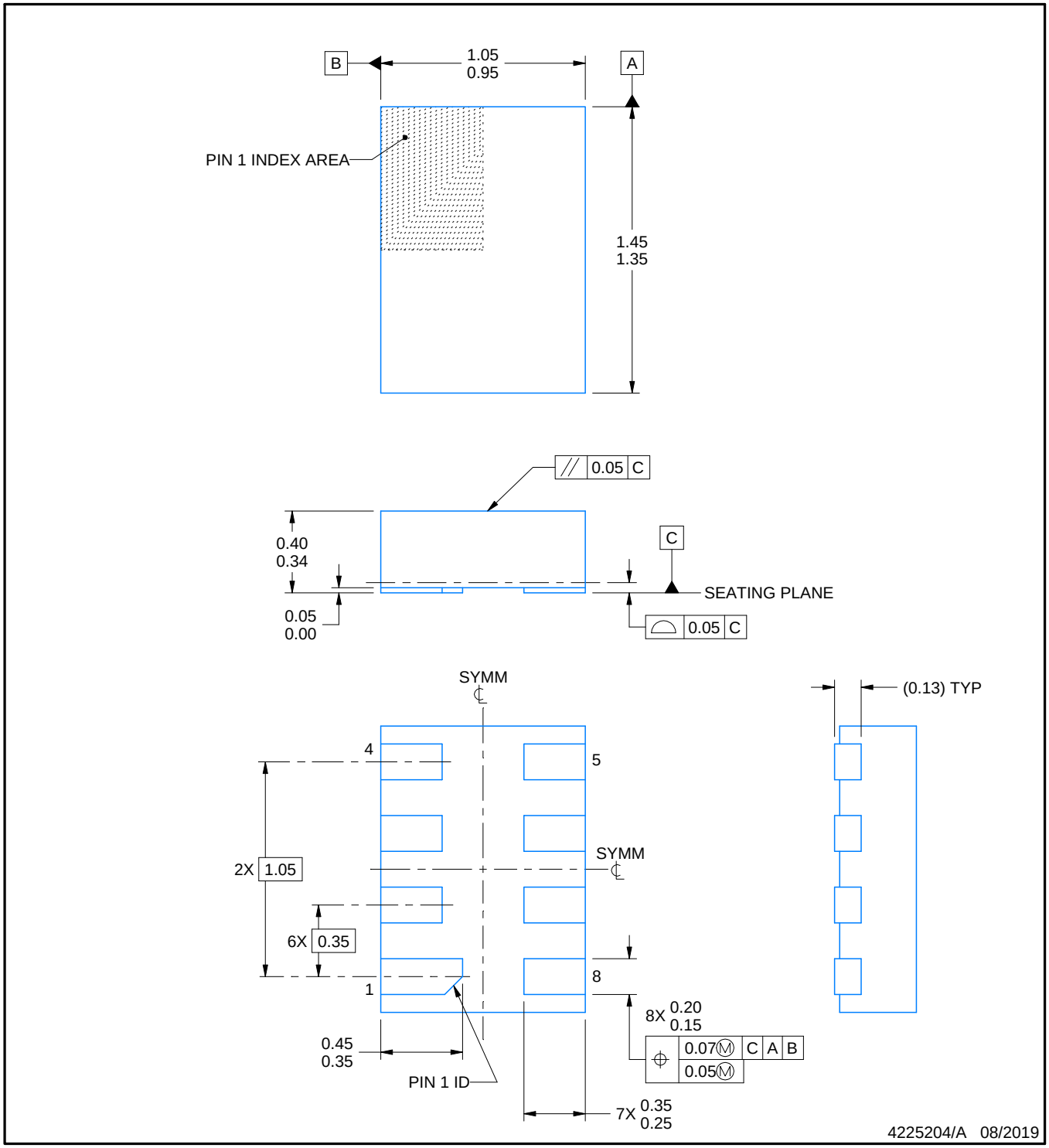
PACKAGE OUTLINE

DQE0008A



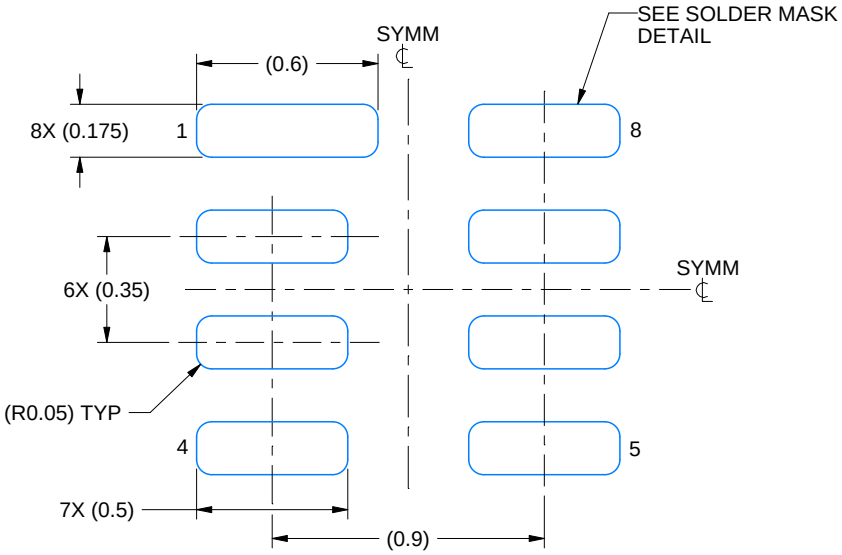
X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

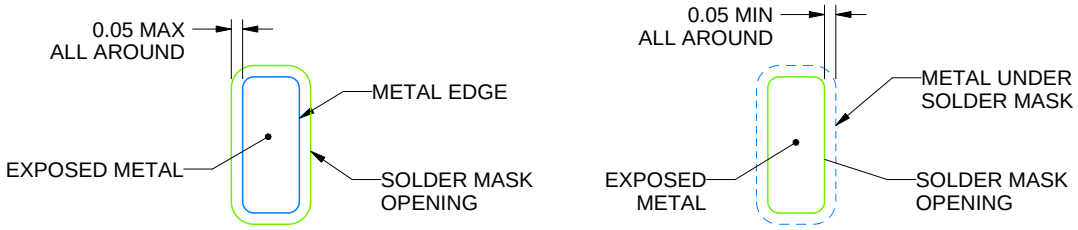


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package complies to JEDEC MO-287 variation X2EAF.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 40X

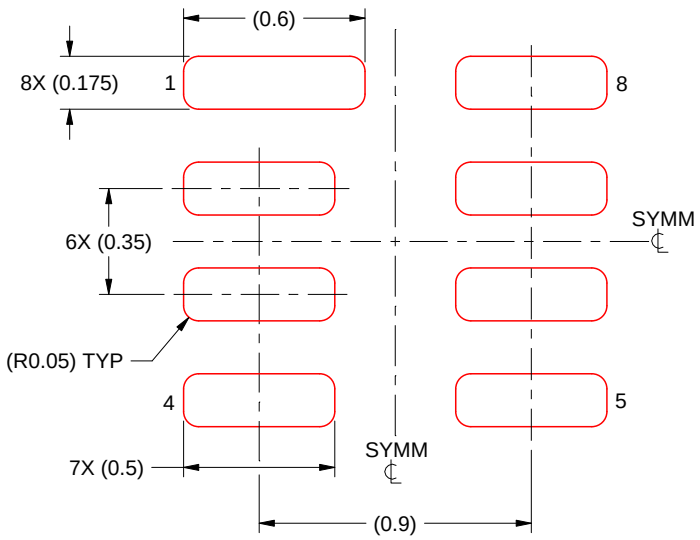


SOLDER MASK DETAILS

4225204/A 08/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.075 MM THICK STENCIL
SCALE: 40X

4225204/A 08/2019

NOTES: (continued)

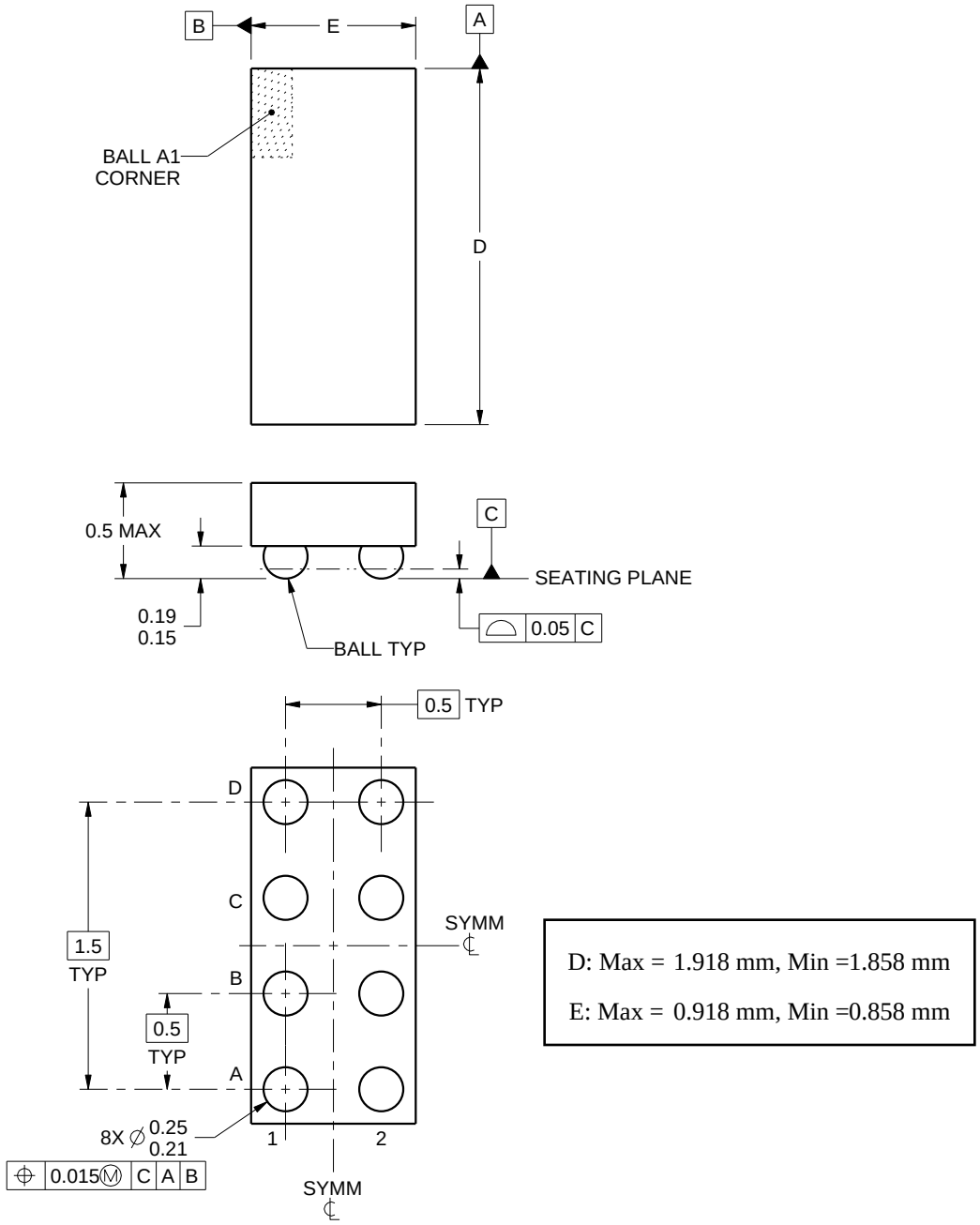
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

YZP0008

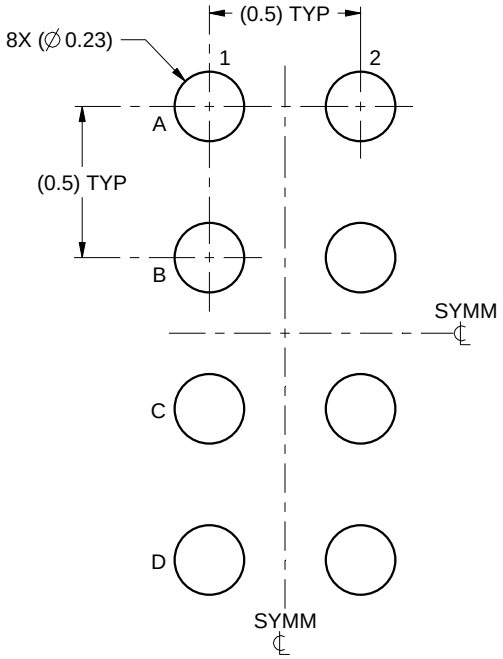
DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY

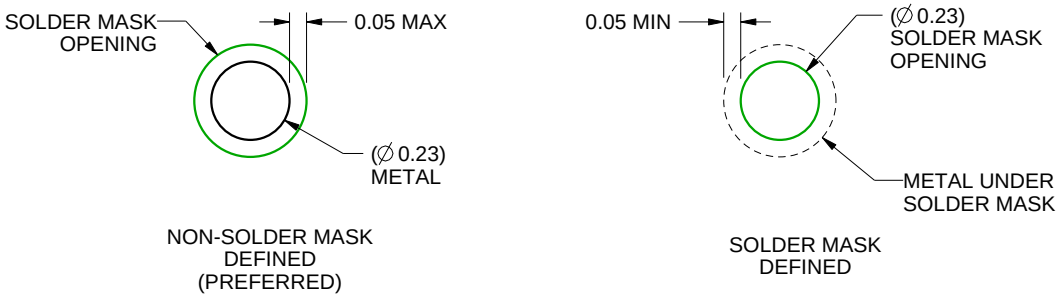


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X

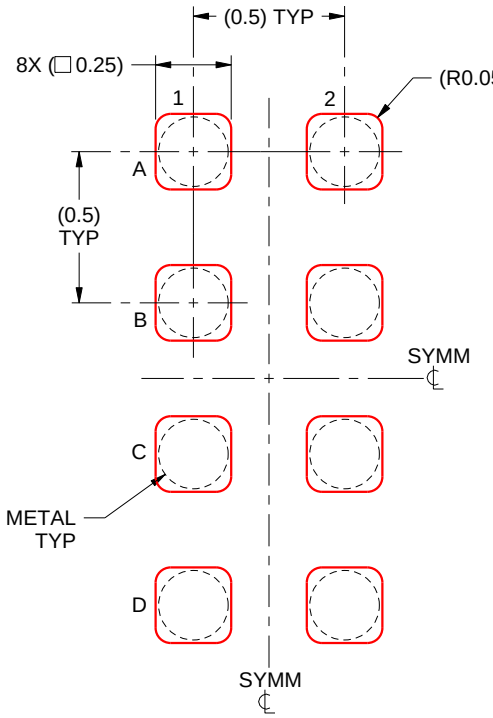


SOLDER MASK DETAILS
NOT TO SCALE

4223082/A 07/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4223082/A 07/2016

NOTES: (continued)

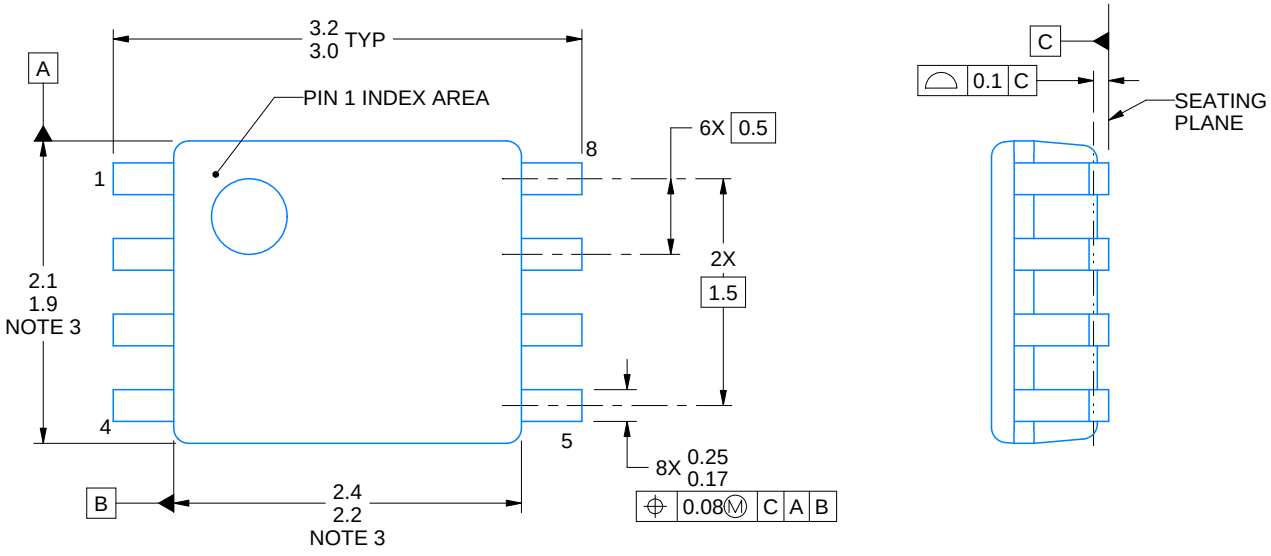
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

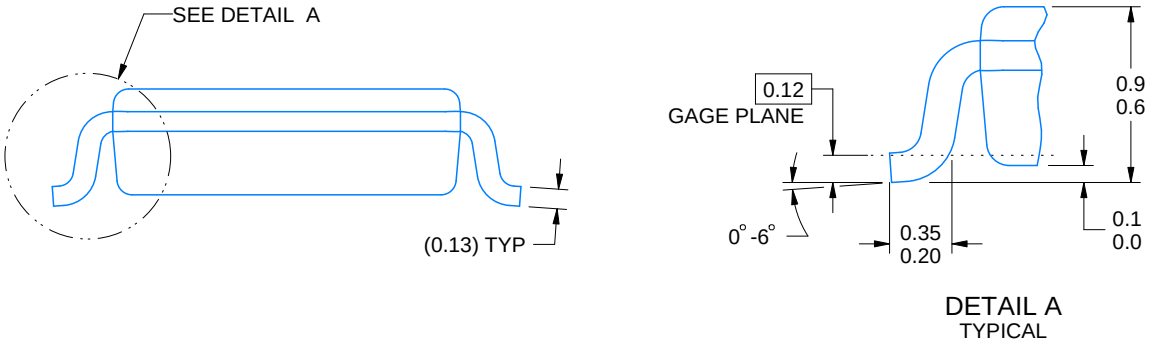
DCU0008A

PACKAGE OUTLINE

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE

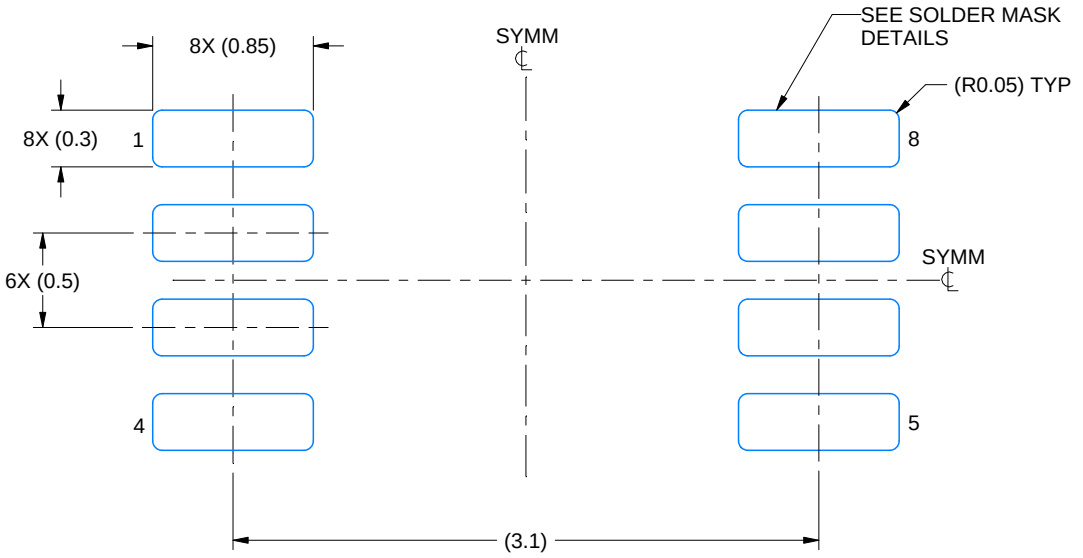




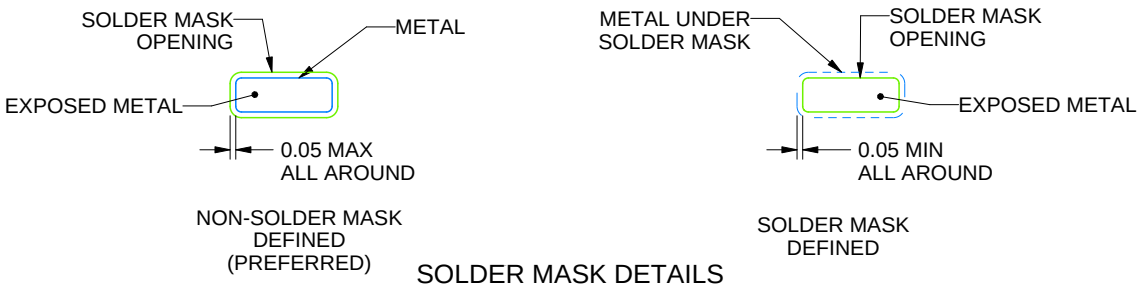
4225266/A 09/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

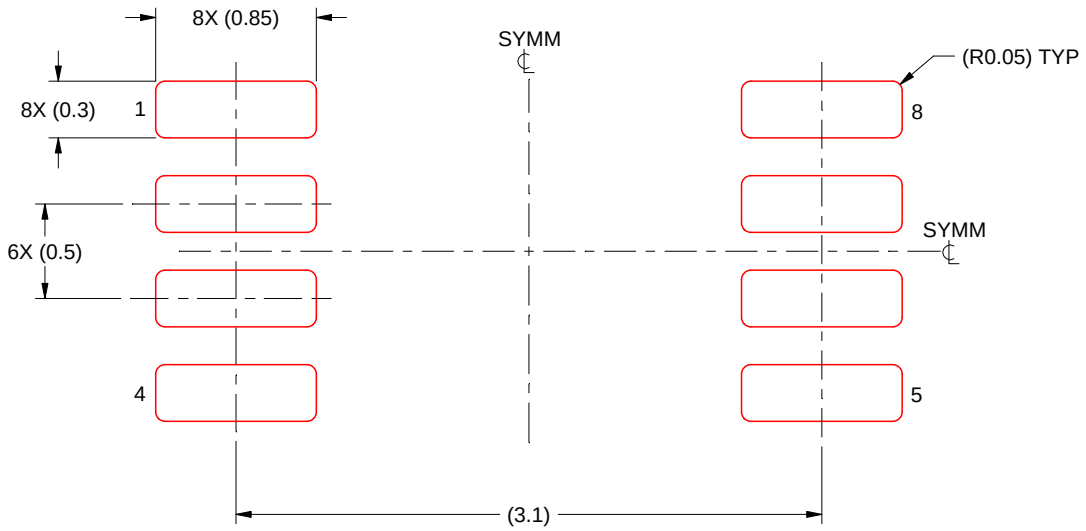


SOLDER MASK DETAILS

4225266/A 09/2014

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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