

# 3.3 V AnyLevel™ Receiver to CML Driver/Translator with Input Hysteresis

2.0 GHz Clock / 2.5 Gb/s Data

## NB4N316M

The NB4N316M is a differential Clock or Data receiver and will accept AnyLevel input signals: LVPECL, CML, LVCMOS, LVTTTL, or LVDS. These signals will be translated to CML, operating up to 2.0 GHz or 2.5 Gb/s, respectively. As such, the NB4N316M is ideal for SONET, GigE, Fiber Channel, Backplane and other Clock or Data distribution applications. The CML outputs are 16 mA open collector (see Figure 18) which requires resistor ( $R_L$ ) load path to  $V_{TT}$  termination voltage (see Figure 19). The open collector CML outputs must be terminated to  $V_{TT}$  at power up. The differential outputs produce Current-Mode Logic (CML) compatible levels when the receiver is loaded with 50  $\Omega$  or 25  $\Omega$  loads connected to 1.8 V, 2.5 V or 3.3 V supplies. This simplifies device interface by eliminating a need for coupling capacitors.

The NB4N316M features an input threshold hysteresis of approximately 25 mV, providing increased noise immunity and stability.

The device is offered in a small 8-pin TSSOP package (MSOP-8 compatible). Application notes, models, and support documentation are available at [www.onsemi.com](http://www.onsemi.com).

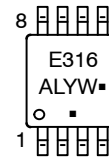
### Features

- Maximum Input Clock Frequency > 2.0 GHz
- Maximum Input Data Rate > 2.5 Gb/s
- Typically 1 ps of RMS Clock Jitter
- Typically 10 ps of Data Dependent Jitter
- 550 ps Typical Propagation Delay
- 150 ps Typical Rise and Fall Times
- Differential CML Outputs
- 25 mV of Receiver Input Threshold Hysteresis
- Operating Range:  $V_{CC} = 3.0\text{ V to }3.6\text{ V}$  with  $V_{EE} = 0\text{ V}$  and  $V_{TT} = 1.8\text{ V to }3.6\text{ V}$
- Functionally Compatible with Existing 2.5 V / 3.3 V LVEL, LVEP, EP, and SG Devices
- -40°C to +85°C Ambient Operating Temperature
- These are Pb-Free Devices\*



TSSOP-8  
DT SUFFIX  
CASE 948R

### MARKING DIAGRAM\*



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\*For additional marking information, refer to Application Note AND8002/D.

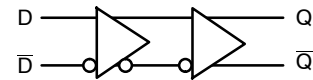


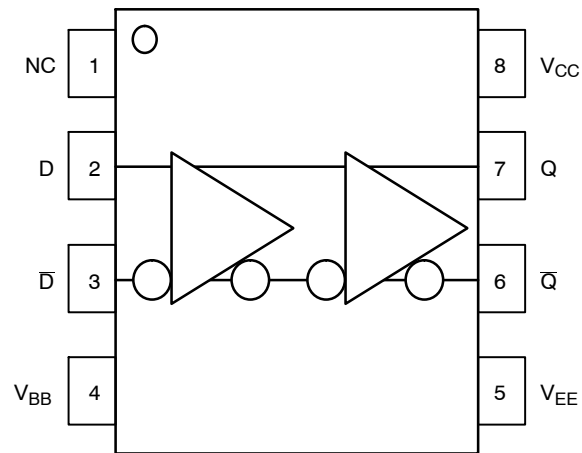
Figure 1. Functional Block Diagram

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

\*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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**Figure 2. Pinout (Top View) and Logic Diagram**

**Table 1. Pin Description**

| Pin | Name      | I/O                                  | Description   |
|-----|-----------|--------------------------------------|---|
| 1   | NC        | -                                    | No Connect.   |
| 2   | D         | ECL, CML, LVCMOS, LVDS, LVTTTL Input | Noninverted Differential Input. (Note 1)  |
| 3   | $\bar{D}$ | ECL, CML, LVCMOS, LVDS, LVTTTL Input | Inverted Differential Input. (Note 1)   |
| 4   | $V_{BB}$  | -                                    | Internally Generated Reference Voltage Supply.  |
| 5   | $V_{EE}$  | -                                    | Negative Supply Voltage.  |
| 6   | $\bar{Q}$ | CML Output                           | Inverted Differential Output. Typically Terminated with 50 $\Omega$ Resistor to $V_{TT}$ .    |
| 7   | Q         | CML Output                           | Noninverted Differential Output. Typically Terminated with 50 $\Omega$ Resistor to $V_{TT}$ . |
| 8   | $V_{CC}$  | -                                    | Positive Supply Voltage.  |

1. In the differential configuration if no signal is applied on D/ $\bar{D}$  input, then the device will be susceptible to self-oscillation.

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**Table 2. ATTRIBUTES**

| Characteristics  |                                   | Value                |
|--|-----------------------------------|----------------------|
| ESD Protection   | Human Body Model<br>Machine Model | > 1000 V<br>> 70 V   |
| Moisture Sensitivity (Note 1)                          | 8-TSSOP                           | Level 3              |
| Flammability Rating                                    | Oxygen Index: 28 to 34            | UL 94 V-0 @ 0.125 in |
| Transistor Count                                       |                                   | 225                  |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test |                                   |                      |

1. For additional information, see Application Note AND8003/D.

**Table 3. MAXIMUM RATINGS**

| Symbol           | Parameter  | Condition 1                                    | Condition 2  | Rating   | Unit         |
|------------------|--|--|--|--|--------------|
| V <sub>CC</sub>  | Positive Power Supply                                | V <sub>EE</sub> = -0.5 V                       |  | 4  | V            |
| V <sub>EE</sub>  | Negative Power Supply                                | V <sub>CC</sub> = +0.5 V                       |  | -4   | V            |
| V <sub>I</sub>   | Positive Input<br>Negative Input                     | V <sub>EE</sub> = 0 V<br>V <sub>CC</sub> = 0 V | V <sub>I</sub> = V <sub>CC</sub> + 0.4 V<br>V <sub>I</sub> = V <sub>EE</sub> - 0.4 V | 4<br>-4  | V<br>V       |
| V <sub>O</sub>   | Output Voltage<br>Minimum<br>Maximum                 |  |  | V <sub>EE</sub> + 600<br>V <sub>CC</sub> + 400 | mV<br>mV     |
| T <sub>A</sub>   | Operating Temperature Range                          |  |  | -40 to +85                                     | °C           |
| T <sub>stg</sub> | Storage Temperature Range                            |  |  | -65 to +150                                    | °C           |
| θ <sub>JA</sub>  | Thermal Resistance (Junction-to-Ambient)<br>(Note 2) | 0 lfpm<br>500 lfpm                             | TSSOP-8<br>TSSOP-8   | 190<br>130                                     | °C/W<br>°C/W |
| θ <sub>JC</sub>  | Thermal Resistance (Junction-to-Case)                | 1S2P (Note 2)                                  | TSSOP-8  | 41 to 44                                       | °C/W         |
| T <sub>sol</sub> | Wave Solder  | < 3 Sec @ 260°C                                |  | 265  | °C           |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. JEDEC standard multilayer board - 1S2P (1 signal, 2 power) with 8 filled thermal vias under exposed pad.

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**Table 4. DC CHARACTERISTICS, CLOCK Inputs, CML Outputs**  $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ ,  $V_{EE} = 0\text{ V}$ ,  $T_A = -40^\circ\text{C to }+85^\circ\text{C}$

| Symbol   | Characteristic                                 | Min | Typ | Max | Unit |
|----------|--|-----|-----|-----|------|
| $I_{CC}$ | Power Supply Current (Inputs and Outputs Open) |     | 20  | 30  | mA   |

$R_L = 50\ \Omega$ ,  $V_{TT} = 3.6\text{ V to }2.5\text{ V}$

|            |                                       |                 |                |                |    |
|------------|---------------------------------------|-----------------|----------------|----------------|----|
| $V_{OH}$   | Output HIGH Voltage (Note 3)          | $V_{TT} - 60$   | $V_{TT} - 10$  | $V_{TT}$       | mV |
| $V_{OL}$   | Output LOW Voltage (Note 3)           | $V_{TT} - 1100$ | $V_{TT} - 800$ | $V_{TT} - 640$ | mV |
| $ V_{OD} $ | Differential Output Voltage Magnitude | 640             | 780            | 1000           | mV |

$R_L = 25\ \Omega$ ,  $V_{TT} = 3.6\text{ V to }2.5\text{ V} \pm 5\%$

|            |                                       |                |                |                |    |
|------------|---------------------------------------|----------------|----------------|----------------|----|
| $V_{OH}$   | Output HIGH Voltage (Note 3)          | $V_{TT} - 60$  | $V_{TT} - 10$  | $V_{TT}$       | mV |
| $V_{OL}$   | Output LOW Voltage (Note 3)           | $V_{TT} - 550$ | $V_{TT} - 400$ | $V_{TT} - 320$ | mV |
| $ V_{OD} $ | Differential Output Voltage Magnitude | 320            | 390            | 500            | mV |

$R_L = 50\ \Omega$ ,  $V_{TT} = 1.8\text{ V} \pm 5\%$

|            |                                       |                 |                |                |    |
|------------|---------------------------------------|-----------------|----------------|----------------|----|
| $V_{OH}$   | Output HIGH Voltage (Note 3)          | $V_{TT} - 170$  | $V_{TT} - 10$  | $V_{TT}$       | mV |
| $V_{OL}$   | Output LOW Voltage (Note 3)           | $V_{TT} - 1100$ | $V_{TT} - 800$ | $V_{TT} - 640$ | mV |
| $ V_{OD} $ | Differential Output Voltage Magnitude | 570             | 780            | 1000           | mV |

$R_L = 25\ \Omega$ ,  $V_{TT} = 1.8\text{ V} \pm 5\%$

|            |                                       |                |                |                |    |
|------------|---------------------------------------|----------------|----------------|----------------|----|
| $V_{OH}$   | Output HIGH Voltage (Note 3)          | $V_{TT} - 85$  | $V_{TT} - 10$  | $V_{TT}$       | mV |
| $V_{OL}$   | Output LOW Voltage (Note 3)           | $V_{TT} - 500$ | $V_{TT} - 400$ | $V_{TT} - 320$ | mV |
| $ V_{OD} $ | Differential Output Voltage Magnitude | 285            | 390            | 500            | mV |

#### DIFFERENTIAL INPUT DRIVEN SINGLE-ENDED (Figures 14 and 16)

|          |  |                 |                 |                 |    |
|----------|--|-----------------|-----------------|-----------------|----|
| $V_{th}$ | Input Threshold Reference Voltage Range (Note 5)                                 | $V_{EE}$        |                 | $V_{CC}$        | mV |
| $V_{IH}$ | Single-ended Input HIGH Voltage  | $V_{th} + 100$  |                 | $V_{CC} + 400$  | mV |
| $V_{IL}$ | Single-ended Input LOW Voltage   | $V_{EE} - 400$  |                 | $V_{th} - 100$  | mV |
| $V_{BB}$ | Internally Generated Reference Voltage Supply (Loaded with $-100\ \mu\text{A}$ ) | $V_{CC} - 1500$ | $V_{CC} - 1400$ | $V_{CC} - 1300$ | mV |

#### DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figures 15 and 17)

|                |   |                |     |                   |    |
|----------------|---|----------------|-----|-------------------|----|
| $V_{IHD}$      | Differential Input HIGH Voltage   | $V_{EE}$       |     | $V_{CC} + 400$    | mV |
| $V_{ILD}$      | Differential Input LOW Voltage  | $V_{EE} - 400$ |     | $V_{CC} - 100$    | mV |
| $V_{CMR}$      | Input Common Mode Range (Differential Configuration)                    | $V_{EE}$       |     | $V_{CC}$          | mV |
| $V_{ID(HYST)}$ | Differential Input Voltage Hysteresis ( $V_{IHD} - V_{ILD}$ )           |                | 25  |                   | mV |
| $ V_{ID} $     | Differential Input Voltage Magnitude ( $ V_{IHD} - V_{ILD} $ ) (Note 7) | 100            |     | $V_{CC} - V_{EE}$ | mV |
| $C_{IN}$       | Input Capacitance (Note 7)  |                | 1.5 |                   | pF |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm.

- CML outputs require  $R_L$  receiver termination resistors to  $V_{TT}$  for proper operation. Outputs must be connected through  $R_L$  to  $V_{TT}$  at power up. The output parameters vary 1:1 with  $V_{TT}$ .  $V_{TT} = 1.71\text{ V to }3.6\text{ V}$ .
- Input parameters vary 1:1 with  $V_{CC}$ .
- $V_{th}$  is applied to the complementary input when operating in single-ended mode.
- $V_{CMR}$  (MIN) varies 1:1 with  $V_{EE}$ .  $V_{CMR}$  max varies 1:1 with  $V_{CC}$ .
- Parameter guaranteed by design and evaluation but not tested in production.

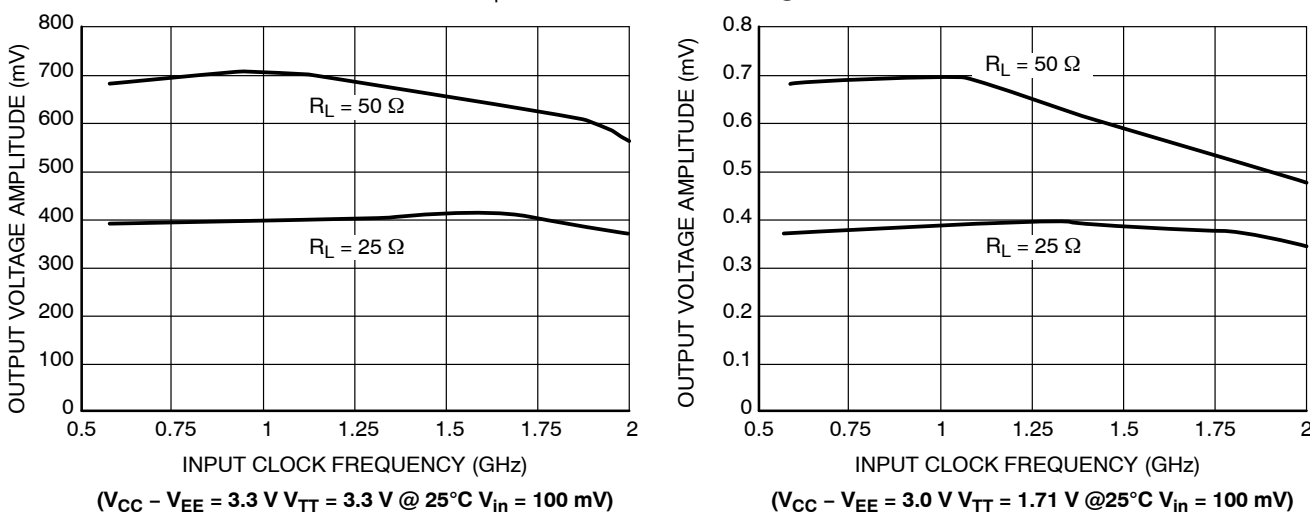
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**Table 5. AC CHARACTERISTICS**  $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ ,  $V_{EE} = 0\text{ V}$ ; (Note 8)

| Symbol                   | Characteristic  | -40°C |             |             | 25°C |             |             | 85°C |             |             | Unit |
|--------------------------|---|-------|-------------|-------------|------|-------------|-------------|------|-------------|-------------|------|
|                          |   | Min   | Typ         | Max         | Min  | Typ         | Max         | Min  | Typ         | Max         |      |
| $V_{OUTPP}$              | Output Voltage Amplitude ( $R_L = 50\ \Omega$ )<br>$f_{in} \leq 1\text{ GHz}$<br>(See Figure 12)<br>$f_{in} \leq 1.5\text{ GHz}$<br>$f_{in} \leq 2.0\text{ GHz}$  | 550   | 660         |             | 550  | 660         |             | 550  | 660         |             | mV   |
| $V_{OUTPP}$              | Output Voltage Amplitude ( $R_L = 25\ \Omega$ )<br>$f_{in} \leq 1\text{ GHz}$<br>(See Figure 12)<br>$f_{in} \leq 1.5\text{ GHz}$<br>$f_{in} \leq 2.0\text{ GHz}$  | 280   | 370         |             | 280  | 370         |             | 280  | 370         |             | mV   |
| $f_{DATA}$               | Maximum Operating Data Rate   | 1.5   | 2.5         |             | 1.5  | 2.5         |             | 1.5  | 2.5         |             | Gb/s |
| $t_{PLH}$ ,<br>$t_{PHL}$ | Propagation Delay to Output Differential<br>@ 0.25 GHz  | 350   | 550         | 750         | 350  | 550         | 750         | 350  | 550         | 750         | ps   |
| $t_{SKEW}$               | Duty Cycle Skew (Note 9)<br>Device to Device Skew (Note 13)   |       | 2<br>20     | 20<br>100   |      | 2<br>20     | 20<br>100   |      | 2<br>20     | 20<br>100   | ps   |
| $t_{JITTER}$             | RMS Random Clock Jitter $R_L = 50\ \Omega$ and<br>$R_L = 25\ \Omega$ (Note 11)<br>$f_{in} = 750\text{ MHz}$<br>$f_{in} = 1.5\text{ GHz}$<br>$f_{in} = 2.0\text{ GHz}$<br>Peak-to-Peak Data Dependent Jitter $R_L = 50\ \Omega$<br>(Note 12)<br>$f_{DATA} = 1.5\text{ Gb/s}$<br>$f_{DATA} = 2.5\text{ Gb/s}$<br>Peak-to-Peak Data Dependent Jitter $R_L = 25\ \Omega$<br>(Note 12)<br>$f_{DATA} = 1.5\text{ Gb/s}$<br>$f_{DATA} = 2.5\text{ Gb/s}$ |       | 1<br>1<br>1 | 3<br>3<br>3 |      | 1<br>1<br>1 | 3<br>3<br>3 |      | 1<br>1<br>1 | 3<br>3<br>3 | ps   |
| $V_{INPP}$               | Input Voltage Swing/Sensitivity<br>(Differential Configuration) (Note 10)   | 200   |             |             | 200  |             |             | 200  |             |             | mV   |
| $t_r$ ,<br>$t_f$         | Output Rise/Fall Times @ 0.25 GHz<br>(20% – 80%)  |       | 150         | 300         |      | 150         | 300         |      | 150         | 300         | ps   |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

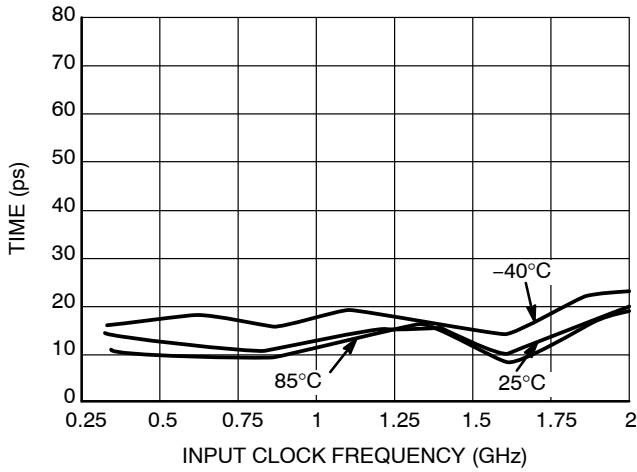
8. Measured by forcing  $V_{INPP}$  (MIN) from a 50% duty cycle clock source. All output loaded with an external  $R_L = 50\ \Omega$  and  $R_L = 25\ \Omega$  to  $V_{TT}$ . Outputs must be connected through  $R_L$  to  $V_{TT}$  at power up. Input edge rates 150 ps (20% – 80%).
9. Duty cycle skew is measured between differential outputs using the deviations of the sum of  $T_{pw-}$  and  $T_{pw+}$  @ 0.25 GHz.
10.  $V_{INPP}$  (MAX) cannot exceed  $V_{CC} - V_{EE}$ . Input voltage swing is a single-ended measurement operating in differential mode.
11. Additive RMS jitter with 50% duty cycle clock signal.
12. Additive peak-to-peak data dependent jitter with input NRZ data signal (PRBS  $2^{23}-1$ ).
13. Device to device skew is measured between outputs under identical transition @ 0.5 GHz.



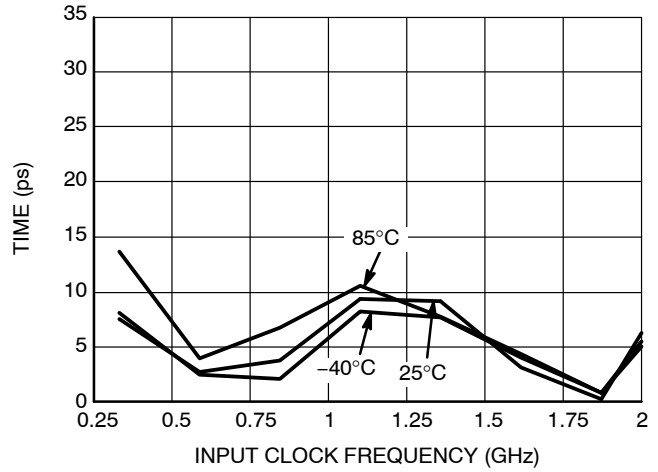
**Figure 3. Output Voltage Amplitude ( $V_{OUTPP}$ ) versus Input Clock Frequency ( $f_{IN}$ ) at Ambient Temperature (Typical)**

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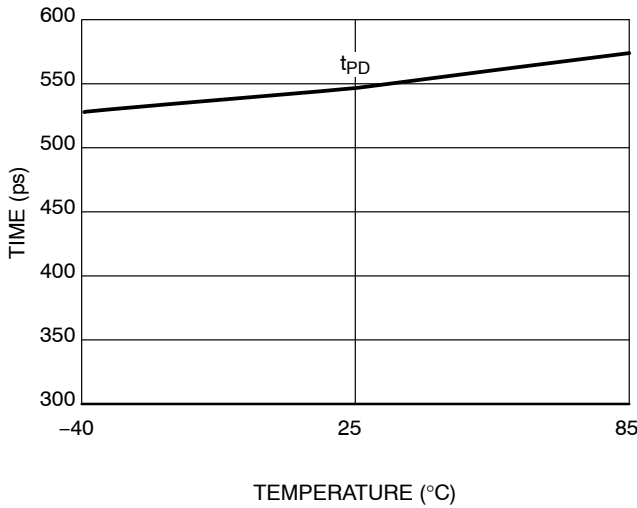
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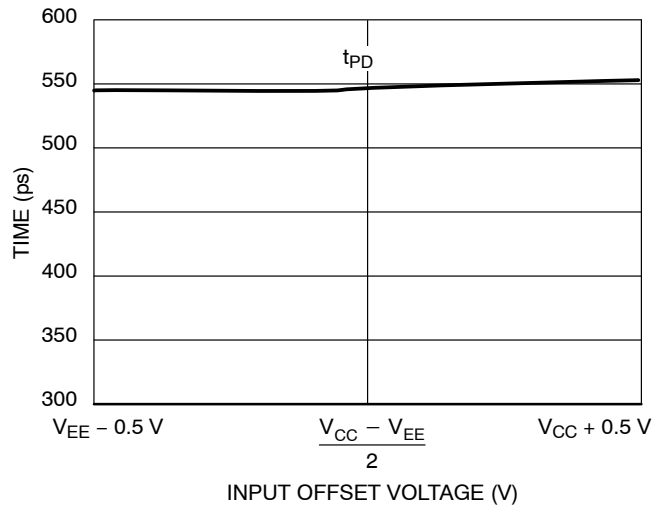
**Figure 4. Data Dependent Jitter vs. Frequency and Temperature** ( $V_{CC} - V_{EE} = 3.3 \text{ V}$ ;  $V_{TT} = 3.3 \text{ V}$  @  $25^\circ\text{C}$ ;  $V_{IN} = 100 \text{ mV}$ ; PRBS  $2^{23}-1$ ;  $R_L = 50 \Omega$ )



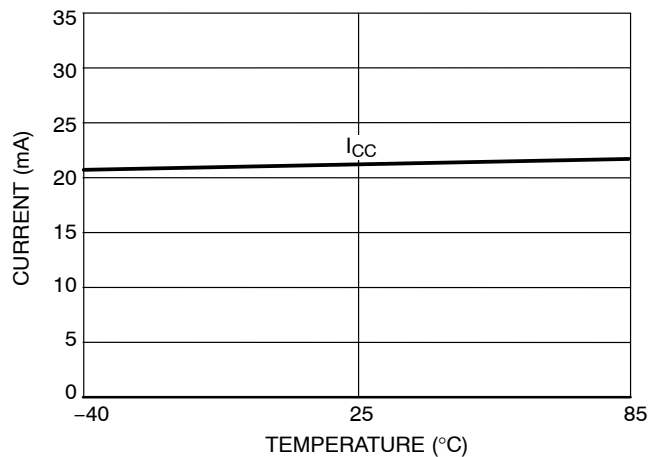
**Figure 5. Data Dependent Jitter vs. Frequency and Temperature** ( $V_{CC} - V_{EE} = 3.3 \text{ V}$ ;  $V_{TT} = 3.3 \text{ V}$  @  $25^\circ\text{C}$ ;  $V_{IN} = 100 \text{ mV}$ ; PRBS  $2^{23}-1$ ;  $R_L = 25 \Omega$ )



**Figure 6. Typical Propagation Delay vs. Temperature** ( $V_{CC} - V_{EE} = 3.3 \text{ V}$ ;  $V_{TT} = 3.3 \text{ V}$  @  $25^\circ\text{C}$ ;  $V_{in} = 100 \text{ mV}$ ;  $R_L = 50 \Omega$ )

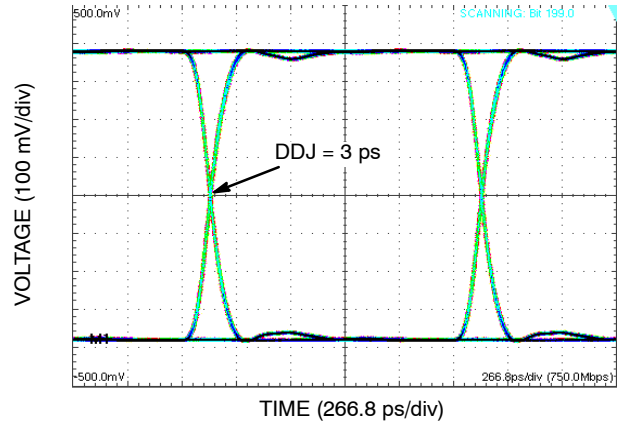
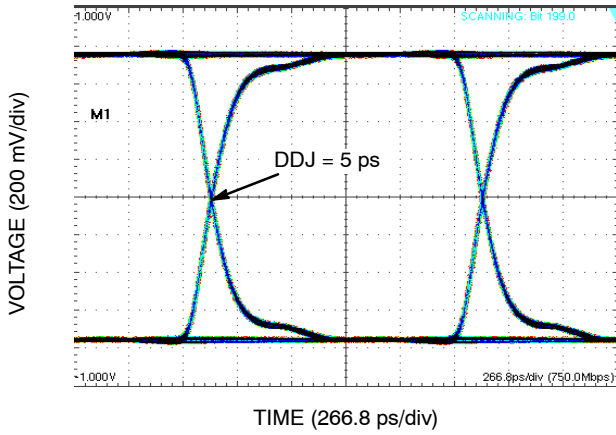


**Figure 7. Typical Propagation Delay vs. Input Offset Voltage** ( $V_{CC} - V_{EE} = 3.3 \text{ V}$ ;  $V_{TT} = 3.3 \text{ V}$  @  $25^\circ\text{C}$ ;  $V_{in} = 100 \text{ mV}$ ;  $R_L = 50 \Omega$ )

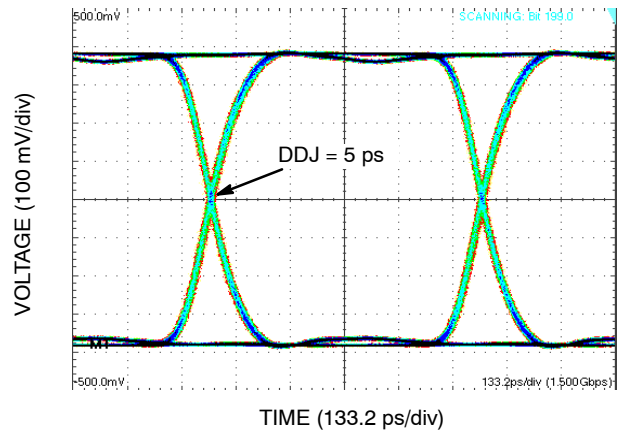
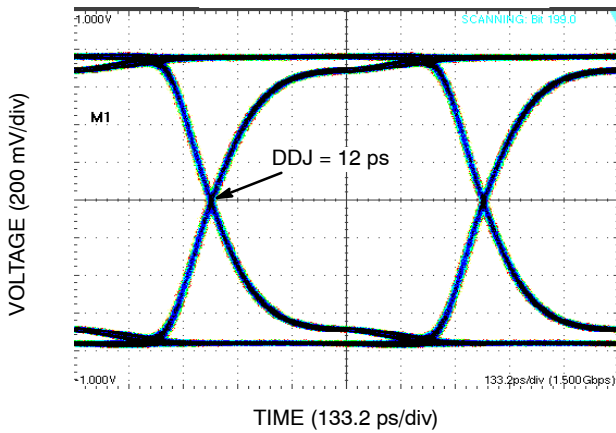


**Figure 8. Supply Current vs. Temperature**

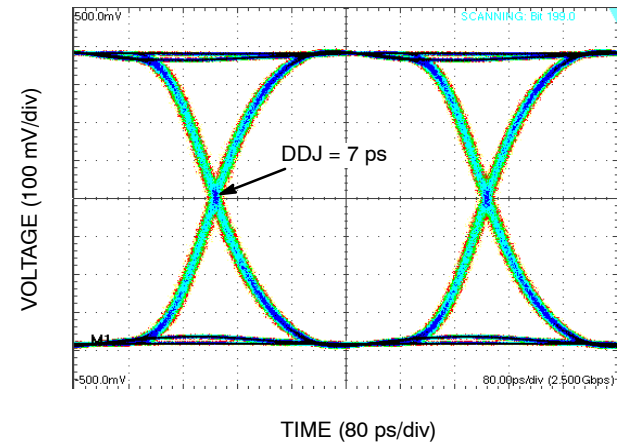
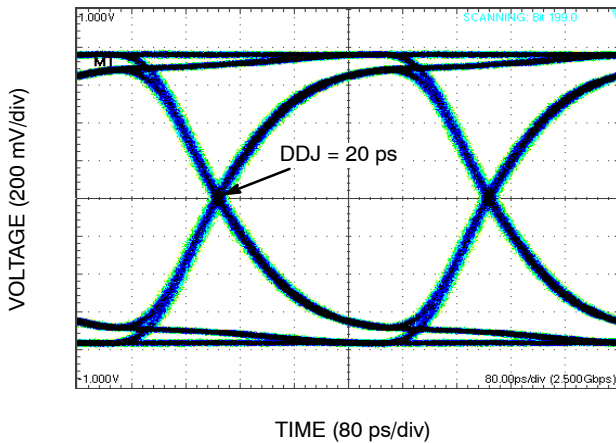
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**Figure 9. Typical Differential Output Waveform at 750 Mb/s**  
 ( $R_L = 50 \Omega$  Left Plot,  $R_L = 25 \Omega$  Right Plot,  $V_{in} = 100$  mV, System DDJ = 24 ps)



**Figure 10. Typical Differential Output Waveform 1.5 Gb/s**  
 ( $R_L = 50 \Omega$  Left Plot,  $R_L = 25 \Omega$  Right Plot,  $V_{in} = 100$  mV, System DDJ = 25 ps)



**Figure 11. Typical Differential Output Waveform 2.5 Gb/s**  
 ( $R_L = 50 \Omega$  Left Plot,  $R_L = 25 \Omega$  Right Plot,  $V_{in} = 100$  mV, System DDJ = 24 ps)

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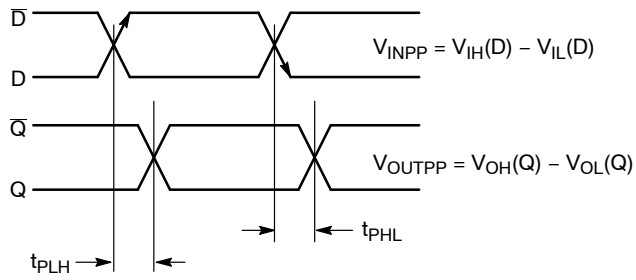


Figure 12. AC Reference Measurement

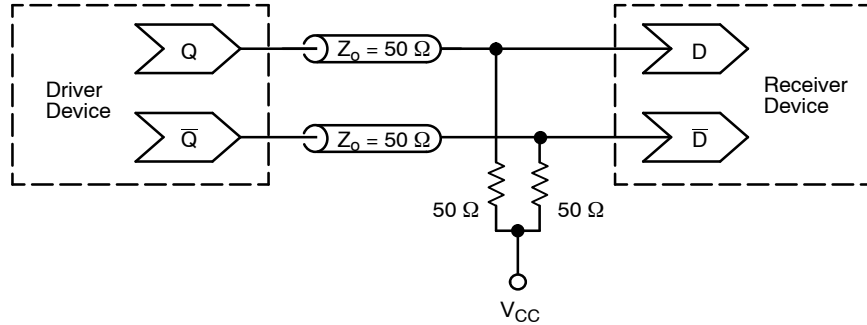


Figure 13. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D – Termination of ECL Logic Devices.)

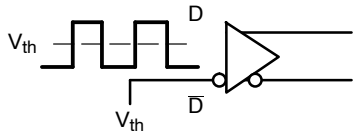


Figure 14. Differential Input Driven Single-Ended

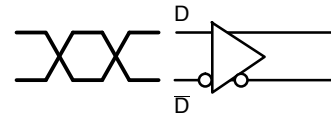


Figure 15. Differential Inputs Driven Differentially

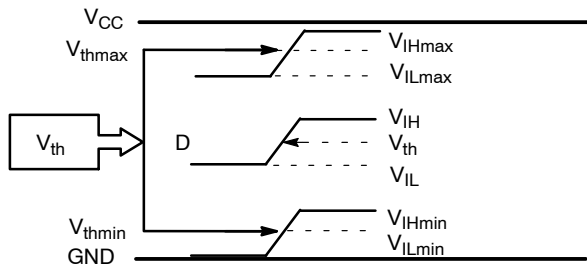


Figure 16.  $V_{th}$  Diagram

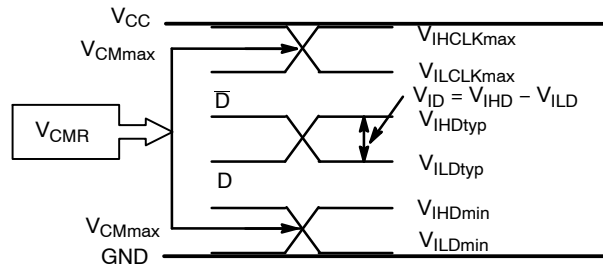


Figure 17.  $V_{CMR}$  Diagram



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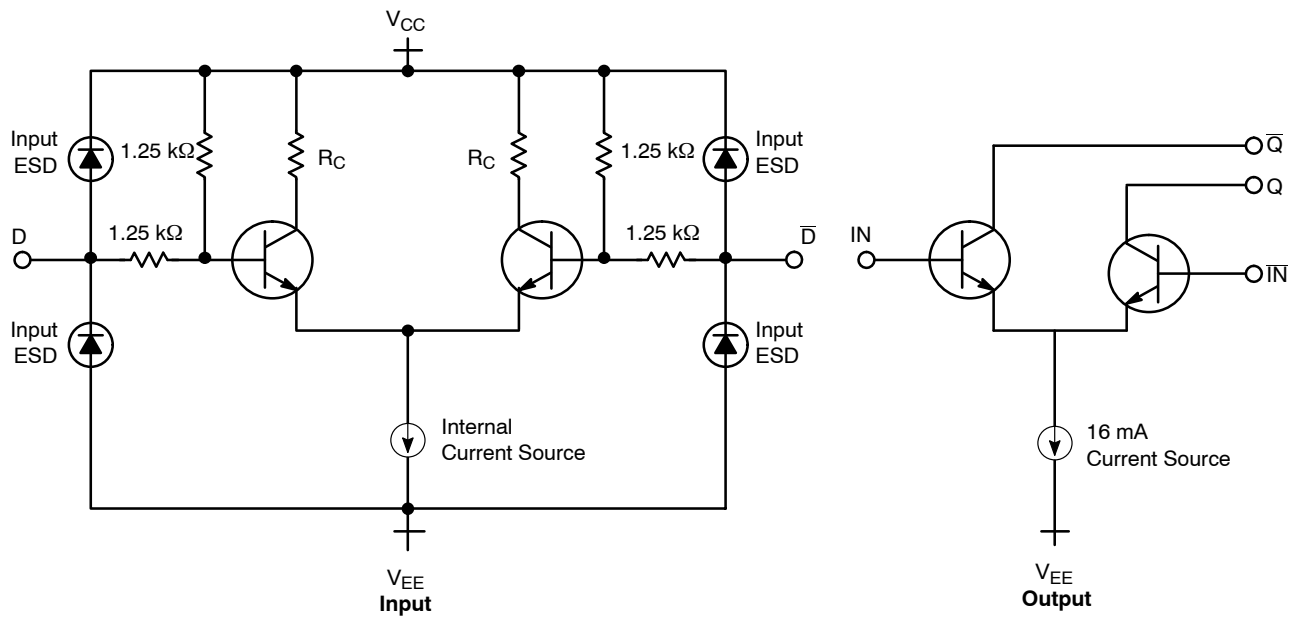


Figure 18. CML Input and Output Structure

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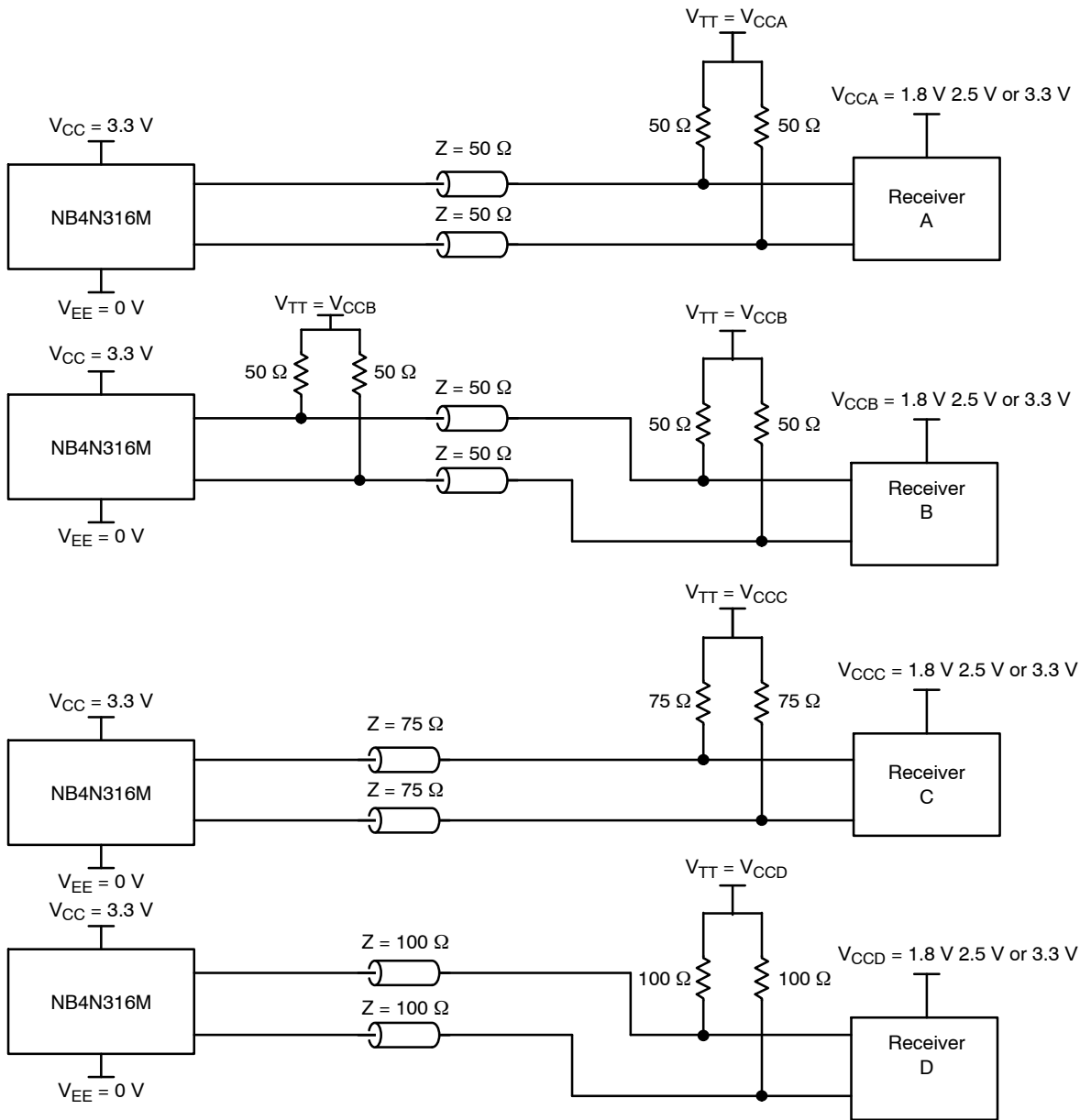


Figure 19. Typical Examples of the Application Interface

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## ORDERING INFORMATION

| Device        | Package              | Shipping†          |
|---------------|----------------------|--------------------|
| NB4N316MDTG   | TSSOP-8<br>(Pb-Free) | 100 Units / Rail   |
| NB4N316MDTR2G | TSSOP-8<br>(Pb-Free) | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

### Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

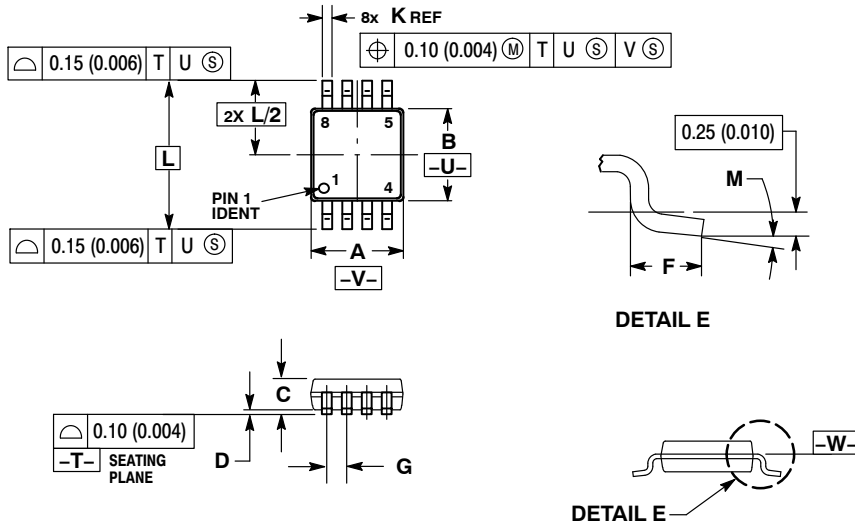
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SCALE 2:1

TSSOP-8 3.00x3.00x0.95  
CASE 948R-02  
ISSUE A

DATE 07 APR 2000



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 2.90        | 3.10 | 0.114     | 0.122 |
| B   | 2.90        | 3.10 | 0.114     | 0.122 |
| C   | 0.80        | 1.10 | 0.031     | 0.043 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.40        | 0.70 | 0.016     | 0.028 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| K   | 0.25        | 0.40 | 0.010     | 0.016 |
| L   | 4.90 BSC    |      | 0.193 BSC |       |
| M   | 0°          | 6°   | 0°        | 6°    |

|                  |                        |  |
|------------------|------------------------|--|
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