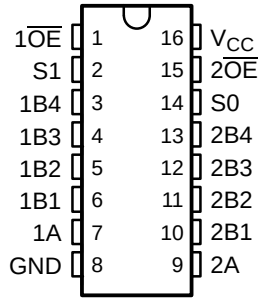
SN74CB3T3253
DUAL 1-OF-4 FET MULTIPLEXER/DEMULTIPLEXER
2.5-V/3.3-V LOW-VOLTAGE BUS SWITCH WITH 5-V TOLERANT LEVEL SHIFTER

SCDS148–OCTOBER 2003–REVISED JUNE 2005

FEATURES

- Output Voltage Translation Tracks V_{CC}
- Supports Mixed-Mode Signal Operation on All Data I/O Ports
  - 5-V Input Down to 3.3-V Output Level Shift With 3.3-V V_{CC}
  - 5-V/3.3-V Input Down to 2.5-V Output Level Shift With 2.5-V V_{CC}
- 5-V Tolerant I/Os With Device Powered Up or Powered Down
- Bidirectional Data Flow With Near-Zero Propagation Delay
- Low ON-State Resistance (r_{on}) Characteristics (r_{on} = 5 Ω Typ)
- Low Input/Output Capacitance Minimizes Loading ($C_{io(OFF)}$ = 5 pF Typ)
- Data and Control Inputs Provide Undershoot Clamp Diodes
- Low Power Consumption (I_{CC} = 20 μA Max)
- V_{CC} Operating Range From 2.3 V to 3.6 V
- Data I/Os Support 0- to 5-V Signaling Levels (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V, 5 V)
- Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- Supports Digital Applications: Level Translation, USB Interface, Memory Interleaving, Bus Isolation
- Ideal for Low-Power Portable Equipment

D, DBQ, DGV, OR PW PACKAGE
(TOP VIEW)



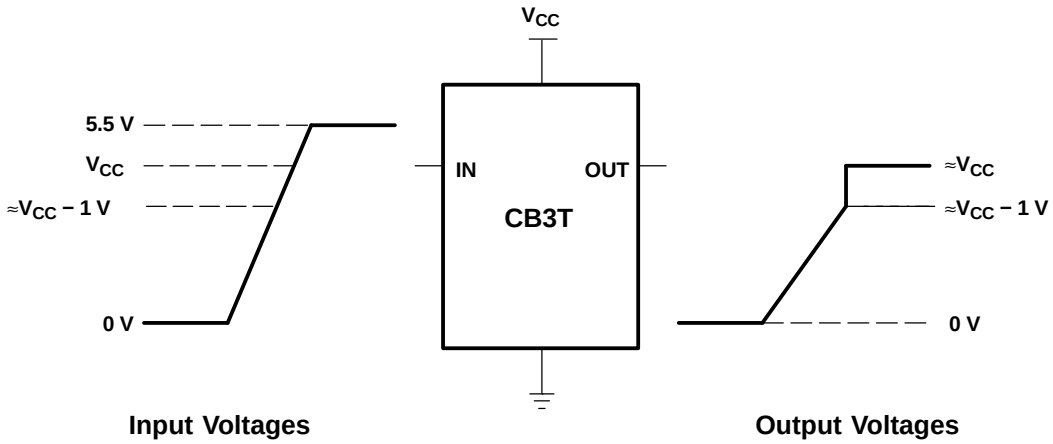
DESCRIPTION/ORDERING INFORMATION

The SN74CB3T3253 is a high-speed TTL-compatible FET multiplexer/demultiplexer with low ON-state resistance (r_{on}), allowing for minimal propagation delay. The device fully supports mixed-mode signal operation on all data I/O ports by providing voltage translation that tracks V_{CC}. The SN74CB3T3253 supports systems using 5-V TTL, 3.3-V LVTTL, and 2.5-V CMOS switching standards, as well as user-defined switching levels (see Figure 1).

The SN74CB3T3253 is organized as two 1-of-4 multiplexer/demultiplexers with separate output-enable ($1\overline{OE}$, $2\overline{OE}$) inputs. The select (S0, S1) inputs control the data path of each multiplexer/demultiplexer. When $\overline{OE}$ is low, the associated multiplexer/demultiplexer is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{OE}$ is high, the associated multiplexer/demultiplexer is OFF, and a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.



NOTE A: If the input high voltage (V_{IH}) level is greater than or equal to V_{CC} − 1 V, and less than or equal to 5.5 V, then the output high voltage (V_{OH}) level will be equal to approximately the V_{CC} voltage level.

Figure 1. Typical DC Voltage-Translation Characteristics

ORDERING INFORMATION

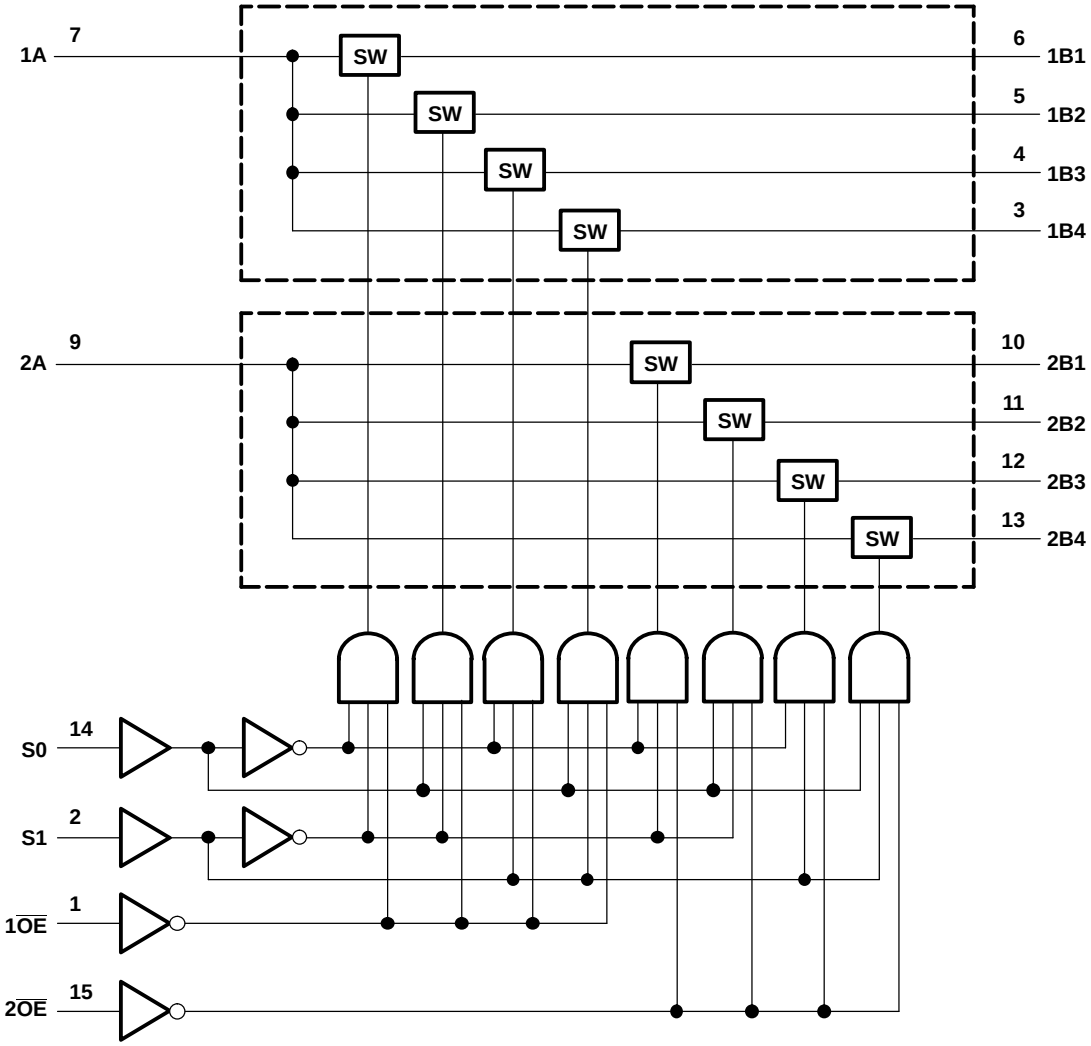
T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – D	Tube	SN74CB3T3253D	CB3T3253
		Tape and reel	SN74CB3T3253DR	
	SSOP (QSOP) – DBQ	Tape and reel	SN74CB3T3253DBQR	KS253
	TSSOP – PW	Tube	SN74CB3T3253PW	KS253
		Tape and reel	SN74CB3T3253PWR	
	TVSOP – DGV	Tape and reel	SN74CB3T3253DGVR	KS253

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

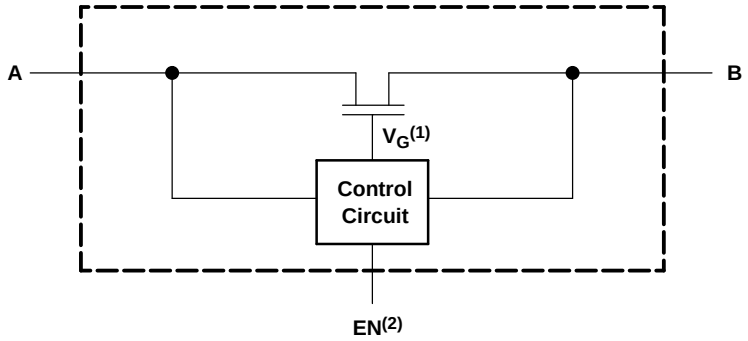
FUNCTION TABLE (EACH MULTIPLEXER/DEMULTIPLEXER)

INPUTS			INPUT/OUTPUT A	FUNCTION
$\overline{OE}$	S1	S0		
L	L	L	B1	A port = B1 port
L	L	H	B2	A port = B2 port
L	H	L	B3	A port = B3 port
L	H	H	B4	A port = B4 port
H	X	X	Z	Disconnect

LOGIC DIAGRAM (POSITIVE LOGIC)



SIMPLIFIED SCHEMATIC, EACH FET SWITCH (SW)



(1) Gate voltage (V_G) is approximately equal to $V_{CC} + V_T$ when the switch is ON and $V_I > V_{CC} + V_T$.
(2) EN is the internal enable signal applied to the switch.

Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range(2)		–0.5	7	V
V_{IN}	Control input voltage range(2)(3)		–0.5	7	V
$V_{I/O}$	Switch I/O voltage range(2)(3)(4)		–0.5	7	V
I_{IK}	Control input clamp current	V_{IN} < 0		–50	mA
$I_{I/OK}$	I/O port clamp current	$V_{I/O}$ < 0		–50	mA
$I_{I/O}$	ON-state switch current(5)			±128	mA
	Continuous current through V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance(6)	D package		73	°C/W
		DBQ package		90	
		DGV package		120	
		PW package		108	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
(5) I_I and I_O are used to denote specific conditions for $I_{I/O}$.
(6) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7	5.5	V
		V_{CC} = 2.7 V to 3.6 V	2	5.5	
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V	0	0.7	V
		V_{CC} = 2.7 V to 3.6 V	0	0.8	
$V_{I/O}$	Data input/output voltage		0	5.5	V
T_A	Operating free-air temperature		–40	85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics[1]

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP[2]	MAX	UNIT
V_{IK}		V_{CC} = 3 V, I_I = –18 mA				–1.2	V
V_{OH}		See Figure 3 and Figure 4					
I_{IN}	Control inputs	V_{CC} = 3.6 V, V_{IN} = 3.6 V to 5.5 V or GND				±10	µA
I_I		V_{CC} = 3.6 V, Switch ON, V_{IN} = V_{CC} or GND	V_I = V_{CC} – 0.7 V to 5.5 V			±20	µA
			V_I = 0.7 V to V_{CC} – 0.7 V			–40	
			V_I = 0 to 0.7 V			±5	
I_{OZ}[3]		V_{CC} = 3.6 V, V_O = 0 to 5.5 V, V_I = 0, Switch OFF, V_{IN} = V_{CC} or GND				±10	µA
I_{off}		V_{CC} = 0, V_O = 0 to 5.5 V, V_I = 0				10	µA
I_{CC}		V_{CC} = 3.6 V, $I_{I/O}$ = 0, Switch ON or OFF, V_{IN} = V_{CC} or GND	V_I = V_{CC} or GND			20	µA
			V_I = 5.5 V			20	
ΔI_{CC}[4]	Control inputs	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND				300	µA
C_{in}	Control inputs	V_{CC} = 3.3 V, V_{IN} = V_{CC} or GND			3		pF
$C_{io(OFF)}$	A port	V_{CC} = 3.3 V, $V_{I/O}$ = 5.5 V, 3.3 V, or GND, Switch OFF, V_{IN} = V_{CC} or GND			12		pF
	B port				5		
$C_{io(ON)}$	A port	V_{CC} = 3.3 V, Switch ON, V_{IN} = V_{CC} or GND	$V_{I/O}$ = 5.5 V or 3.3 V		10		pF
			$V_{I/O}$ = GND		22		
	B port		$V_{I/O}$ = 5.5 V or 3.3 V		4		
			$V_{I/O}$ = GND		22		
r_{on}[5]		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V, V_I = 0	I_O = 24 mA		5	8	Ω
			I_O = 16 mA		5	8	
		V_{CC} = 3 V, V_I = 0	I_O = 64 mA		5	7	
			I_O = 32 mA		5	7	

(1) V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.
(2) All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.
(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.
(5) Measured by the voltage drop between A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

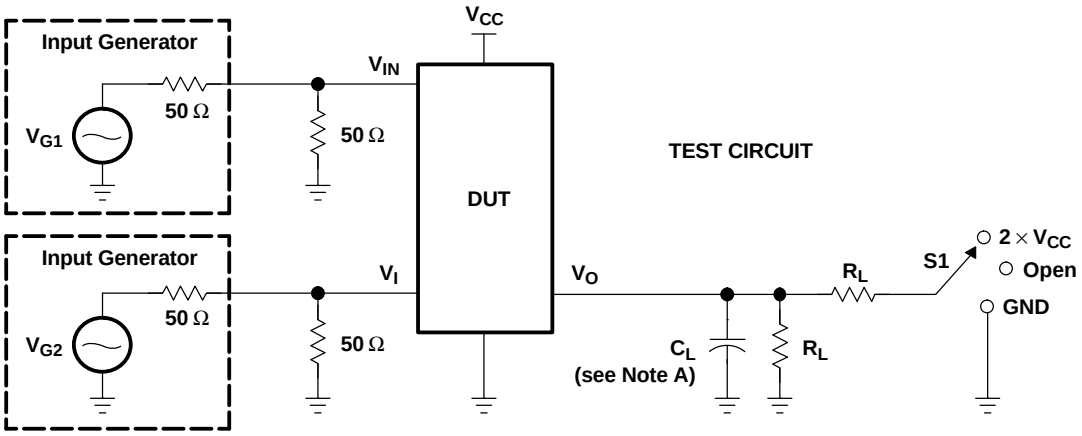
Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

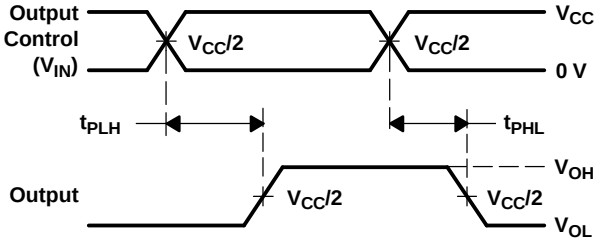
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}[1]	A or B	B or A		0.15		0.25	ns
$t_{pd(s)}$	S	A	1	10.5	1	8	ns
t_{en}	S	B	1	10	1	8	ns
	$\overline{OE}$	A or B	1	8.5	1	8	
t_{dis}	S	B	1	7.5	1	8.5	ns
	$\overline{OE}$	A or B	1	6.5	1	8	

(1) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

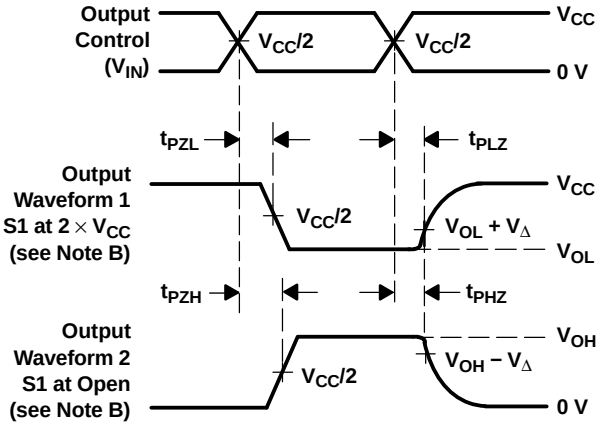
PARAMETER MEASUREMENT INFORMATION



TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	3.6 V or GND 5.5 V or GND	30 pF 50 pF	
t_{PLZ}/t_{PZL}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	2 × V_{CC} 2 × V_{CC}	500 Ω 500 Ω	GND GND	30 pF 50 pF	0.15 V 0.3 V
t_{PHZ}/t_{PZH}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	3.6 V 5.5 V	30 pF 50 pF	0.15 V 0.3 V



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The t_{pd} propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
H. All parameters and waveforms are not applicable to all devices.

Figure 2. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

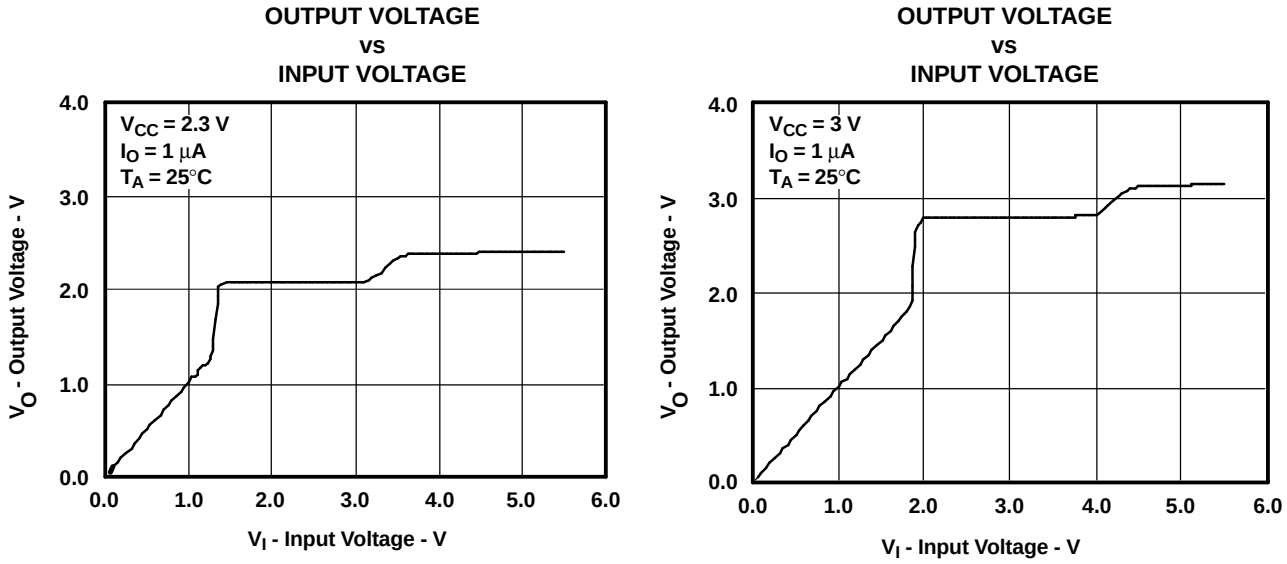


Figure 3. Data Output Voltage vs Data Input Voltage

TYPICAL CHARACTERISTICS

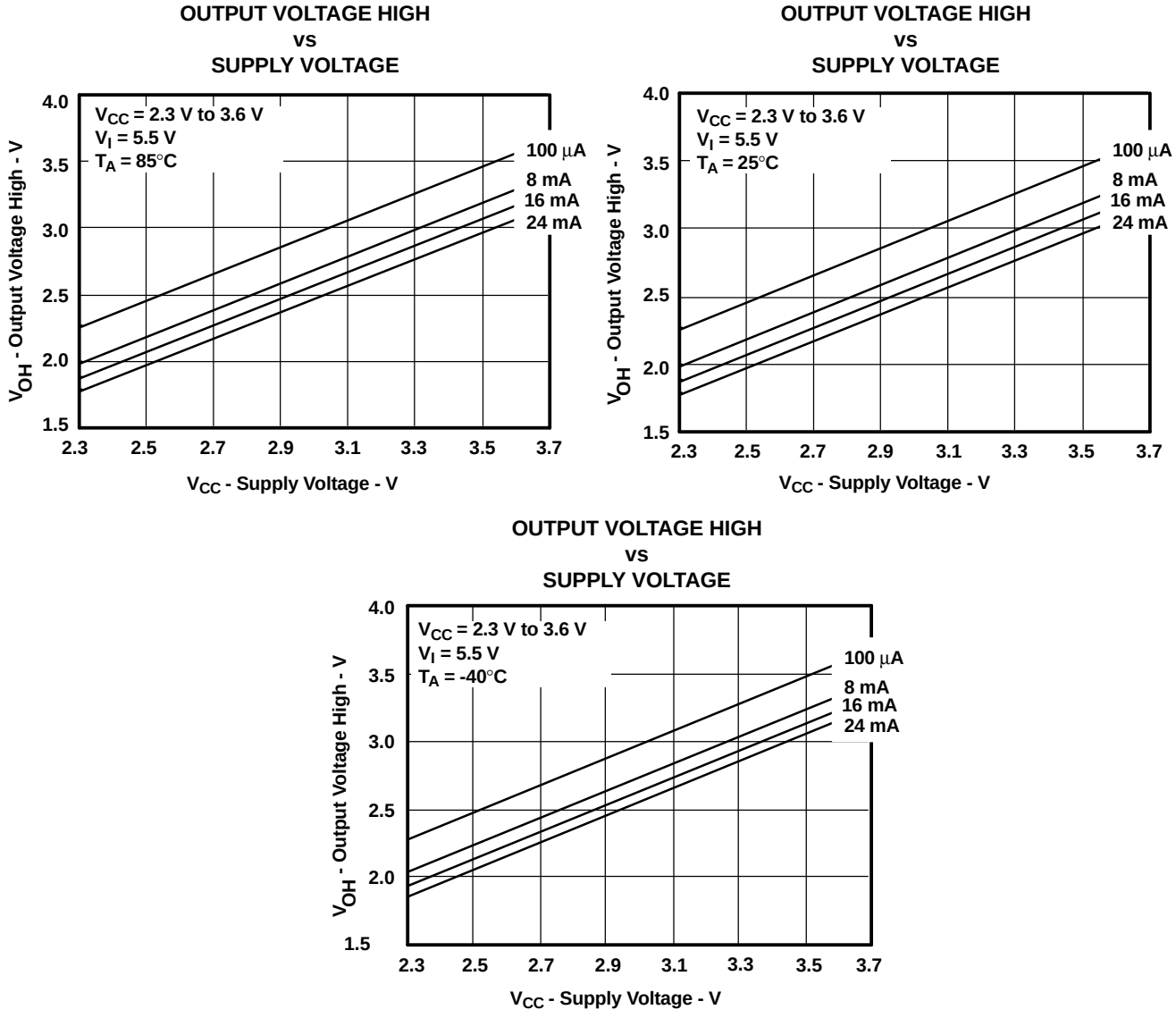


Figure 4. V_{OH} Values

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74CB3T3253D	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3T3253	Samples
SN74CB3T3253DBQR	ACTIVE	SSOP	DBQ	16	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	KS253	Samples
SN74CB3T3253DGVR	ACTIVE	TVSOP	DGV	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS253	Samples
SN74CB3T3253DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3T3253	Samples
SN74CB3T3253PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS253	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

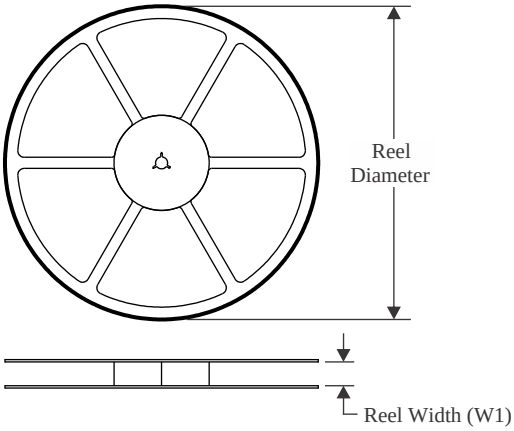
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

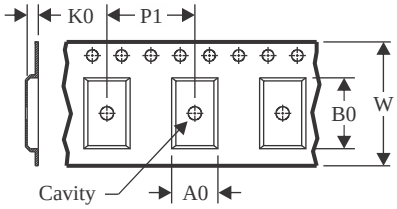
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

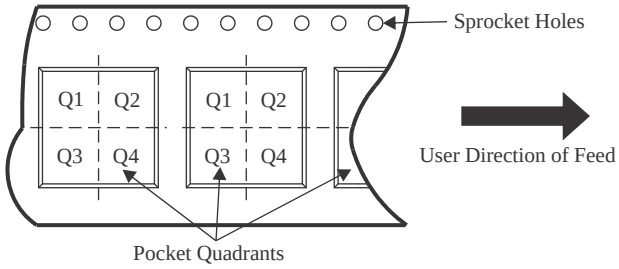


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

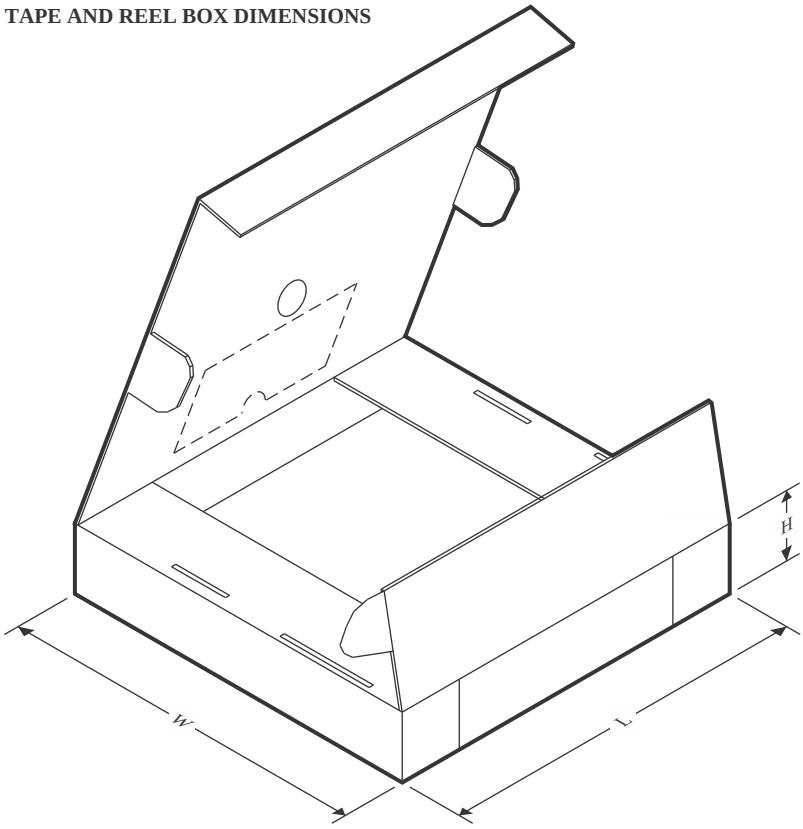
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CB3T3253DBQR	SSOP	DBQ	16	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
SN74CB3T3253DGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74CB3T3253DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74CB3T3253PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

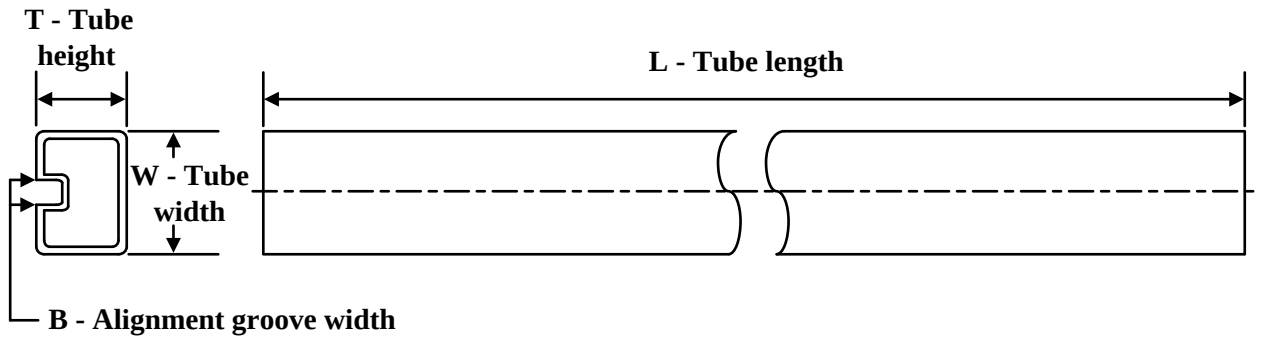
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CB3T3253DBQR	SSOP	DBQ	16	2500	340.5	338.1	20.6
SN74CB3T3253DGVR	TVSOP	DGV	16	2000	367.0	367.0	35.0
SN74CB3T3253DR	SOIC	D	16	2500	340.5	336.1	32.0
SN74CB3T3253PWR	TSSOP	PW	16	2000	367.0	367.0	35.0

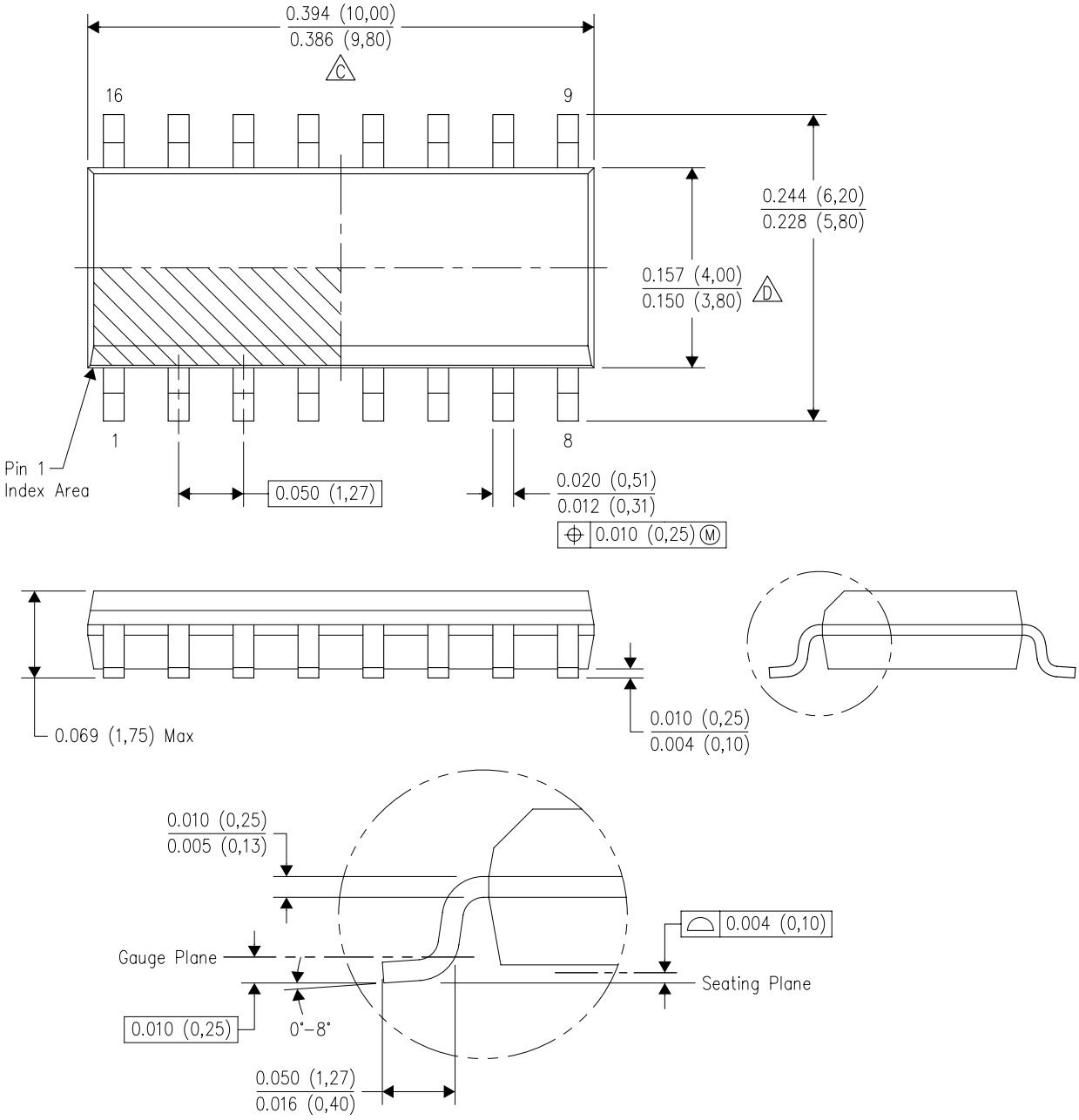
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74CB3T3253D	D	SOIC	16	40	507	8	3940	4.32

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



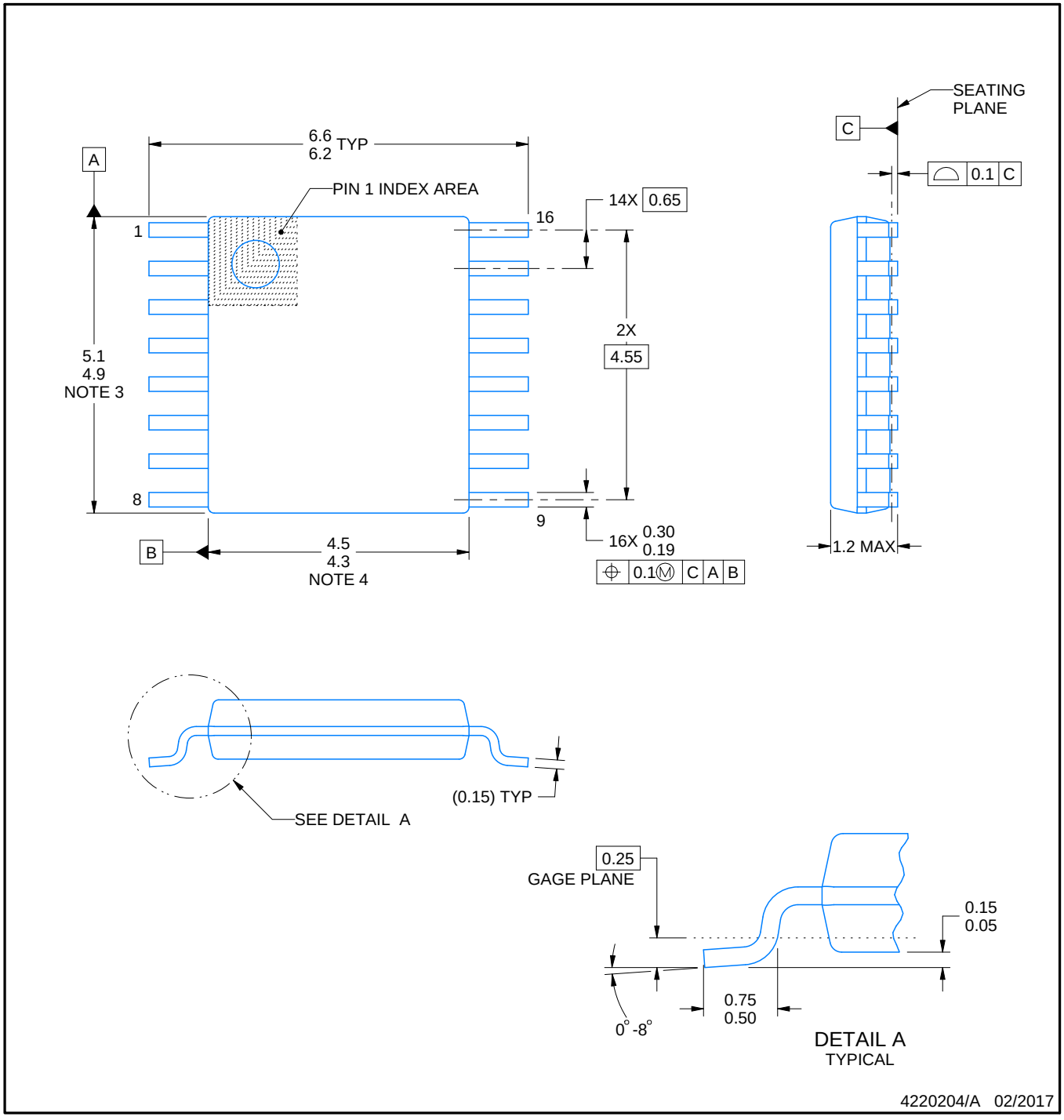
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

PACKAGE OUTLINE

PW0016A

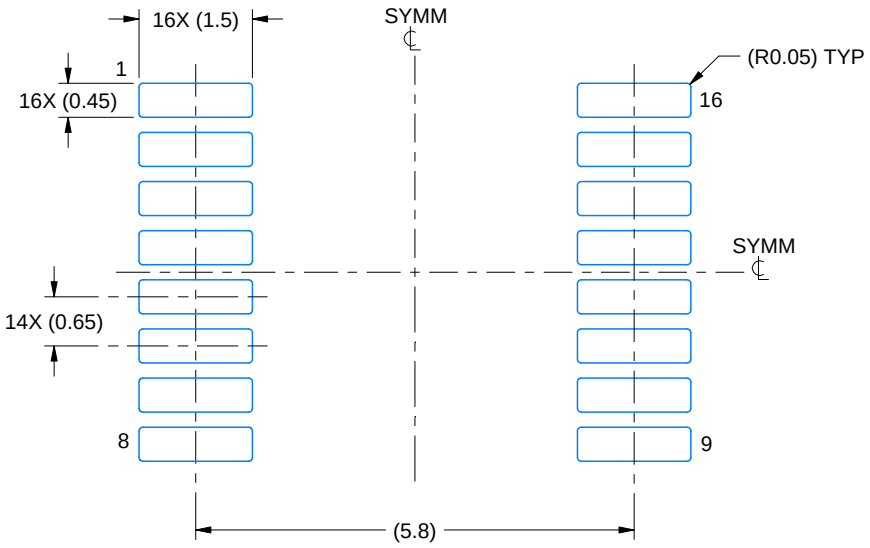
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

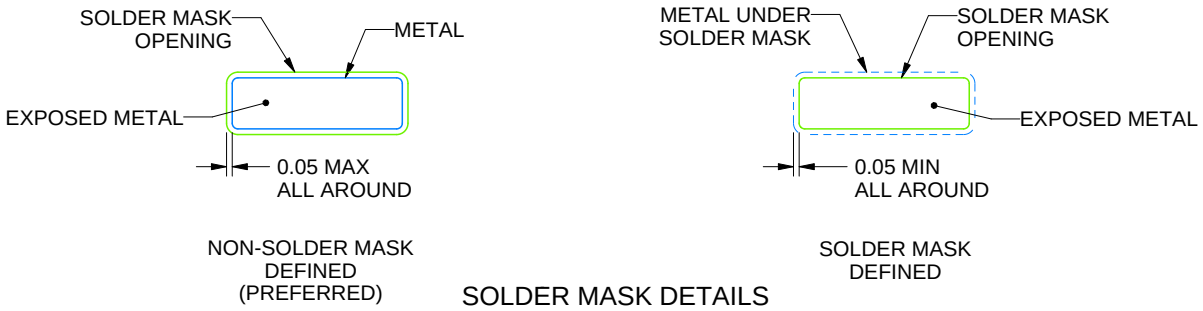


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

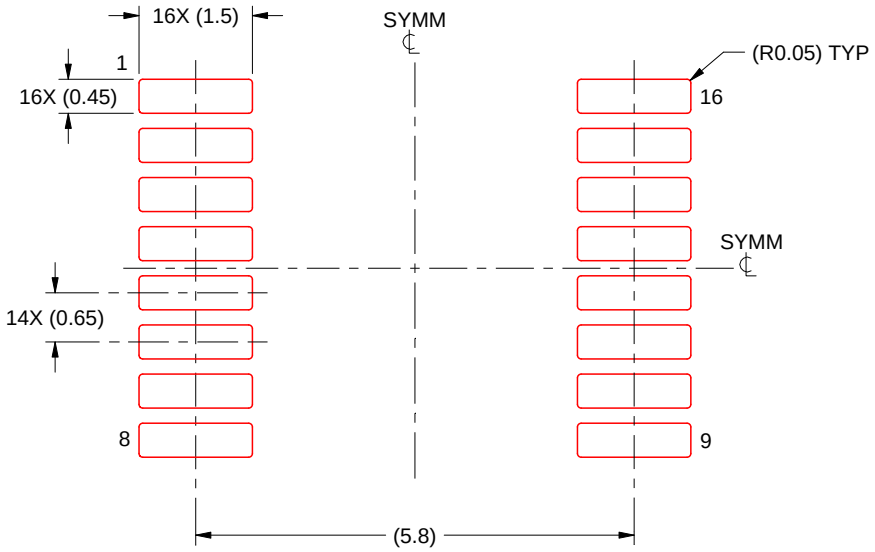


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

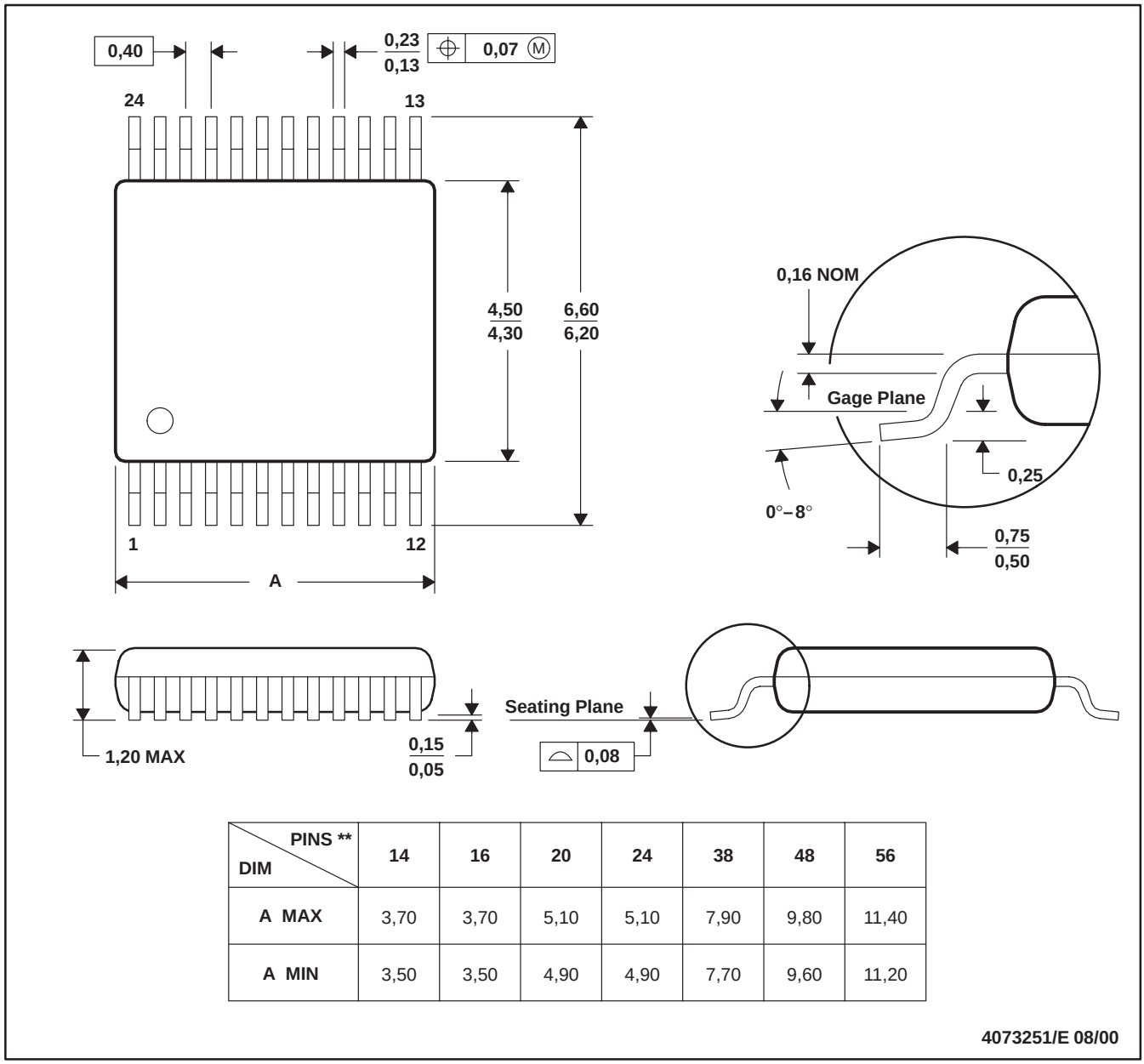
4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

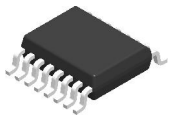
24 PINS SHOWN



DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

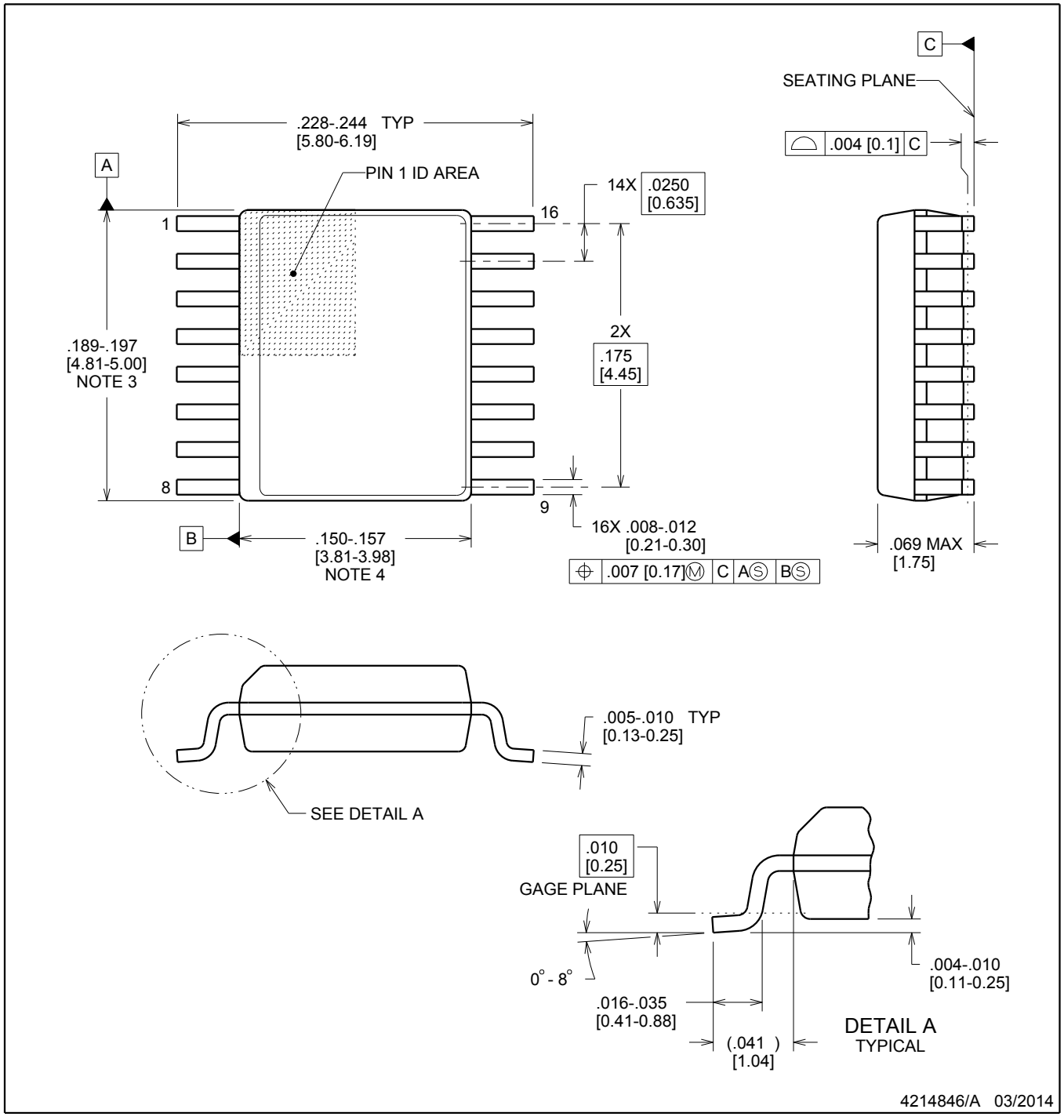


PACKAGE OUTLINE

DBQ0016A

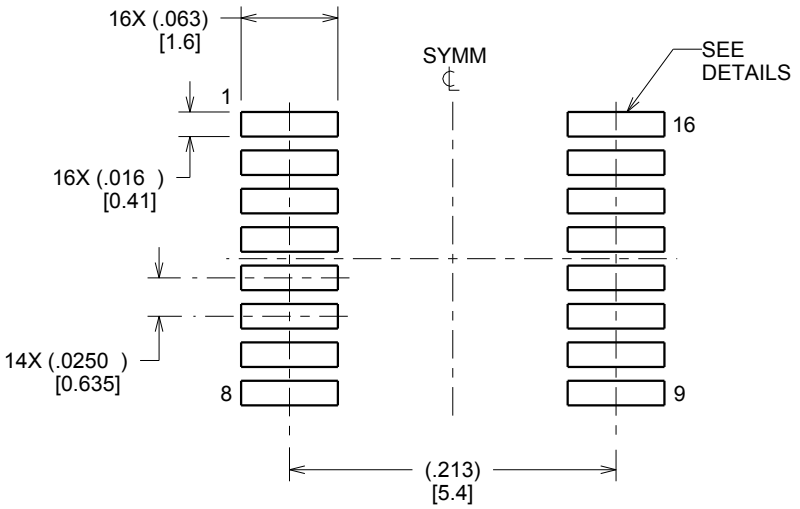
SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE

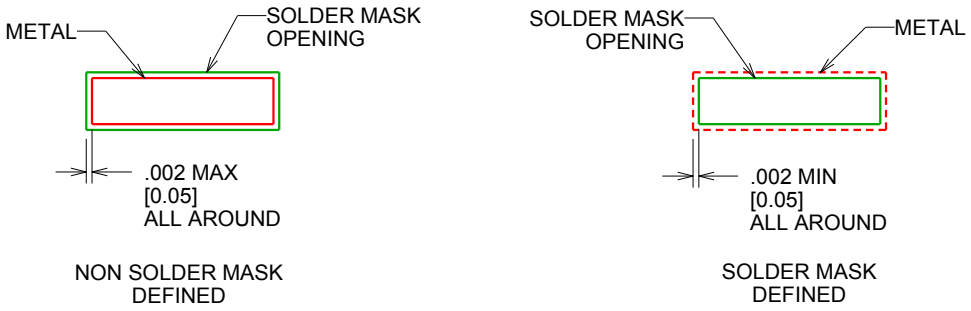


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

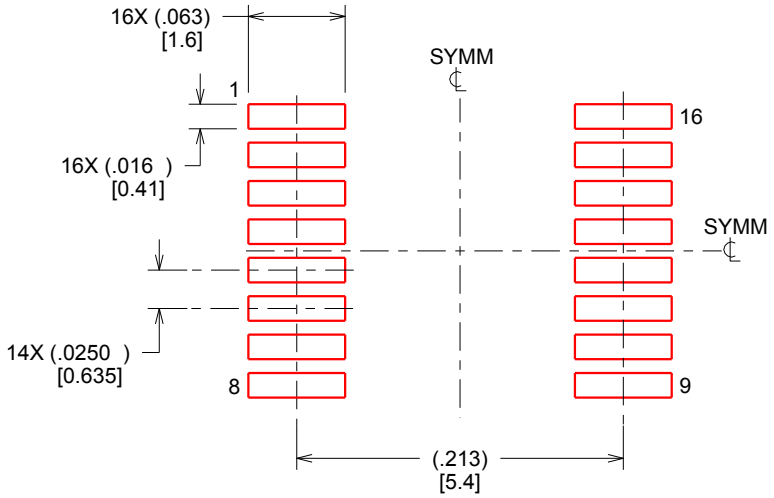
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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