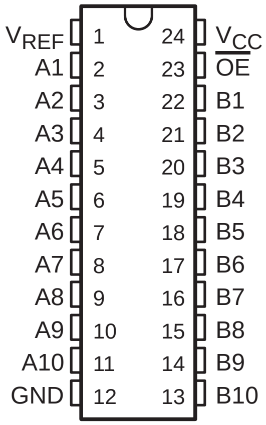
SN74CBTLV3857
LOW-VOLTAGE 10-BIT FET BUS SWITCH WITH INTERNAL PULLDOWN RESISTORS

SCDS085E − OCTOBER 1998 − REVISED OCTOBER 2003

- **Enable Signal Is SSTL_2 Compatible**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Designed for Use With 200 Mbit/s Double Data-Rate (DDR) SDRAM Applications**
- **Switch On-State Resistance Is Designed to Eliminate Series Resistor to DDR SDRAM**
- **Internal 10-kΩ Pulldown Resistors to Ground on B Port**
- **Internal 50-kΩ Pullup Resistor on Output-Enable Input**
- **Rail-to-Rail Switching on Data I/O Ports**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**

DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)



description/ordering information

This 10-bit FET bus switch is designed for 3-V to 3.6-V V_{CC} operation and SSTL_2 output-enable ($\overline{\text{OE}}$) input levels.

When $\overline{\text{OE}}$ is low, the 10-bit bus switch is on, and port A is connected to port B. When $\overline{\text{OE}}$ is high, the switch is open, and the high-impedance state exists between the two ports. There are 10-kΩ pulldown resistors to ground on the B port.

The FET switch on-state resistance is designed to replace the series terminating resistor in the SSTL_2 data path.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

ORDERING INFORMATION

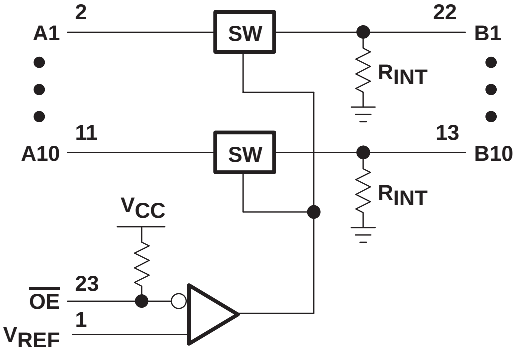
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	QSOP − DBQ	Tape and reel	SN74CBTLV3857DBQR	CL857
	SOIC − DW	Tube	SN74CBTLV3857DW	CBTLV3857
		Tape and reel	SN74CBTLV3857DWR	
	TSSOP − PW	Tape and reel	SN74CBTLV3857PWR	CL857
	TVSOP − DGV	Tape and reel	SN74CBTLV3857DGVR	CL857

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

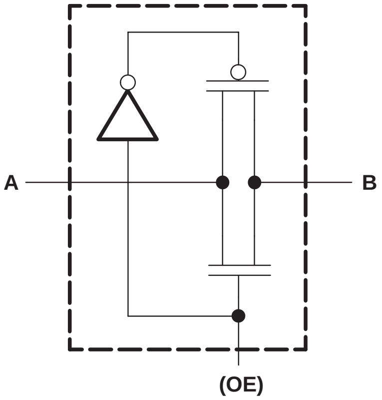
FUNCTION TABLE

INPUT $\overline{\text{OE}}$	FUNCTION
L	A port = B port
H	Disconnect

logic diagram (positive logic)



simplified schematic, each FET switch



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}		−0.5 V to 4.6 V
Input voltage range ($\overline{OE}$ only), V_I (see Note 1)		−0.5 V to V_{CC} + 0.5 V
Input voltage range (except $\overline{OE}$), V_I (see Note 1)		−0.5 V to 4.6 V
Continuous channel current		48 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)		−50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DBQ package	61°C/W
	DGV package	86°C/W
	DW package	46°C/W
	PW package	88°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{REF}	Reference voltage (0.38 × V_{CC})	1.15	1.25	1.35	V
V_{IH}	AC high-level control input voltage	V_{REF} + 350 mV			V
V_{IL}	AC low-level control input voltage			V_{REF} − 350 mV	V
V_{IH}	DC high-level control input voltage	V_{REF} + 180 mV			V
V_{IL}	DC low-level control input voltage			V_{REF} − 180 mV	V
T_A	Operating free-air temperature	−40		85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3 V,	I_I = −18 mA				−1.2	V
I_I	$\overline{OE}$	V_{CC} = 3.6 V,	V_I = V_{CC} or GND				±1	mA
	A port						±5	µA
	B port						±1	mA
	V_{REF}						±5	µA
I_{CC}		V_{CC} = 3.6 V,	I_O = 0,	V_I = V_{CC} or GND			25	mA
C_i	Control inputs	V_I = 3 V or 0				3.5		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}			5		pF
r_{on}‡		V_{CC} = 3 V	V_I = 0,	I_I = 24 mA		5	8	Ω
			V_I = 0.9 V,	I_I = 24 mA		6	11	
			V_I = 1.25 V,	I_I = 24 mA		7	13	
			V_I = 1.6 V,	I_I = 24 mA		9	40	
r_{off}‡		V_{CC} = 0			1			MΩ
		V_{CC} = 3 V to 3.6 V,	V_I = 1.65 V,	$\overline{OE}$ = V_{CC}	1			

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

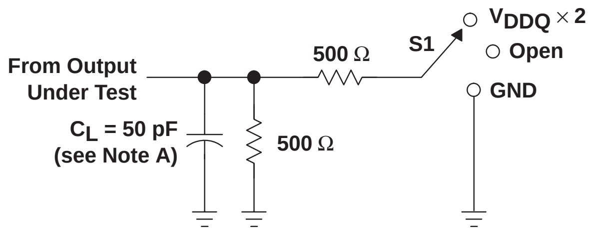
‡ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. Resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	
t_{pd}§	A or B	B or A		0.25	ns
t_{en}	$\overline{OE}$	A or B	1.4	4.2	ns
t_{dis}	$\overline{OE}$	A or B	1.4	4.8	ns

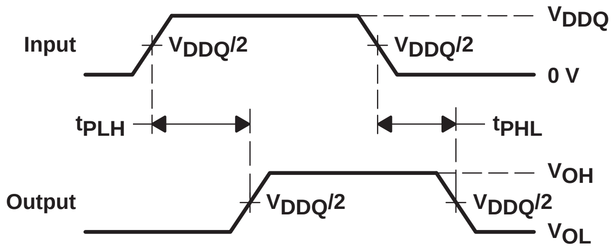
§ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 3.3 V ± 0.3 V AND V_{DDQ} = 2.5 ± 0.2 V

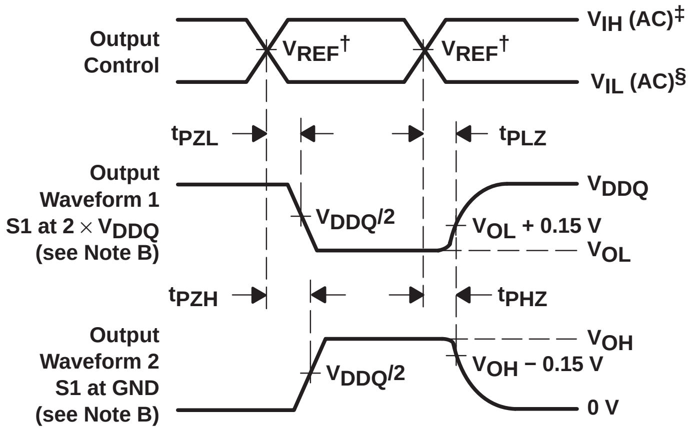


LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	V_{DDQ} × 2
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

† $V_{REF} = 0.38 \times V_{CC}$
‡ $V_{IH}(AC) = V_{REF} + 350$ mV
§ $V_{IL}(AC) = V_{REF} - 350$ mV

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74CBTLV3857DWR	ACTIVE	SOIC	DW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV3857	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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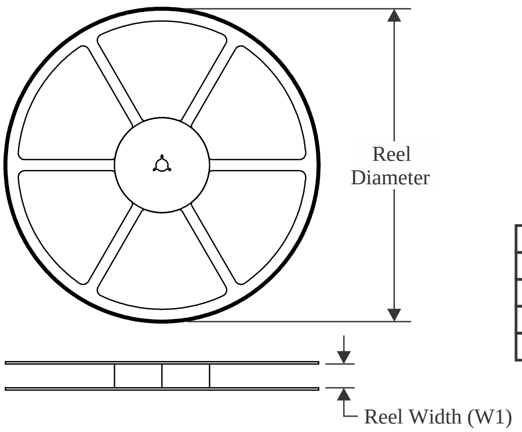
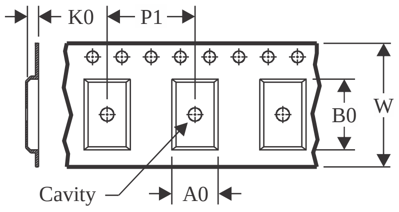
TAPE AND REEL INFORMATION

REEL DIMENSIONS

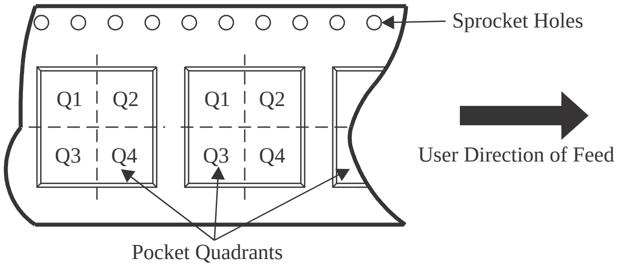


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

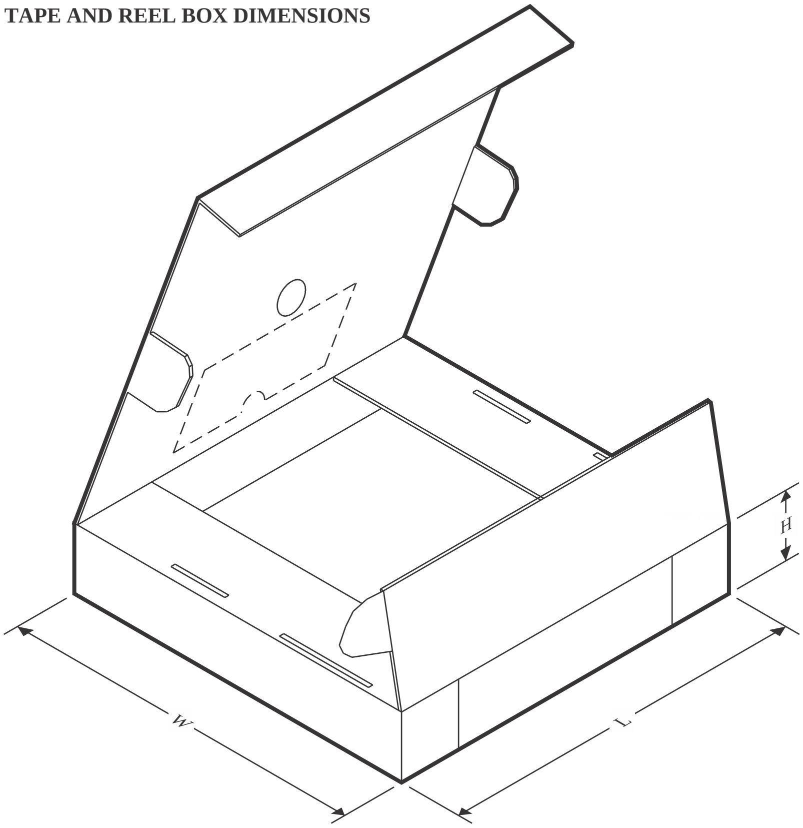
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBTLV3857DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

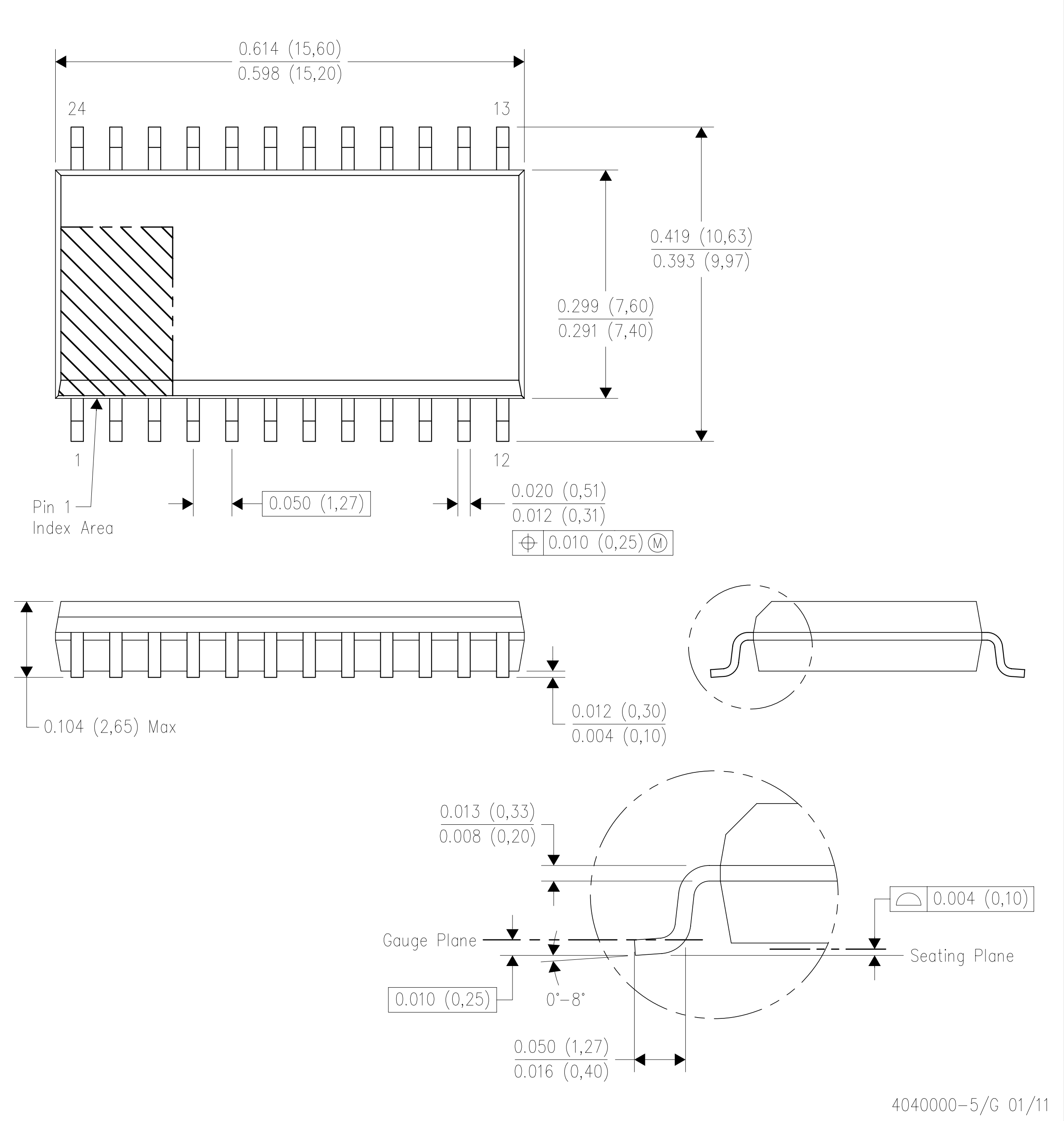
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBTLV3857DWR	SOIC	DW	24	2000	350.0	350.0	43.0

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS–013 variation AD.

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