

Dual 1-of-4 Decoder/Demultiplexer

MC74AC139, MC74ACT139

The MC74AC139/74ACT139 is a high-speed, dual 1-of-4 decoder/demultiplexer. The device has two independent decoders, each accepting two inputs and providing four mutually-exclusive active-LOW outputs. Each decoder has an active-LOW Enable input which can be used as a data input for a 4-output demultiplexer. Each half of the MC74AC139/74ACT139 can be used as a function generator providing four minterms of two variables.

Features

- Multifunctional Capability
- Two Completely Independent 1-of-4 Decoders
- Active LOW Mutually Exclusive Outputs
- Outputs Source/Sink 24 mA
- 'ACT139 Has TTL Compatible Inputs
- These are Pb-Free Devices

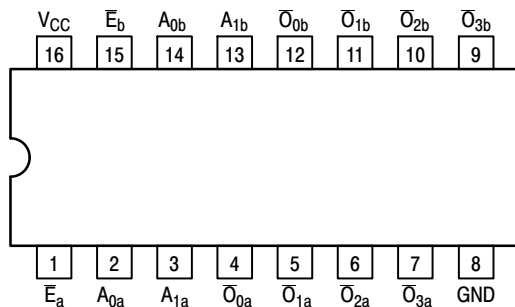


Figure 1. Pinout: 16-Lead Packages Conductors (Top View)

PIN ASSIGNMENT

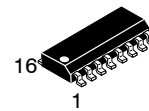
PIN	FUNCTION
A ₀ , A ₁	Address Inputs
\bar{E}	Enable Inputs
\bar{O}_0 - \bar{O}_3	Outputs

TRUTH TABLE

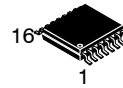
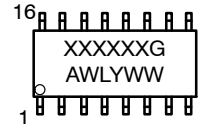
Inputs			Outputs			
\bar{E}	A ₀	A ₁	\bar{O}_0	\bar{O}_1	\bar{O}_2	\bar{O}_3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

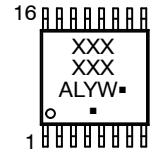
MARKING DIAGRAMS



SOIC-16
D SUFFIX
CASE 751B



TSSOP-16
DT SUFFIX
CASE 948F



XXX = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
Y = Year
WW, W = Work Week
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

MC74AC139, MC74ACT139

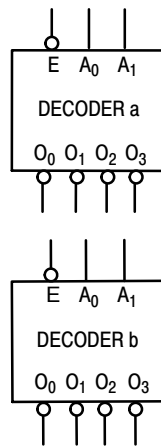
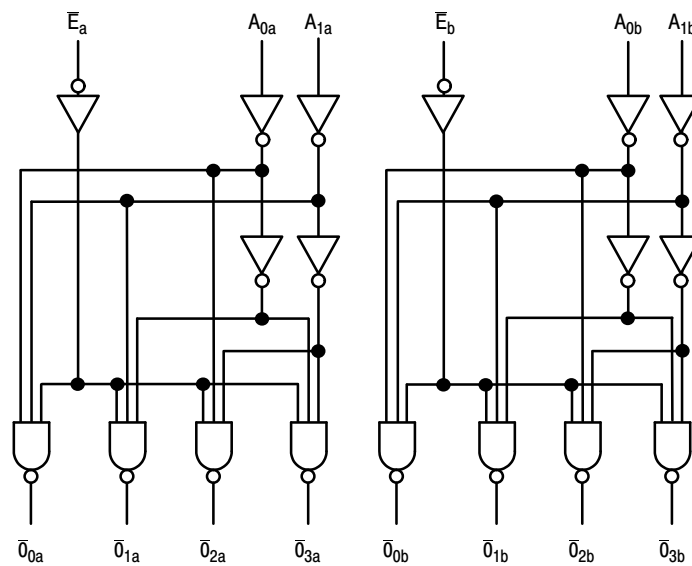


Figure 2. Logic Symbol



NOTE: This diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 3. Logic Diagram

FUNCTIONAL DESCRIPTION

The MC74AC139/74ACT139 is a high-speed dual 1-of-4 decoder/demultiplexer. The device has two independent decoders, each of which accepts two binary weighted inputs (A_0 - A_1) and provides four mutually exclusive active-LOW outputs (\bar{O}_0 - \bar{O}_3). Each decoder has an active-LOW enable (\bar{E}). When \bar{E} is HIGH all outputs are forced HIGH. The enable can be used as the data input for a 4-output demultiplexer application. Each half of the MC74AC139/74ACT139 generates all four minterms of two variables. These four minterms are useful in some applications, replacing multiple gate functions as shown in Figure 4, and thereby reducing the number of packages required in a logic network.

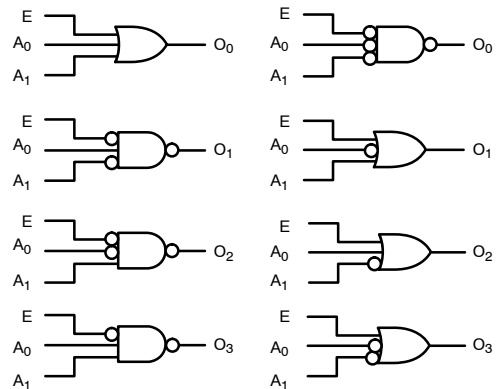


Figure 4. Gate Functions (Each Half)

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MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage	-0.5 to +6.5	V
V _I	DC Input Voltage	$-0.5 \leq V_I \leq V_{CC} + 0.5$	V
V _O	DC Output Voltage (Note 1)	$-0.5 \leq V_O \leq V_{CC} + 0.5$	V
I _{IK}	DC Input Diode Current	±20	mA
I _{OK}	DC Output Diode Current	±50	mA
I _O	DC Output Sink/Source Current	±50	mA
I _{CC}	DC Supply Current per Output Pin	±50	mA
I _{GND}	DC Ground Current per Output Pin	±50	mA
T _{STG}	Storage Temperature Range	-65 to +150	°C
T _L	Lead temperature, 1 mm from Case for 10 Seconds	260	°C
T _J	Junction temperature under Bias	+150	°C
θ _{JA}	Thermal Resistance (Note 2)	SOIC TSSOP 126 159	°C/W
P _D	Power Dissipation in Still Air at 25°C (Note 3)	SOIC TSSOP 995 787	mW
MSL	Moisture Sensitivity	Level 1	
F _R	Flammability Rating	Oxygen Index: 30% – 35% UL 94 V-0 @ 0.125 in	
V _{ESD}	ESD Withstand Voltage	Human Body Model (Note 4) Charged Device Model (Note 5) > 2000 > 1000	V
I _{Latch-Up}	Latch-Up Performance Above V _{CC} and Below GND at 85°C (Note 6)	±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. I_O absolute maximum rating must be observed.
2. The package thermal impedance is calculated in accordance with JESD51-7.
3. 500 mW at 65°C; derate to 300 mW by 10 mW/ from 65°C to 85°C.
4. Tested to EIA/JESD22-A114-A.
5. Tested to JESD22-C101-A.
6. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit	
V _{CC}	Supply Voltage	'AC	2.0	5.0	6.0	V
		'ACT	4.5	5.0	5.5	
V _{IN} , V _{OUT}	DC Input Voltage, Output Voltage (Ref. to GND)	0	-	V _{CC}	V	
t _r , t _f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V	-	150	-	ns/V
		V _{CC} @ 4.5 V	-	40	-	
		V _{CC} @ 5.5 V	-	25	-	
t _r , t _f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V	-	10	-	ns/V
		V _{CC} @ 5.5 V	-	8.0	-	
T _A	Operating Ambient Temperature Range	-40	25	85	°C	
I _{OH}	Output Current – High	-	-	-24	mA	
I _{OL}	Output Current – Low	-	-	24	mA	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

1. V_{IN} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. V_{IN} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

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DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Unit	Conditions	
			T _A = +25°C		T _A = -40°C to +85°C				
			Typ	Guaranteed Limits					
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1		V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V	
		4.5	2.25	3.15	3.15				
		5.5	2.75	3.85	3.85				
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9		V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V	
		4.5	2.25	1.35	1.35				
		5.5	2.75	1.65	1.65				
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9		V	I _{OUT} = -50 μA	
		4.5	4.49	4.4	4.4				
		5.5	5.49	5.4	5.4				
	V _{OH}	Minimum High Level Output Voltage	3.0	-	2.56	2.46		V	*V _{IN} = V _{IL} or V _{IH} I _{OH} = -12 mA -24 mA -24 mA
			4.5	-	3.86	3.76			
			5.5	-	4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1		V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1				
		5.5	0.001	0.1	0.1				
	V _{OL}	Maximum Low Level Output Voltage	3.0	-	0.36	0.44		V	*V _{IN} = V _{IL} or V _{IH} I _{OL} = 12 mA 24 mA 24 mA
			4.5	-	0.36	0.44			
			5.5	-	0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5	-	±0.1	±1.0		μA	V _I = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5	-	-	75		mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5	-	-	-75		mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5	-	8.0	80		μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

NOTE: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

AC CHARACTERISTICS

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Unit
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF		
			Min	Typ	Max	Min	Max	
t _{PLH}	Propagation Delay A _n to \bar{O}_n	3.3	4.0	8.0	11.5	3.5	13	ns
		5.0	3.0	6.5	8.5	2.5	9.5	
t _{PHL}	Propagation Delay A _n to \bar{O}_n	3.3	3.0	7.0	10	2.5	11	ns
		5.0	2.5	5.5	7.5	2.0	8.5	
t _{PLH}	Propagation Delay E _n to \bar{O}_n	3.3	4.5	9.5	12	3.5	13	ns
		5.0	3.5	7.0	8.5	3.0	10	
t _{PHL}	Propagation Delay E _n to \bar{O}_n	3.3	4.0	8.0	10	3.0	11	ns
		5.0	2.5	6.0	7.5	2.5	8.5	

*Voltage Range 3.3 V is 3.3 V ±0.3 V.

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

MC74AC139, MC74ACT139

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Unit	Conditions
			T _A = +25°C		T _A = -40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0		V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V
		5.5	1.5	2.0	2.0			
V _{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8		V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V
		5.5	1.5	0.8	0.8			
V _{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4		V	I _{OUT} = -50 μA
		5.5	5.49	5.4	5.4			
		4.5	-	3.86	3.76		V	*V _{IN} = V _{IL} or V _{IH} -24 mA I _{OH} -24 mA
		5.5	-	4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1		V	I _{OUT} = 50 μA
		5.5	0.001	0.1	0.1			
		4.5	-	0.36	0.44		V	*V _{IN} = V _{IL} or V _{IH} 24 mA I _{OL} 24 mA
		5.5	-	0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5	-	±0.1	±1.0		μA	V _I = V _{CC} , GND
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6	-	1.5		mA	V _I = V _{CC} - 2.1 V
I _{OLD}	†Minimum Dynamic Output Current	5.5	-	-	75		mA	V _{OLD} = 1.65 V Max
I _{OHD}		5.5	-	-	-75		mA	V _{OHD} = 3.85 V Min
I _{CC}	Maximum Quiescent Supply Current	5.5	-	8.0	80		μA	V _{IN} = V _{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Unit
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF		
			Min	Typ	Max	Min	Max	
t _{PLH}	Propagation Delay A _n to \bar{O}_n	5.0	1.5	6.0	8.5	1.5	9.5	ns
t _{PHL}	Propagation Delay A _n to \bar{O}_n	5.0	1.5	6.0	9.5	1.5	10.5	ns
t _{PLH}	Propagation Delay E _n to \bar{O}_n	5.0	2.5	7.0	10.0	2.0	11.0	ns
t _{PHL}	Propagation Delay E _n to \bar{O}_n	5.0	2.0	7.0	9.5	1.5	10.5	ns

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

CAPACITANCE

Symbol	Parameter	Value Typ	Unit	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	40	pF	V _{CC} = 5.0 V

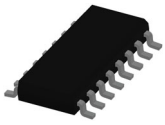
MC74AC139, MC74ACT139

ORDERING INFORMATION

Device Order Number	Marking	Package	Shipping [†]
MC74AC139DG	AC139	SOIC-16 (Pb-Free)	48 Units / Rail
MC74AC139DR2G	AC139	SOIC-16 (Pb-Free)	2500 Tape & Reel
MC74AC139DTR2G	AC 139	TSSOP-16 (Pb-Free)	2500 Tape & Reel
MC74ACT139DG	ACT139	SOIC-16 (Pb-Free)	48 Units / Rail
MC74ACT139DR2G	ACT139	SOIC-16 (Pb-Free)	2500 Tape & Reel
MC74ACT139DR2G-Q*	ACT139	SOIC-16 (Pb-Free)	2500 Tape & Reel
MC74ACT139DTR2G	ACT 139	TSSOP-16 (Pb-Free)	2500 Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*-Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

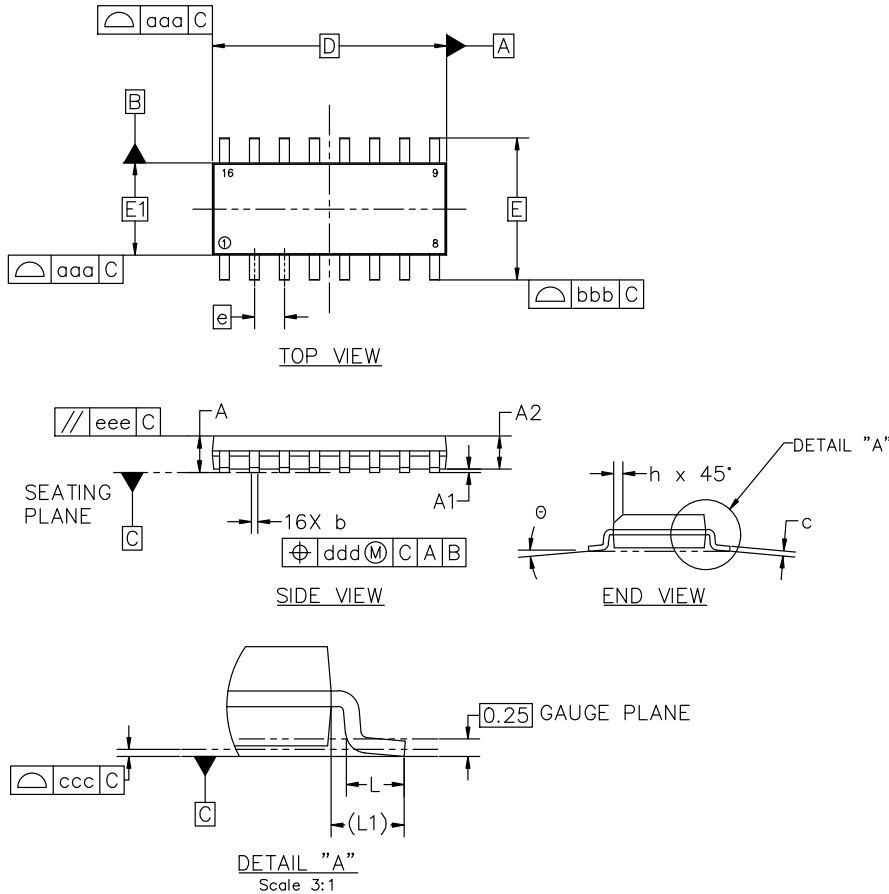


SOIC-16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

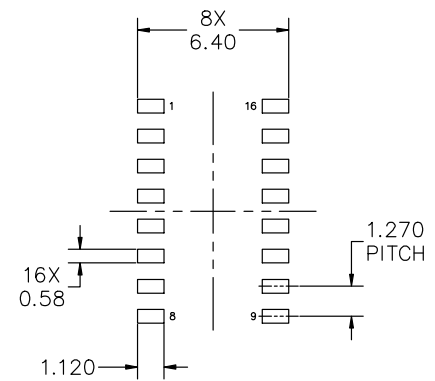
DATE 18 OCT 2024

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.18	0.25
A2	1.25	1.37	1.50
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	---	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
θ	0°	---	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



RECOMMENDED MOUNTING FOOTPRINT

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D

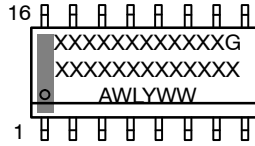
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SOIC-16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

DATE 18 OCT 2024

GENERIC
MARKING DIAGRAM*



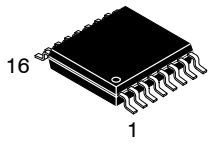
XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

<p>STYLE 1:</p> <p>PIN 1. COLLECTOR</p> <p>2. BASE</p> <p>3. EMITTER</p> <p>4. NO CONNECTION</p> <p>5. EMITTER</p> <p>6. BASE</p> <p>7. COLLECTOR</p> <p>8. COLLECTOR</p> <p>9. BASE</p> <p>10. EMITTER</p> <p>11. NO CONNECTION</p> <p>12. EMITTER</p> <p>13. BASE</p> <p>14. COLLECTOR</p> <p>15. EMITTER</p> <p>16. COLLECTOR</p>	<p>STYLE 2:</p> <p>PIN 1. CATHODE</p> <p>2. ANODE</p> <p>3. NO CONNECTION</p> <p>4. CATHODE</p> <p>5. CATHODE</p> <p>6. NO CONNECTION</p> <p>7. ANODE</p> <p>8. CATHODE</p> <p>9. CATHODE</p> <p>10. ANODE</p> <p>11. NO CONNECTION</p> <p>12. CATHODE</p> <p>13. CATHODE</p> <p>14. NO CONNECTION</p> <p>15. ANODE</p> <p>16. CATHODE</p>	<p>STYLE 3:</p> <p>PIN 1. COLLECTOR, DYE #1</p> <p>2. BASE, #1</p> <p>3. EMITTER, #1</p> <p>4. COLLECTOR, #1</p> <p>5. COLLECTOR, #2</p> <p>6. BASE, #2</p> <p>7. EMITTER, #2</p> <p>8. COLLECTOR, #2</p> <p>9. COLLECTOR, #3</p> <p>10. BASE, #3</p> <p>11. EMITTER, #3</p> <p>12. COLLECTOR, #3</p> <p>13. COLLECTOR, #4</p> <p>14. BASE, #4</p> <p>15. EMITTER, #4</p> <p>16. COLLECTOR, #4</p>	<p>STYLE 4:</p> <p>PIN 1. COLLECTOR, DYE #1</p> <p>2. COLLECTOR, #1</p> <p>3. COLLECTOR, #2</p> <p>4. COLLECTOR, #2</p> <p>5. COLLECTOR, #3</p> <p>6. COLLECTOR, #3</p> <p>7. COLLECTOR, #4</p> <p>8. COLLECTOR, #4</p> <p>9. BASE, #4</p> <p>10. EMITTER, #4</p> <p>11. BASE, #3</p> <p>12. EMITTER, #3</p> <p>13. BASE, #2</p> <p>14. EMITTER, #2</p> <p>15. BASE, #1</p> <p>16. EMITTER, #1</p>
<p>STYLE 5:</p> <p>PIN 1. DRAIN, DYE #1</p> <p>2. DRAIN, #1</p> <p>3. DRAIN, #2</p> <p>4. DRAIN, #2</p> <p>5. DRAIN, #3</p> <p>6. DRAIN, #3</p> <p>7. DRAIN, #4</p> <p>8. DRAIN, #4</p> <p>9. GATE, #4</p> <p>10. SOURCE, #4</p> <p>11. GATE, #3</p> <p>12. SOURCE, #3</p> <p>13. GATE, #2</p> <p>14. SOURCE, #2</p> <p>15. GATE, #1</p> <p>16. SOURCE, #1</p>	<p>STYLE 6:</p> <p>PIN 1. CATHODE</p> <p>2. CATHODE</p> <p>3. CATHODE</p> <p>4. CATHODE</p> <p>5. CATHODE</p> <p>6. CATHODE</p> <p>7. CATHODE</p> <p>8. CATHODE</p> <p>9. ANODE</p> <p>10. ANODE</p> <p>11. ANODE</p> <p>12. ANODE</p> <p>13. ANODE</p> <p>14. ANODE</p> <p>15. ANODE</p> <p>16. ANODE</p>	<p>STYLE 7:</p> <p>PIN 1. SOURCE N-CH</p> <p>2. COMMON DRAIN (OUTPUT)</p> <p>3. COMMON DRAIN (OUTPUT)</p> <p>4. GATE P-CH</p> <p>5. COMMON DRAIN (OUTPUT)</p> <p>6. COMMON DRAIN (OUTPUT)</p> <p>7. COMMON DRAIN (OUTPUT)</p> <p>8. SOURCE P-CH</p> <p>9. SOURCE P-CH</p> <p>10. COMMON DRAIN (OUTPUT)</p> <p>11. COMMON DRAIN (OUTPUT)</p> <p>12. COMMON DRAIN (OUTPUT)</p> <p>13. GATE N-CH</p> <p>14. COMMON DRAIN (OUTPUT)</p> <p>15. COMMON DRAIN (OUTPUT)</p> <p>16. SOURCE N-CH</p>	

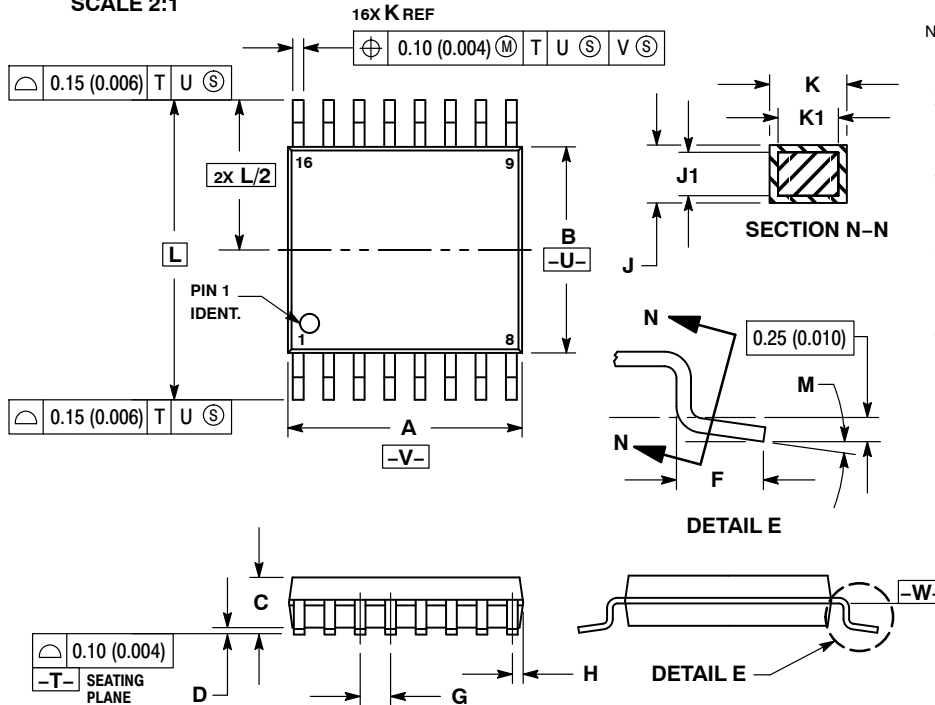
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DESCRIPTION:	SOIC-16 9.90X3.90X1.37 1.27P	PAGE 2 OF 2

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TSSOP-16 WB
CASE 948F
ISSUE B

DATE 19 OCT 2006

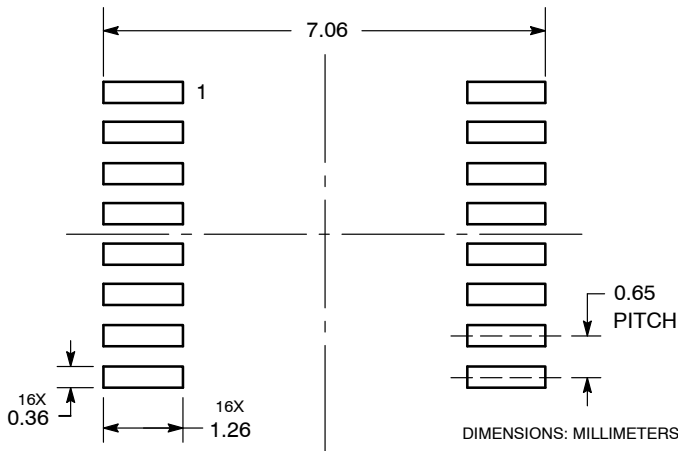


NOTES:

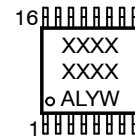
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

RECOMMENDED
SOLDERING FOOTPRINT*



GENERIC
MARKING DIAGRAM*



- XXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- G or ■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	TSSOP-16	PAGE 1 OF 1

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