

# Dual Precision Retriggerable/Resettable Monostable Multivibrator

## MC14538B

The MC14538B is a dual, retriggerable, resettable monostable multivibrator. It may be triggered from either edge of an input pulse, and produces an accurate output pulse over a wide range of widths, the duration and accuracy of which are determined by the external timing components,  $C_X$  and  $R_X$ . Output Pulse Width  $T = R_X \cdot C_X$  (secs)

$$R_X = \Omega$$

$$C_X = \text{Farads}$$

### Features

- Unlimited Rise and Fall Time Allowed on the A Trigger Input
- Pulse Width Range = 10  $\mu$ s to 10 s
- Latched Trigger Inputs
- Separate Latched Reset Inputs
- 3.0 Vdc to 18 Vdc Operational Limits
- Triggerable from Positive (A Input) or Negative-Going Edge (B-Input)
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-pin Compatible with MC14528B and CD4528B (CD4098)
- Use the MC54/74HC4538A for Pulse Widths Less Than 10  $\mu$ s with Supplies Up to 6 V
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ )

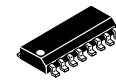
Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 1)	500	mW
$T_A$	Operating Temperature Range	-55 to +125	$^{\circ}$ C
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}$ C
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}$ C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

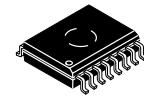
1. Temperature Derating: "D/DW" Packages: -7.0 mW/ $^{\circ}$ C From 65 $^{\circ}$ C To 125 $^{\circ}$ C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

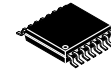
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



SOIC-16  
D SUFFIX  
CASE 751B

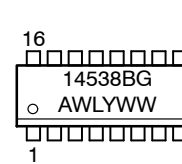


SOIC-16WB  
DW SUFFIX  
CASE 751G



TSSOP-16  
DT SUFFIX  
CASE 948F

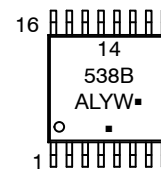
### MARKING DIAGRAMS



SOIC-16



SOIC-16WB



TSSOP-16

- A = Assembly Location
- WL, L = Wafer Lot
- YY, Y = Year
- WW, W = Work Week
- G or  $\blacksquare$  = Pb-Free Indicator

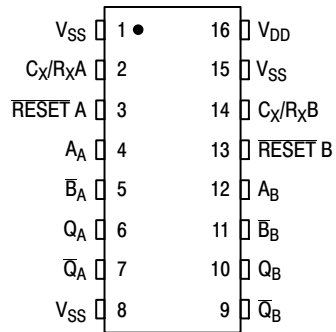
(Note: Microdot may be in either location)

### ORDERING INFORMATION

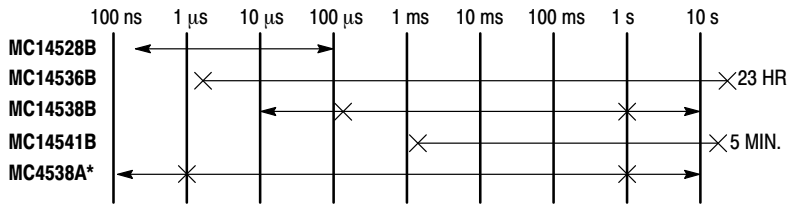
See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

# MC14538B

## PIN ASSIGNMENT



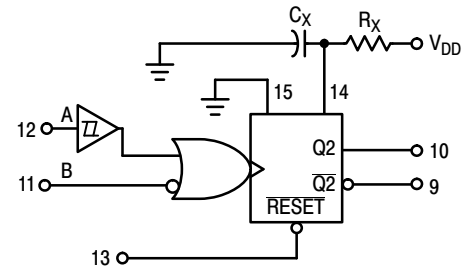
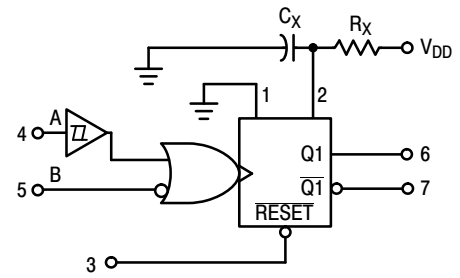
## ONE-SHOT SELECTION GUIDE



\*LIMITED OPERATING VOLTAGE (2 - 6 V)

TOTAL OUTPUT PULSE WIDTH RANGE ← →  
 RECOMMENDED PULSE WIDTH RANGE × ×

## BLOCK DIAGRAM



R<sub>X</sub> AND C<sub>X</sub> ARE EXTERNAL COMPONENTS.  
 V<sub>DD</sub> = PIN 16  
 V<sub>SS</sub> = PIN 8, PIN 1, PIN 15

## ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
MC14538BDG	SOIC-16 (Pb-Free)	48 Units / Rail
MC14538BDR2G	SOIC-16 (Pb-Free)	2500 Units / Tape & Reel
NLV14538BDR2G*	SOIC-16 (Pb-Free)	2500 Units / Tape & Reel
MC14538BDTR2G	TSSOP-16 (Pb-Free)	2500 Units / Tape & Reel
NLV14538BDTR2G*	TSSOP-16 (Pb-Free)	2500 Units / Tape & Reel
MC14538BDWG	SOIC-16 WB (Pb-Free)	47 Units / Rail
NLV14538BDWG*	SOIC-16 WB (Pb-Free)	47 Units / Rail
MC14538BDWR2G	SOIC-16 WB (Pb-Free)	1000 Units / Tape & Reel
NLV14538BDWR2G*	SOIC-16 WB (Pb-Free)	1000 Units / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

# MC14538B

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ (Note 2)	Max	Min	Max		
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0	"0" Level	V <sub>OL</sub>	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
			10	-	0.05	-	0	0.05	-	0.05	
			15	-	0.05	-	0	0.05	-	0.05	
	"1" Level	V <sub>OH</sub>	5.0	4.95	-	4.95	5.0	-	4.95	-	Vdc
			10	9.95	-	9.95	10	-	9.95	-	
			15	14.95	-	14.95	15	-	14.95	-	
Input Voltage (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)	"0" Level	V <sub>IL</sub>	5.0	-	1.5	-	2.25	1.5	-	1.5	Vdc
			10	-	3.0	-	4.50	3.0	-	3.0	
			15	-	4.0	-	6.75	4.0	-	4.0	
	"1" Level	V <sub>IH</sub>	5.0	3.5	-	3.5	2.75	-	3.5	-	Vdc
			10	7.0	-	7.0	5.50	-	7.0	-	
			15	11	-	11	8.25	-	11	-	
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)	Source	I <sub>OH</sub>	5.0	-3.0	-	-2.4	-4.2	-	-1.7	-	mA
			5.0	-0.64	-	-0.51	-0.88	-	-0.36	-	
			10	-1.6	-	-1.3	-2.25	-	-0.9	-	
			15	-4.2	-	-3.4	-8.8	-	-2.4	-	
	Sink	I <sub>OL</sub>	5.0	0.64	-	0.51	0.88	-	0.36	-	mA
			10	1.6	-	1.3	2.25	-	0.9	-	
15	4.2	-	3.4	8.8	-	2.4	-	-			
Input Current, Pin 2 or 14	I <sub>in</sub>	15	-	±0.05	-	±0.00001	±0.05	-	±0.5	μA	
Input Current, Other Inputs	I <sub>in</sub>	15	-	±0.1	-	±0.00001	±0.1	-	±1.0	μA	
Input Capacitance, Pin 2 or 14	C <sub>in</sub>	-	-	-	-	25	-	-	-	pF	
Input Capacitance, Other Inputs (V <sub>in</sub> = 0)	C <sub>in</sub>	-	-	-	-	5.0	7.5	-	-	pF	
Quiescent Current (Per Package) Q = Low, $\bar{Q}$ = High	I <sub>DD</sub>	5.0	-	5.0	-	0.005	5.0	-	150	μA	
		10	-	10	-	0.010	10	-	300		
		15	-	20	-	0.015	20	-	600		
Quiescent Current, Active State (Both) (Per Package) Q = High, $\bar{Q}$ = Low	I <sub>DD</sub>	5.0	-	2.0	-	0.04	0.20	-	2.0	mA	
		10	-	2.0	-	0.08	0.45	-	2.0		
		15	-	2.0	-	0.13	0.70	-	2.0		
Total Supply Current at an external load capacitance (C <sub>L</sub> ) and at external timing network (R <sub>X</sub> , C <sub>X</sub> ) (Note 3)	I <sub>T</sub>	5.0 10	$I_T = (3.5 \times 10^{-2}) R_X C_X f + 4 C_X f + 1 \times 10^{-5} C_L f$ $I_T = (8.0 \times 10^{-2}) R_X C_X f + 9 C_X f + 2 \times 10^{-5} C_L f$ $I_T = (1.25 \times 10^{-1}) R_X C_X f + 12 C_X f + 3 \times 10^{-5} C_L f$ where: I <sub>T</sub> in μA (one monostable switching only), C <sub>X</sub> in μF, C <sub>L</sub> in pF, R <sub>X</sub> in k ohms, and f in Hz is the input frequency.							μA	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

3. The formulas given are for the typical characteristics only at 25°C.

## OPERATING CONDITIONS

External Timing Resistance	R <sub>X</sub>	-	5.0	-	(Note 4)	kΩ
External Timing Capacitance	C <sub>X</sub>	-	0	-	No Limit (Note 5)	μF

4. The maximum usable resistance R<sub>X</sub> is a function of the leakage of the capacitor C<sub>X</sub>, leakage of the MC14538B, and leakage due to board layout and surface resistance. Susceptibility to externally induced noise signals may occur for R<sub>X</sub> > 1 MΩ.

5. If C<sub>X</sub> > 15 μF, use discharge protection diode per Fig. 11.

# MC14538B

## SWITCHING CHARACTERISTICS (Note 6) ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$ Vdc	All Types			Unit
			Min	Typ (Note 7)	Max	
Output Rise Time $t_{TLH} = (1.35 \text{ ns/pF}) C_L + 33 \text{ ns}$ $t_{TLH} = (0.60 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{TLH} = (0.40 \text{ ns/pF}) C_L + 20 \text{ ns}$	$t_{TLH}$	5.0 10 15	– – –	100 50 40	200 100 80	ns
Output Fall Time $t_{THL} = (1.35 \text{ ns/pF}) C_L + 33 \text{ ns}$ $t_{THL} = (0.60 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{THL} = (0.40 \text{ ns/pF}) C_L + 20 \text{ ns}$	$t_{THL}$	5.0 10 15	– – –	100 50 40	200 100 80	ns
Propagation Delay Time A or B to Q or $\bar{Q}$ $t_{PLH}, t_{PHL} = (0.90 \text{ ns/pF}) C_L + 255 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.36 \text{ ns/pF}) C_L + 132 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.26 \text{ ns/pF}) C_L + 87 \text{ ns}$	$t_{PLH},$ $t_{PHL}$	5.0 10 15	– – –	300 150 100	600 300 220	ns
Reset to Q or $\bar{Q}$ $t_{PLH}, t_{PHL} = (0.90 \text{ ns/pF}) C_L + 205 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.36 \text{ ns/pF}) C_L + 107 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.26 \text{ ns/pF}) C_L + 82 \text{ ns}$		5.0 10 15	– – –	250 125 95	500 250 190	ns
Input Rise and Fall Times Reset	$t_r, t_f$	5 10 15	– – –	– – –	15 5 4	$\mu\text{s}$
B Input		5 10 15	– – –	300 1.2 0.4	1.0 0.1 0.05	ms
A Input		5 10 15	No Limit			–
Input Pulse Width A, B, or Reset	$t_{WH},$ $t_{WL}$	5.0 10 15	170 90 80	85 45 40	– – –	ns
Retrigger Time	$t_{rr}$	5.0 10 15	0 0 0	– – –	– – –	ns
Output Pulse Width — Q or $\bar{Q}$ Refer to Figures 8 and 9 $C_X = 0.002 \mu\text{F}, R_X = 100 \text{ k}\Omega$	T	5.0 10 15	198 200 202	210 212 214	230 232 234	$\mu\text{s}$
$C_X = 0.1 \mu\text{F}, R_X = 100 \text{ k}\Omega$		5.0 10 15	9.3 9.4 9.5	9.86 10 10.14	10.5 10.6 10.7	ms
$C_X = 10 \mu\text{F}, R_X = 100 \text{ k}\Omega$		5.0 10 15	0.91 0.92 0.93	0.965 0.98 0.99	1.03 1.04 1.06	s
Pulse Width Match between circuits in the same package. $C_X = 0.1 \mu\text{F}, R_X = 100 \text{ k}\Omega$	100 [[ $T_1 - T_2$ ]/ $T_1$ ]	5.0 10 15	– – –	$\pm 1.0$ $\pm 1.0$ $\pm 1.0$	$\pm 5.0$ $\pm 5.0$ $\pm 5.0$	%

6. The formulas given are for the typical characteristics only at  $25^\circ\text{C}$ .

7. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

# MC14538B

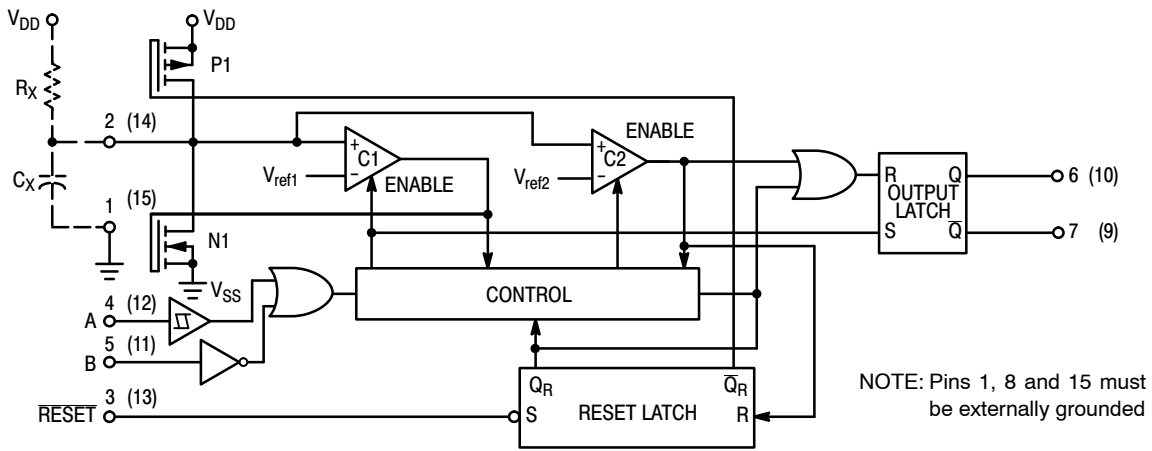


Figure 1. Logic Diagram  
(1/2 of Device Shown)

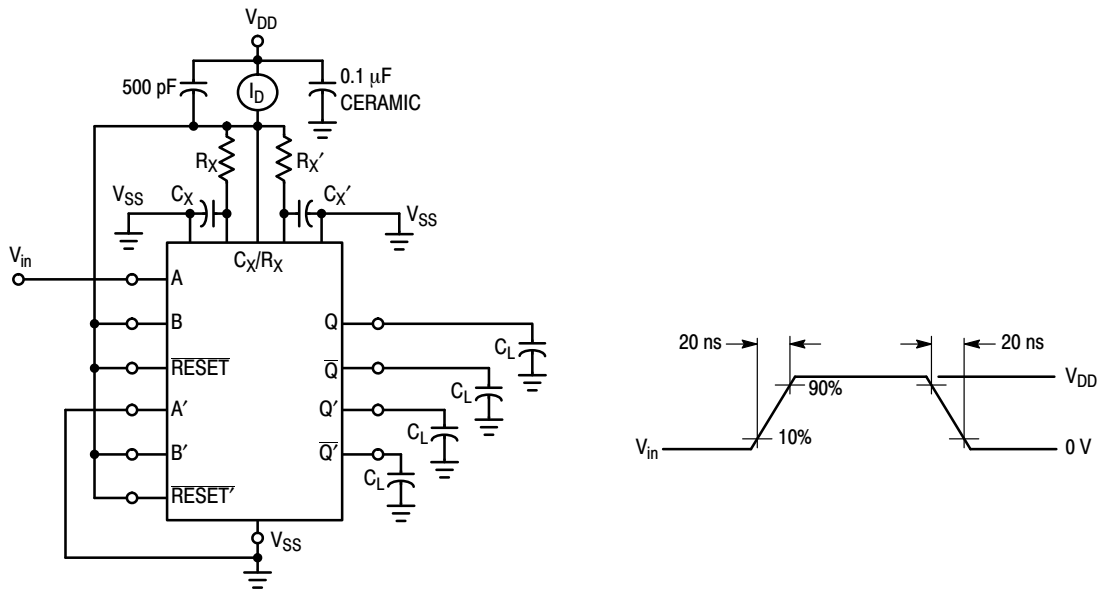
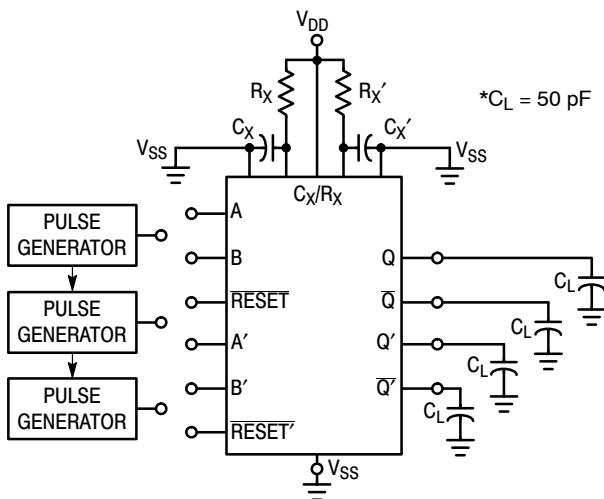


Figure 2. Power Dissipation Test Circuit and Waveforms



### INPUT CONNECTIONS

Characteristics	Reset	A	B
$t_{PLH}$ , $t_{PHL}$ , $t_{TLH}$ , $t_{THL}$ , $T$ , $t_{WH}$ , $t_{WL}$	$V_{DD}$	PG1	$V_{DD}$
$t_{PLH}$ , $t_{PHL}$ , $t_{TLH}$ , $t_{THL}$ , $T$ , $t_{WH}$ , $t_{WL}$	$V_{DD}$	$V_{SS}$	PG2
$t_{PLH(R)}$ , $t_{PHL(R)}$ , $t_{WH}$ , $t_{WL}$	PG3	PG1	PG2

\*Includes capacitance of probes, wiring, and fixture parasitic.

NOTE: Switching test waveforms for PG1, PG2, PG3 are shown in Figure 4.

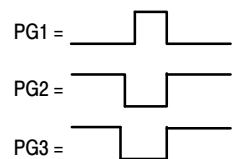


Figure 3. Switching Test Circuit

# MC14538B

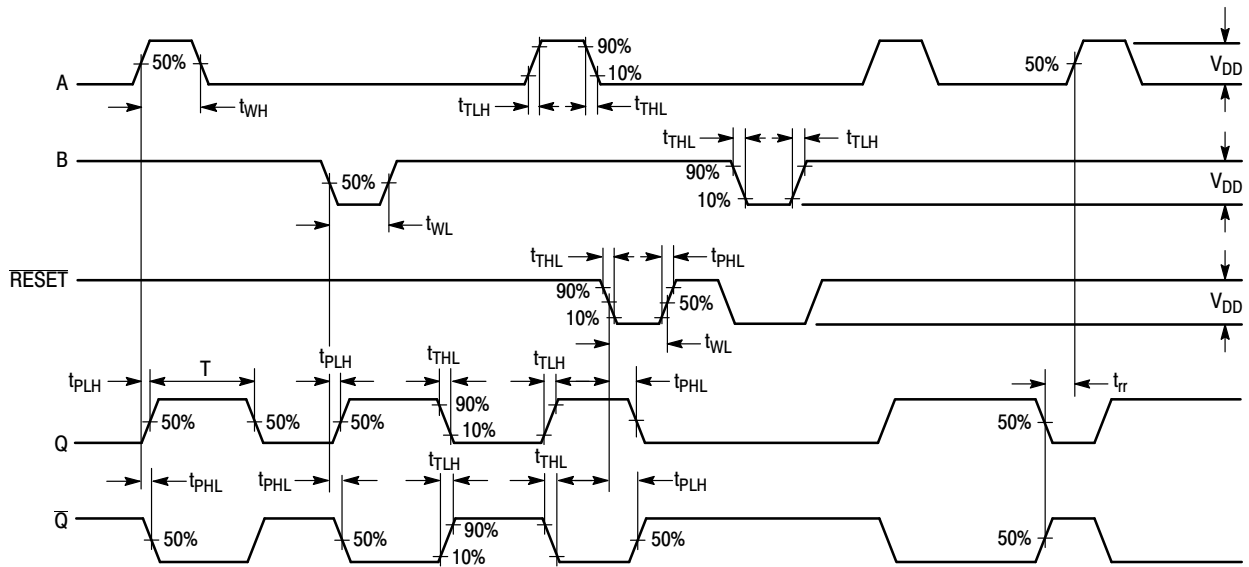


Figure 4. Switching Test Waveforms

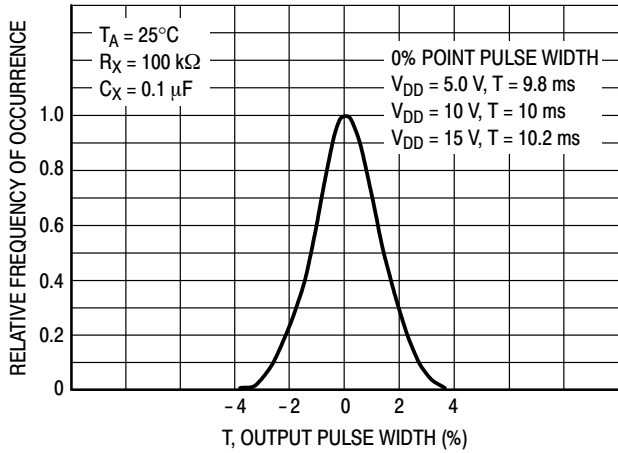


Figure 5. Typical Normalized Distribution of Units for Output Pulse Width

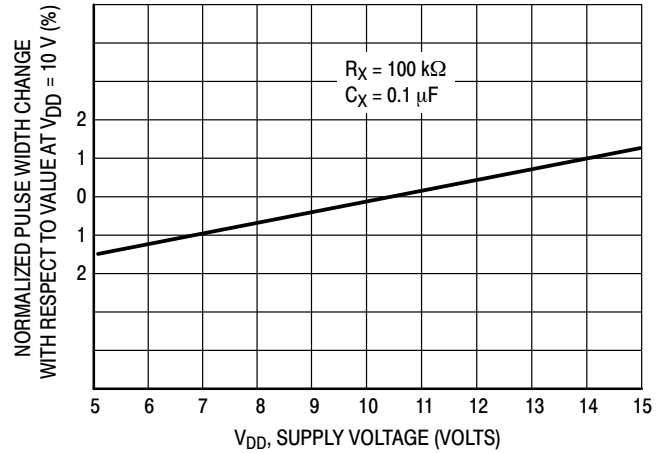


Figure 6. Typical Pulse Width Variation as a Function of Supply Voltage  $V_{DD}$

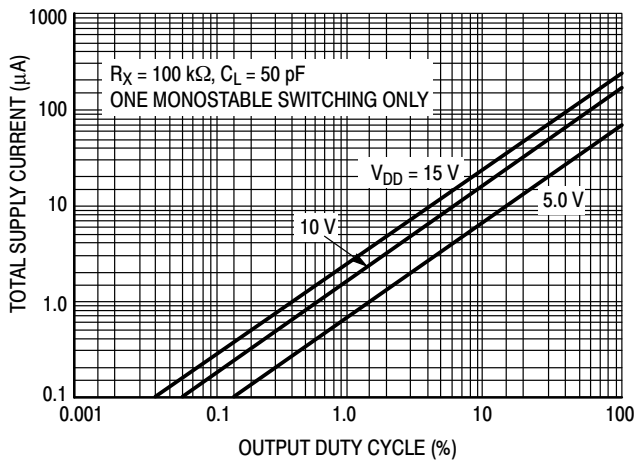


Figure 7. Typical Total Supply Current versus Output Duty Cycle

## FUNCTION TABLE

Inputs			Outputs	
Reset	A	B	Q	$\bar{Q}$
H		H		
H	L			
H		L	Not Triggered	Not Triggered
H	H		Not Triggered	Not Triggered
H	L, H,	H	Not Triggered	Not Triggered
H	L	L, H,	Not Triggered	Not Triggered
L	X	X	L	H
	X	X	Not Triggered	Not Triggered

# MC14538B



**Figure 8. Typical Error of Pulse Width Equation versus Temperature**



**Figure 9. Typical Error of Pulse Width Equation versus Temperature**

## THEORY OF OPERATION



**Figure 10. Timing Operation**

**TRIGGER OPERATION**

The block diagram of the MC14538B is shown in Figure 1, with circuit operation following.

As shown in Figure 1 and 10, before an input trigger occurs, the monostable is in the quiescent state with the Q output low, and the timing capacitor  $C_X$  completely charged to  $V_{DD}$ . When the trigger input A goes from  $V_{SS}$  to  $V_{DD}$  (while inputs B and  $\overline{\text{Reset}}$  are held to  $V_{DD}$ ) a valid trigger is recognized, which turns on comparator C1 and N-channel transistor N1 ①. At the same time the output latch is set. With transistor N1 on, the capacitor  $C_X$  rapidly discharges toward  $V_{SS}$  until  $V_{ref1}$  is reached. At this point the output of comparator C1 changes state and transistor N1 turns off. Comparator C1 then turns off while at the same time comparator C2 turns on. With transistor N1 off, the capacitor  $C_X$  begins to charge through the timing resistor,  $R_X$ , toward  $V_{DD}$ . When the voltage across  $C_X$  equals  $V_{ref2}$ , comparator C2 changes state, causing the output latch to reset (Q goes low) while at the same time disabling comparator C2 ②. This ends at the timing cycle with the monostable in the quiescent state, waiting for the next trigger.

In the quiescent state,  $C_X$  is fully charged to  $V_{DD}$  causing the current through resistor  $R_X$  to be zero. Both comparators are “off” with total device current due only to reverse junction leakages. An added feature of the MC14538B is that the output latch is set via the input trigger without regard to the capacitor voltage. Thus, propagation delay from trigger to Q is independent of the value of  $C_X$ ,  $R_X$ , or the duty cycle of the input waveform.

**RETRIGGER OPERATION**

The MC14538B is retriggered if a valid trigger occurs ③ followed by another valid trigger ④ before the Q output has returned to the quiescent (zero) state. Any retrigger, after the timing node voltage at pin 2 or 14 has begun to rise from  $V_{ref1}$ , but has not yet reached  $V_{ref2}$ , will cause an increase in output pulse width T. When a valid retrigger is initiated ④, the voltage at  $C_X/R_X$  will again drop to  $V_{ref1}$  before progressing along the RC charging curve toward  $V_{DD}$ . The Q output will remain high until time T, after the last valid retrigger.

**RESET OPERATION**

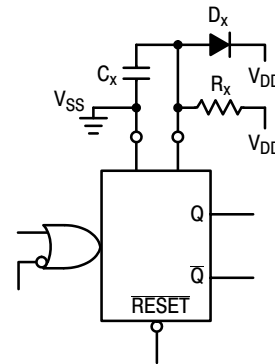
The MC14538B may be reset during the generation of the output pulse. In the reset mode of operation, an input pulse

on  $\overline{\text{Reset}}$  sets the reset latch and causes the capacitor to be fast charged to  $V_{DD}$  by turning on transistor P1 ⑤. When the voltage on the capacitor reaches  $V_{ref2}$ , the reset latch will clear, and will then be ready to accept another pulse. If the  $\overline{\text{Reset}}$  input is held low, any trigger inputs that occur will be inhibited and the Q and  $\overline{Q}$  outputs of the output latch will not change. Since the Q output is reset when an input low level is detected on the  $\overline{\text{Reset}}$  input, the output pulse T can be made significantly shorter than the minimum pulse width specification.

**POWER-DOWN CONSIDERATIONS**

Large capacitance values can cause problems due to the large amount of energy stored. When a system containing the MC14538B is powered down, the capacitor voltage may discharge from  $V_{DD}$  through the standard protection diodes at pin 2 or 14. Current through the protection diodes should be limited to 10 mA and therefore the discharge time of the  $V_{DD}$  supply must not be faster than  $(V_{DD}) \cdot (C)/(10 \text{ mA})$ . For example, if  $V_{DD} = 10 \text{ V}$  and  $C_X = 10 \mu\text{F}$ , the  $V_{DD}$  supply should discharge no faster than  $(10 \text{ V}) \times (10 \mu\text{F})/(10 \text{ mA}) = 10 \text{ ms}$ . This is normally not a problem since power supplies are heavily filtered and cannot discharge at this rate.

When a more rapid decrease of  $V_{DD}$  to zero volts occurs, the MC14538B can sustain damage. To avoid this possibility use an external clamping diode,  $D_X$ , connected as shown in Fig. 11.

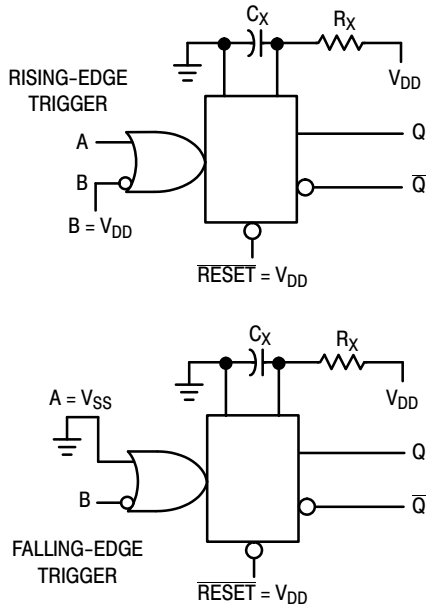


**Figure 11. Use of a Diode to Limit Power Down Current Surge**

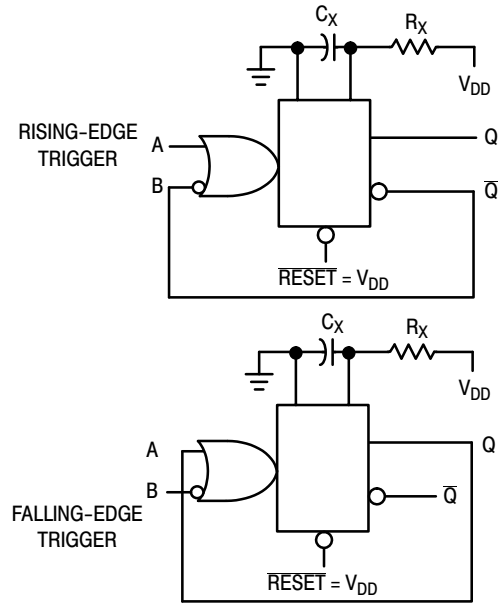


# MC14538B

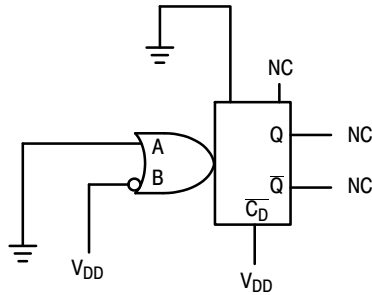
## TYPICAL APPLICATIONS



**Figure 12. Retriggerable Monostables Circuitry**



**Figure 13. Non-Retriggerable Monostables Circuitry**



**Figure 14. Connection of Unused Sections**

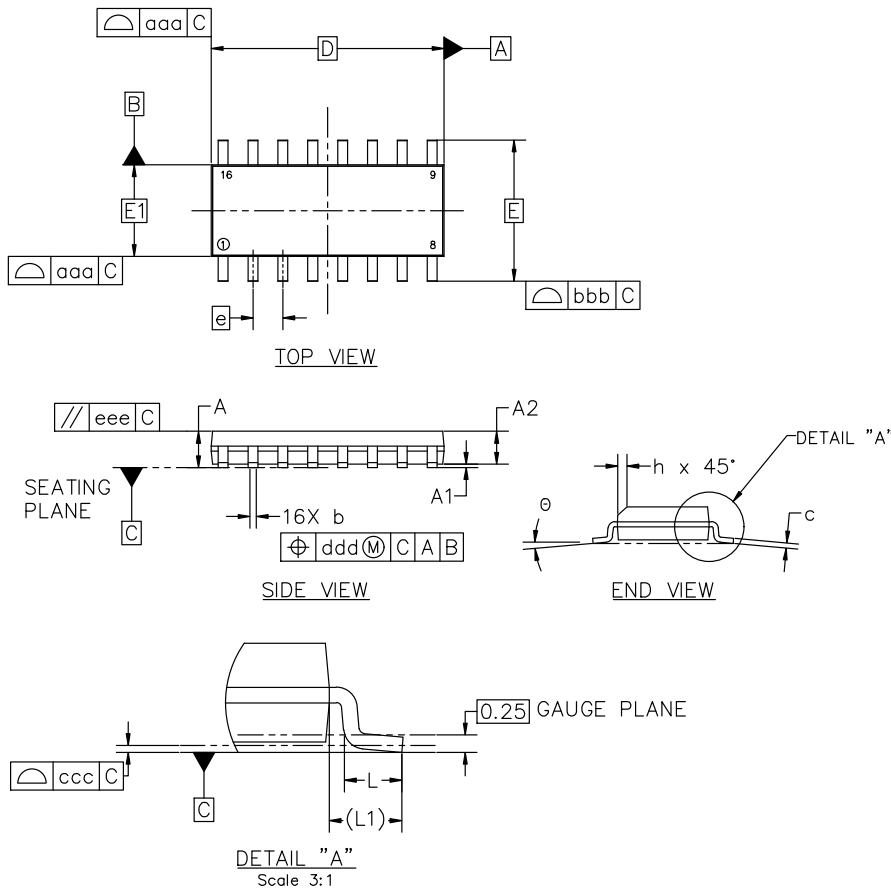


SOIC-16 9.90x3.90x1.50 1.27P  
CASE 751B  
ISSUE L

DATE 29 MAY 2024

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.00	0.05	0.10
A2	1.35	1.50	1.65
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	---	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
θ	0°	---	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



RECOMMENDED MOUNTING FOOTPRINT

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

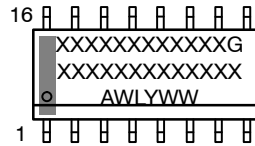
<b>DOCUMENT NUMBER:</b>	<b>98ASB42566B</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>SOIC-16 9.90X3.90X1.50 1.27P</b>	<b>PAGE 1 OF 2</b>

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SOIC-16 9.90x3.90x1.50 1.27P  
CASE 751B  
ISSUE L

DATE 29 MAY 2024

GENERIC  
MARKING DIAGRAM\*



XXXXX = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
Y = Year  
WW = Work Week  
G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

<p>STYLE 1:</p> <p>PIN 1. COLLECTOR</p> <p>2. BASE</p> <p>3. EMITTER</p> <p>4. NO CONNECTION</p> <p>5. EMITTER</p> <p>6. BASE</p> <p>7. COLLECTOR</p> <p>8. COLLECTOR</p> <p>9. BASE</p> <p>10. EMITTER</p> <p>11. NO CONNECTION</p> <p>12. EMITTER</p> <p>13. BASE</p> <p>14. COLLECTOR</p> <p>15. EMITTER</p> <p>16. COLLECTOR</p>	<p>STYLE 2:</p> <p>PIN 1. CATHODE</p> <p>2. ANODE</p> <p>3. NO CONNECTION</p> <p>4. CATHODE</p> <p>5. CATHODE</p> <p>6. NO CONNECTION</p> <p>7. ANODE</p> <p>8. CATHODE</p> <p>9. CATHODE</p> <p>10. ANODE</p> <p>11. NO CONNECTION</p> <p>12. CATHODE</p> <p>13. CATHODE</p> <p>14. NO CONNECTION</p> <p>15. ANODE</p> <p>16. CATHODE</p>	<p>STYLE 3:</p> <p>PIN 1. COLLECTOR, DYE #1</p> <p>2. BASE, #1</p> <p>3. EMITTER, #1</p> <p>4. COLLECTOR, #1</p> <p>5. COLLECTOR, #2</p> <p>6. BASE, #2</p> <p>7. EMITTER, #2</p> <p>8. COLLECTOR, #2</p> <p>9. COLLECTOR, #3</p> <p>10. BASE, #3</p> <p>11. EMITTER, #3</p> <p>12. COLLECTOR, #3</p> <p>13. COLLECTOR, #4</p> <p>14. BASE, #4</p> <p>15. EMITTER, #4</p> <p>16. COLLECTOR, #4</p>	<p>STYLE 4:</p> <p>PIN 1. COLLECTOR, DYE #1</p> <p>2. COLLECTOR, #1</p> <p>3. COLLECTOR, #2</p> <p>4. COLLECTOR, #2</p> <p>5. COLLECTOR, #3</p> <p>6. COLLECTOR, #3</p> <p>7. COLLECTOR, #4</p> <p>8. COLLECTOR, #4</p> <p>9. BASE, #4</p> <p>10. EMITTER, #4</p> <p>11. BASE, #3</p> <p>12. EMITTER, #3</p> <p>13. BASE, #2</p> <p>14. EMITTER, #2</p> <p>15. BASE, #1</p> <p>16. EMITTER, #1</p>
<p>STYLE 5:</p> <p>PIN 1. DRAIN, DYE #1</p> <p>2. DRAIN, #1</p> <p>3. DRAIN, #2</p> <p>4. DRAIN, #2</p> <p>5. DRAIN, #3</p> <p>6. DRAIN, #3</p> <p>7. DRAIN, #4</p> <p>8. DRAIN, #4</p> <p>9. GATE, #4</p> <p>10. SOURCE, #4</p> <p>11. GATE, #3</p> <p>12. SOURCE, #3</p> <p>13. GATE, #2</p> <p>14. SOURCE, #2</p> <p>15. GATE, #1</p> <p>16. SOURCE, #1</p>	<p>STYLE 6:</p> <p>PIN 1. CATHODE</p> <p>2. CATHODE</p> <p>3. CATHODE</p> <p>4. CATHODE</p> <p>5. CATHODE</p> <p>6. CATHODE</p> <p>7. CATHODE</p> <p>8. CATHODE</p> <p>9. ANODE</p> <p>10. ANODE</p> <p>11. ANODE</p> <p>12. ANODE</p> <p>13. ANODE</p> <p>14. ANODE</p> <p>15. ANODE</p> <p>16. ANODE</p>	<p>STYLE 7:</p> <p>PIN 1. SOURCE N-CH</p> <p>2. COMMON DRAIN (OUTPUT)</p> <p>3. COMMON DRAIN (OUTPUT)</p> <p>4. GATE P-CH</p> <p>5. COMMON DRAIN (OUTPUT)</p> <p>6. COMMON DRAIN (OUTPUT)</p> <p>7. COMMON DRAIN (OUTPUT)</p> <p>8. SOURCE P-CH</p> <p>9. SOURCE P-CH</p> <p>10. COMMON DRAIN (OUTPUT)</p> <p>11. COMMON DRAIN (OUTPUT)</p> <p>12. COMMON DRAIN (OUTPUT)</p> <p>13. GATE N-CH</p> <p>14. COMMON DRAIN (OUTPUT)</p> <p>15. COMMON DRAIN (OUTPUT)</p> <p>16. SOURCE N-CH</p>	

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<b>DESCRIPTION:</b>	<b>SOIC-16 9.90X3.90X1.50 1.27P</b>	<b>PAGE 2 OF 2</b>

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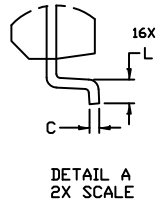
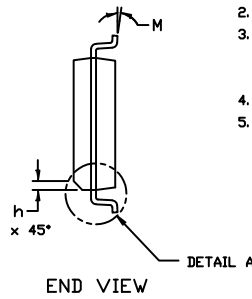
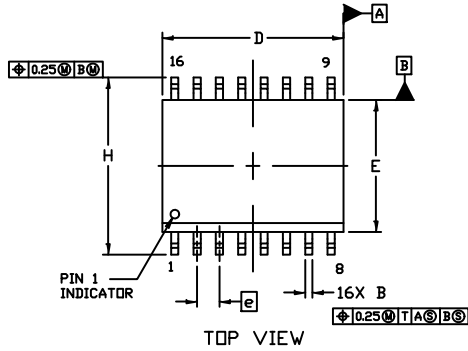
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



1  
SCALE 1:1

SOIC-16 WB  
CASE 751G  
ISSUE E

DATE 08 OCT 2021

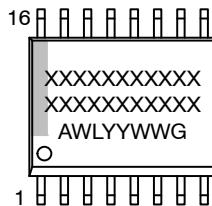


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION OR FLASH TO BE 0.15 PER SIDE.

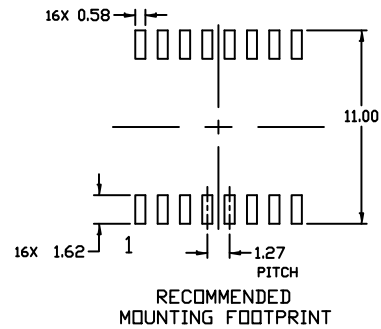
DIM	MILLIMETERS	
	MIN.	MAX.
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.53 REF	
L	0.50	0.90
M	0°	7°

GENERIC MARKING DIAGRAM\*



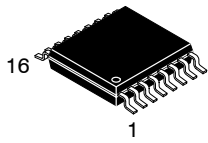
- XXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



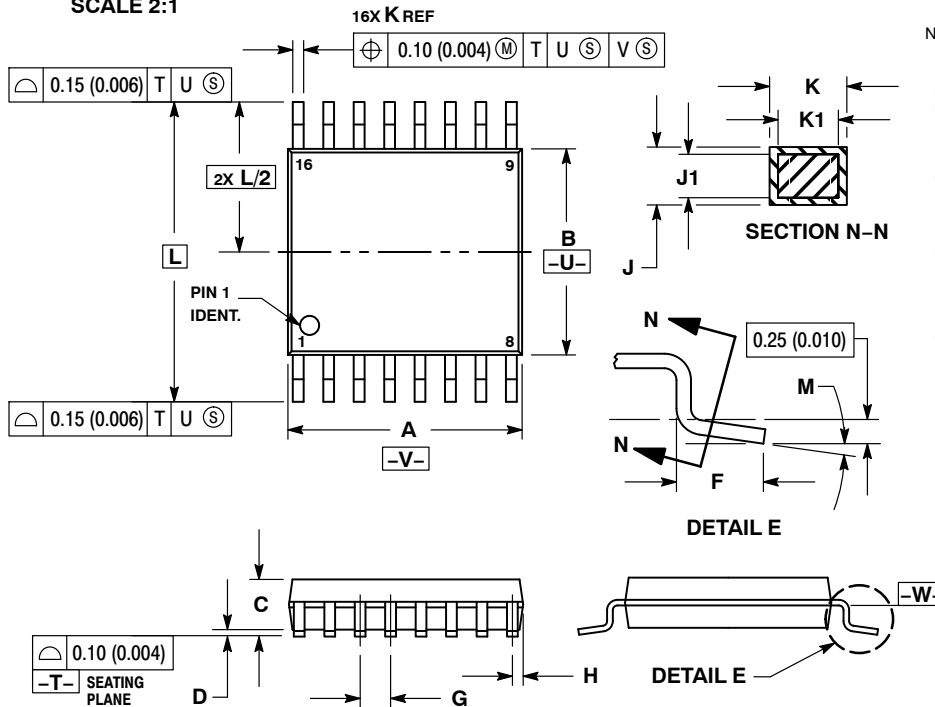
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DESCRIPTION:	SOIC-16 WB	PAGE 1 OF 1

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TSSOP-16 WB  
CASE 948F  
ISSUE B

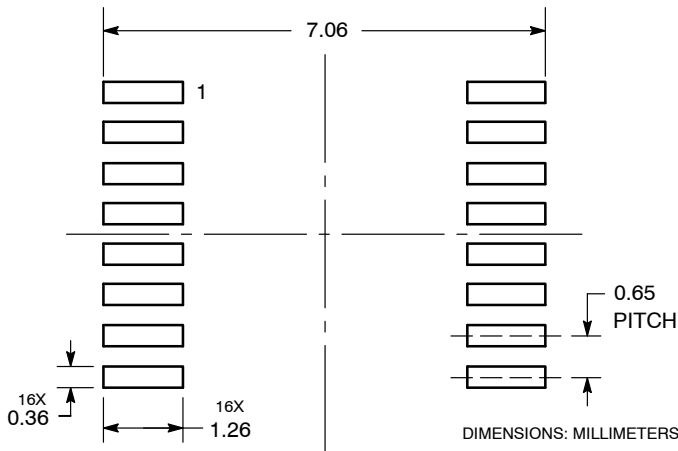
DATE 19 OCT 2006



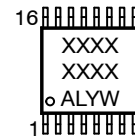
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
  4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
  5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
  7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

RECOMMENDED  
SOLDERING FOOTPRINT\*



GENERIC  
MARKING DIAGRAM\*



- XXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- G or ■ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

\*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	TSSOP-16	PAGE 1 OF 1

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