Configurable Multiple-Function Gate

Check for Samples: SN74LVC1G98

FEATURES

- **Available in the Texas Instruments NanoFree™ Package**
- **Supports 5-V V_{CC} Operation**
- **Inputs Accept Voltages to 5.5 V**
- **Supports Down Translation to V_{CC}**
- **Max t_{pd} of 6.3 ns at 3.3 V**
- **Low Power Consumption, 10-μA Max I_{CC}**
- **±24-mA Output Drive at 3.3 V**
- **I_{off} Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

DESCRIPTION

This configurable multiple-function gate is designed for 1.65-V to 5.5-V V_{CC} operation.

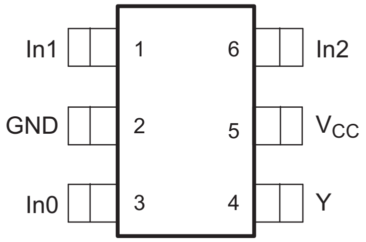
The SN74LVC1G98 device features configurable multiple functions. The output state is determined by eight patterns of 3-bit input. The user can choose the logic functions MUX, AND, OR, NAND, NOR, inverter, and noninverter. All inputs can be connected to V_{CC} or GND.

This device functions as an independent gate, but because of Schmitt action, it may have different input threshold levels for positive-going (V_{T+}) and negative-going (V_{T-}) signals.

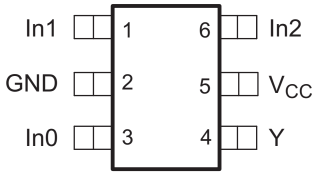
NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

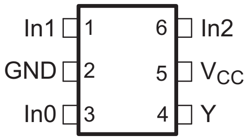
DBV PACKAGE
(TOP VIEW)



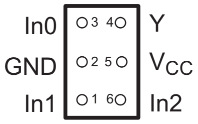
DCK PACKAGE
(TOP VIEW)



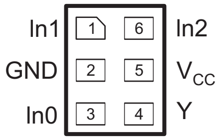
DRL PACKAGE
(TOP VIEW)



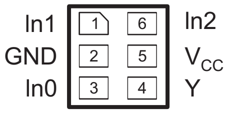
YZP PACKAGE
(BOTTOM VIEW)



DRY PACKAGE
(TOP VIEW)



DSF PACKAGE
(TOP VIEW)



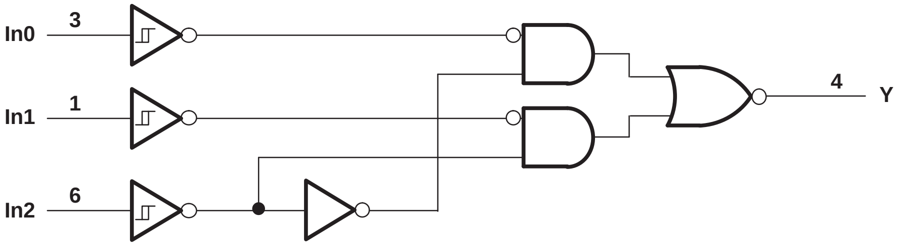
See mechanical drawings for dimensions.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Function Table

INPUTS			OUTPUT Y
In2	In1	In0	
L	L	L	H
L	L	H	H
L	H	L	L
L	H	H	L
H	L	L	H
H	L	H	L
H	H	L	H
H	H	H	L

Logic Diagram (Positive Logic)



Function Selection Table

LOGIC FUNCTION	FIGURE NO.
2-to-1 data selector with inverted output	Figure 1
2-input NAND gate	Figure 2
2-input NOR gate with one inverted input	Figure 3
2-input AND gate with one inverted input	Figure 3
2-input NAND gate with one inverted input	Figure 4
2-input OR gate with one inverted input	Figure 4
2-input NOR gate	Figure 5
Noninverted buffer	Figure 6
Inverter	Figure 7

Logic Configurations

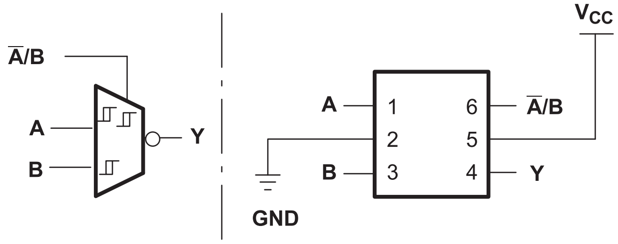


Figure 1. 2-to-1 Data Selector With Inverted Output

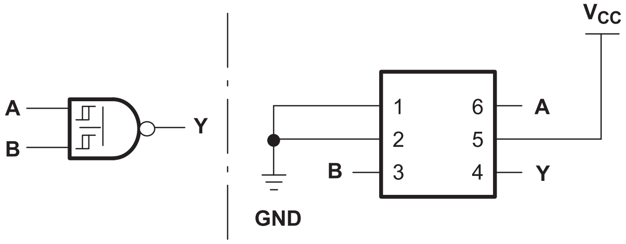


Figure 2. 2-Input NAND Gate

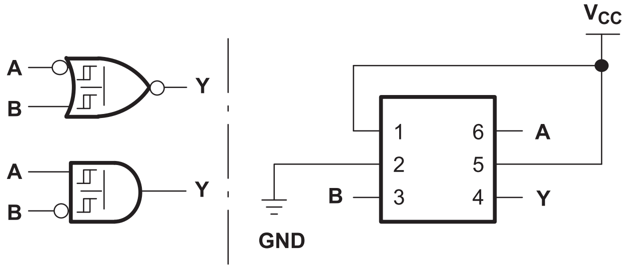


Figure 3. 2-Input NOR Gate With One Inverted Input 2-Input AND Gate With One Inverted Input

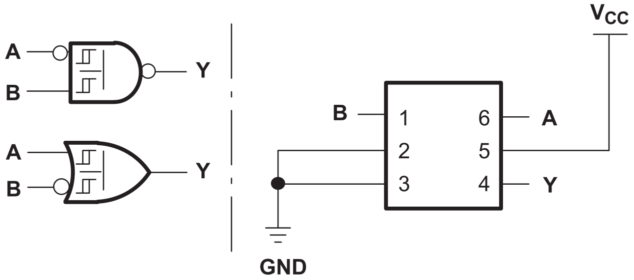


Figure 4. 2-Input NAND Gate With One Inverted Input 2-Input OR Gate With One Inverted Input

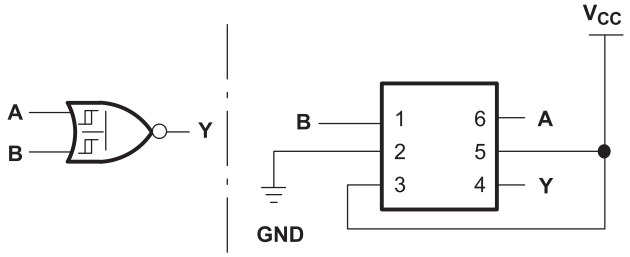


Figure 5. 2-Input NOR Gate

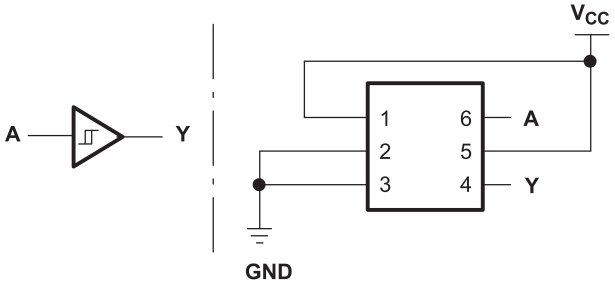


Figure 6. Noninverted Buffer

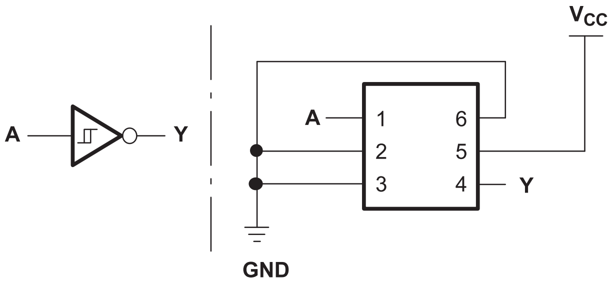


Figure 7. Inverter

Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	6.5	V
V_I	Input voltage range[2]		–0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state[2][3]		–0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance[4]	DBV package		165	°C/W
		DCK package		259	
		DRL package		142	
		YZP package		123	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CC} is provided in the recommended operating conditions table.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.65 V		–4	mA
		V_{CC} = 2.3 V		–8	
		V_{CC} = 3 V		–16	
				–24	
		V_{CC} = 4.5 V		–32	
I_{OL}	Low-level output current	V_{CC} = 1.65 V		4	mA
		V_{CC} = 2.3 V		8	
		V_{CC} = 3 V		16	
				24	
		V_{CC} = 4.5 V		32	
T_A	Operating free-air temperature		–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	–40°C to 85°C			–40°C to 125°C			UNIT
			MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
V_{T+} Positive-going input threshold voltage		1.65 V	0.79		1.16	0.79		1.16	V
		2.3 V	1.11		1.56	1.11		1.56	
		3 V	1.5		1.87	1.5		1.87	
		4.5 V	2.16		2.74	2.16		2.74	
		5.5 V	2.61		3.33	2.61		3.33	
V_{T-} Negative-going input threshold voltage		1.65 V	0.35		0.62	0.35		0.62	V
		2.3 V	0.58		0.87	0.58		0.87	
		3 V	0.84		1.19	0.84		1.19	
		4.5 V	1.41		1.9	1.41		1.9	
		5.5 V	1.87		2.29	1.87		2.29	
ΔV_T Hysteresis ($V_{T+} - V_{T-}$)		1.65 V	0.3		0.62	0.3		0.62	V
		2.3 V	0.4		0.8	0.4		0.8	
		3 V	0.53		0.87	0.53		0.87	
		4.5 V	0.71		1.04	0.71		1.04	
		5.5 V	0.71		1.11	0.71		1.11	
V_{OH}	I_{OH} = –100 µA	1.65 V to 5.5 V	V_{CC} – 0.1			V_{CC} – 0.1			V
	I_{OH} = –4 mA	1.65 V	1.2			1.2			
	I_{OH} = –8 mA	2.3 V	1.9			1.9			
	I_{OH} = –16 mA	3 V	2.4			2.4			
	I_{OH} = –24 mA		2.3			2.3			
	I_{OH} = –32 mA	4.5 V	3.8			3.8			
V_{OL}	I_{OL} = 100 µA	1.65 V to 5.5 V			0.1			0.1	V
	I_{OL} = 4 mA	1.65 V			0.45			0.45	
	I_{OL} = 8 mA	2.3 V			0.3			0.3	
	I_{OL} = 16 mA	3 V			0.4			0.45	
	I_{OL} = 24 mA				0.55			0.55	
	I_{OL} = 32 mA	4.5 V			0.55			0.58	
I_I	V_I = 5.5 V or GND	0 to 5.5 V			±5			±5	µA
I_{off}	V_I or V_O = 5.5 V	0			±10			±10	µA
I_{CC}	V_I = 5.5 V or GND, I_O = 0	1.65 V to 5.5 V			10			10	µA
ΔI_{CC}	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3 V to 5.5 V			500			500	µA
C_i	V_I = V_{CC} or GND	3.3 V		3.5			3.5		pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 8)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC1G98 –40°C to 85°C								UNIT
			V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Any In	Y	3.2	14.4	2	8.3	1.5	6.3	1.1	5.1	ns

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 8)

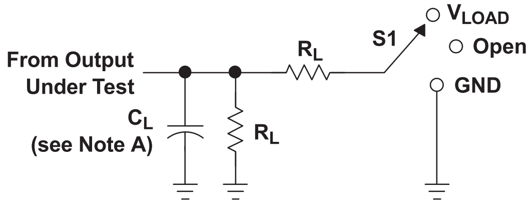
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC1G98 –40°C to 125°C								UNIT
			V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Any In	Y	3.2	16.4	2	9.3	1.5	7.3	1.1	6.1	ns

Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC} = 1.8 V	V_{CC} = 2.5 V	V_{CC} = 3.3 V	V_{CC} = 5 V	UNIT
			TYP	TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	f = 10 MHz	23	23	23	26	pF

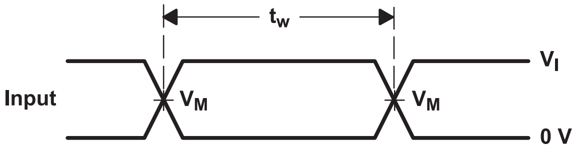
Parameter Measurement Information



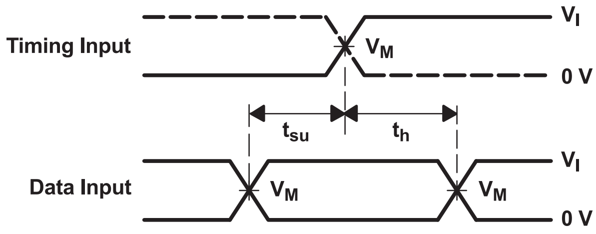
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

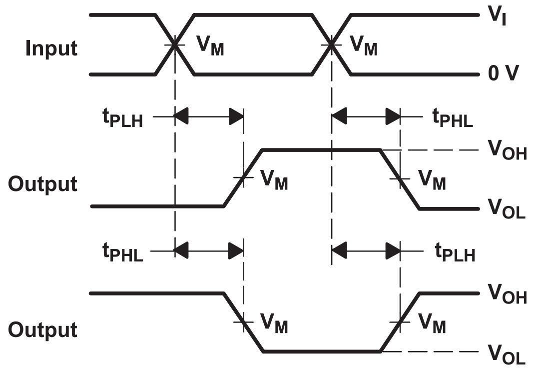
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_D
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	1 kW	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	500 W	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 W	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 W	0.3 V



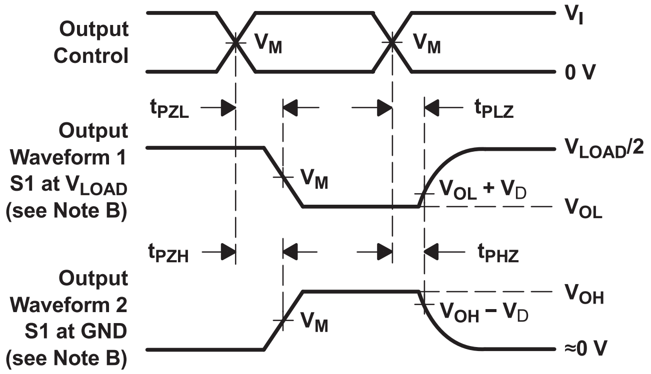
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 W.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. All parameters and waveforms are not applicable to all devices.

Figure 8. Load Circuit and Voltage Waveforms

REVISION HISTORY

Changes from Revision J (January 2007) to Revision K	Page
• Added DRY and DSF package and pin out to document.	1

Changes from Revision K (October 2011) to Revision L	Page
• Updated document to new TI data sheet format.	1
• Updated Features.	1
• Removed Ordering Information table.	1
• Added ESD warning.	2
• Updated operating temperature range.	4

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC1G98DBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C98O, C98R, C98S)	Samples
SN74LVC1G98DBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C98R, C98S)	Samples
SN74LVC1G98DCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(CWJ, CWR, CWS)	Samples
SN74LVC1G98DCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(CWJ, CWR, CWS)	Samples
SN74LVC1G98DCKTG4	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CWR	Samples
SN74LVC1G98DRLR	ACTIVE	SOT-5X3	DRL	6	4000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(1K5, CW7, CWR)	Samples
SN74LVC1G98DRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CW	Samples
SN74LVC1G98DSFR	ACTIVE	SON	DSF	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CW	Samples
SN74LVC1G98YZPR	ACTIVE	DSBGA	YZP	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	CWN	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN74LVC1G98 :

- Automotive : SN74LVC1G98-Q1

- Enhanced Product : SN74LVC1G98-EP

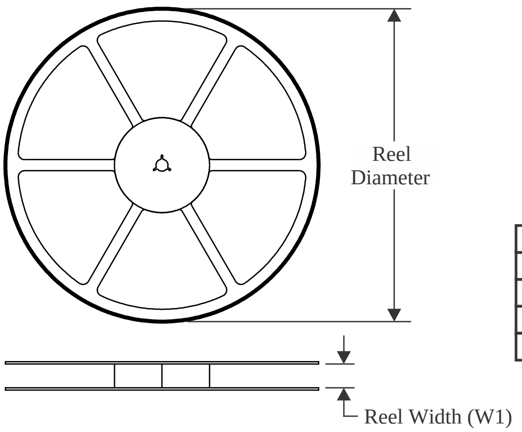
NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

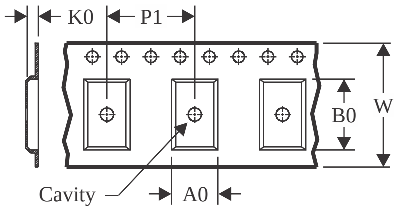
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

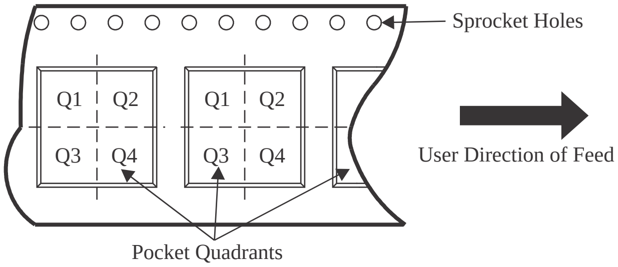


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

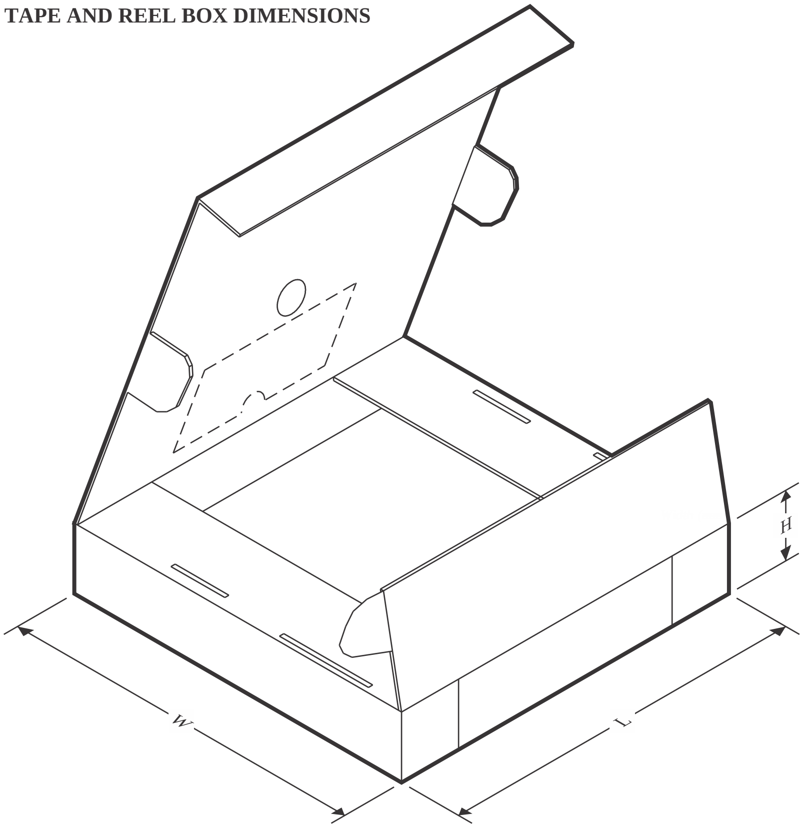
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G98DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G98DBVR	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G98DBVT	SOT-23	DBV	6	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G98DCKR	SC70	DCK	6	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
SN74LVC1G98DCKT	SC70	DCK	6	250	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
SN74LVC1G98DCKTG4	SC70	DCK	6	250	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74LVC1G98DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
SN74LVC1G98DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74LVC1G98DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74LVC1G98DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74LVC1G98YZPR	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



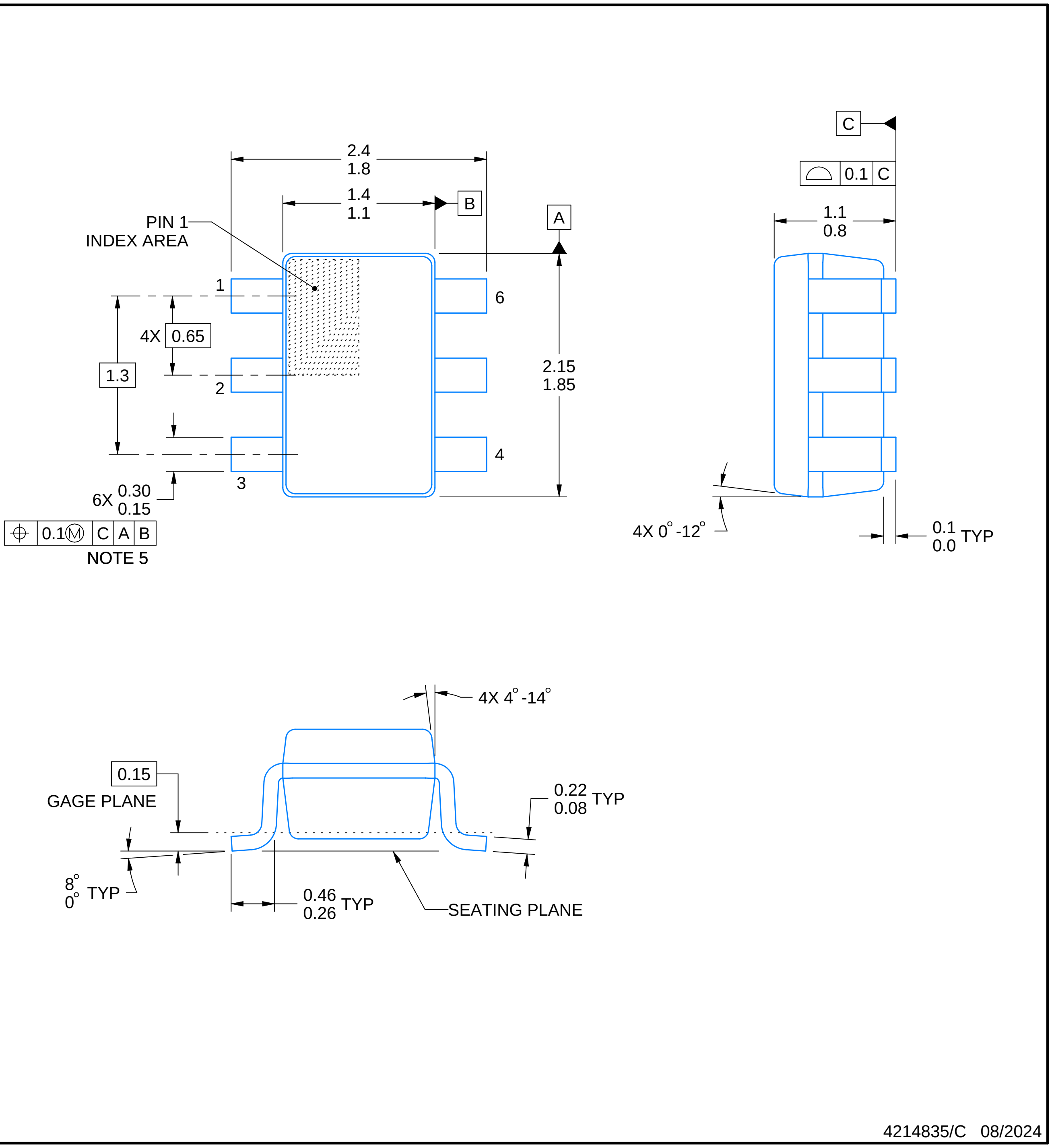
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G98DBVR	SOT-23	DBV	6	3000	202.0	201.0	28.0
SN74LVC1G98DBVR	SOT-23	DBV	6	3000	203.0	203.0	35.0
SN74LVC1G98DBVT	SOT-23	DBV	6	250	202.0	201.0	28.0
SN74LVC1G98DCKR	SC70	DCK	6	3000	210.0	185.0	35.0
SN74LVC1G98DCKT	SC70	DCK	6	250	210.0	185.0	35.0
SN74LVC1G98DCKTG4	SC70	DCK	6	250	183.0	183.0	20.0
SN74LVC1G98DRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
SN74LVC1G98DRLR	SOT-5X3	DRL	6	4000	202.0	201.0	28.0
SN74LVC1G98DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74LVC1G98DSFR	SON	DSF	6	5000	184.0	184.0	19.0
SN74LVC1G98YZPR	DSBGA	YZP	6	3000	220.0	220.0	35.0

PACKAGE OUTLINE

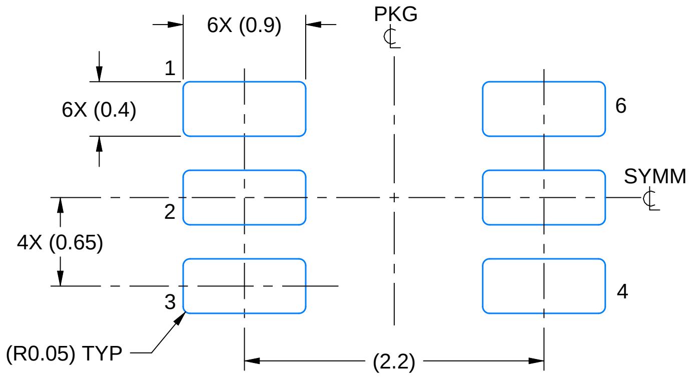
SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR

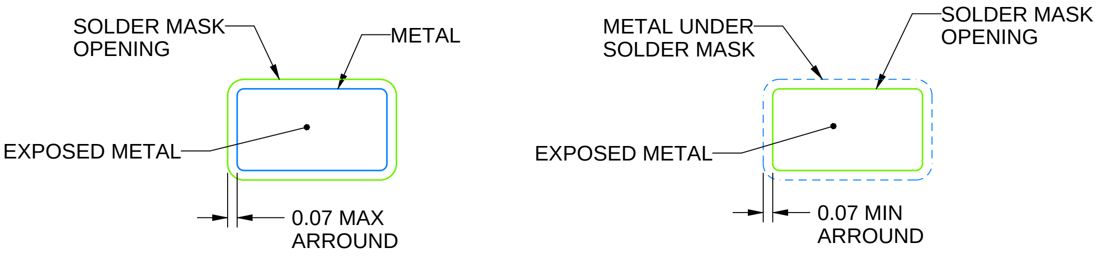


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



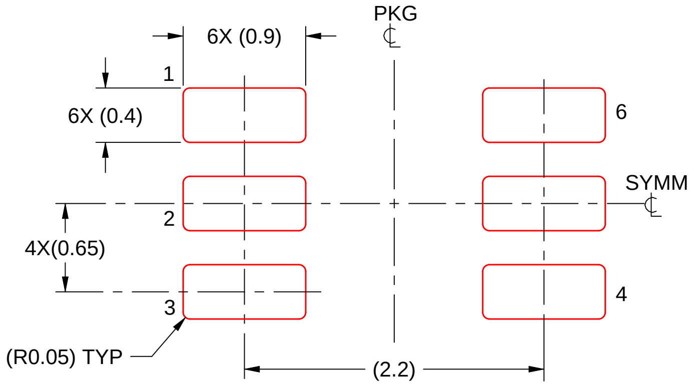
NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

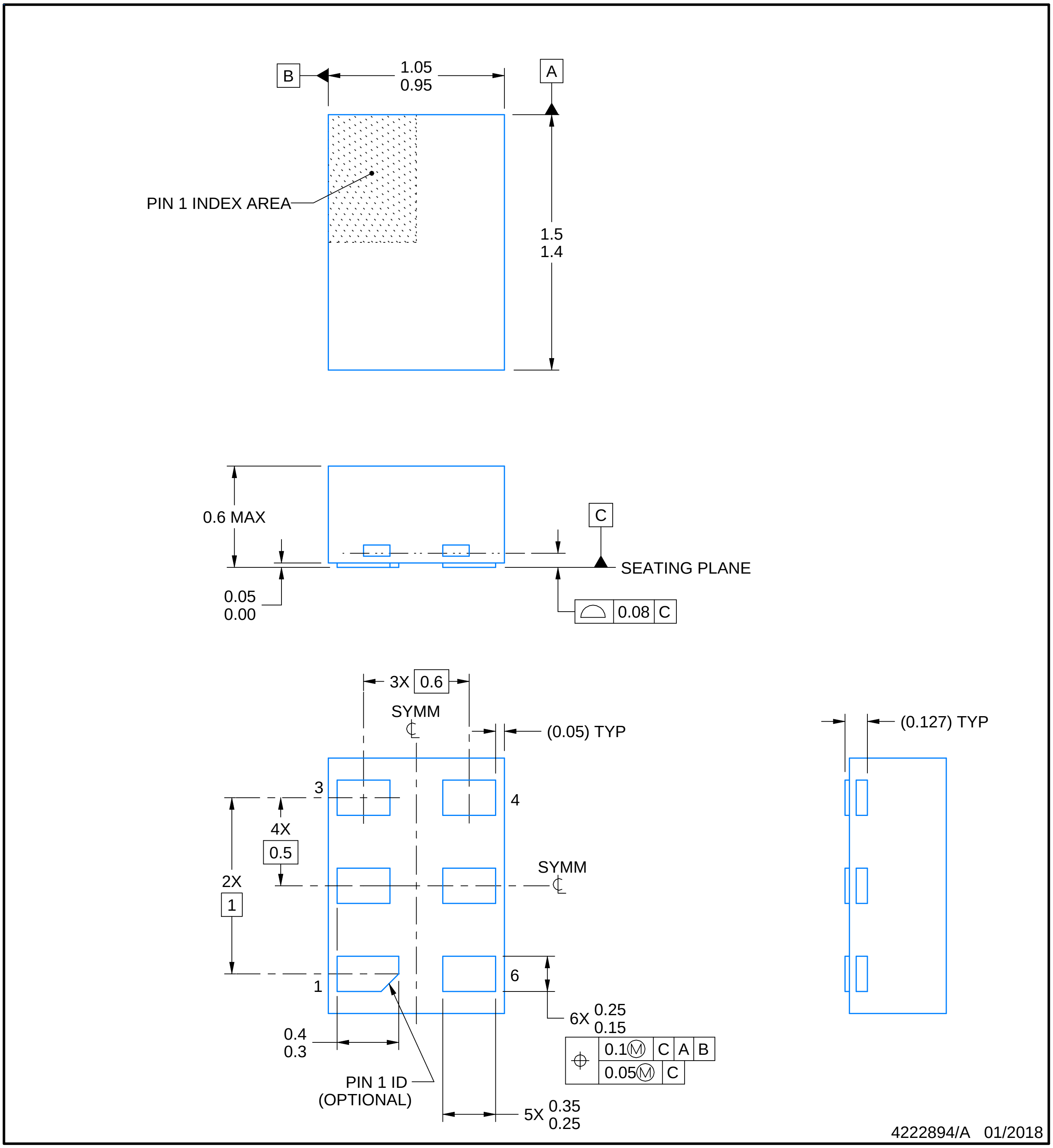
GENERIC PACKAGE VIEW

DRY 6 **USON - 0.6 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

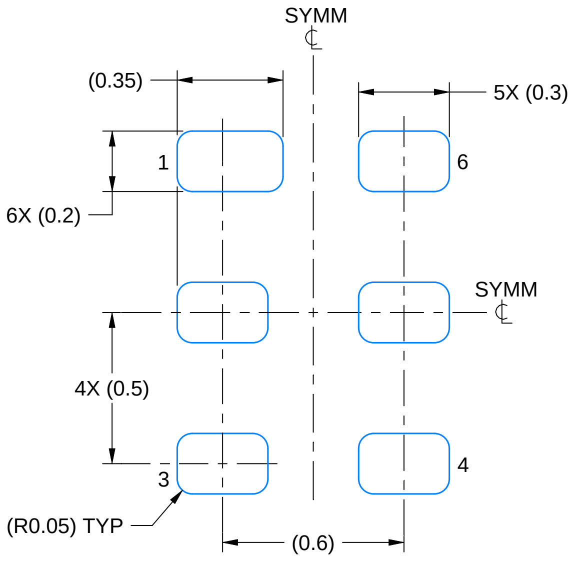
4207181/G



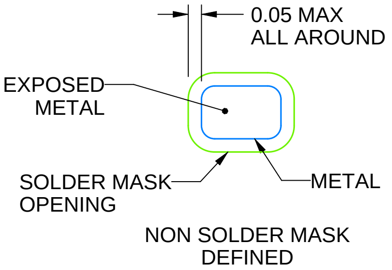
4222894/A 01/2018

NOTES:

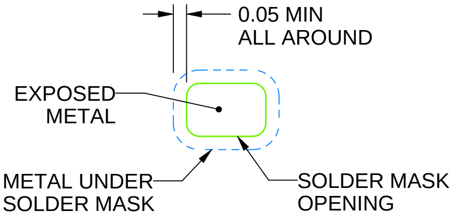
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X



NON SOLDER MASK
DEFINED



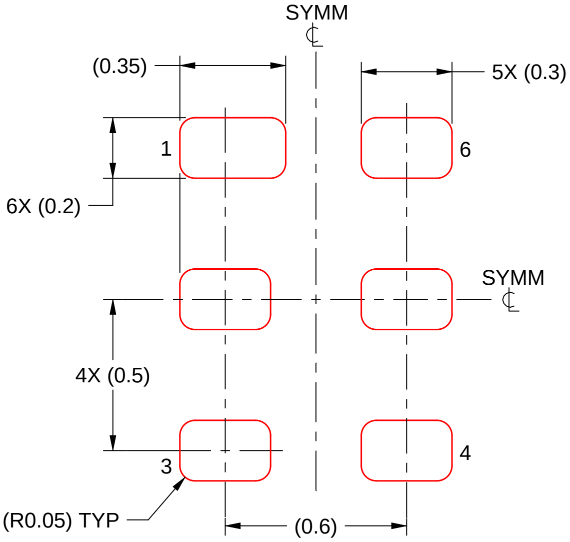
SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

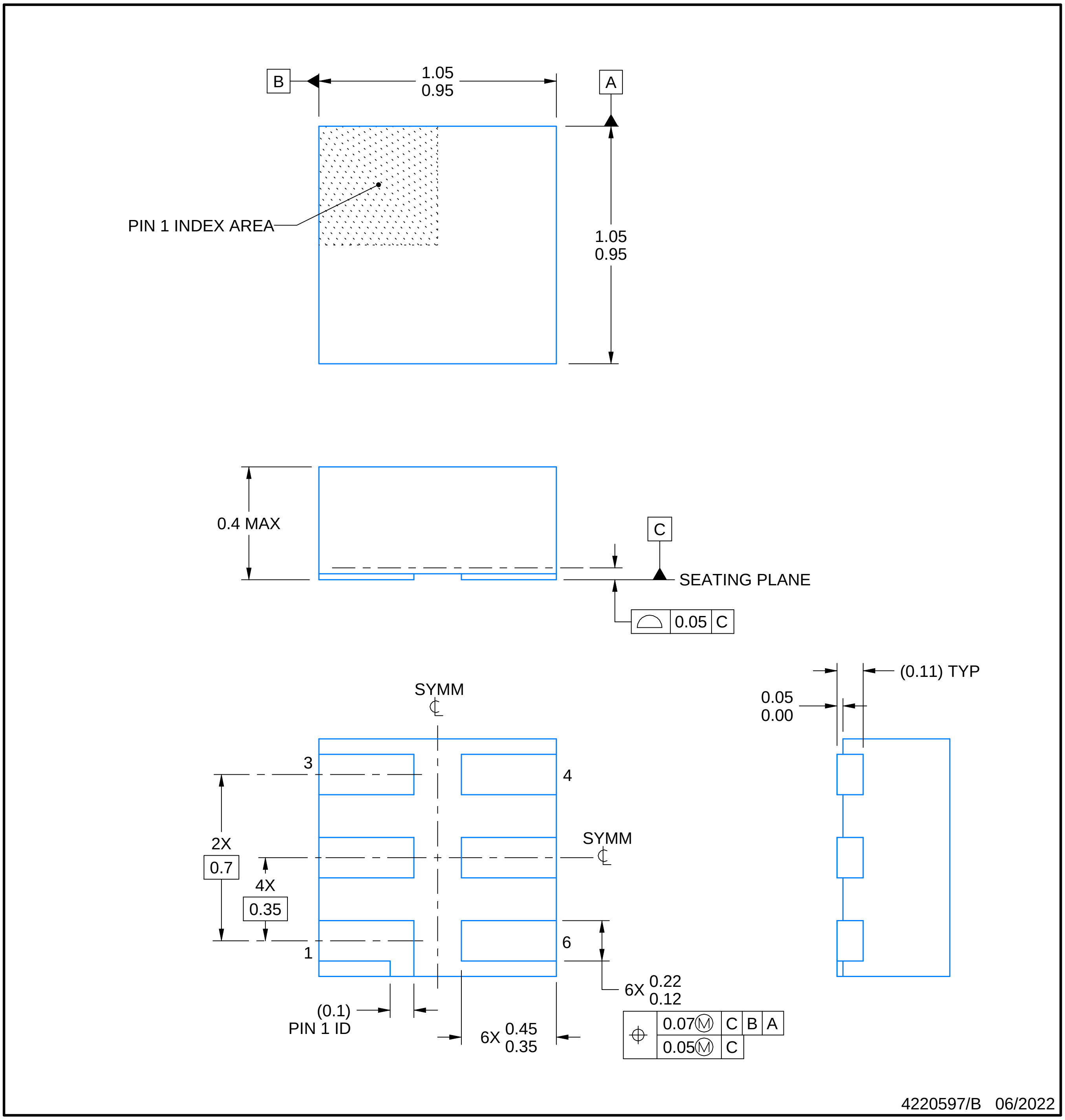
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

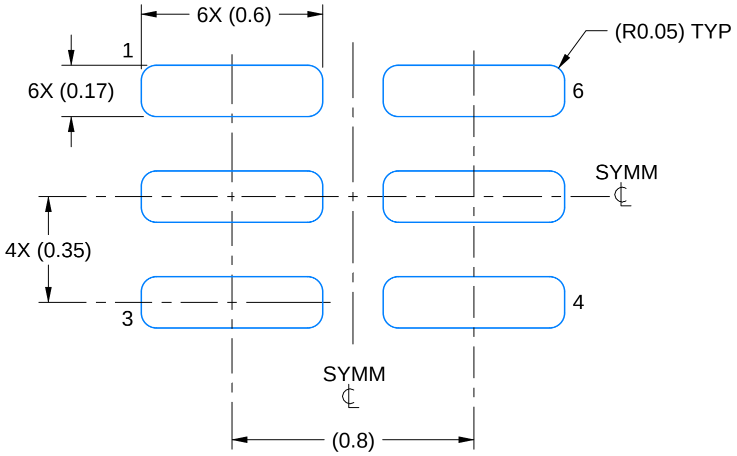
NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

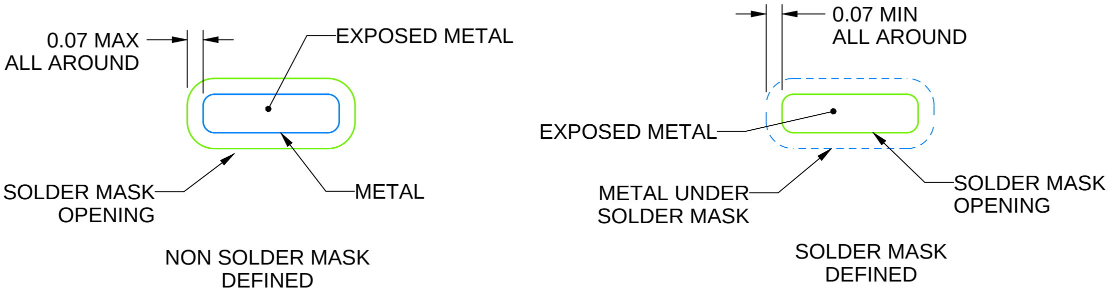


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X

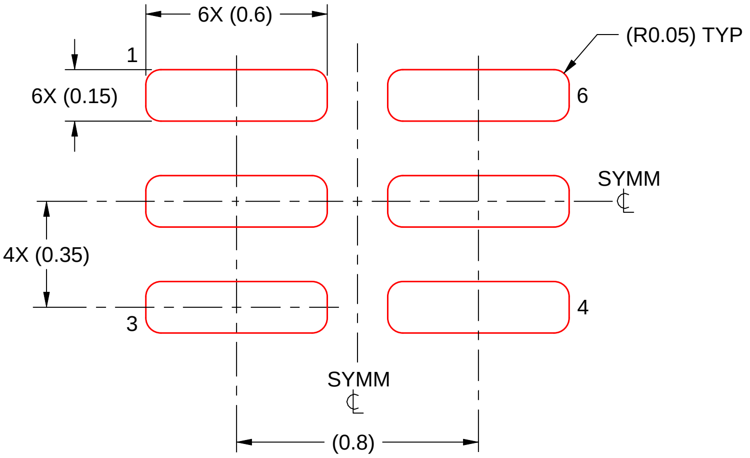


SOLDER MASK DETAILS

4220597/B 06/2022

NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

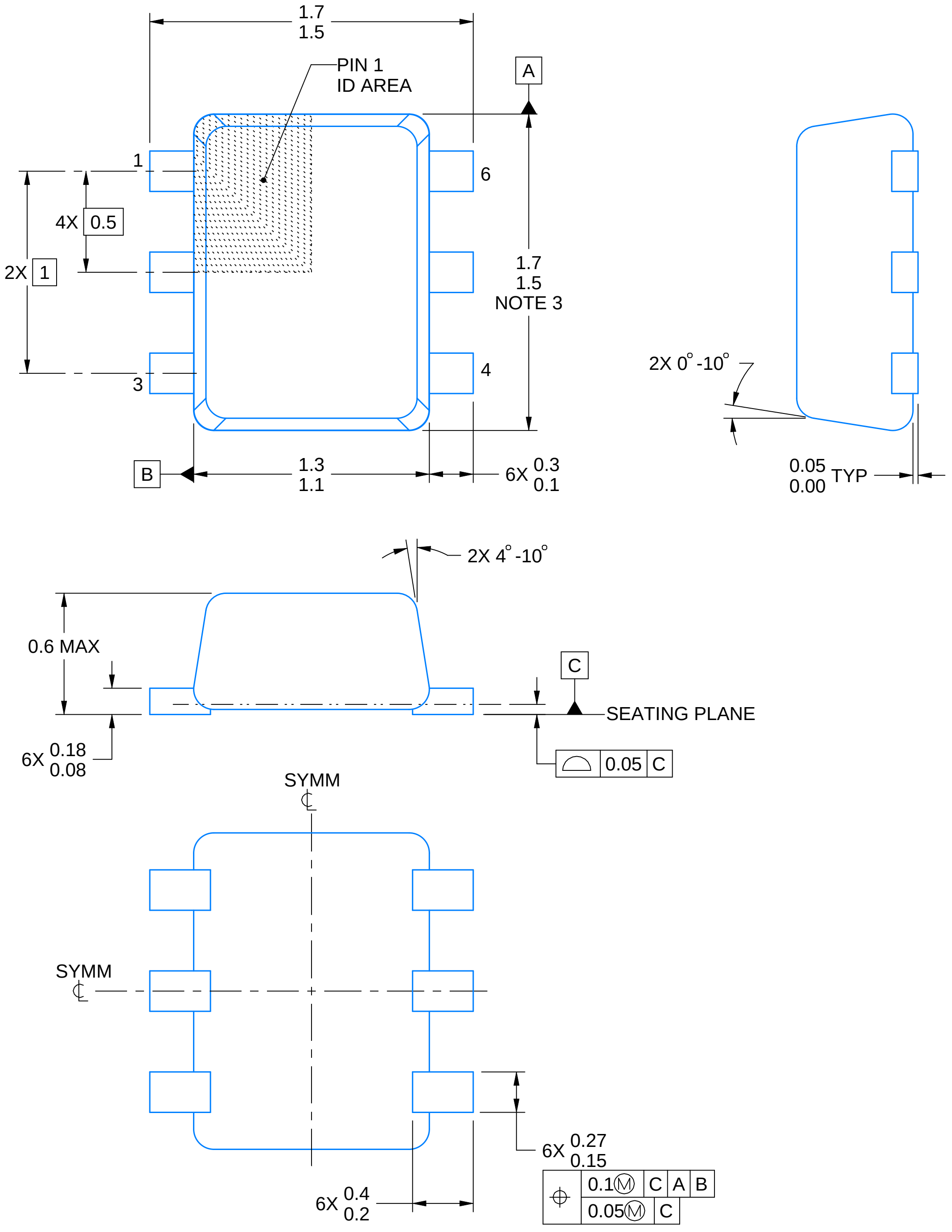


SOLDER PASTE EXAMPLE
BASED ON 0.09 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220597/B 06/2022

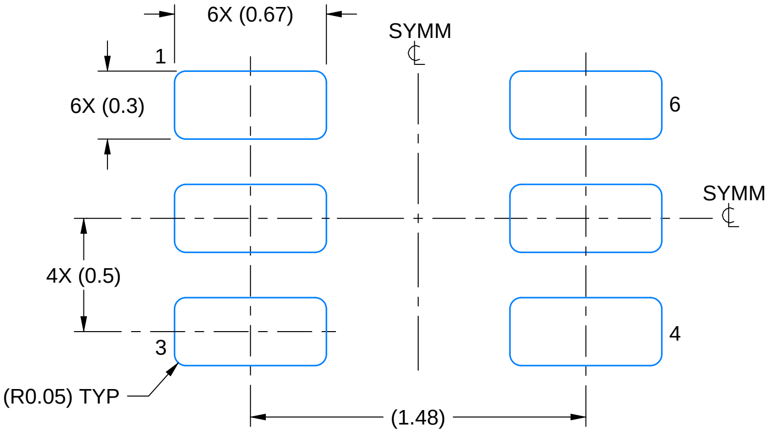
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



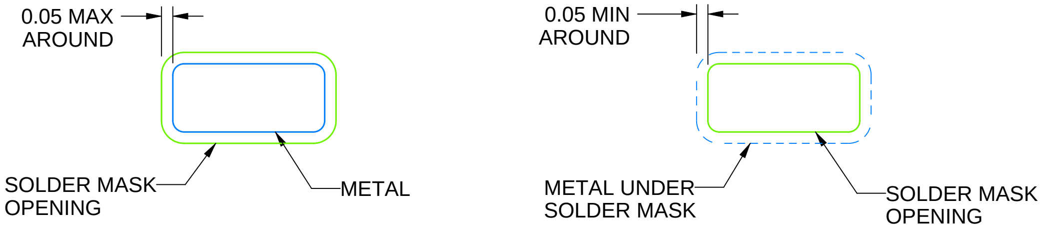
4223266/E 07/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD



LAND PATTERN EXAMPLE
SCALE:30X



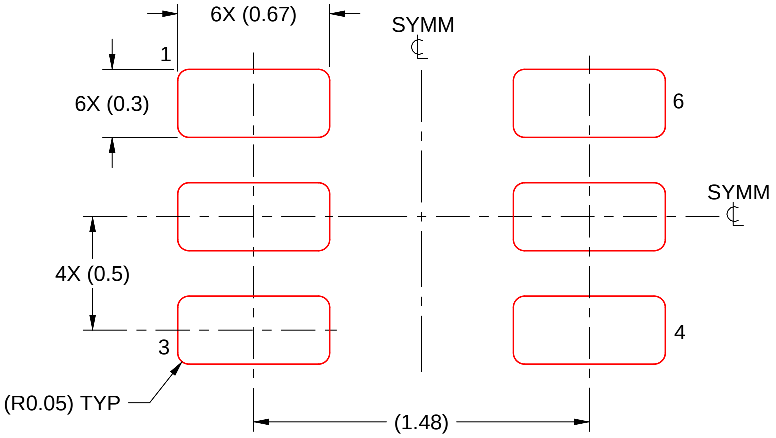
NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDERMASK DETAILS

NOTES: (continued)

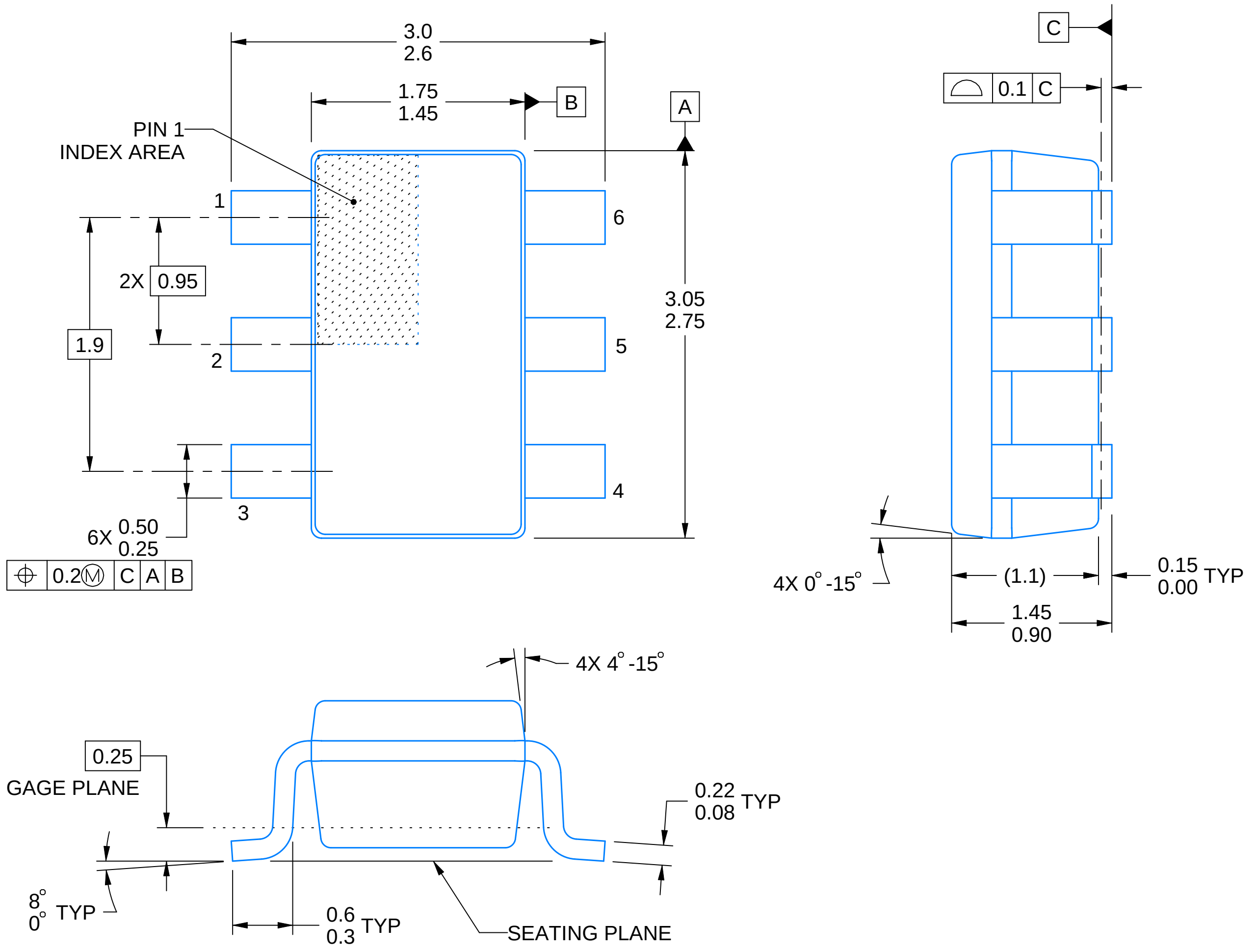
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

NOTES: (continued)

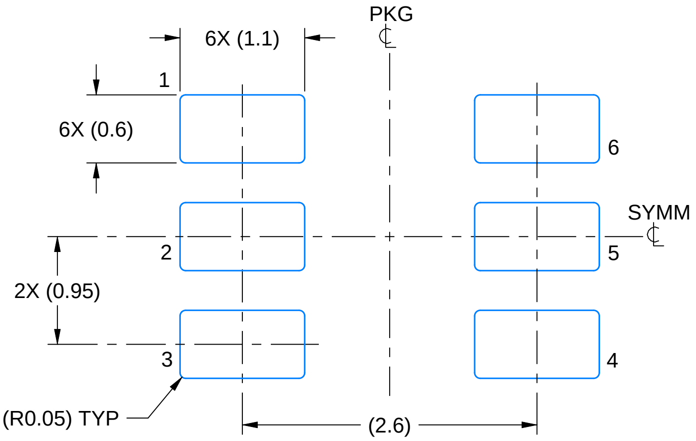
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



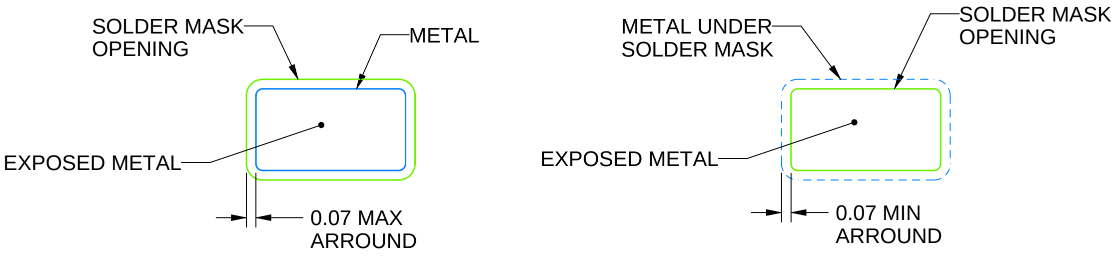
4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



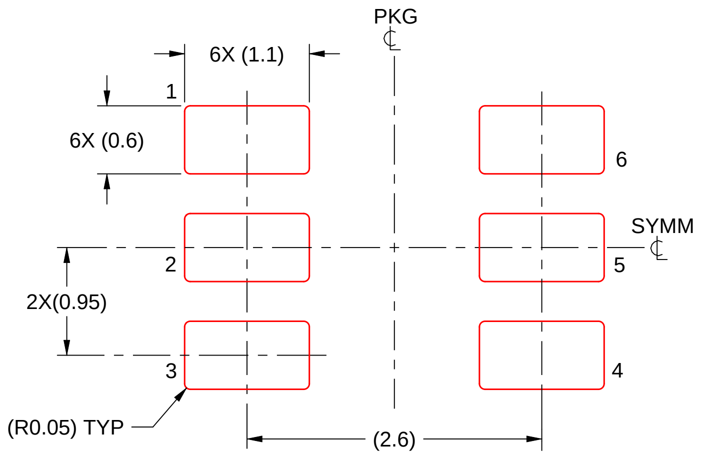
NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

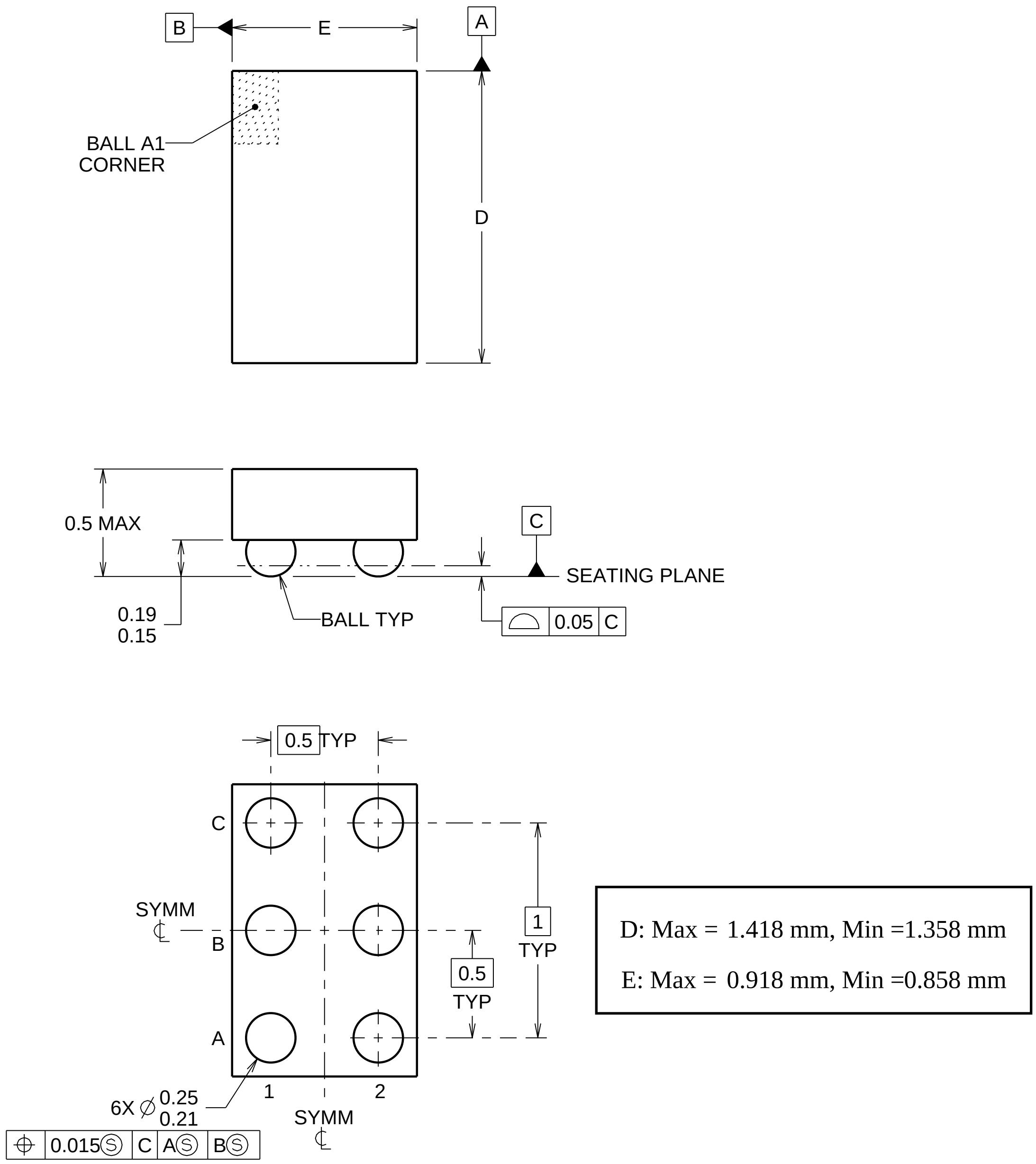
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



D: Max = 1.418 mm, Min =1.358 mm

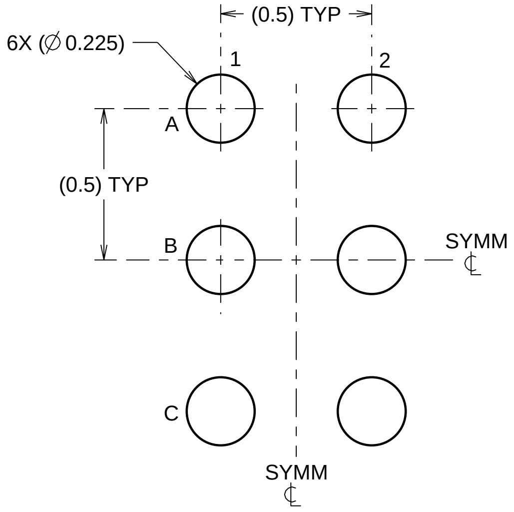
E: Max = 0.918 mm, Min =0.858 mm

4219524/A 06/2014

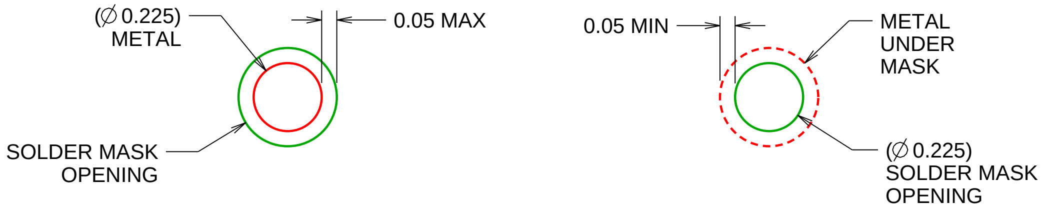
NOTES:

NanoFree Is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.



LAND PATTERN EXAMPLE
SCALE:40X



NON-SOLDER MASK
DEFINED
(PREFERRED)

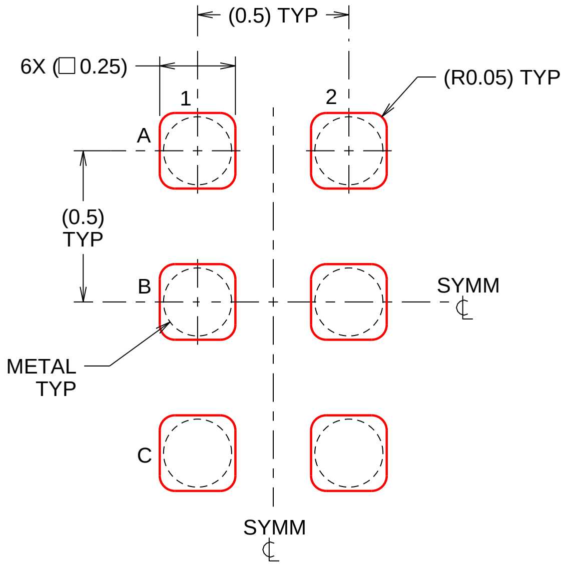
SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4219524/A 06/2014

NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219524/A 06/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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