DATA SHEET
www.onsemi.com

Quad 2-Input OR Gate

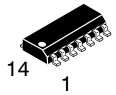
74AC32, 74ACT32

General Description

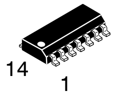
The AC32/ACT32 contains four, 2–input OR gates.

Features

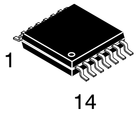
- I_{CC} Reduced by 50% on 74AC Only
- Outputs Source/Sink 24 mA
- ACT32 Has TTL–Compatible Inputs
- These are Pb–Free and Halide Free Devices



SOIC–14 NB
CASE 751A–03



SOIC14
CASE 751EF



TSSOP–14 WB
CASE 948G

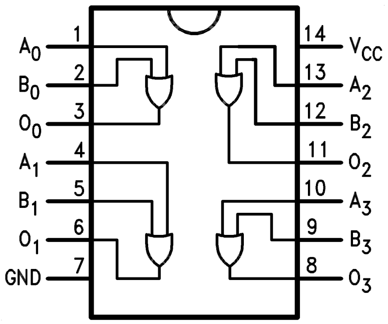


Figure 1. Connection Diagram

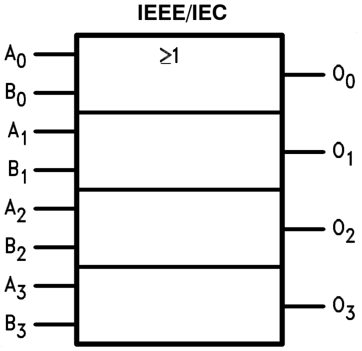
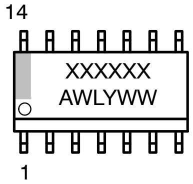


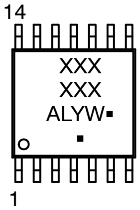
Figure 2. Logic Symbol

PIN DESCRIPTION

Pin Names	Description
A_n, B_n	Inputs
O_n	Outputs

MARKING DIAGRAMS





XXX	= Specific Device Code
A	= Assembly Location
WL, L	= Wafer Lot
Y	= Year
WW, W	= Work Week
G or ▪	= Pb–Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

February, 2024 – Rev. 3

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		− 0.5 to + 6.5	V
I_{IK}	DC Input Diode Current	$V_I = –0.5$ V	− 20	mA
		$V_I = V_{CC} + 0.5$ V	+20	mA
V_I	DC Input Voltage		− 0.5 to V_{CC} + 0.5	V
I_{OK}	DC Output Diode Current	$V_O = –0.5$ V	−20	mA
I_{OK}	DC Output Diode Current	$V_O = V_{CC} + 0.5$ V	+20	mA
V_O	DC Output Voltage		− 0.5 to V_{CC} + 0.5	V
I_O	DC Output Source or Sink Current		± 50	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current per Output Pin		± 50	mA
T_{STG}	Storage Temperature		− 65 to + 150	°C
T_J	Junction temperature		140	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage	AC	2.0	6.0	V
		ACT	4.5	5.5	
V_I	Input Voltage		0	V_{CC}	V
V_O	Output Voltage		0	V_{CC}	V
T_A	Operating Temperature		−40	+85	°C
$\Delta V / \Delta t$	Minimum Input Edge Rate, AC Devices: V_{IN} from 30% to 70% of V_{CC}, V_{CC} @ 3.3 V, 4.5 V, 5.5 V		–	125	mV/ns
$\Delta V / \Delta t$	Minimum Input Edge Rate, ACT Devices: V_{IN} from 0.8 V to 2.0 V, V_{CC} @ 4.5 V, 5.5 V		–	125	mV/ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC CHARACTERISTICS FOR AC

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = +25°C		T_A = −40°C to +85°C	Unit
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage	3.0	V_{OUT} = 0.1 V or V_{CC} − 0.1 V	1.5	2.1	2.1	V
		4.5		2.25	3.15	3.15	V
		5.5		2.75	3.85	3.85	V
V_{IL}	Maximum Low Level Input Voltage	3.0	V_{OUT} = 0.1 V or V_{CC} − 0.1 V	1.5	0.9	0.9	V
		4.5		2.25	1.35	1.35	V
		5.5		2.75	1.65	1.65	V
V_{OH}	Minimum High Level Output Voltage	3.0	I_{OUT} = −50 μA	2.99	2.9	2.9	V
		4.5		4.49	4.4	4.4	V
		5.5		5.49	5.4	5.4	V
		3.0	V_{IN} = V_{IL} or V_{IH}, I_{OH} = −12 mA		2.56	2.46	V
		4.5	V_{IN} = V_{IL} or V_{IH}, I_{OH} = −24 mA		3.86	3.76	
		5.5	V_{IN} = V_{IL} or V_{IH}, I_{OH} = −24 mA (Note 1)		4.86	4.76	
V_{OL}	Maximum Low Level Output Voltage	3.0	I_{OUT} = 50 μA	0.002	0.1	0.1	V
		4.5		0.001	0.1	0.1	V
		5.5		0.001	0.1	0.1	V
		3.0	V_{IN} = V_{IL} or V_{IH}, I_{OL} = 12 mA		0.36	0.44	V
		4.5	V_{IN} = V_{IL} or V_{IH}, I_{OL} = 24 mA		0.36	0.44	
		5.5	V_{IN} = V_{IL} or V_{IH}, I_{OL} = 24 mA (Note 1)		0.36	0.44	
I_{IN} (Note 3)	Maximum Input Leakage Current	5.5	V_I = V_{CC}, GND	–	±0.1	±1.0	μA
I_{OLD}	Minimum Dynamic Output Current (Note 2)	5.5	V_{OLD} = 1.65 V Max	–	–	75	mA
I_{OHD}		5.5	V_{OHD} = 3.85 V Min	–	–	−75	mA
I_{CC} (Note 3)	Maximum Quiescent Supply Current	5.5	V_{IN} = V_{CC} or GND	–	2.0	20.0	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. All outputs loaded; thresholds on input associated with output under test.
2. Maximum test duration 2.0 ms, one output loaded at a time.
3. I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

DC CHARACTERISTICS FOR ACT

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = +25°C		T_A = –40°C to +85°C	Unit
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage	4.5	V_{OUT} = 0.1 V or V_{CC} – 0.1 V	1.5	2.0	2.0	V
		5.5		1.5	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage	4.5	V_{OUT} = 0.1 V or V_{CC} – 0.1 V	1.5	0.8	0.8	V
		5.5		1.5	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	4.5	I_{OUT} = –50 μA	4.49	4.4	4.4	V
		5.5		5.49	5.4	5.4	V
		4.5	V_{IN} = V_{IL} or V_{IH}, I_{OH} = –24 mA		3.86	3.76	V
		5.5	V_{IN} = V_{IL} or V_{IH}, I_{OH} = –24 mA (Note 4)		4.86	4.76	
V_{OL}	Maximum Low Level Output Voltage	4.5	I_{OUT} = 50 μA	0.001	0.1	0.1	V
		5.5		0.001	0.1	0.1	V
		4.5	V_{IN} = V_{IL} or V_{IH}, I_{OL} = 24 mA		0.36	0.44	V
		5.5	V_{IN} = V_{IL} or V_{IH}, I_{OL} = 24 mA (Note 4)		0.36	0.44	
I_{IN}	Maximum Input Leakage Current	5.5	V_I = V_{CC}, GND	–	±0.1	±1.0	μA
I_{CCT}	Maximum I_{CC}/Input	5.5	V_I = V_{CC} – 2.1 V	0.6	–	1.5	mA
I_{OLD}	Minimum Dynamic Output Current (Note 5)	5.5	V_{OLD} = 1.65 V Max	–	–	75	mA
I_{OHD}		5.5	V_{OHD} = 3.85 V Min	–	–	–75	mA
I_{CC}	Maximum Quiescent Supply Current	5.5	V_{IN} = V_{CC} or GND	–	4.0	40.0	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. All outputs loaded; thresholds on input associated with output under test.
5. Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS FOR AC

Symbol	Characteristics	V_{CC} (V) (Note 6)	T_A = +25°C, C_L = 50 pF			T_A = −40°C to +85°C, C_L = 50 pF		Unit
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay	3.3	1.5	7.5	9.0	1.5	10.0	ns
		5.0	1.5	5.5	7.5	1.0	8.5	
t_{PHL}	Propagation Delay	3.3	1.5	7.0	8.5	1.0	9.0	ns
		5.0	1.5	5.0	7.0	1.0	7.5	

6. Voltage range 3.3 is 3.3 V ± 0.3 V. Voltage range 5.0 is 5.0 V ± 0.5 V.

AC CHARACTERISTICS FOR ACT

Symbol	Characteristics	V_{CC} (V) (Note 6)	T_A = +25°C, C_L = 50 pF			T_A = −40°C to +85°C, C_L = 50 pF		Unit
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay	5.0	1.0	6.5	9.0	1.0	10.0	ns
t_{PHL}	Propagation Delay	5.0	1.0	6.5	9.0	1.0	10.0	ns

7. Voltage Range 5.0 is 5.0 V ± 0.5 V.

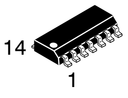
CAPACITANCE

Symbol	Parameter	Test Conditions	Typ	Unit
C_{IN}	Input Capacitance	V_{CC} = Open	4.5	pF
C_{PD}	Power Dissipation Capacitance	V_{CC} = 5.0 V	20.0	pF

ORDERING INFORMATION

Device	Marking	Package	Shipping†
74AC32SCX	AC32	SOIC14, Case 751EF (Pb−Free)	2500 / Tape & Reel
74AC32MTCX	AC 32	TSSOP−14 WB, Case 948G (Pb−Free)	2500 / Tape & Reel
74ACT32SC	ACT32	SOIC−14 NB, Case 751A−03 (Pb−Free)	55 Units / Tube
74ACT32SCX	ACT32	SOIC14, Case 751EF (Pb−Free)	2500 / Tape & Reel
74ACT32MTCX	ACT 32	TSSOP−14 WB, Case 948G (Pb−Free)	2500 / Tape & Reel

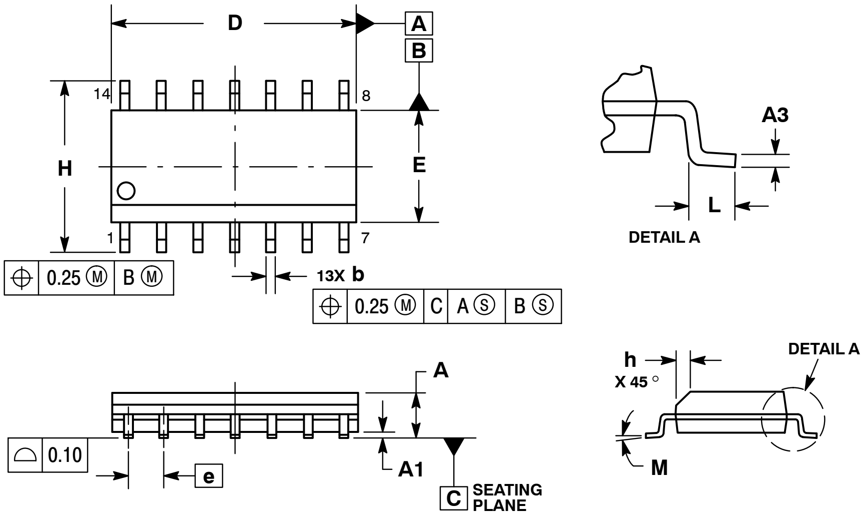
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



SCALE 1:1

SOIC−14 NB
CASE 751A−03
ISSUE L

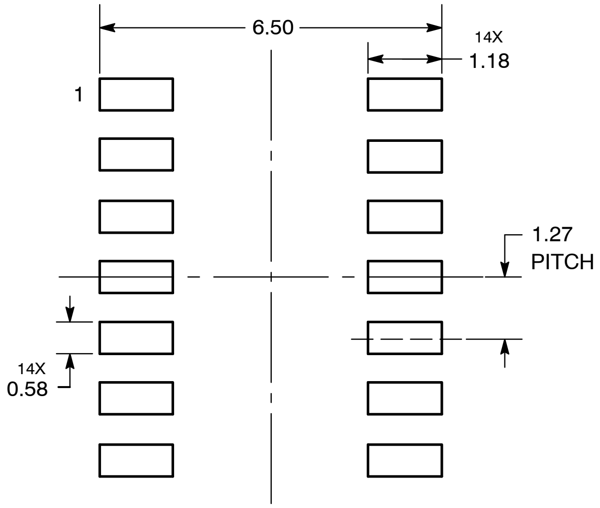
DATE 03 FEB 2016



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

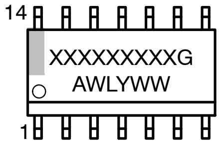
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42565B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**SOIC−14 NB**	**PAGE 1 OF 2**

SOIC−14

CASE 751A−03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

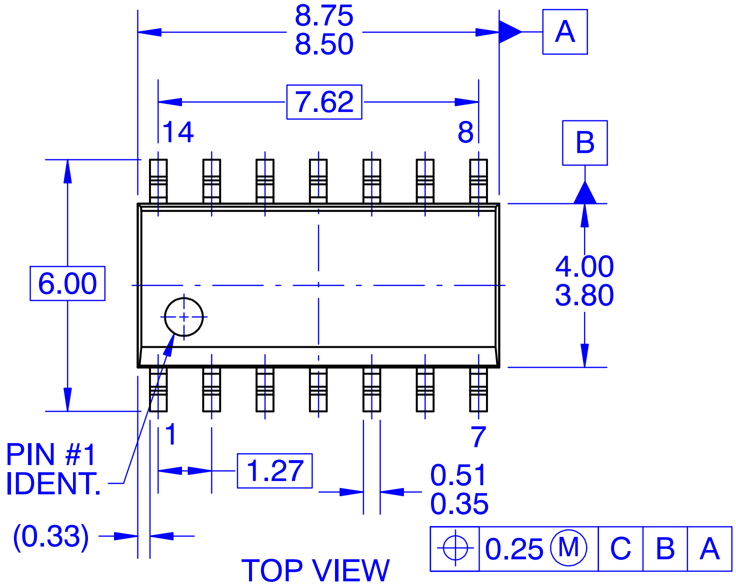
STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

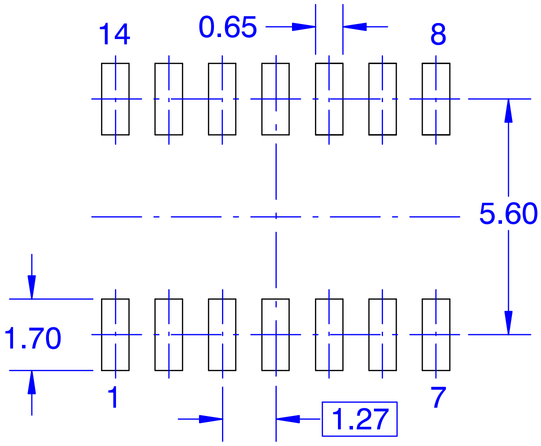
STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

SOIC14
CASE 751EF
ISSUE O

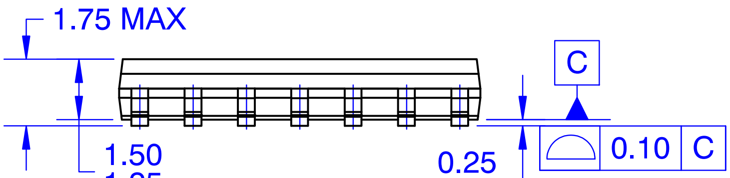
DATE 30 SEP 2016



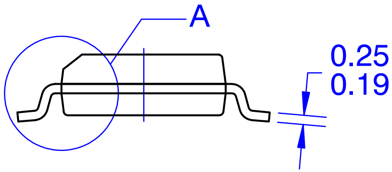
TOP VIEW



LAND PATTERN RECOMMENDATION

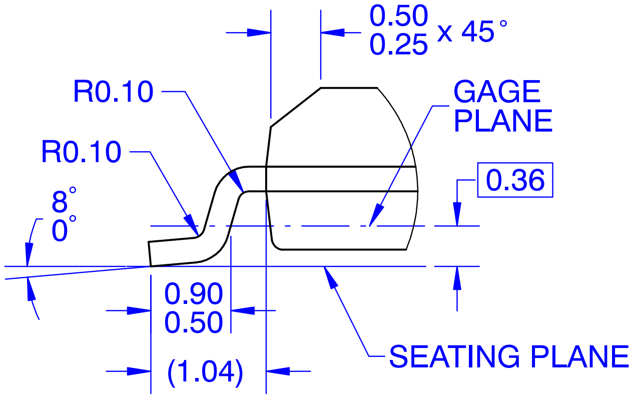


FRONT VIEW



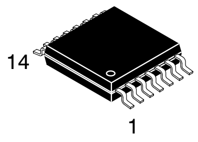
SIDE VIEW

NOTES:
- A. CONFORMS TO JEDEC MS−012, VARIATION AB, ISSUE C
- B. ALL DIMENSIONS ARE IN MILLIMETERS
- C. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS
- D. LAND PATTERN STANDARD: SOIC127P600X145−14M
- E. CONFORMS TO ASME Y14.5M, 2009



DETAIL A
SCALE 16 : 1

DOCUMENT NUMBER:	**98AON13739G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC14**		**PAGE 1 OF 1**

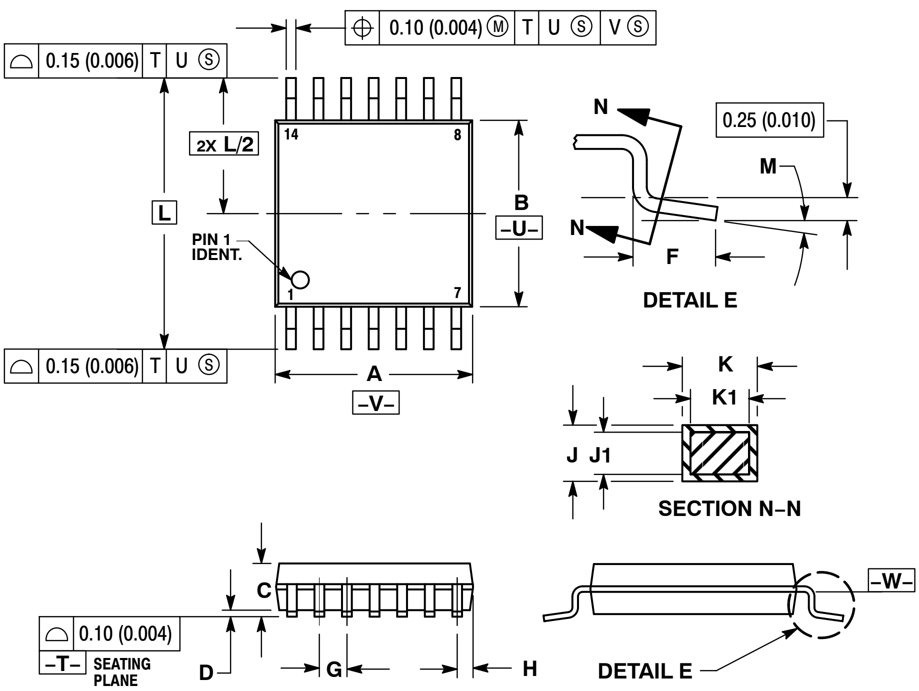


SCALE 2:1

TSSOP−14 WB

CASE 948G
ISSUE C

DATE 17 FEB 2016

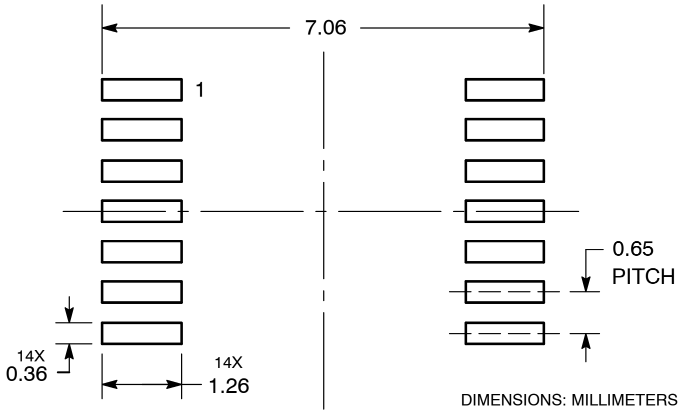


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

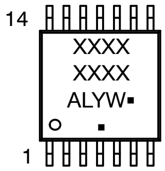
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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