DATA SHEET
www.onsemi.com

Hex Buffers

MC14049UB

The MC14049UB hex inverter/buffer is constructed with MOS P−channel and N−channel enhancement mode devices in a single monolithic structure. This complementary MOS device finds primary use where low power dissipation and/or high noise immunity is desired. This device provides logic−level conversion using only one supply voltage, V_{DD}. The input−signal high level (V_{IH}) can exceed the V_{DD} supply voltage for logic−level conversions. Two TTL/DTL Loads can be driven when the device is used as CMOS−to−TTL/DTL converters (V_{DD} = 5.0 V, $V_{OL} \leq 0.4$ V, $I_{OL} \geq 3.2$ mA). Note that pins 13 and 16 are not connected internally on this device; consequently connections to these terminals will not affect circuit operation.

Features

- High Source and Sink Currents
- High−to−Low Level Converter
- Supply Voltage Range = 3.0 V to 18 V
- Meets JEDEC UB Specifications
- V_{IN} can exceed V_{DD}
- Improved ESD Protection on All Inputs
- These Devices are Pb−Free and are RoHS Compliant
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}	Input Voltage Range (DC or Transient)	−0.5 to +18.0	V
V_{out}	Output Voltage Range (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}	Input Current (DC or Transient) per Pin	±10	mA
I_{out}	Output Current (DC or Transient) per Pin	+45	mA
P_D	Power Dissipation, per Package (Note 1) Plastic SOIC	 825 740	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

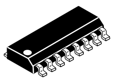
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: All Packages: See Figure 4.

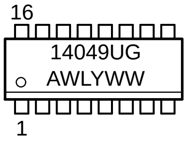
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields referenced to the V_{SS} pin, only. Extra precautions must be taken to avoid applications of any voltage higher than the maximum rated voltages to this high−impedance circuit. For proper operation, the ranges $V_{SS} \leq V_{in} \leq 18$ V and $V_{SS} \leq V_{out} \leq V_{DD}$ are recommended.

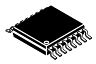
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

MARKING DIAGRAMS

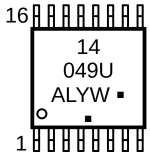


SOIC−16
D SUFFIX
CASE 751B





TSSOP−16
DT SUFFIX
CASE 948F



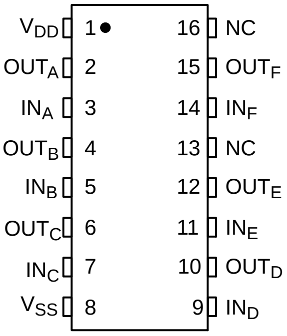
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or ▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

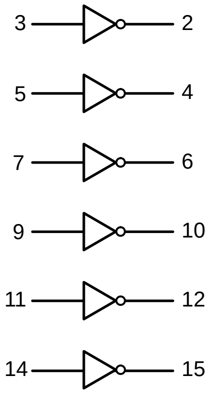
See detailed ordering and shipping information on page 3 of this data sheet.

March, 2022 − Rev. 11



NC = NO CONNECTION

Figure 1. Pin Assignment



NC = PIN 13, 16
V_{SS} = PIN 8
V_{DD} = PIN 1

Figure 2. Logic Diagram MC14049UB

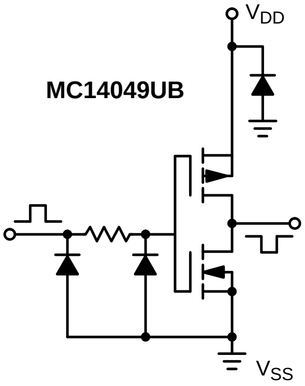


Figure 3. Circuit Schematic
(1/6 of circuit shown)

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	– 55°C Min	– 55°C Max	25°C Min	25°C Typ (Note 2)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 Vdc)		5.0	–	1.0	–	2.25	1.0	–	1.0	
(V_O = 9.0 Vdc)		10	–	2.0	–	4.50	2.0	–	2.0	
(V_O = 13.5 Vdc)		15	–	2.5	–	6.75	2.5	–	2.5	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 Vdc)		5.0	4.0	–	4.0	2.75	–	4.0	–	
(V_O = 1.0 Vdc)		10	8.0	–	8.0	5.50	–	8.0	–	
(V_O = 1.5 Vdc)		15	12.5	–	12.5	8.25	–	12.5	–	
Output Drive Current	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	– 1.6	–	– 1.25	– 2.5	–	– 1.0	–	
(V_{OH} = 9.5 Vdc)		10	– 1.6	–	– 1.3	– 2.6	–	– 1.0	–	
(V_{OH} = 13.5 Vdc)		15	– 4.7	–	– 3.75	– 10	–	– 3.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	3.75	–	3.2	6.0	–	2.6	–	mAdc
(V_{OL} = 0.5 Vdc)		10	10	–	8.0	16	–	6.6	–	
(V_{OL} = 1.5 Vdc)		15	30	–	24	40	–	19	–	
Input Current	I_{in}	15	–	± 0.1	–	±0.00001	± 0.1	–	± 1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	10	20	–	–	pF
Quiescent Current (Per Package)	I_{DD}	5.0	–	1.0	–	0.002	1.0	–	30	µAdc
		10	–	2.0	–	0.004	2.0	–	60	
		15	–	4.0	–	0.006	4.0	–	120	
Total Supply Current (Note 3 and 4) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.8 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (3.5 µA/kHz) f + I_{DD}							
		15	I_T = (5.3 µA/kHz) f + I_{DD}							

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
3. The formulas given are for the typical characteristics only at 25°C.
4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\text{ pF}) + (C_L - 50)\,Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.002.

SWITCHING CHARACTERISTICS (Note 5) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ (Note 6)	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (0.8 ns/pF) C_L + 60 ns		5.0	–	100	160	
t_{TLH} = (0.3 ns/pF) C_L + 35 ns		10	–	50	100	
t_{TLH} = (0.27 ns/pF) C_L + 26.5 ns		15	–	40	60	
Output Fall Time	t_{THL}					ns
t_{THL} = (0.3 ns/pF) C_L + 25 ns		5.0	–	40	60	
t_{THL} = (0.12 ns/pF) C_L + 14 ns		10	–	20	40	
t_{THL} = (0.1 ns/pF) C_L + 10 ns		15	–	15	30	
Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (0.38 ns/pF) C_L + 61 ns		5.0	–	80	120	
t_{PLH} = (0.20 ns/pF) C_L + 30 ns		10	–	40	65	
t_{PLH} = (0.11 ns/pF) C_L + 24.5 ns		15	–	30	50	
Propagation Delay Time	t_{PHL}					ns
t_{PHL} = (0.38 ns/pF) C_L + 11 ns		5.0	–	30	60	
t_{PHL} = (0.12 ns/PF) C_L + 9 ns		10	–	15	30	
t_{PHL} = (0.11 ns/pF) C_L + 4.5 ns		15	–	10	20	

5. The formulas given are for the typical characteristics only at 25°C.
6. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

ORDERING INFORMATION

Device	Package	Shipping†
MC14049UBDG	SOIC−16 (Pb−Free)	48 Units / Rail
MC14049UBDR2G	SOIC−16 (Pb−Free)	2500 / Tape & Reel
NLV14049UBDR2G*		
MC14049UBDTR2G	TSSOP−16 (Pb−Free)	2500 / Tape & Reel
NLV14049UBDTR2G*		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

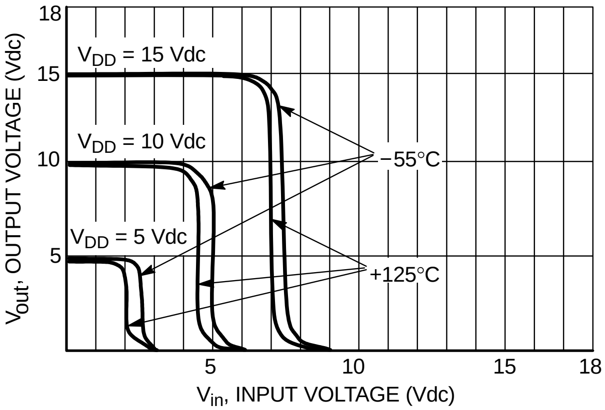


Figure 4. Typical Voltage Transfer Characteristics versus Temperature

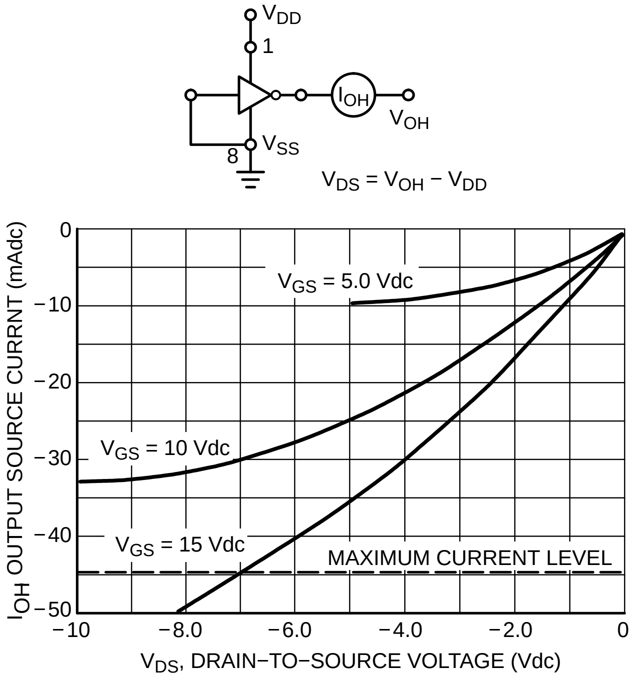


Figure 5. Typical Output Source Characteristics

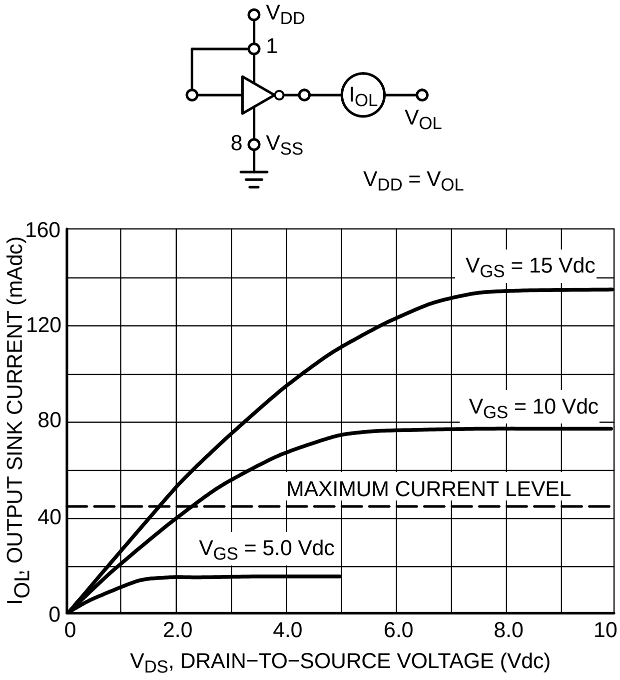


Figure 6. Typical Output Sink Characteristics

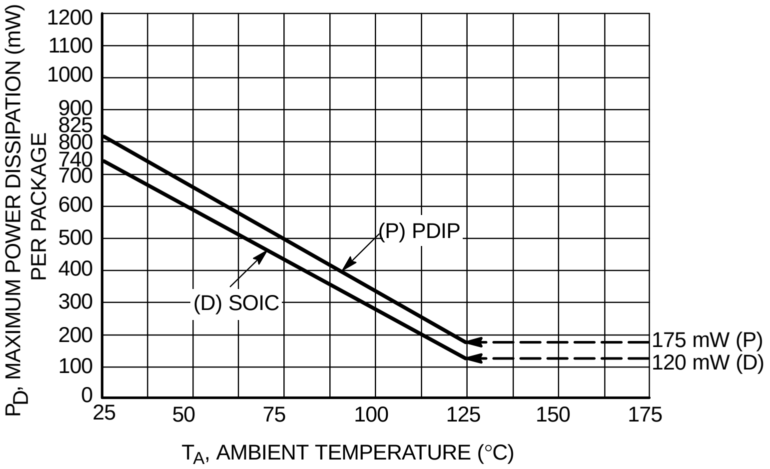


Figure 7. Ambient Temperature Power Derating

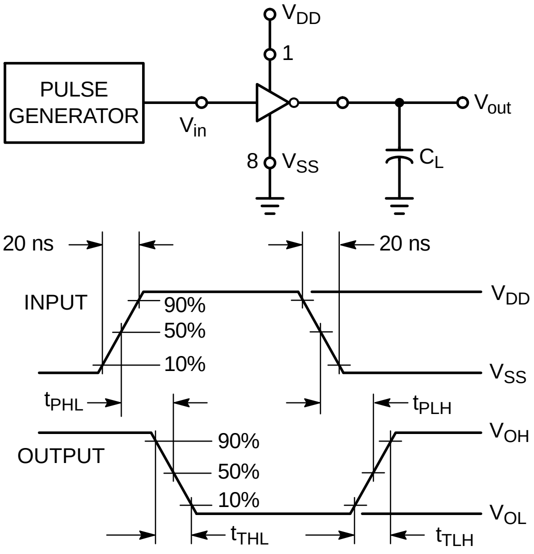
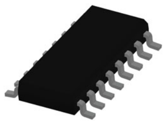


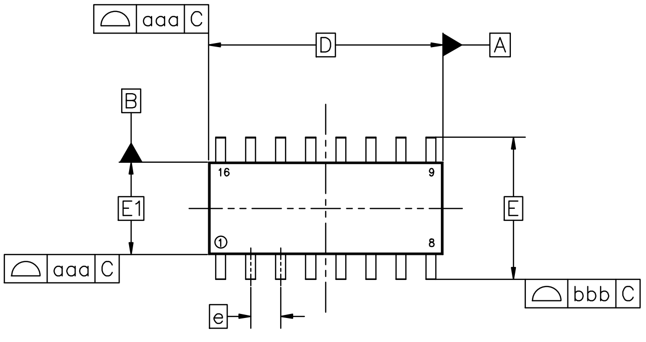
Figure 8. Switching Time Test Circuit and Waveforms



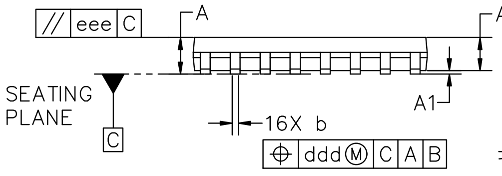
SOIC-16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

DATE 18 OCT 2024

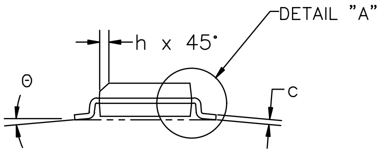
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



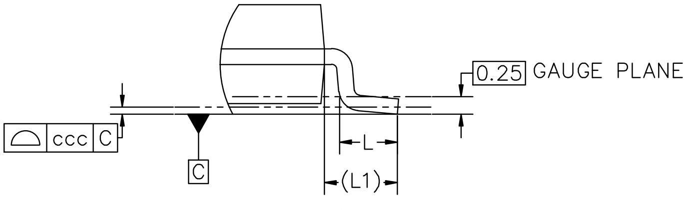
TOP VIEW



SIDE VIEW

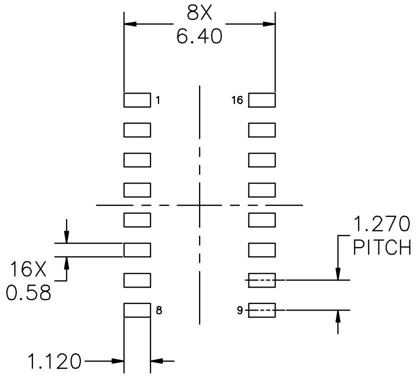


END VIEW



DETAIL "A"
Scale 3:1

DIM	MILLIMETERS MIN	MILLIMETERS NOM	MILLIMETERS MAX
A	1.35	1.55	1.75
A1	0.10	0.18	0.25
A2	1.25	1.37	1.50
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	---	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
θ	0°	---	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



RECOMMENDED MOUNTING FOOTPRINT

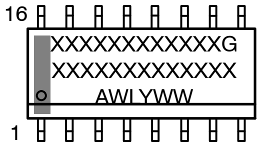
*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

DOCUMENT NUMBER:	**98ASB42566B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**SOIC-16 9.90X3.90X1.37 1.27P**	**PAGE 1 OF 2**

SOIC−16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

DATE 18 OCT 2024

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

	STYLE 1:	STYLE 2:	STYLE 3:	STYLE 4:
PIN 1.	COLLECTOR	CATHODE	COLLECTOR, DYE #1	COLLECTOR, DYE #1
2.	BASE	ANODE	BASE, #1	COLLECTOR, #1
3.	EMITTER	NO CONNECTION	EMITTER, #1	COLLECTOR, #2
4.	NO CONNECTION	CATHODE	COLLECTOR, #1	COLLECTOR, #2
5.	EMITTER	CATHODE	COLLECTOR, #2	COLLECTOR, #3
6.	BASE	NO CONNECTION	BASE, #2	COLLECTOR, #3
7.	COLLECTOR	ANODE	EMITTER, #2	COLLECTOR, #4
8.	COLLECTOR	CATHODE	COLLECTOR, #2	COLLECTOR, #4
9.	BASE	CATHODE	COLLECTOR, #3	BASE, #4
10.	EMITTER	ANODE	BASE, #3	EMITTER, #4
11.	NO CONNECTION	NO CONNECTION	EMITTER, #3	BASE, #3
12.	EMITTER	CATHODE	COLLECTOR, #3	EMITTER, #3
13.	BASE	CATHODE	COLLECTOR, #4	BASE, #2
14.	COLLECTOR	NO CONNECTION	BASE, #4	EMITTER, #2
15.	EMITTER	ANODE	EMITTER, #4	BASE, #1
16.	COLLECTOR	CATHODE	COLLECTOR, #4	EMITTER, #1

	STYLE 5:	STYLE 6:	STYLE 7:
PIN 1.	DRAIN, DYE #1	CATHODE	SOURCE N-CH
2.	DRAIN, #1	CATHODE	COMMON DRAIN (OUTPUT)
3.	DRAIN, #2	CATHODE	COMMON DRAIN (OUTPUT)
4.	DRAIN, #2	CATHODE	GATE P-CH
5.	DRAIN, #3	CATHODE	COMMON DRAIN (OUTPUT)
6.	DRAIN, #3	CATHODE	COMMON DRAIN (OUTPUT)
7.	DRAIN, #4	CATHODE	COMMON DRAIN (OUTPUT)
8.	DRAIN, #4	CATHODE	SOURCE P-CH
9.	GATE, #4	ANODE	SOURCE P-CH
10.	SOURCE, #4	ANODE	COMMON DRAIN (OUTPUT)
11.	GATE, #3	ANODE	COMMON DRAIN (OUTPUT)
12.	SOURCE, #3	ANODE	COMMON DRAIN (OUTPUT)
13.	GATE, #2	ANODE	GATE N-CH
14.	SOURCE, #2	ANODE	COMMON DRAIN (OUTPUT)
15.	GATE, #1	ANODE	COMMON DRAIN (OUTPUT)
16.	SOURCE, #1	ANODE	SOURCE N-CH

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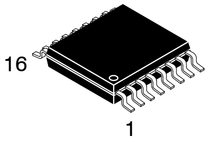
DESCRIPTION:	**SOIC−16 9.90X3.90X1.37 1.27P**	**PAGE 2 OF 2**

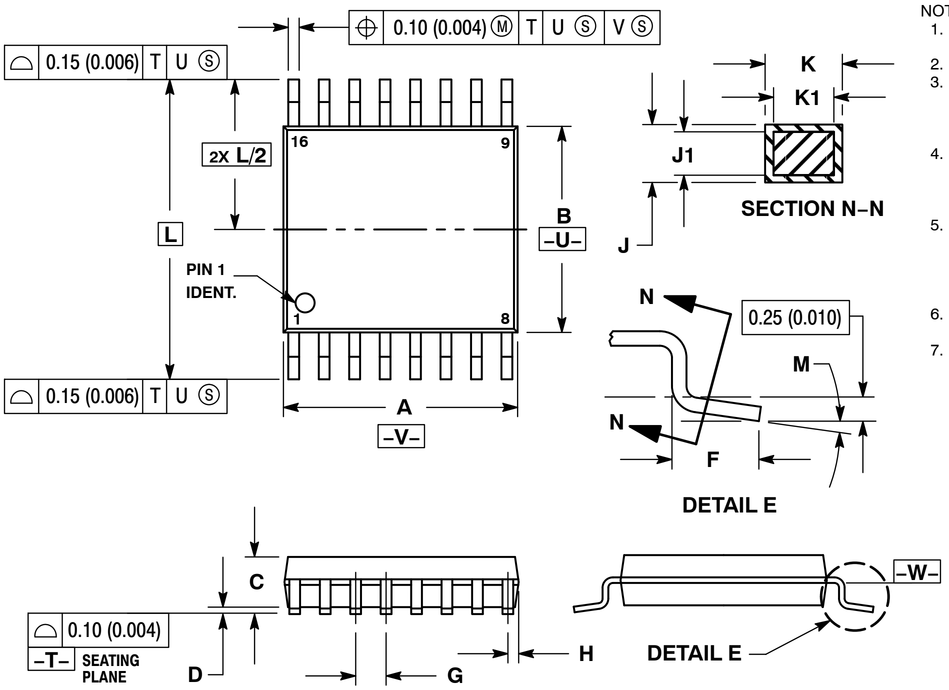
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



SCALE 2:1

TSSOP−16 WB
CASE 948F
ISSUE B

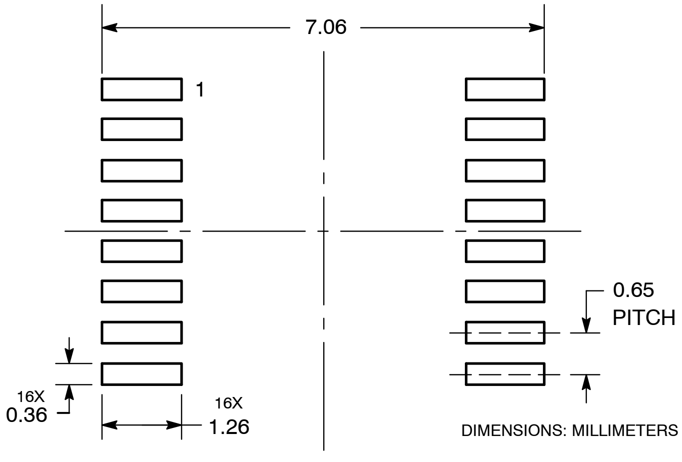
DATE 19 OCT 2006



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

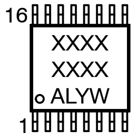
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



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A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
G or ▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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