SN74AHC00-Q1 Automotive Quadruple 2-Input Positive-NAND Gate

1 Features

- Qualified for Automotive Applications
- Operating Range 2-V to 5.5-V V_{CC}
- Latch-Up Performance Exceeds 250 mA Per JESD 17

2 Description

The SN74AHC00 device performs the Boolean function $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

Package Information

PART NUMBER	PACKAGE[1]	PACKAGE SIZE[2]
SN74AHC00-Q1	D (SOIC, 14)	8.65 mm × 6 mm
	PW (TSSOP, 14)	5.00 mm x 6.4 mm
	BQA (WQFN, 14)	3 mm × 2.5 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

Figure 2-1. Logic Diagram, Each Gate (Positive Logic)

Table of Contents

3 Revision History

Changes from Revision B (April 2008) to Revision C (June 2023)	Page
• Added *Package Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Device Functional Modes, Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Added BQA package to *Package Information* table	1
• Updated thermal values for PW package from RθJA = 113 to 147.7, all values in °C/W	5
• Added thermal value for RθJA: BQA = 88.3, all values in °C/W	5

4 Pin Configuration and Functions

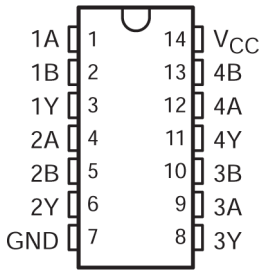


Figure 4-1. D or PW Package (Top View)

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
1	1A	I	1A Input
2	1B	I	1B Input
3	1Y	O	1Y Output
4	2A	I	2A Input
5	2B	I	2B Input
6	2Y	O	2Y Output
7	GND	–	GND
8	3Y	O	3Y Output
9	3A	I	3A Input
10	3B	I	3B Input
11	4Y	O	4Y Output
12	4A	I	4A Input
13	4B	I	4B Input
14	V_{CC}	—	Power Pin

1. Signal Types: I = Input, O = Output, I/O = Input or Output.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		−0.5	7	V
V_I [1]	Input voltage range		−0.5	7	V
V_O [1]	Output voltage range		−0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	(V_I < 0)		−20	mA
I_{OK}	Output clamp current	(V_O < 0 or V_O > V_{CC})		±20	mA
I_O	Continuous output current	(V_O = 0 to V_{CC})		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1]	±2000	V
		Charged device model (CDM), per AEC Q100-011	±1000	

5.3 Recommended Operating Conditions

over recommended operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 3 V	2.1		
		V_{CC} = 5.5 V	3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 3 V		0.9	
		V_{CC} = 5.5 V		1.65	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		−50	μA
		V_{CC} = 3.3 V ± 0.3 V		−4	mA
		V_{CC} = 5 V ± 0.5 V		−8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4	mA
		V_{CC} = 5 V ± 0.5 V		8	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20	
T_A	Operating free-air temperature	Q-suffix devices	−40	125	°C
		I-suffix devices	−40	85	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

5.4 Thermal Information

THERMAL METRIC[1]		SN74AHC00-Q1			UNIT
		D (SOIC)	PW (TSSOP)	BQA (WQFN)	
		14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	86	147.7	88.3	°C/W

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25 °C			T_A = −40 °C to 125°C		T_A = −40 °C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 µA		2 V	1.9	2		1.9		1.9		V
			3 V	2.9	3		2.9		2.9		
			4.5 V	4.4	4.5		4.4		4.4		
	I_{OH} = −4 mA		3 V	2.58			2.48		2.48		
	I_{OH} = −8 mA		4.5 V	3.94			3.8		3.8		
V_{OL}	I_{OL} = 50 µA		2 V			0.1		0.1		0.1	V
			3 V			0.1		0.1		0.1	
			4.5 V			0.1		0.1		0.1	
	I_{OL} = 4 mA		3 V			0.36		0.5		0.44	
	I_{OL} = 8 mA		4.5 V			0.36		0.5		0.44	
I_I	V_I = 5.5 V or GND		0 V to 5.5 V			±0.1		±1		±1	µA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	5.5 V			2		20		20	µA
C_i	V_I = V_{CC} or GND		5 V		2	10				10	pF

5.6 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25 °C			T_A = −40 °C to 125°C		T_A = −40 °C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	C_L = 15 pF		5.5	7.9	1	9.5	1	9.5	ns
t_{PHL}					5.5	7.9	1	9.5	1	9.5	
t_{PLH}	A or B	Y	C_L = 50 pF		8	11.4	1	13	1	13	ns
t_{PHL}					8	11.4	1	13	1	13	

5.7 Switching Characteristics, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25 °C			T_A = −40 °C to 125°C		T_A = −40 °C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	C_L = 15 pF		3.7	5.5	1	6.5	1	6.5	ns
t_{PHL}					3.7	5.5	1	6.5	1	6.5	
t_{PLH}	A or B	Y	C_L = 50 pF		5.2	7.5	1	8.5	1	8.5	ns
t_{PHL}					5.2	7.5	1	8.5	1	8.5	

5.8 Noise Characteristics

V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C [1]

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL}(P)$	Quiet output, maximum dynamic V_{OL}		0.3	0.8	V
$V_{OL}(V)$	Quiet output, minimum dynamic V_{OL}		−0.3	−0.8	V
$V_{OH}(V)$	Quiet output, minimum dynamic V_{OH}		4.6[1]		V
$V_{IH}(D)$	High-level dynamic input voltage	3.5			V
$V_{IL}(D)$	Low-level dynamic input voltage			1.5	V

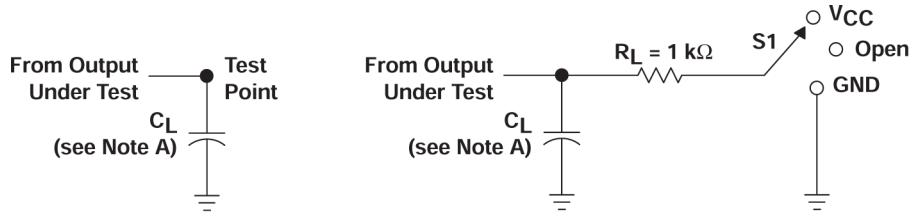
1. Characteristics are for surface-mount packages only.

5.9 Operating Characteristics

V_{CC} = 5 V, T_A = 25°C

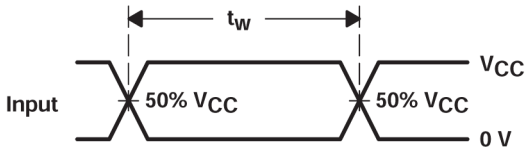
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	9.5	pF

6 Parameter Measurement Information

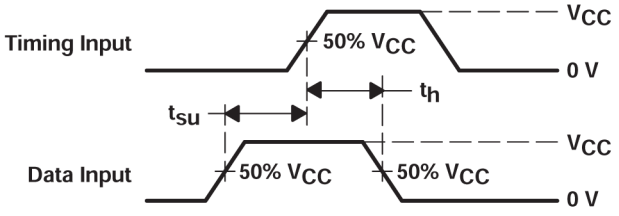


LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

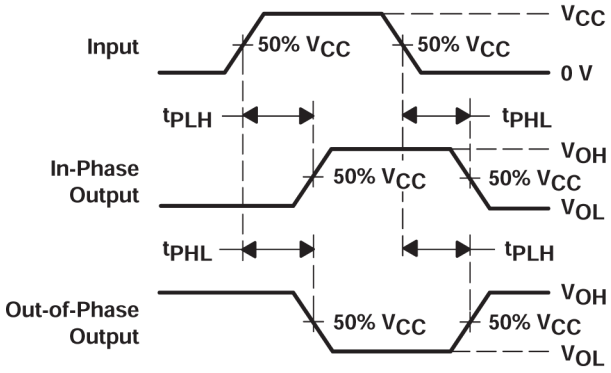
LOAD CIRCUIT FOR 3-STATE AND OPEN-DRAIN OUTPUTS



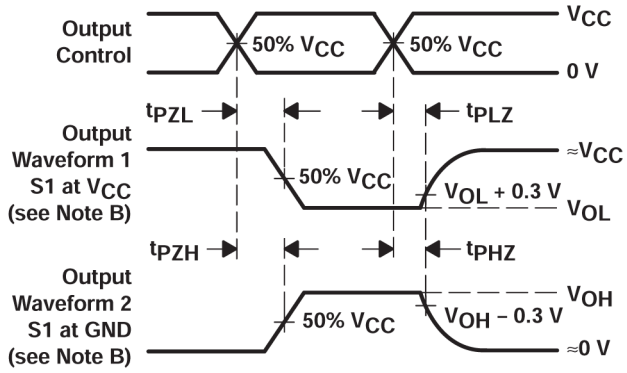
VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

Figure 6-1. Load Circuit and Voltage Waveforms

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

7 Detailed Description

7.1 Functional Block Diagram

Figure 7-1. Logic Diagram, Each Gate (Positive Logic)

7.2 Device Functional Modes

Table 7-1. Function Table (Each Gate)

INPUTS		OUTPUT Y
A	B	
H	H	L
L	X	H
X	L	H

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Documentation Support

8.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 8-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74AHC00-Q1	Click here	Click here	Click here	Click here	Click here

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHC00QDRG4Q1	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC00Q	Samples
SN74AHC00QDRQ1	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC00Q	Samples
SN74AHC00QPWRG4Q1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA00Q	Samples
SN74AHC00QPWRQ1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA00Q	Samples
SN74AHC00QWBQARQ1	ACTIVE	WQFN	BQA	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC00Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN74AHC00-Q1 :

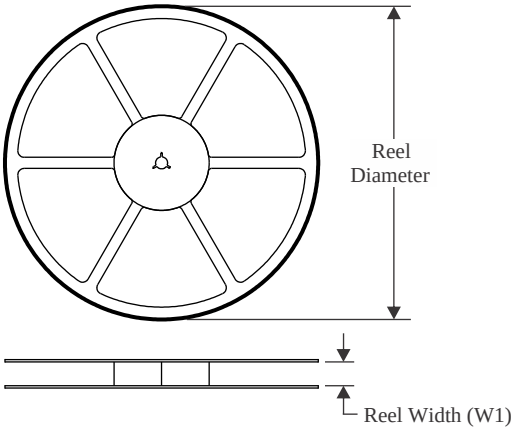
- Catalog : SN74AHC00
- Enhanced Product : SN74AHC00-EP
- Military : SN54AHC00

NOTE: Qualified Version Definitions:

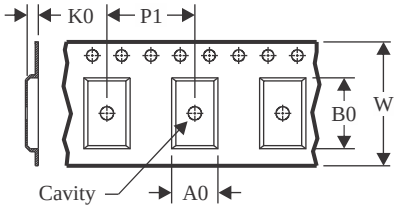
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

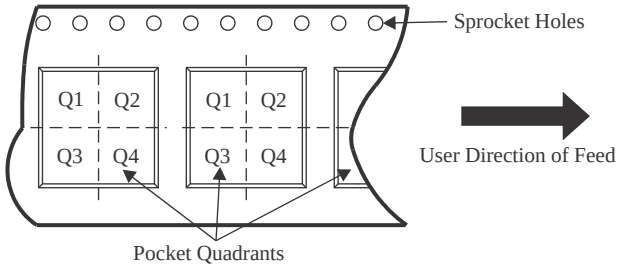


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

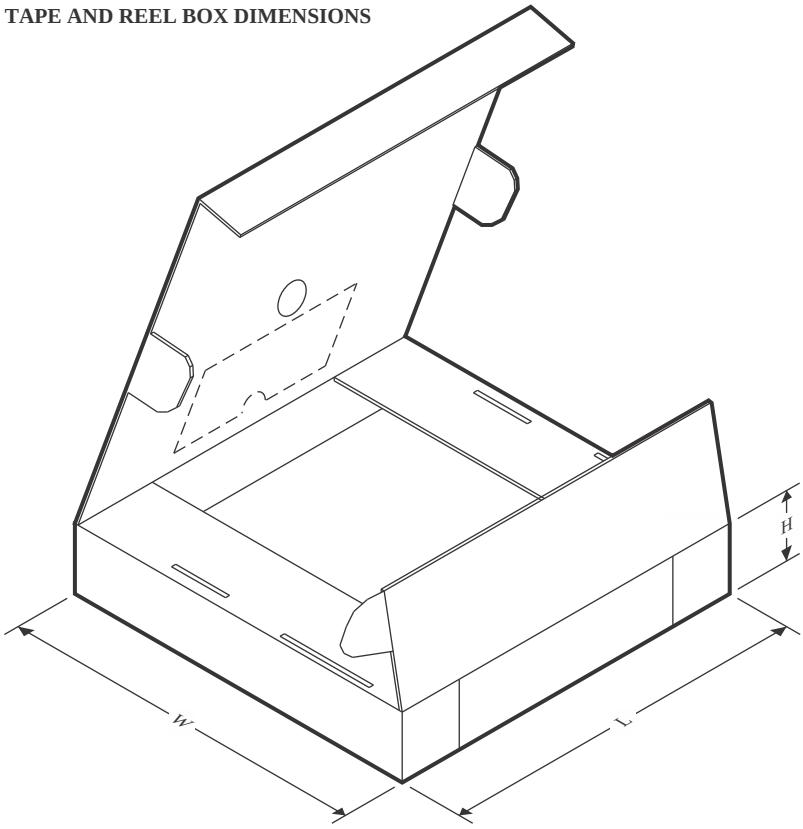
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

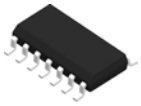
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC00QPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC00QPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC00QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC00QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC00QWBQARQ1	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC00QPWRG4Q1	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74AHC00QPWRG4Q1	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74AHC00QPWRQ1	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74AHC00QPWRQ1	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74AHC00QWBQARQ1	WQFN	BQA	14	3000	210.0	185.0	35.0

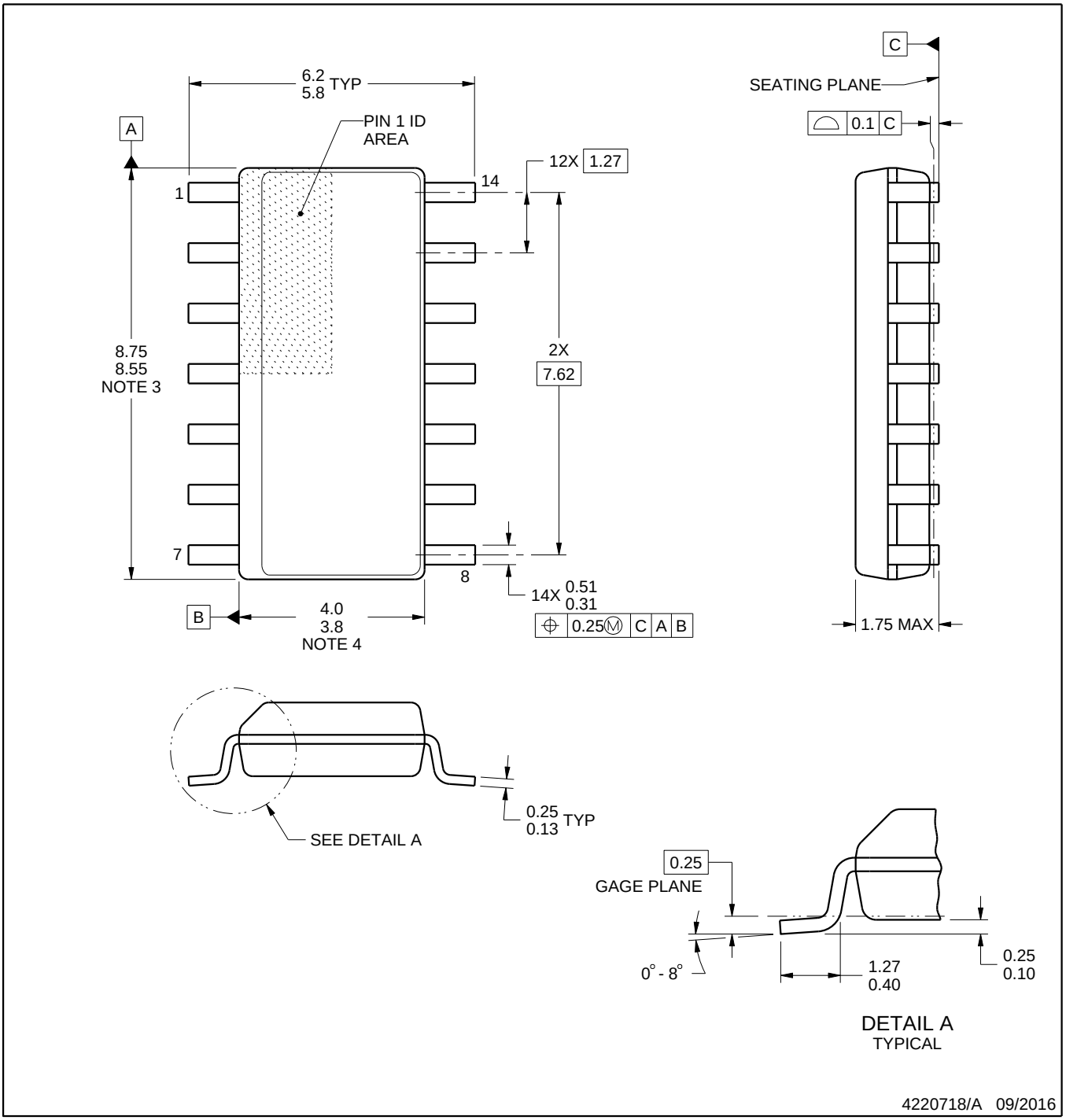


PACKAGE OUTLINE

D0014A

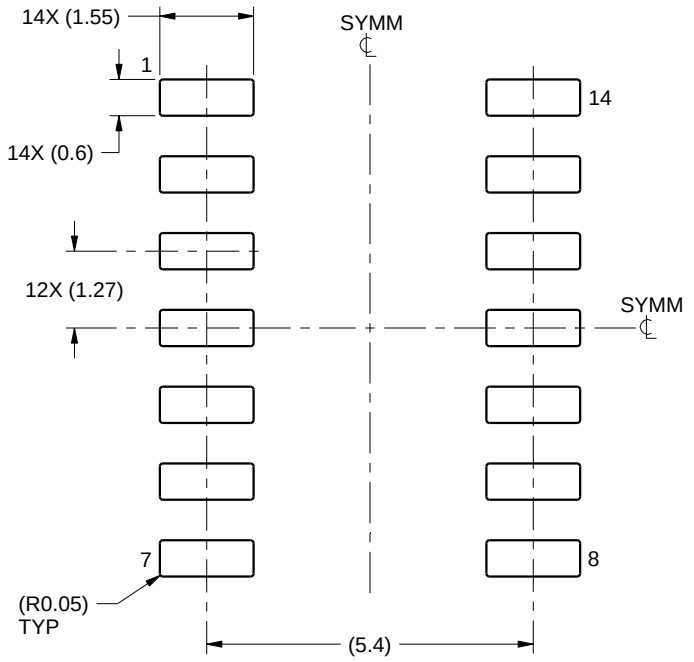
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

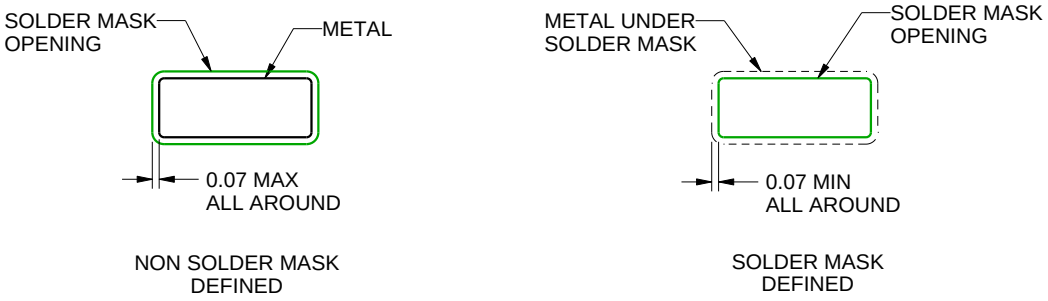


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

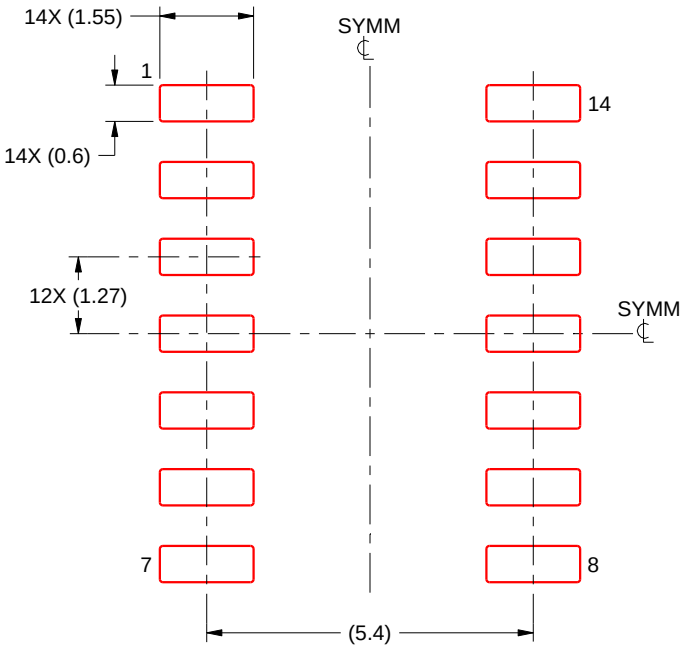
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

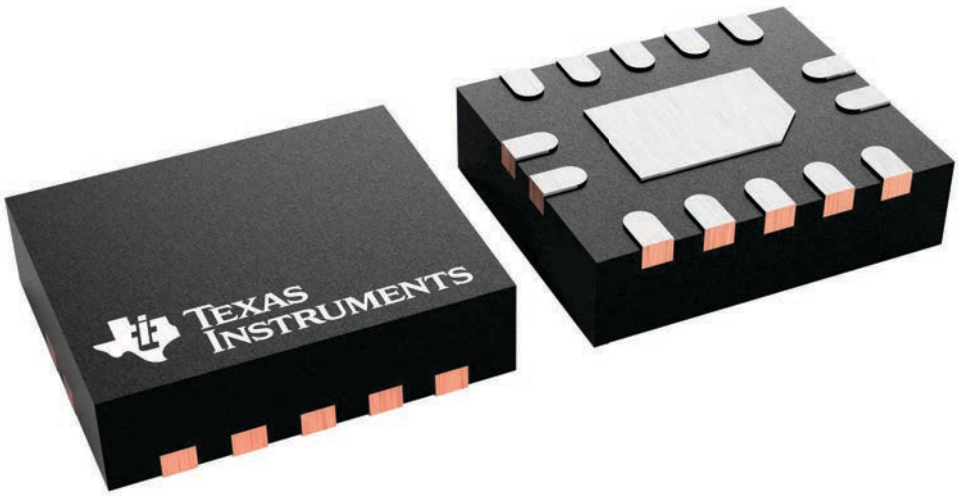
BQA 14

WQFN - 0.8 mm max height

2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

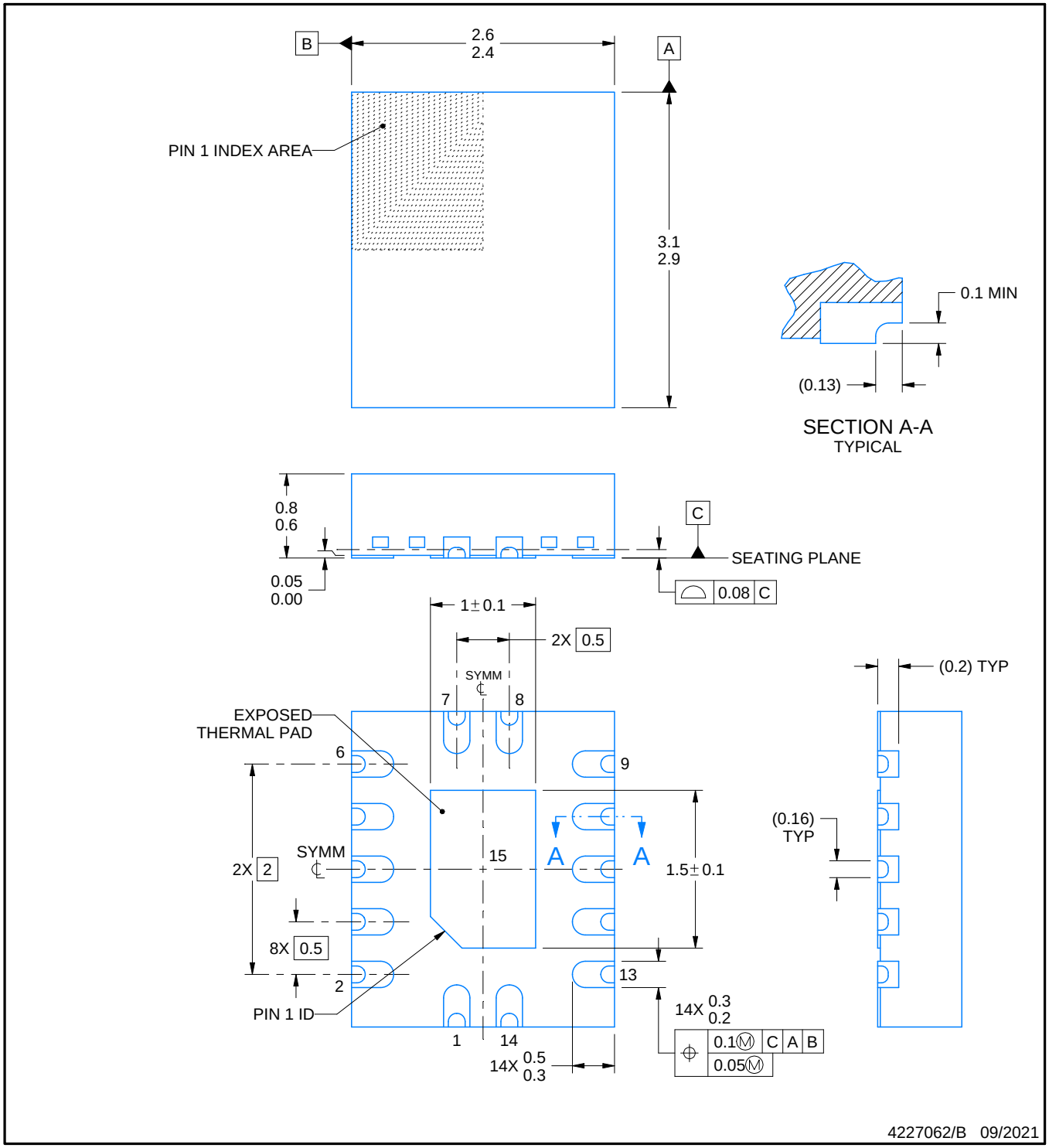


BQA0014B

PACKAGE OUTLINE

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

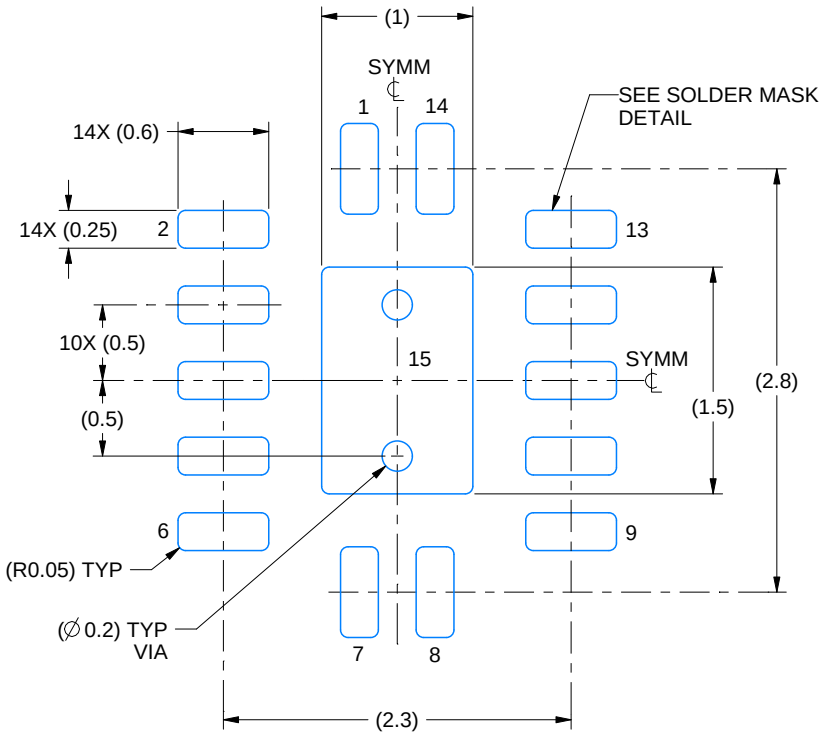
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

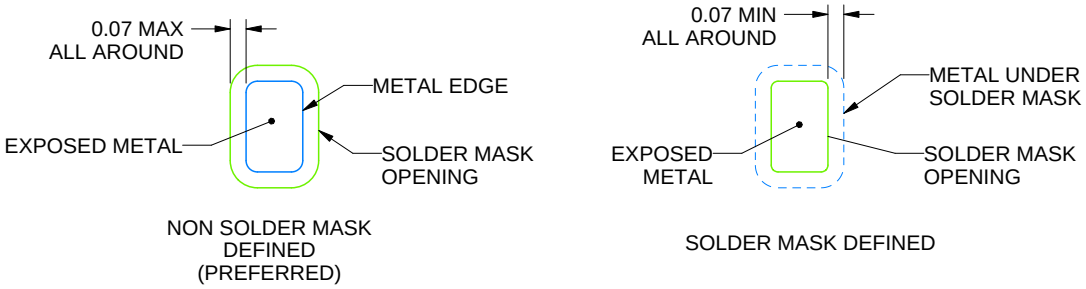
BQA0014B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

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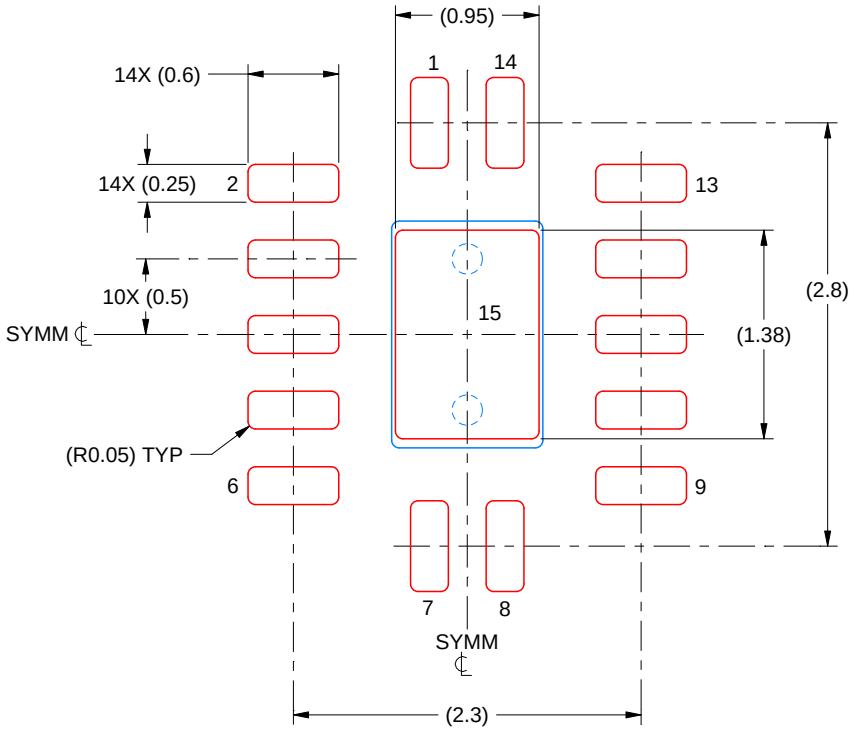
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 15
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

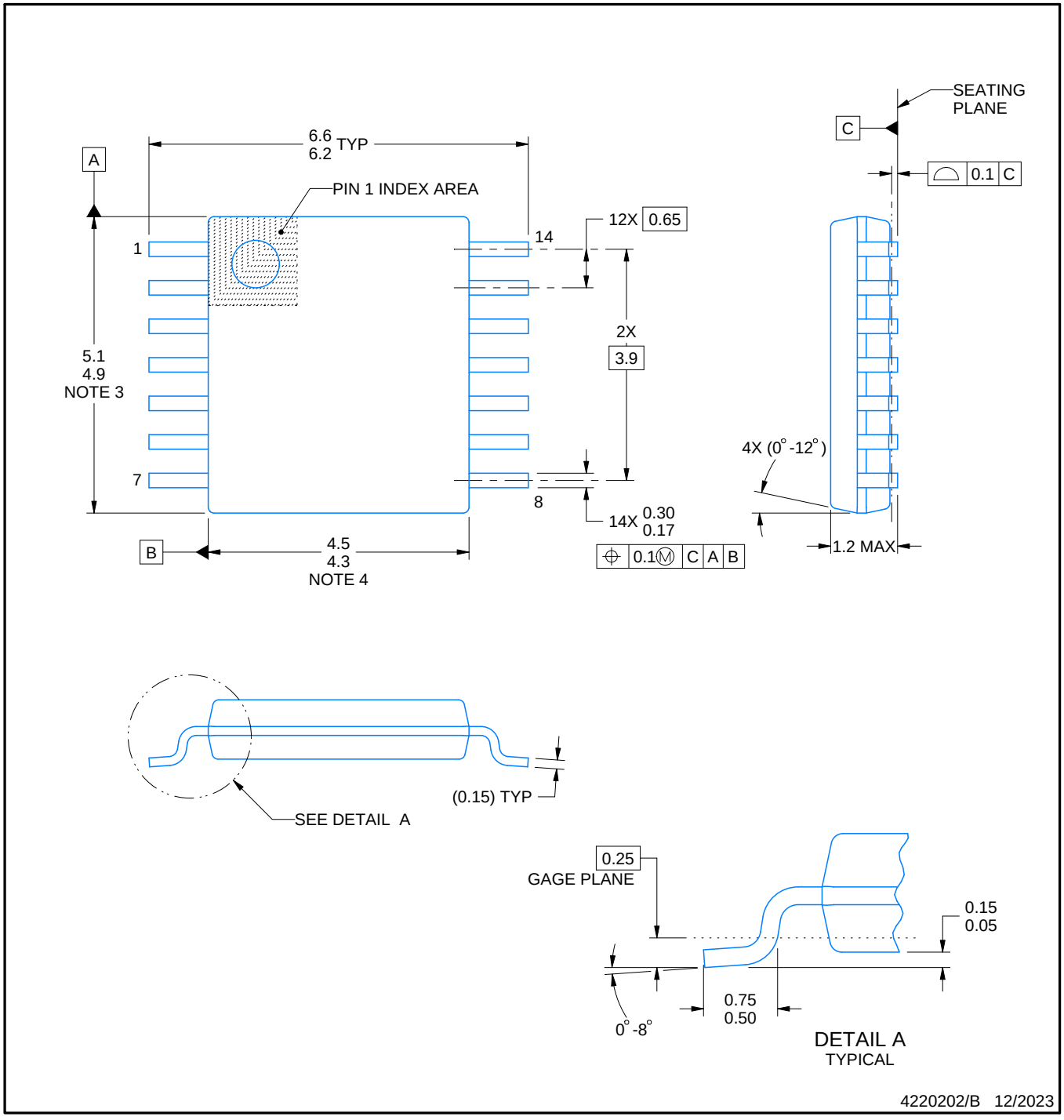
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

PW0014A

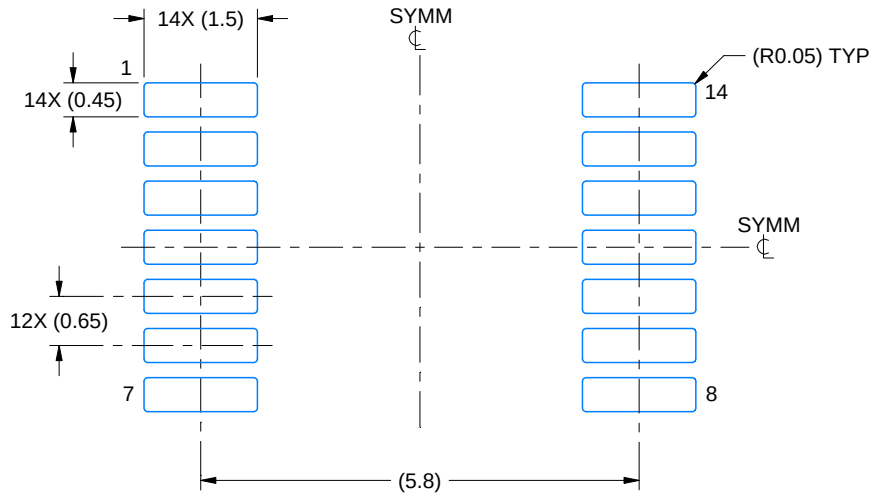
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

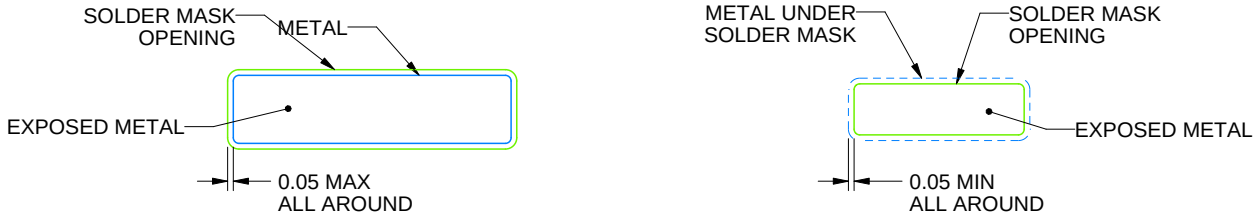


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

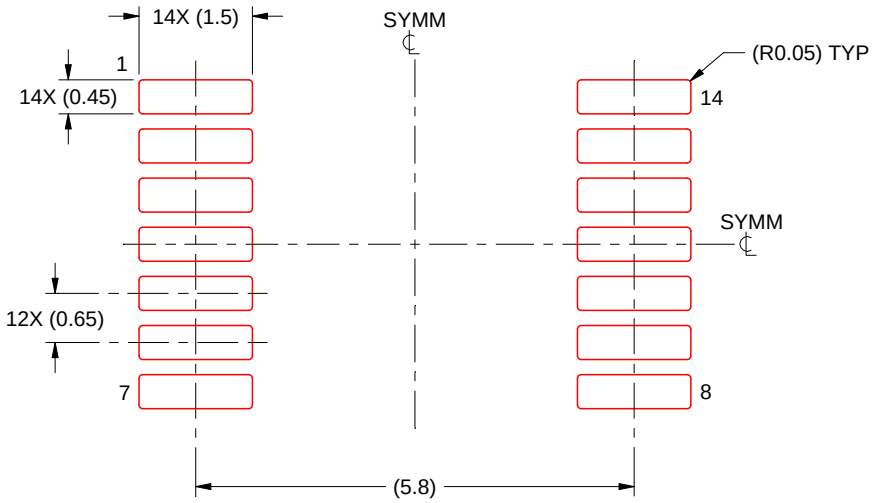


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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