Hex Schmitt-Trigger Inverter

High−Performance Silicon−Gate CMOS

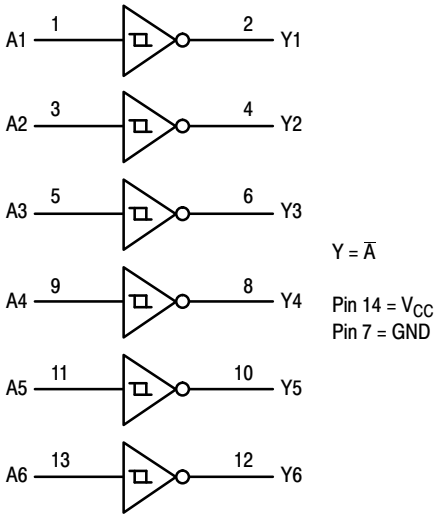
MC74HC14A, MC74HCT14A

The MC74HC14A/MC74HCT14A is useful to “square up” slow input rise and fall times. Due to hysteresis voltage of the Schmitt trigger, the device finds applications in noisy environments. The MC74HC14A has CMOS−level input thresholds while the MC74HCT14A has TTL−Level input thresholds.

Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance With the JEDEC Standard No. 7.0 A Requirements
- Chip Complexity: 72 FETs or 18 Equivalent Gates
- −Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

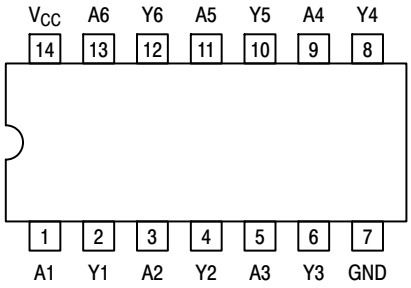
LOGIC DIAGRAM



SOIC−14 NB
D SUFFIX
CASE 751A

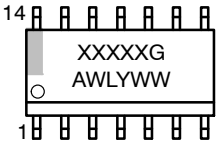
TSSOP−14
DT SUFFIX
CASE 948G

PIN ASSIGNMENT

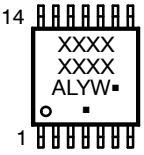


14−Lead (Top View)

MARKING DIAGRAMS



SOIC−14 NB



TSSOP−14

XXXX	= Specific Device Code
A	= Assembly Location
L, WL	= Wafer Lot
Y, YY	= Year
W, WW	= Work Week
G or ▪	= Pb−Free Package

(Note: Microdot may be in either location)

FUNCTION TABLE

Inputs	Outputs
A	Y
L	H
H	L

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		–0.5 to +6.5	V
V_{IN}	DC Input Voltage		–0.5 to V_{CC} + 0.5	V
V_{OUT}	DC Output Voltage		–0.5 to V_{CC} + 0.5	V
I_{IN}	DC Input Current, per Pin		±20	mA
I_{OUT}	DC Output Current, per Pin		±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins		±50	mA
I_{IK}	Input Clamp Current (V_{IN} < 0 or V_{IN} > V_{CC})		±20	mA
I_{OK}	Output Clamp Current (V_{OUT} < 0 or V_{OUT} > V_{CC})		±20	mA
T_{STG}	Storage Temperature		–65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature Under Bias		±150	°C
θ_{JA}	Thermal Resistance (Note 1)	SOIC–14 TSSOP–14	116 150	°C/W
P_D	Power Dissipation in Still Air at 25°C	SOIC–14 TSSOP–14	1077 833	mW
MSL	Moisture Sensitivity		Level 1	–
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V–0 @ 0.125 in	–
V_{ESD}	ESD Withstand Voltage (Note 2)	Human Body Model Charged Device Model	4000 1000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 76mm–by–114mm, 2–ounce copper trace no air flow per JESD51–7.
2. HBM tested to EIA / JESD22–A114–A. CDM tested to JESD22–C101–A. JEDEC recommends that ESD qualification to EIA/JESD22–A115A (Machine Model) be discontinued.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
MC74HC					
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND) (Note 4)		0	V_{CC}	V
T_A	Operating Free–Air Temperature		–55	+125	°C
t_r, t_f	Input Rise or Fall Time (Note 3)	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	No Limit No Limit No Limit	ns
MC74HCT					
V_{CC}	DC Supply Voltage (Referenced to GND)		4.5	5.5	V
V_{IN}, V_{OUT}	DC Input Voltage, DC Output Voltage (Referenced to GND) (Note 4)		0	V_{CC}	V
T_A	Operating Free–Air Temperature		–55	+125	°C
t_r, t_f	Input Rise or Fall Time (Note 3)		0	No Limit	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. No Limit when V_{IN} ⌣ 50% x V_{CC}, I_{CC} > 1 mA.
4. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC CHARACTERISTICS (MC74HC14A)

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit			Unit
				−55 to 25°C	≤85°C	≤125°C	
V_{T+} max	Maximum Positive−Going Input Threshold Voltage (Figure 3)	V_{out} = 0.1V $\|I_{out}\| \le 20\mu A$	2.0 3.0 4.5 6.0	1.50 2.15 3.15 4.20	1.50 2.15 3.15 4.20	1.50 2.15 3.15 4.20	V
V_{T+} min	Minimum Positive−Going Input Threshold Voltage (Figure 3)	V_{out} = 0.1V $\|I_{out}\| \le 20\mu A$	2.0 3.0 4.5 6.0	1.0 1.5 2.3 3.0	0.95 1.45 2.25 2.95	0.95 1.45 2.25 2.95	V
V_{T-} max	Maximum Negative−Going Input Threshold Voltage (Figure 3)	$V_{out} = V_{CC} - 0.1V$ $\|I_{out}\| \le 20\mu A$	2.0 3.0 4.5 6.0	0.9 1.4 2.0 2.6	0.95 1.45 2.05 2.65	0.95 1.45 2.05 2.65	V
V_{T-} min	Minimum Negative−Going Input Threshold Voltage (Figure 3)	$V_{out} = V_{CC} - 0.1V$ $\|I_{out}\| \le 20\mu A$	2.0 3.0 4.5 6.0	0.3 0.5 0.9 1.2	0.3 0.5 0.9 1.2	0.3 0.5 0.9 1.2	V
$V_H$max (Note 5)	Maximum Hysteresis Voltage (Figure 3)	V_{out} = 0.1V or V_{CC} − 0.1V $\|I_{out}\| \le 20\mu A$	2.0 3.0 4.5 6.0	1.20 1.65 2.25 3.00	1.20 1.65 2.25 3.00	1.20 1.65 2.25 3.00	V
$V_H$min (Note 5)	Minimum Hysteresis Voltage (Figure 3)	V_{out} = 0.1V or V_{CC} − 0.1V $\|I_{out}\| \le 20\mu A$	2.0 3.0 4.5 6.0	0.20 0.25 0.40 0.50	0.20 0.25 0.40 0.50	0.20 0.25 0.40 0.50	V
V_{OH}	Minimum High−Level Output Voltage	$V_{in} \le V_{T-}$ min $\|I_{out}\| \le 20\mu A$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} \le V_{T-}$ min $\|I_{out}\| \le 2.4mA$ $\|I_{out}\| \le 4.0mA$ $\|I_{out}\| \le 5.2mA$	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.20 3.70 5.20	
V_{OL}	Maximum Low−Level Output Voltage	$V_{in} \ge V_{T+}$ max $\|I_{out}\| \le 20\mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} \ge V_{T+}$ max $\|I_{out}\| \le 2.4mA$ $\|I_{out}\| \le 4.0mA$ $\|I_{out}\| \le 5.2mA$	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.40 0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND I_{out} = 0μA	6.0	1.0	10	40	μA

5. $V_H$min > (V_{T+} min) − (V_{T-} max); $V_H$max = (V_{T+} max) − (V_{T-} min).

AC CHARACTERISTICS (MC74HC14A)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			−55 to 25°C	≤85°C	≤125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2)	2.0 3.0 4.5 6.0	75 30 15 13	95 40 19 16	110 55 22 19	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 3.0 4.5 6.0	75 27 15 13	95 32 19 16	110 36 22 19	ns
C_{in}	Maximum Input Capacitance		10	10	10	pF
		Typical @ 25°C, V_{CC} = 5.0 V				
C_{PD}	Power Dissipation Capacitance (Per Inverter) (Note 6)	22				pF

6. Used to determine the no−load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

DC ELECTRICAL CHARACTERISTICS (MC74HCT14A)

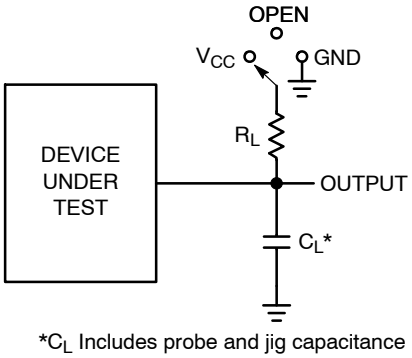
Symbol	Parameter	Test Conditions	V_{CC} Volts	Temperature Limit: −55°C to 25°C Min	−55°C to 25°C Max	≤85°C Min	≤85°C Max	≤125°C Min	≤125°C Max	Unit
V_{T+} max	Maximum Positive−Going Input Threshold Voltage	V_O = 0.1 V or V_{CC} − 0.1 V $\|I_{out}\| \le 20$ μA	4.5 5.5		1.9 2.1		1.9 2.1		1.9 2.1	V
V_{T+} min	Minimum Positive−Going Input Threshold Voltage	V_O = 0.1 V or V_{CC} − 0.1 V $\|I_{out}\| \le 20$ μA	4.5 5.5	1.2 1.4		1.2 1.4		1.2 1.4		V
V_{T-} max	Maximum Negative−Going Input Threshold Voltage	V_O = 0.1 V or V_{CC} − 0.1 V $\|I_{out}\| \le 20$ μA	4.5 5.5		1.2 1.4		1.2 1.4		1.2 1.4	
V_{T-} min	Minimum Negative−Going Input Threshold Voltage	V_O = 0.1 V or V_{CC} − 0.1 V $\|I_{out}\| \le 20$ μA	4.5 5.5	0.5 0.6		0.5 0.6		0.5 0.6		
V_H max	Maximum Hysteresis Voltage	V_O = 0.1 V or V_{CC} − 0.1 V $\|I_{out}\| \le 20$ μA	4.5 5.5		1.4 1.5		1.4 1.5		1.4 1.5	
V_H min	Minimum Hysteresis Voltage	V_O = 0.1 V or V_{CC} − 0.1 V $\|I_{out}\| \le 20$ μA	4.5 5.5	0.4 0.4		0.4 0.4		0.4 0 4		
V_{OH}	Minimum High−Level Output Voltage	$V_I < V_{T-}$ min $\|I_{out}\| \le 20$ μA	4.5 5.5	4.4 5.4		4.4 5.4		4.4 5.4		V
		$V_I < V_{T-}$ min $\|I_{out}\| \le 4.0$ mA	4.5	3.98		3.84		3.7		
V_{OL}	Maximum Low−Level Output Voltage	$V_I \ge V_{T+}$ max $\|I_{out}\| \le 20$ μA	4.5 5.5		0.1 0.1		0.1 0.1		0.1 0.1	V
		$V_I \ge V_{T+}$ max $\|I_{out}\| \le 4.0$ mA	4.5		0.26		0.33		0.4	
I_{IK}	Maximum Input Leakage Current	V_I = V_{CC} or GND	5.5		±0.1		±1.0		±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per package)	V_I = V_{CC} or GND I_{out} = 0 μA	5.5		1.0		10		40	μA
ΔI_{CC}	Additional Quiescent Supply Current	V_I = 2.4 V, Any One Input V_I = V_{CC} or GND, Other Inputs I_{out} = 0 μA	5.5	≥ −55°C: 2.9		25°C to 125°C: 2.4				mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC CHARACTERISTICS (MC74HCT14A)

Symbol	Parameter	Test Conditions	Figures	Guaranteed Limit: −55°C to 25°C Min	−55°C to 25°C Max	≤85°C Min	≤85°C Max	≤125°C Min	≤125°C Max	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A to Output Y (L to H)	V_{CC} = 5.0 V ±10% C_L = 50 pF, Input t_r = t_f = 6.0 ns	1 & 2		32		40		48	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output	V_{CC} = 5.0 V ±10% C_L = 50 pF, Input t_r = t_f = 6.0 ns	1 & 2		15		19		22	ns

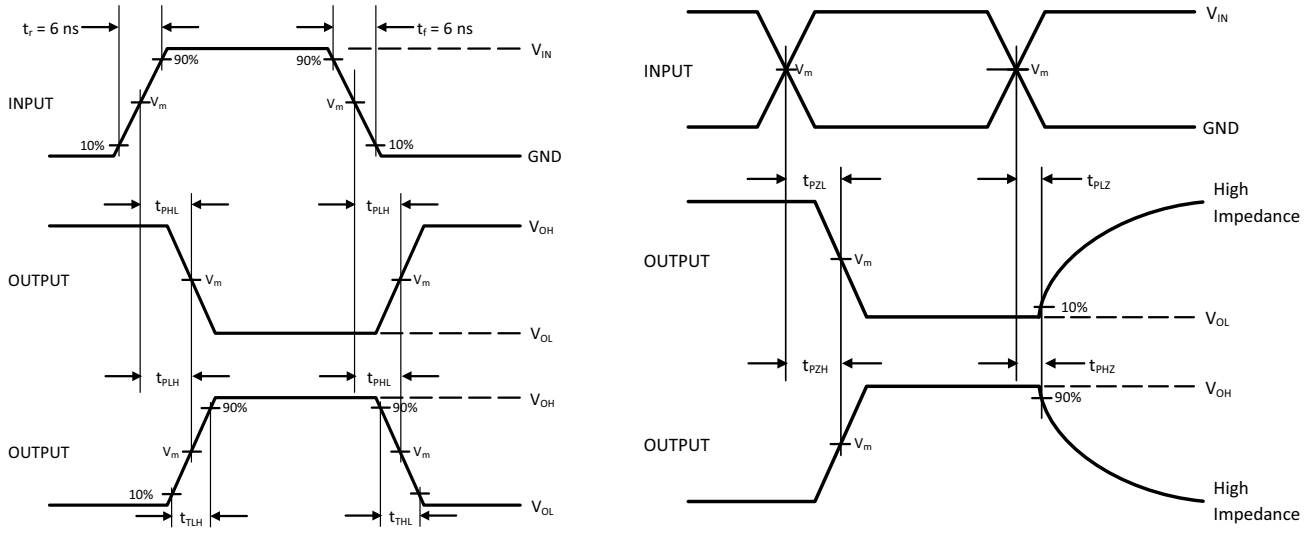
		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance, per Inverter (Note 6)	32	pF



*C_L Includes probe and jig capacitance

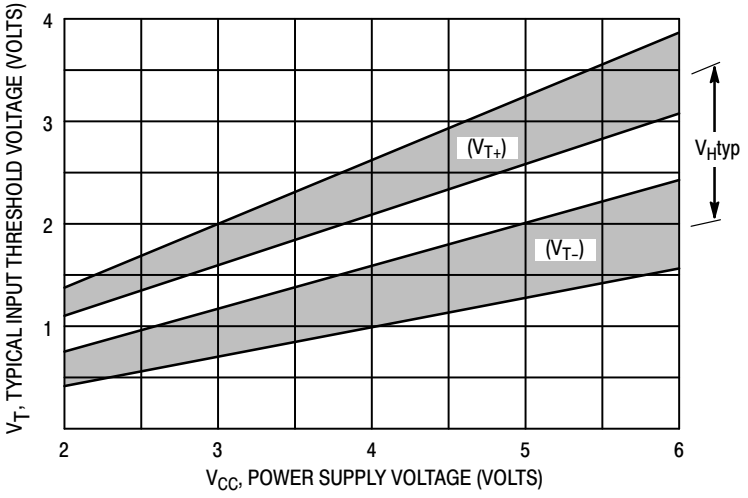
Test	Switch Position	C_L	R_L
t_{PLH} / t_{PHL}	Open	50 pF	1 kΩ
t_{PLZ} / t_{PZL}	V_{CC}		
t_{PHZ} / t_{PZH}	GND		

Figure 1. Test Circuit



Device	V_{IN}, V	V_m, V
MC74HC14A	V_{CC}	50% x V_{CC}
MC74HCT14A	3 V	1.3 V

Figure 2. Switching Waveforms



$V_H$typ = (V_{T+} typ) − (V_{T-} typ)

Figure 3. Typical Input Threshold, V_{T+}, V_{T-} versus Power Supply Voltage

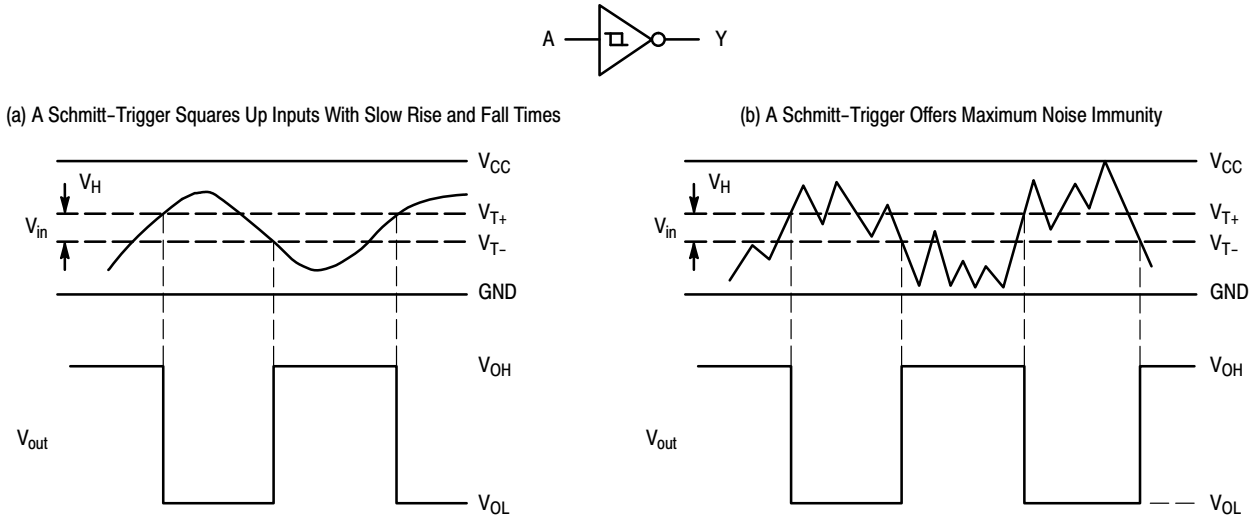


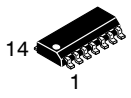
Figure 4. Typical Schmitt−Trigger Applications

ORDERING INFORMATION

Device	Marking†	Package	Shipping†
MC74HC14ADG	HC14AG	SOIC−14	55 Units / Rail
MC74HC14ADR2G	HC14AG	SOIC−14	2500 / Tape & Reel
MC74HC14ADR2G−Q*	HC14AG	SOIC−14	2500 / Tape & Reel
MC74HC14ADTG	HC 14A	TSSOP−14	96 Units / Rail
MC74HC14ADTR2G	HC 14A	TSSOP−14	2500 / Tape & Reel
MC74HC14ADTR2G−Q*	HC 14A	TSSOP−14	2500 / Tape & Reel
MC74HCT14ADG	HCT14AG	SOIC−14	55 Units / Rail
MC74HCT14ADR2G	HCT14AG	SOIC−14	2500 / Tape & Reel
MC74HCT14ADR2G−Q*	HCT14AG	SOIC−14	2500 / Tape & Reel
MC74HCT14ADTR2G	HCT 14A	TSSOP−14	2500 / Tape & Reel
MC74HCT14ADTR2G−Q*	HCT 14A	TSSOP−14	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

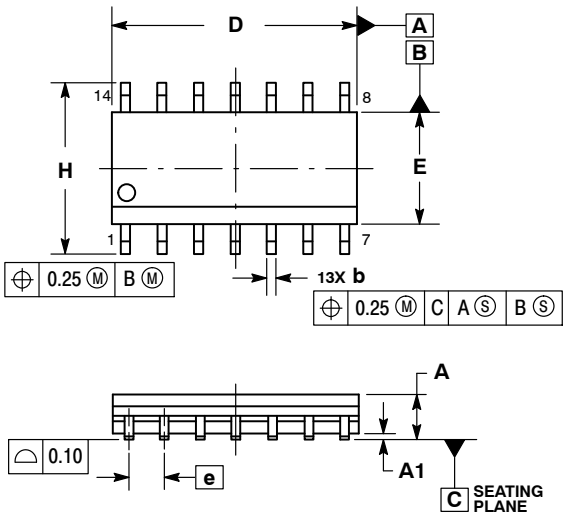
*−Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable

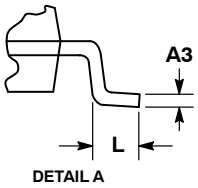


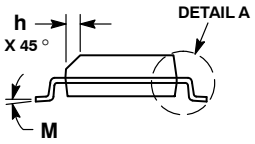
SCALE 1:1

SOIC−14 NB
CASE 751A−03
ISSUE L

DATE 03 FEB 2016



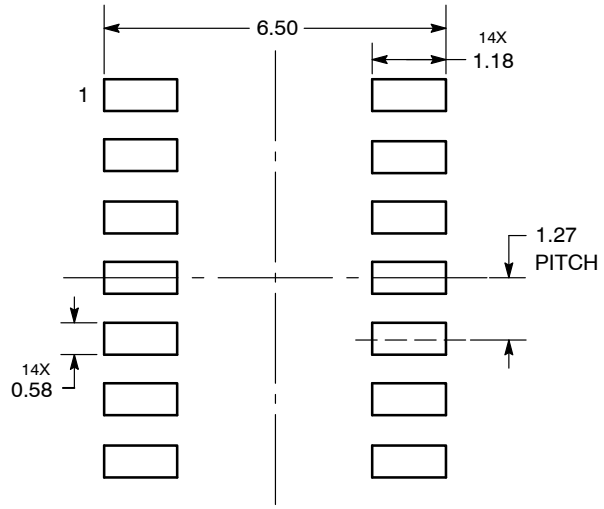




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

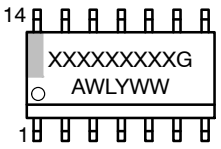
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42565B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**SOIC−14 NB**		**PAGE 1 OF 2**

SOIC−14
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

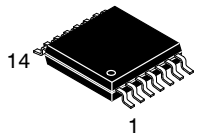
STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

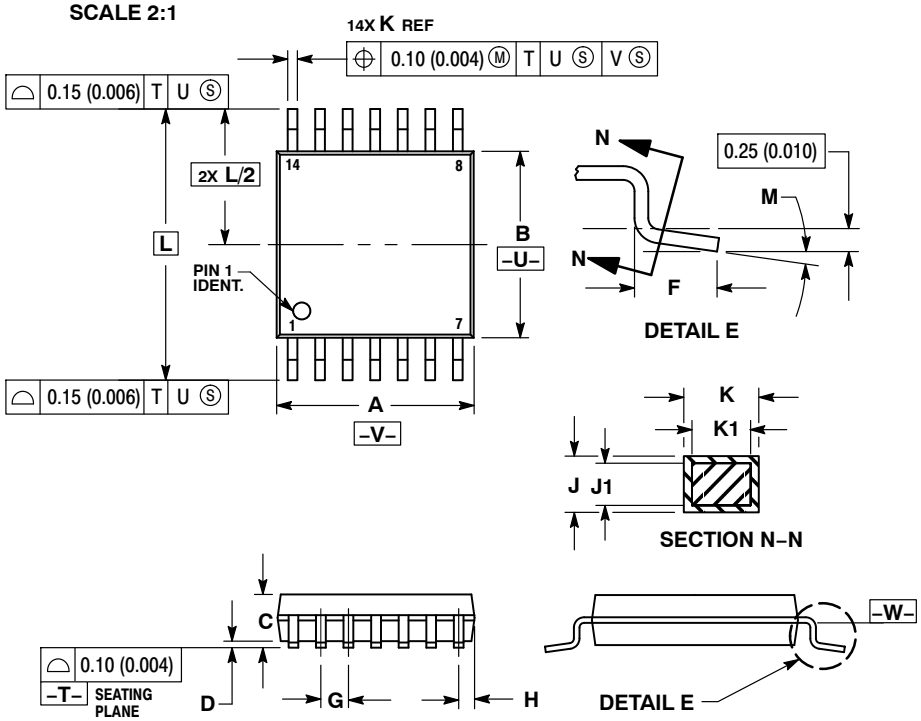
STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE



SCALE 2:1

TSSOP−14 WB
CASE 948G
ISSUE C

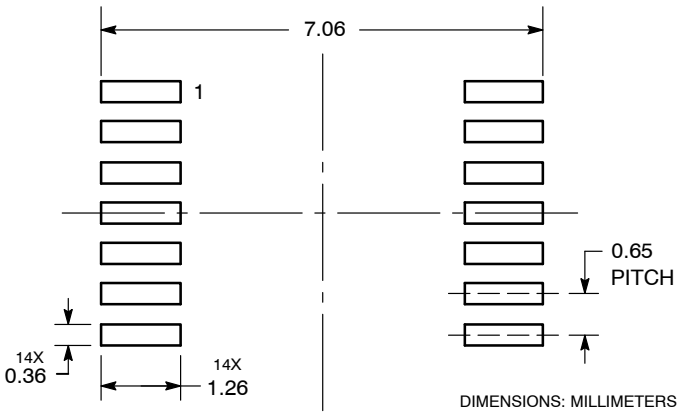
DATE 17 FEB 2016



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

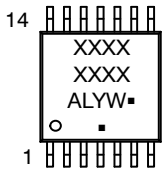
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**TSSOP−14 WB**	**PAGE 1 OF 1**

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