TEXAS INSTRUMENTS

SN74AUP1G08
SCES502Q – NOVEMBER 2003 – REVISED MARCH 2024

SN74AUP1G08 Low-Power Single 2-Input Positive-AND Gate

1 Features

- Available in the Ultra Small 0.64mm^2 Package (DPW) With 0.5mm Pitch
- Low Static-Power Consumption:
  I_{CC} = 0.9µA Maximum
- Low Dynamic-Power Consumption:
  C_{pd} = 4.3pF Typical at 3.3V
- Low Input Capacitance: C_i = 1.5pF Typical
- Low Noise: Overshoot and Undershoot <10% of V_{CC}
- I_{off} Supports Live Insertion, Partial-Power-Down Mode, and Back Drive Protection
- Schmitt-Trigger Action Allows Slow Input Transition and Better Switching Noise Immunity at the Input (V_{hys} = 250 mV Typical at 3.3V)
- Wide Operating V_{CC} Range of 0.8V to 3.6V
- Optimized for 3.3V Operation
- 3.6V I/O Tolerant to Support Mixed-Mode Signal Operation
- t_{pd} = 4.3ns Maximum at 3.3V
- Suitable for Point-to-Point Applications
- Latch-Up Performance Exceeds 100mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000V Human-Body Model (A114-B, Class II)
  - 1000V Charged-Device Model (C101)
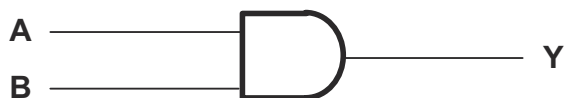
Simplified Schematic

2 Applications

- ATCA Solutions
- Active Noise Cancellation (ANC)
- Barcode Scanner
- Blood Pressure Monitor
- CPAP Machine
- Cable Solutions
- DLP 3D Machine Vision, Hyperspectral Imaging, Optical Networking, and Spectroscopy
- E-Book
- Embedded PC
- Field Transmitter: Temperature or Pressure Sensor
- Fingerprint Biometrics
- HVAC: Heating, Ventilating, and Air Conditioning
- Network-Attached Storage (NAS)
- Server Motherboard and PSU
- Software Defined Radio (SDR)
- TV: High-Definition (HDTV), LCD, and Digital
- Video Communications System
- Wireless Data Access Card, Headset, Keyboard, Mouse, and LAN Card
- X-ray: Baggage Scanner, Medical, and Dental

3 Description

This single 2-input positive-AND gate is designed for 0.8V to 3.6V V_{CC} operation and performs the Boolean function $Y = A \bullet B$ or $Y = \overline{\overline{A} + \overline{B}}$ in positive logic.

Device Information

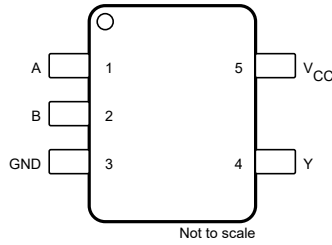| PART NUMBER	PACKAGE [1]	BODY SIZE (NOM)
SN74AUP1G08DBV	SOT-23 (5)	2.90 mm × 1.60mm
SN74AUP1G08DRL	SOT (5)	1.60 mm × 1.20mm
SN74AUP1G08DRY	SON (6)	1.45 mm × 1.00mm
SN74AUP1G08DPW	X2SON (5)	0.80 mm × 0.80mm
SN74AUP1G08YZP	DSBGA (5)	1.37 mm × 0.88mm
SN74AUP1G08DCK	SC70 (5)	1.25 mm x 2.00mm
SN74AUP1G08DSF	SON (6)	1.00 mm x 1.00mm
SN74AUP1G08YFP	DSBGA (6)	1.16 mm x 0.76mm

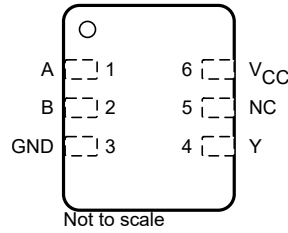(1) For all available packages, see the orderable addendum at the end of the data sheet.

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4 Pin Configuration and Functions

Figure 4-1. DRL, DCK, or DBV Packages 5-Pin SOT, SC70, or SOT-23 Top View

N.C. – No internal connection

Figure 4-2. DRY or DSF Packages 6-Pin SON Top View
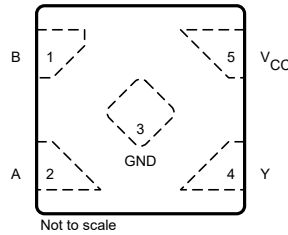
See mechanical drawings for dimensions.

Figure 4-3. DPW Package 5-PIN X2SON Top View
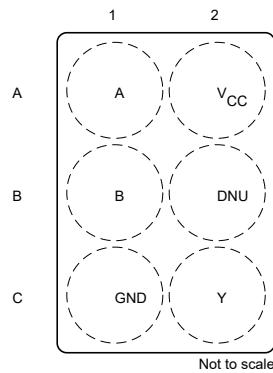
DNU – Do not use

Figure 4-4. YFP Package 6-Pin DSBGA Top View

Product Folder Links: *SN74AUP1G08*

Not to scale
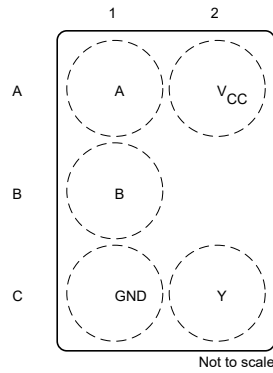
Figure 4-5. YZP Package 5-Pin DSBGA Top View

Table 4-1. Pin Functions

	PIN					I/O	DESCRIPTION
NAME	DRL, DCK, DBV	DPW	DRY, DSF	YZP	YFP		
A	1	2	1	A1	A1	I	Input A
B	2	1	2	B1	B1	I	Input B
DNU	–	–	–	–	B2	–	Do not use
GND	3	3	3	C1	C1	–	Ground
N.C.	–	–	5	–	–	–	No internal connection
V_{CC}	5	5	6	A2	A2	–	Power Pin
Y	4	4	4	C2	C2	O	Output Y

Product Folder Links: *SN74AUP1G08*

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		−0.5	4.6	V
V_I	Input voltage[2]		−0.5	4.6	V
V_O	Voltage range applied to any output in the high-impedance or power-off state[2]		−0.5	4.6	V
V_O	Output voltage range in the high or low state[2]		−0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		−50	mA
I_{OK}	Output clamp current	V_O < 0		−50	mA
I_O	Continuous output current			±20	mA
	Continuous current through V_{CC} or GND			±50	mA
T_J	Maximum junction temperature			150	°C
T_{stg}	Storage temperature		−65	150	°C

(1)   Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2)   The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101[2]	1000	

(1)   JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2)   JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) [1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		0.8	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 0.8 V	V_{CC}		V
		V_{CC} = 1.1 V to 1.95 V	0.65 × V_{CC}		
		V_{CC} = 2.3 V to 2.7 V	1.6		
		V_{CC} = 3 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 0.8 V		0	V
		V_{CC} = 1.1 V to 1.95 V		0.35 × V_{CC}	
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 3 V to 3.6 V		0.9	
V_I	Input voltage		0	3.6	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 0.8 V		−20	µA
		V_{CC} = 1.1 V		−1.1	mA
		V_{CC} = 1.4 V		−1.7	
		V_{CC} = 1.65		−1.9	
		V_{CC} = 2.3 V		−3.1	
		V_{CC} = 3 V		−4	

5.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted) [1]

			MIN	MAX	UNIT
I_{OL}	Low-level output current	V_{CC} = 0.8 V		20	µA
		V_{CC} = 1.1 V		1.1	
		V_{CC} = 1.4 V		1.7	
		V_{CC} = 1.65 V		1.9	mA
		V_{CC} = 2.3 V		3.1	
		V_{CC} = 3 V		4	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 0.8 V to 3.6 V		200	ns/V
T_A	Operating free-air temperature		–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

5.4 Thermal Information

THERMAL METRIC[1]		SN74AUP1G08						UNIT
		DBV (SOT-23)	DCK (SC70)	DRL (SOT)	DSF (SON)	DRY (SON)	DPW (X2SON)	
		5 PINS	5 PINS	5 PINS	6 PINS	6 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	298.6	314.4	349.7	407.1	554.9	291.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	240.2	128.7	120.5	232	385.4	224.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	134.6	100.6	171.4	306.9	388.2	245.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	114.5	7.1	10.8	40.3	159	245.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	133.9	99.8	169.4	306	384.1	195.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_CC	T_A = 25°C MIN	T_A = 25°C TYP	T_A = 25°C MAX	T_A = –40°C to +85°C MIN	T_A = –40°C to +85°C MAX	UNIT
V_{OH}	I_{OH} = –20 µA	0.8 V to 3.6 V	V_{CC} – 0.1			V_{CC} – 0.1		V
	I_{OH} = –1.1 mA	1.1 V	0.75 × V_{CC}			0.7 × V_{CC}		
	I_{OH} = –1.7 mA	1.4 V	1.11			1.03		
	I_{OH} = –1.9 mA	1.65 V	1.32			1.3		
	I_{OH} = –2.3 mA	2.3 V	2.05			1.97		
	I_{OH} = –3.1 mA		1.9			1.85		
	I_{OH} = –2.7 mA	3 V	2.72			2.67		
	I_{OH} = –4 mA		2.6			2.55		
V_{OL}	I_{OL} = 20 µA	0.8 V to 3.6 V			0.1		0.1	V
	I_{OL} = 1.1 mA	1.1 V			0.3 × V_{CC}		0.3 × V_{CC}	
	I_{OL} = 1.7 mA	1.4 V			0.31		0.37	
	I_{OL} = 1.9 mA	1.65 V			0.31		0.35	
	I_{OL} = 2.3 mA	2.3 V			0.31		0.33	
	I_{OL} = 3.1 mA				0.44		0.45	
	I_{OL} = 2.7 mA	3 V			0.31		0.33	
	I_{OL} = 4 mA				0.44		0.45	
I_I A or B input	V_I = GND to 3.6 V	0 V to 3.6 V			0.1		0.5	µA
I_{off}	V_I or V_O = 0 V to 3.6 V	0 V			0.2		0.6	µA
ΔI_{off}	V_I or V_O = 0 V to 3.6 V	0 V to 0.2 V			0.2		0.6	µA
I_{CC}	V_I = GND or (V_{CC} to 3.6 V) I_O = 0	0.8 V to 3.6 V			0.5		0.9	µA
ΔI_{CC}	V_I = V_{CC} – 0.6 V[1] I_O = 0	3.3 V			40		50	µA
C_i	V_I = V_{CC} or GND	0 V		1.5				pF
		3.6 V		1.5				
C_o	V_O = GND	0 V		3				pF

(1)   One input at V_{CC} – 0.6 V, other input at V_{CC} or GND.

5.6 Switching Characteristics, C_L = 5 pF

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 6-1 and Figure 6-2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_CC	T_A = 25°C MIN	T_A = 25°C TYP	T_A = 25°C MAX	T_A = –40°C to +85°C MIN	T_A = –40°C to +85°C MAX	UNIT
t_{pd}	A or B	Y	0.8 V		18				ns
			1.2 V ± 0.1 V	2.6	7.3	12.8	2.1	15.6	
			1.5 V ± 0.1 V	1.4	5.2	8.7	0.9	10.3	
			1.8 V ± 0.15 V	1	4.2	6.6	0.5	8.2	
			2.5 V ± 0.2 V	1	3	4.4	0.5	5.5	
			3.3 V ± 0.3 V	1	2.4	3.5	0.5	4.3	

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Product Folder Links: SN74AUP1G08

5.7 Switching Characteristics, C$_L$ = 10 pF

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 6-1 and Figure 6-2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V$_{CC}$	T$_A$ = 25°C			T$_A$ = –40°C to +85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t$_{pd}$	A or B	Y	0.8 V		21				ns
			1.2 V ± 0.1 V	1.5	8.5	14.7	1	17.2	
			1.5 V ± 0.1 V	1	6.2	10	0.5	11.3	
			1.8 V ± 0.15 V	1	5	7.7	0.5	9	
			2.5 V ± 0.2 V	1	3.6	5.2	0.5	6.1	
			3.3 V ± 0.3 V	1	2.9	4.2	0.5	4.7	

5.8 Switching Characteristics, C$_L$ = 15 pF

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 6-1 and Figure 6-2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V$_{CC}$	T$_A$ = 25°C			T$_A$ = –40°C to +85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t$_{pd}$	A or B	Y	0.8 V		24				ns
			1.2 V ± 0.1 V	3.6	9.9	16.3	3.1	19.9	
			1.5 V ± 0.1 V	2.3	7.2	11.1	1.8	13.2	
			1.8 V ± 0.15 V	1.6	5.8	8.7	1.1	10.6	
			2.5 V ± 0.2 V	1	4.3	5.9	0.5	7.3	
			3.3 V ± 0.3 V	1	3.4	4.8	0.5	5.9	

5.9 Switching Characteristics, C$_L$ = 30 pF

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 6-1 and Figure 6-2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V$_{CC}$	T$_A$ = 25°C			T$_A$ = –40°C to +85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t$_{pd}$	A or B	Y	0.8 V		32.8				ns
			1.2 V ± 0.1 V	4.9	13.1	20.9	4.4	25.5	
			1.5 V ± 0.1 V	3.4	9.5	14.2	2.9	16.9	
			1.8 V ± 0.15 V	2.5	7.7	11	2	13.5	
			2.5 V ± 0.2 V	1.8	5.7	7.6	1.3	9.4	
			3.3 V ± 0.3 V	1.5	4.7	6.2	1	7.5	

5.10 Operating Characteristics

T$_A$ = 25°C

PARAMETER		TEST CONDITIONS	V$_{CC}$	TYP	UNIT
C$_{pd}$	Power dissipation capacitance	f = 10 MHz	0.8 V	4	pF
			1.2 V ± 0.1 V	4	
			1.5 V ± 0.1 V	4	
			1.8 V ± 0.15 V	4	
			2.5 V ± 0.2 V	4.1	
			3.3 V ± 0.3 V	4.3	

Product Folder Links: *SN74AUP1G08*

5.11 Typical Characteristics

Figure 5-1. TPD vs V_{CC}, 15 pF Load

Figure 5-2. TPD vs Temperature 1.8 V, 15 pF Load

Product Folder Links: *SN74AUP1G08*
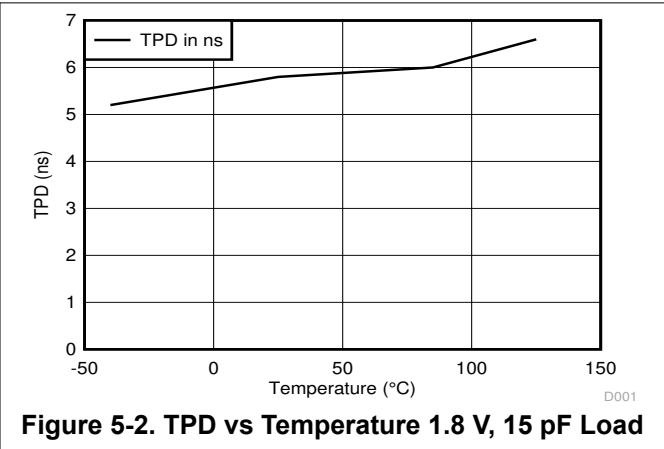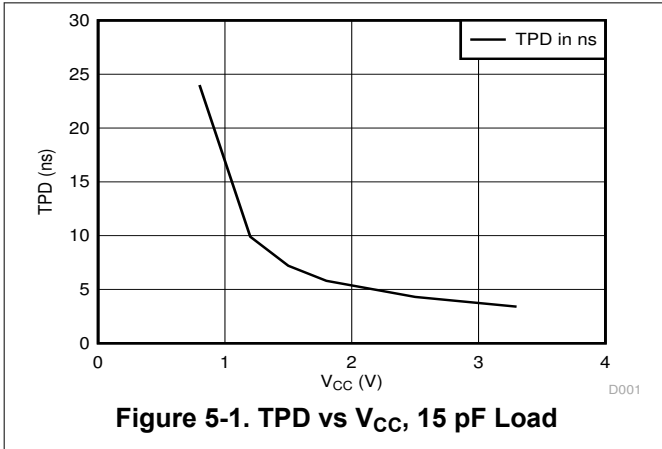
6 Parameter Measurement Information

6.1 Propagation Delays, Setup and Hold Times, and Pulse Duration

From Output
Under Test

C_L
(see Note A)

1 MΩ
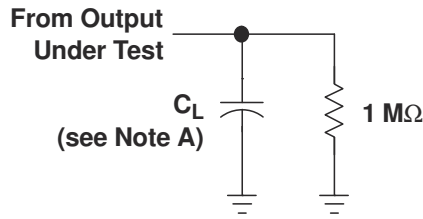
LOAD CIRCUIT

	V_{CC} = 0.8 V	V_{CC} = 1.2 V $\pm$ 0.1 V	V_{CC} = 1.5 V $\pm$ 0.1 V	V_{CC} = 1.8 V $\pm$ 0.15 V	V_{CC} = 2.5 V $\pm$ 0.2 V	V_{CC} = 3.3 V $\pm$ 0.3 V
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS
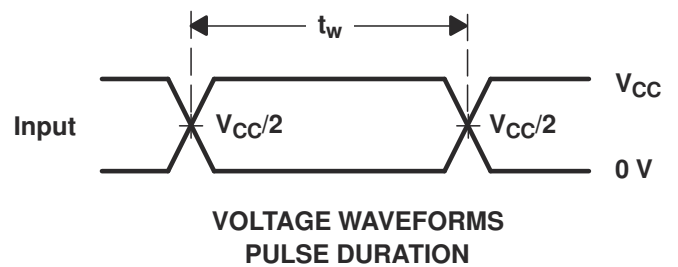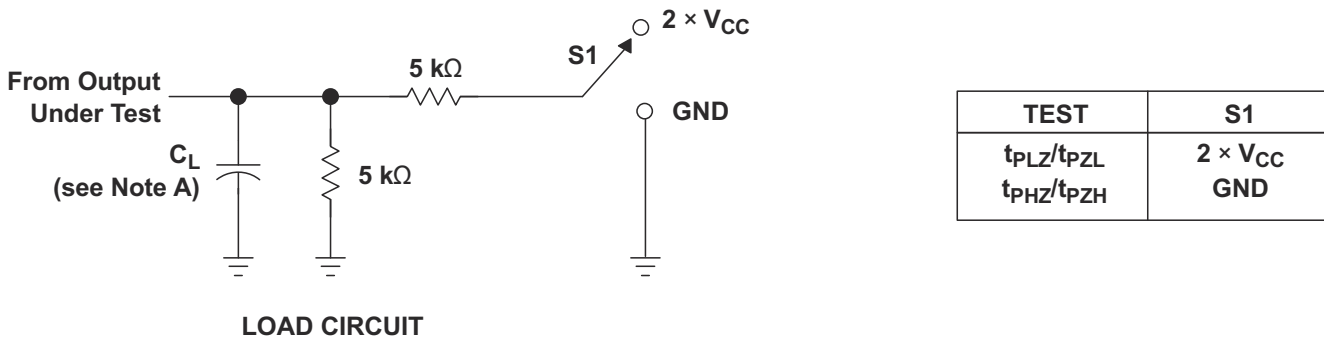
VOLTAGE WAVEFORMS
PULSE DURATION
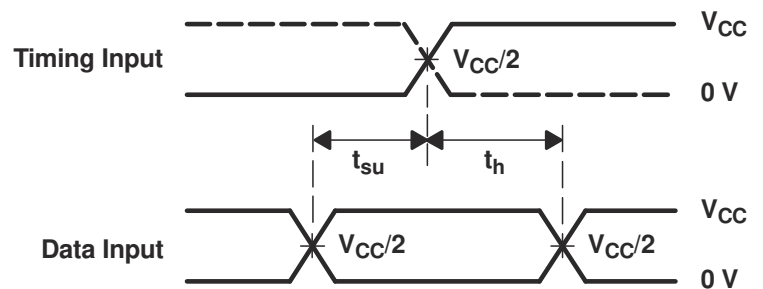
VOLTAGE WAVEFORMS
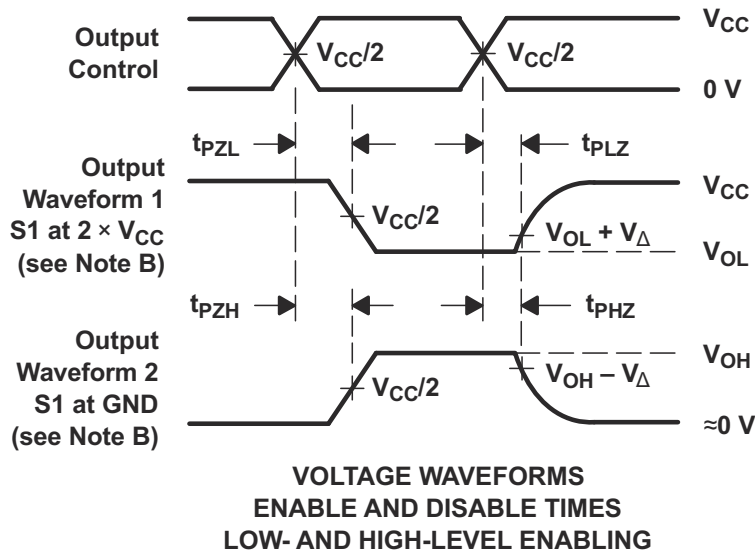**SETUP AND HOLD TIMES**

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 10 MHz, Z_O = 50 Ω, slew rate $\geq$ 1 V/ns.
C. The outputs are measured one at a time, with one transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.
E. All parameters and waveforms are not applicable to all devices.

Figure 6-1. Load Circuit and Voltage Waveforms

6.2 Enable and Disable Times

LOAD CIRCUIT

TEST	S1
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

	$V_{CC} = 0.8$ V	$V_{CC} = 1.2$ V ± 0.1 V	$V_{CC} = 1.5$ V ± 0.1 V	$V_{CC} = 1.8$ V ± 0.15 V	$V_{CC} = 2.5$ V ± 0.2 V	$V_{CC} = 3.3$ V ± 0.3 V
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
V_Δ	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
      B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
         Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
      C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O = 50$ Ω, slew rate ≥ 1 V/ns.
      D. The outputs are measured one at a time, with one transition per measurement.
      E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
      F. t_{PZL} and t_{PZH} are the same as t_{en}.
      G. All parameters and waveforms are not applicable to all devices.

Figure 6-2. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

This single 2-input positive-AND gate is designed for 0.8-V to 3.6-V V_{CC} operation and performs the Boolean function $Y = A \bullet B$ or $Y = \overline{\overline{A} + \overline{B}}$ in positive logic.

The AUP family of devices has quiescent power consumption less than 1 µA and comes in the ultra small DPW package. The DPW package technology is a major breakthrough in IC packaging. Its tiny 0.64 mm^2 square footprint saves significant board space over other package options while still retaining the traditional manufacturing friendly lead pitch of 0.5 mm.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered. The I_{off} feature also allows for live insertion.

7.2 Functional Block Diagram
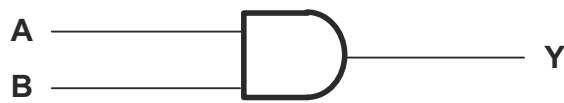
7.3 Feature Description

- Wide operating V_{CC} range of 0.8 V to 3.6 V
- 3.6-V I/O tolerant to support down translation
- Input hysteresis allows slow input transition and better switching noise immunity at the input
- I_{off} feature allows voltages on the inputs and outputs when V_{CC} is 0 V
- Low noise due to slower edge rates

7.4 Device Functional Modes

Table 7-1. Function Table

INPUTS		OUTPUT Y
A	B	
L	L	L
L	H	L
H	L	L
H	H	H

Product Folder Links: *SN74AUP1G08*

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static and dynamic power consumption across the entire V_{CC} range of 0.8 V to 3.6 V, resulting in an increased battery life. This product also maintains excellent signal integrity. It has a small amount of hysteresis built in allowing for slower or noisy input signals. The lowered drive produces slower edges and prevents overshoot and undershoot on the outputs.

The AUP family of single gate logic makes excellent translators for the new lower voltage Micro- processors that typically are powered from 0.8 V to 1.2 V. They can drop the voltage of peripheral drivers and accessories that are still powered by 3.3 V to the new μC power levels.

8.2 Typical Application
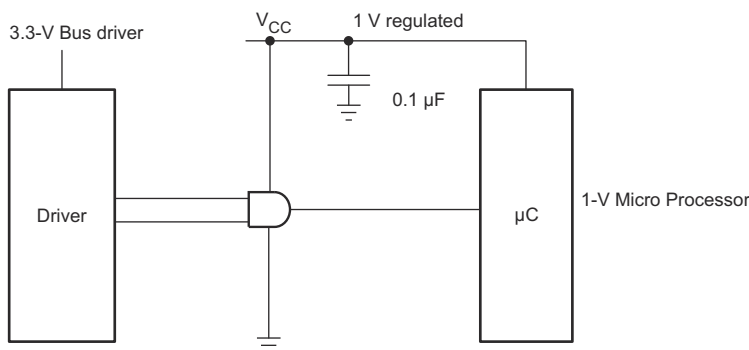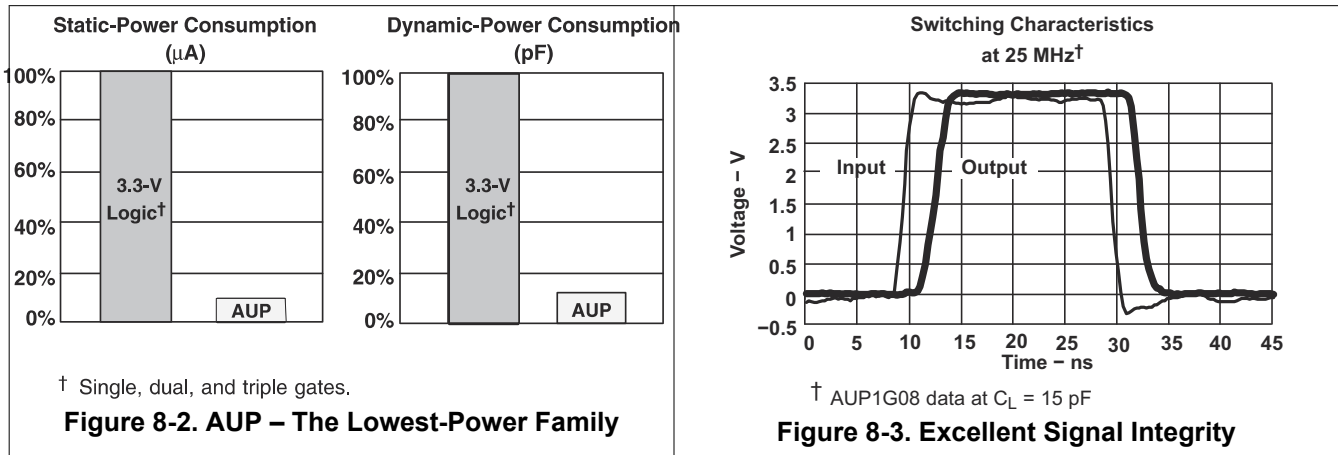

Figure 8-1. Typical Application Schematic

8.2.1 Design Requirements

SN74AUP1G08 device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits.

8.2.2 Detailed Design Procedure

1. Recommended Input conditions
   - Rise time and fall time specifications. See (Δt/ΔV) in *Recommended Operating Conditions* table.
   - Specified high and low levels. See (V_{IH} and V_{IL}) in *Recommended Operating Conditions* table.
   - Inputs are overvoltage tolerant allowing them to go as high as 3.6 V at any valid V_{CC}
2. Recommended output conditions
   - Load currents should not exceed 20 mA on the output and 50 mA total for the part
   - Outputs should not be pulled above V_{CC}

8.2.3 Application Curves

† Single, dual, and triple gates.

Figure 8-2. AUP – The Lowest-Power Family

† AUP1G08 data at C_L = 15 pF

Figure 8-3. Excellent Signal Integrity

9 Power Supply Recommendations

The power supply can be any voltage between the Min and Max supply voltage rating located in the *Recommended Operating Conditions* table.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 µF is recommended and if there are multiple V_{CC} terminals then 0.01 µF or 0.022 µF is recommended for each power terminal. It is ok to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.
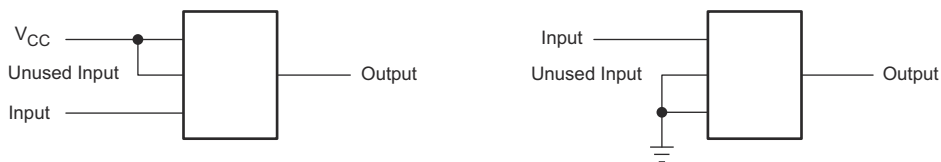
10 Layout

10.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified in Figure 10-1 are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient. It is generally OK to float outputs unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

10.2 Layout Example

Figure 10-1. Layout Diagram

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

12 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device (1)	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AUP1G08DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(H08F, H08R)	Samples
SN74AUP1G08DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(H08F, H08R)	Samples
SN74AUP1G08DCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(HE5, HEF, HEK, HE R) (HEH, HEP, HES)	Samples
SN74AUP1G08DCKRE4	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HE5, HEF, HEK, HE R) (HEH, HEP, HES)	Samples
SN74AUP1G08DCKT	ACTIVE	SC70	DCK	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HE5, HER)	Samples
SN74AUP1G08DPWR	ACTIVE	X2SON	DPW	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(E, E4)	Samples
SN74AUP1G08DRLR	ACTIVE	SOT-5X3	DRL	5	4000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(HE7, HER)	Samples
SN74AUP1G08DRY2	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HE	Samples
SN74AUP1G08DRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	HE	Samples
SN74AUP1G08DSF2	ACTIVE	SON	DSF	6	5000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(HE, HER) HEH	Samples
SN74AUP1G08DSFR	ACTIVE	SON	DSF	6	5000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(HE, HER) HEH	Samples
SN74AUP1G08YFPR	ACTIVE	DSBGA	YFP	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM		HEN	Samples
SN74AUP1G08YZPR	ACTIVE	DSBGA	YZP	5	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	HEN	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74AUP1G08 :

- Automotive : SN74AUP1G08-Q1

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

![Texas Instruments logo]

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1G08DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74AUP1G08DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74AUP1G08DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74AUP1G08DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74AUP1G08DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AUP1G08DCKRE4	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AUP1G08DCKT	SC70	DCK	5	250	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74AUP1G08DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AUP1G08DPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q3
SN74AUP1G08DRLR	SOT-5X3	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74AUP1G08DRY2	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q3
SN74AUP1G08DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74AUP1G08DRYR	SON	DRY	6	5000	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
SN74AUP1G08DSF2	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q3
SN74AUP1G08DSFR	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
SN74AUP1G08YFPR	DSBGA	YFP	6	3000	178.0	9.2	0.89	1.29	0.62	4.0	8.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1G08YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP1G08DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
SN74AUP1G08DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
SN74AUP1G08DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
SN74AUP1G08DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
SN74AUP1G08DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AUP1G08DCKRE4	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AUP1G08DCKT	SC70	DCK	5	250	202.0	201.0	28.0
SN74AUP1G08DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74AUP1G08DPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
SN74AUP1G08DRLR	SOT-5X3	DRL	5	4000	202.0	201.0	28.0
SN74AUP1G08DRY2	SON	DRY	6	5000	184.0	184.0	19.0
SN74AUP1G08DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74AUP1G08DRYR	SON	DRY	6	5000	202.0	201.0	28.0
SN74AUP1G08DSF2	SON	DSF	6	5000	210.0	185.0	35.0
SN74AUP1G08DSFR	SON	DSF	6	5000	210.0	185.0	35.0
SN74AUP1G08YFPR	DSBGA	YFP	6	3000	220.0	220.0	35.0
SN74AUP1G08YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0
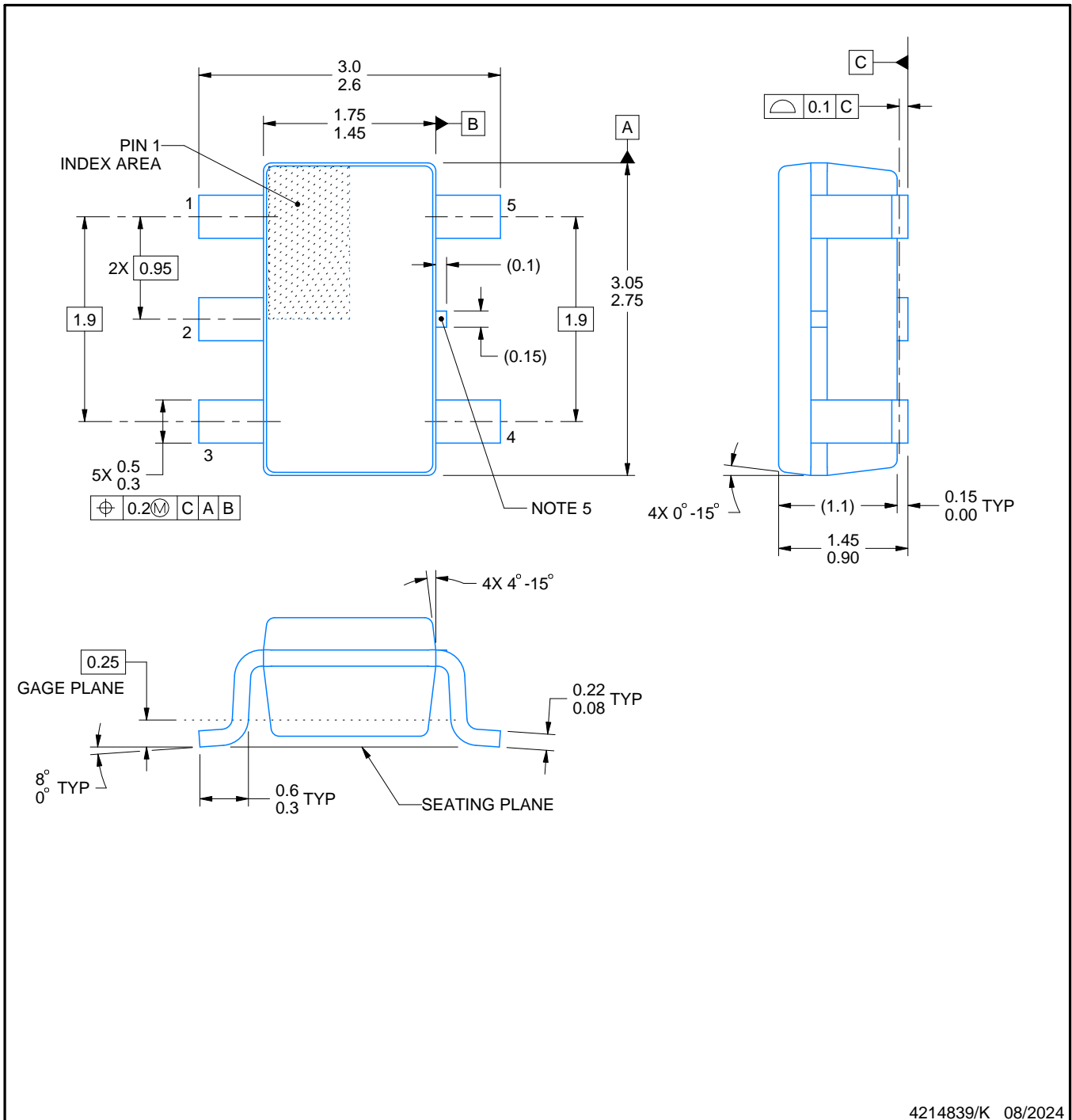
4214839/K   08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

PKG
℄

5X (1.1)

1

5X (0.6)

5

2

SYMM
℄

(1.9)

2X (0.95)

3

4

(R0.05) TYP

(2.6)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.07 MAX
ARROUND

NON SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.07 MIN
ARROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214839/K   08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

5X (1.1)

5X (0.6)

2X(0.95)

(R0.05) TYP

(2.6)

(1.9)

PKG

SYMM

4214839/K   08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

TEXAS
INSTRUMENTS

B | 1.05 / 0.95 | A

PIN 1 INDEX AREA

1.5 / 1.4

0.6 MAX

C

0.05 / 0.00

SEATING PLANE

◯ | 0.08 | C

3X | 0.6

SYMM ℄

(0.05) TYP

3

4X / 0.5

2X / 1

SYMM ℄

4

1

6

0.4 / 0.3

6X | 0.25 / 0.15

⊕ | 0.1 Ⓜ | C | A | B
| 0.05 Ⓜ | C

PIN 1 ID (OPTIONAL)

5X | 0.35 / 0.25

(0.127) TYP
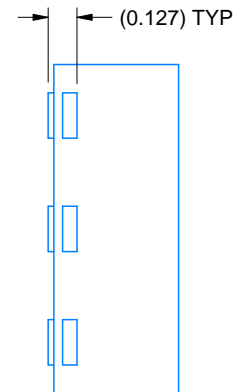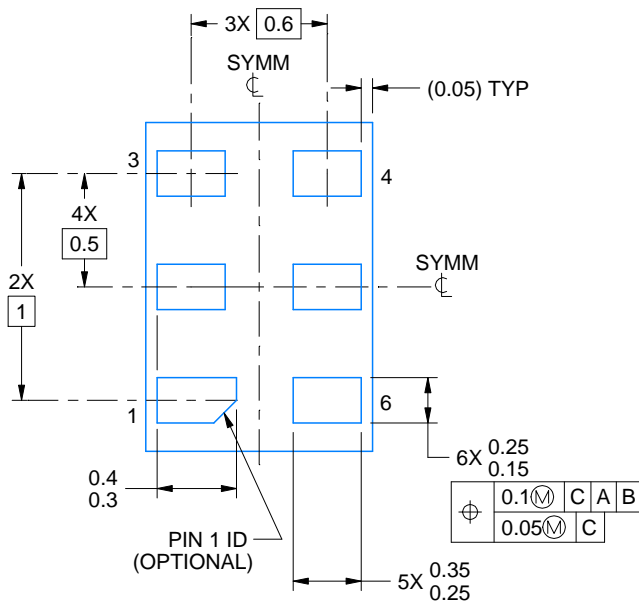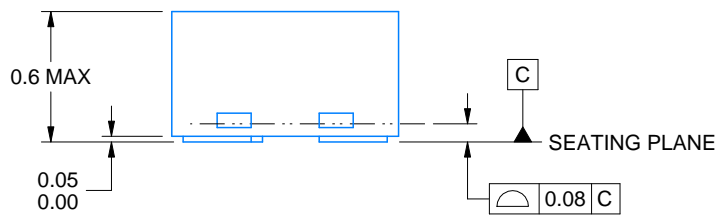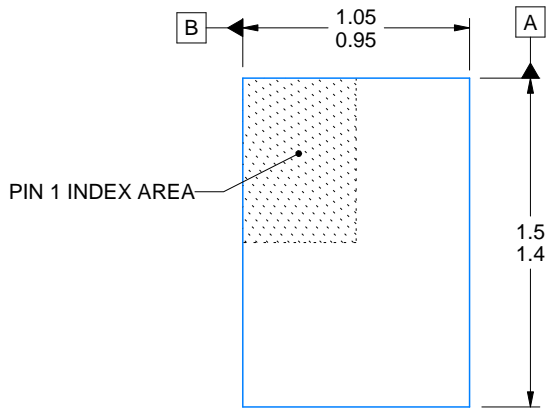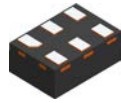
4222894/A 01/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

SYMM

(0.35)

5X (0.3)

1

6

6X (0.2)

SYMM

4X (0.5)

3

4

(R0.05) TYP

(0.6)

LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X

0.05 MAX
ALL AROUND

0.05 MIN
ALL AROUND

EXPOSED
METAL

EXPOSED
METAL

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK DETAILS

4222894/A   01/2018

NOTES: (continued)

3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

SYMM

(0.35)

5X (0.3)

1

6

6X (0.2)

SYMM

4X (0.5)

3

4

(R0.05) TYP

(0.6)
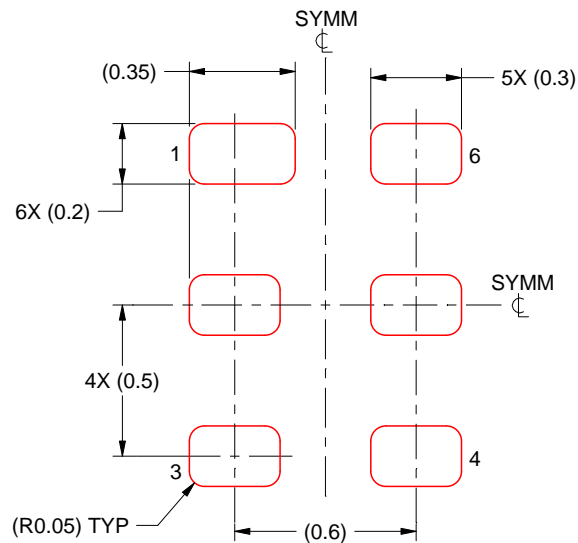
SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A   01/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
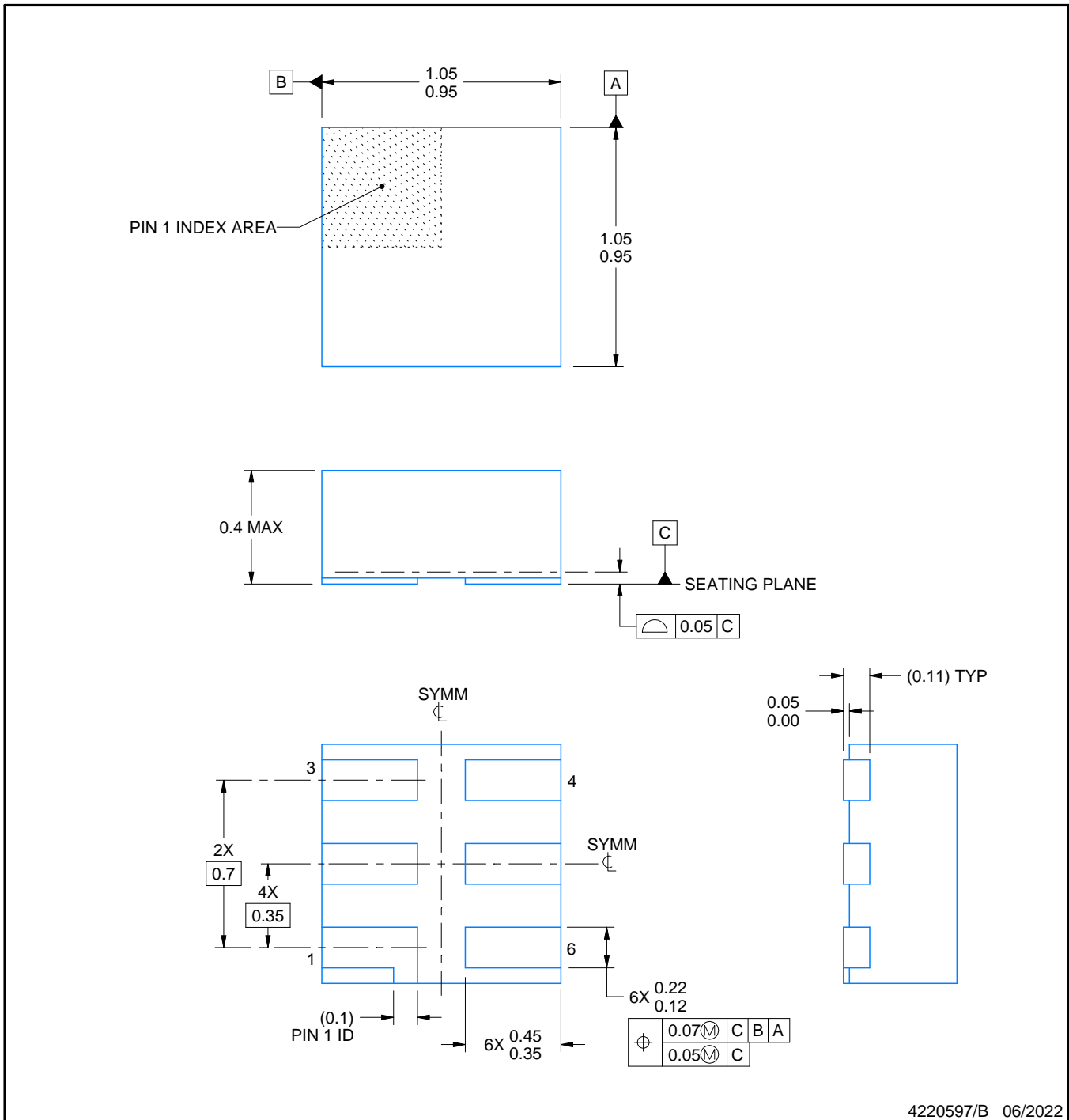design recommendations.

B

1.05
0.95

A

PIN 1 INDEX AREA

1.05
0.95

0.4 MAX

C

SEATING PLANE

⌒ 0.05 C

(0.11) TYP

0.05
0.00

SYMM
℄

3

4

2X
0.7

SYMM
℄

4X
0.35

1

6

(0.1)
PIN 1 ID

6X 0.45
0.35

6X 0.22
0.12

⊕ 0.07 Ⓜ C B A
0.05 Ⓜ C

4220597/B   06/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.

6X (0.6)

1

6X (0.17)

(R0.05) TYP

6

SYMM
℄

4X (0.35)

3

4

SYMM
℄

(0.8)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X

0.07 MAX
ALL AROUND

EXPOSED METAL

SOLDER MASK
OPENING

METAL

NON SOLDER MASK
DEFINED

0.07 MIN
ALL AROUND

EXPOSED METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220597/B   06/2022

NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

6X (0.6)

1

6X (0.15)

(R0.05) TYP

6

SYMM
⊄

4X (0.35)

3

4

SYMM
⊄

(0.8)

SOLDER PASTE EXAMPLE
BASED ON 0.09 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220597/B   06/2022

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

Images above are just a representation of the package family, actual package may vary.
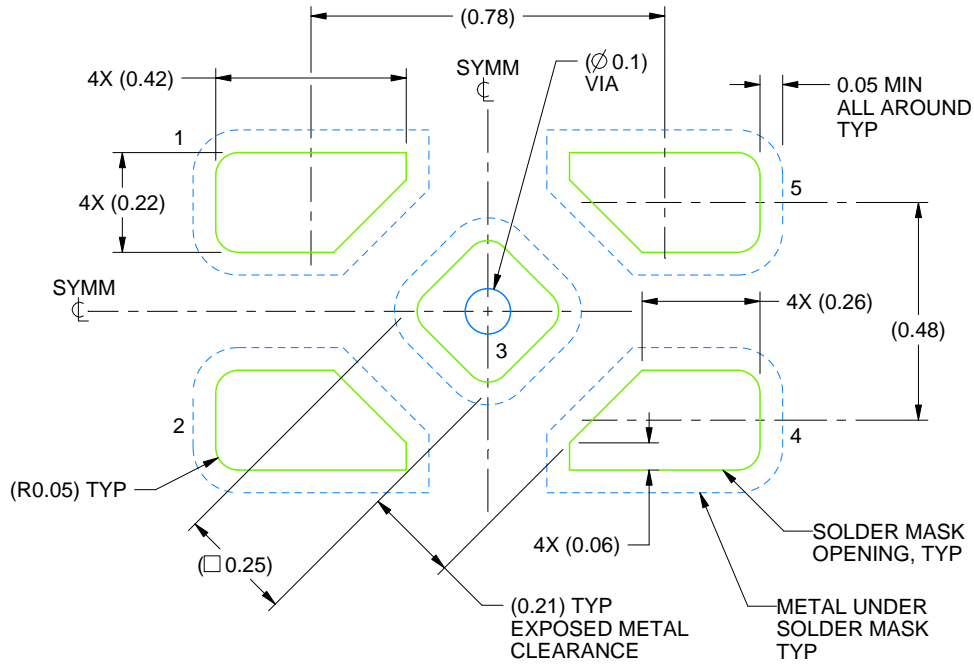Refer to the product data sheet for package details.

4211218-3/D

B | 0.85 / 0.75 | A

PIN 1 INDEX AREA

0.85 / 0.75

0.4 MAX

C

SEATING PLANE

NOTE 3

4X (0.05)

(0.324)

□ 0.25 ± 0.1

2

4

2X 0.48

3

2X (0.26)

1

5

0.239 / 0.139

4X 0.27 / 0.17

3X 0.288 / 0.188

⊕ | 0.1 Ⓜ | C | A | B
| 0.05 Ⓜ | C

(0.1)

0.05 / 0.00

NOTE 3
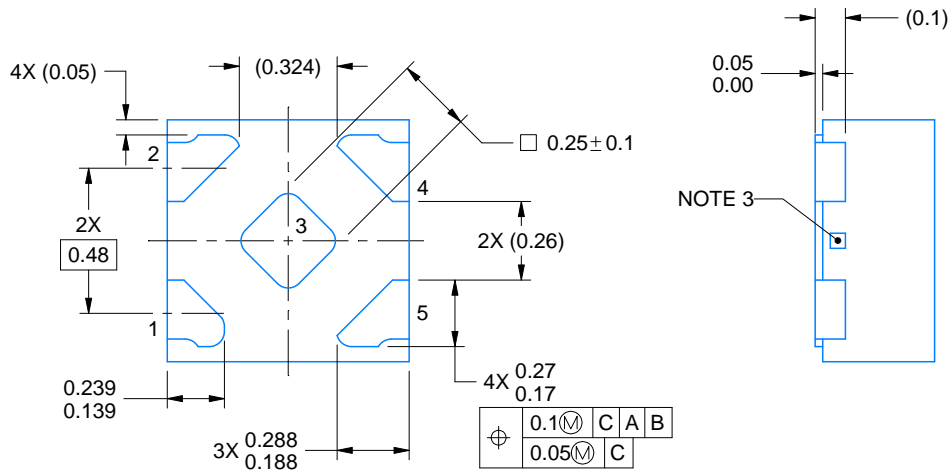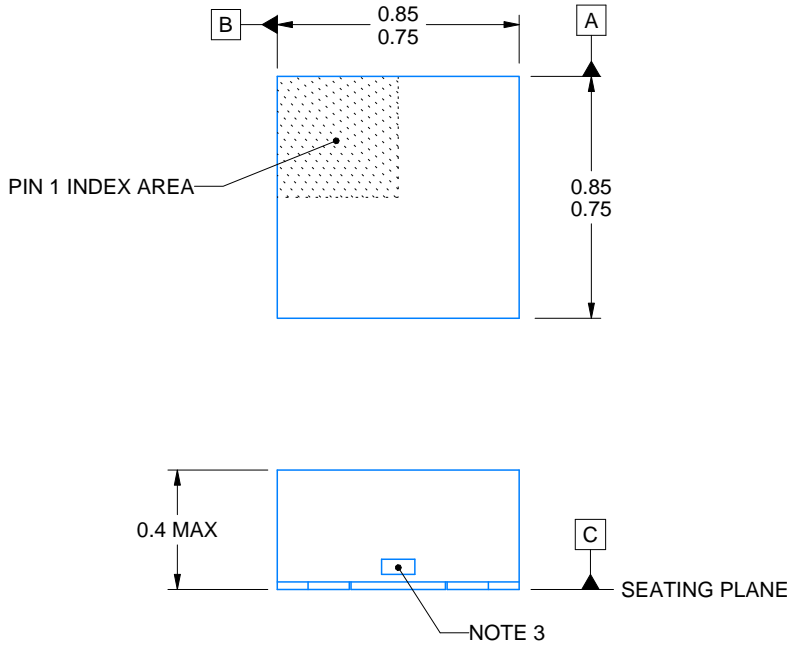
4223102/D   03/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.

(0.78)

4X (0.42)

SYMM

($\emptyset$ 0.1)
VIA

0.05 MIN
ALL AROUND
TYP

1

4X (0.22)

5

SYMM

3

4X (0.26)

(0.48)

2

4

4X (0.06)

(R0.05) TYP

($\square$ 0.25)

SOLDER MASK
OPENING, TYP

(0.21) TYP
EXPOSED METAL
CLEARANCE

METAL UNDER
SOLDER MASK
TYP
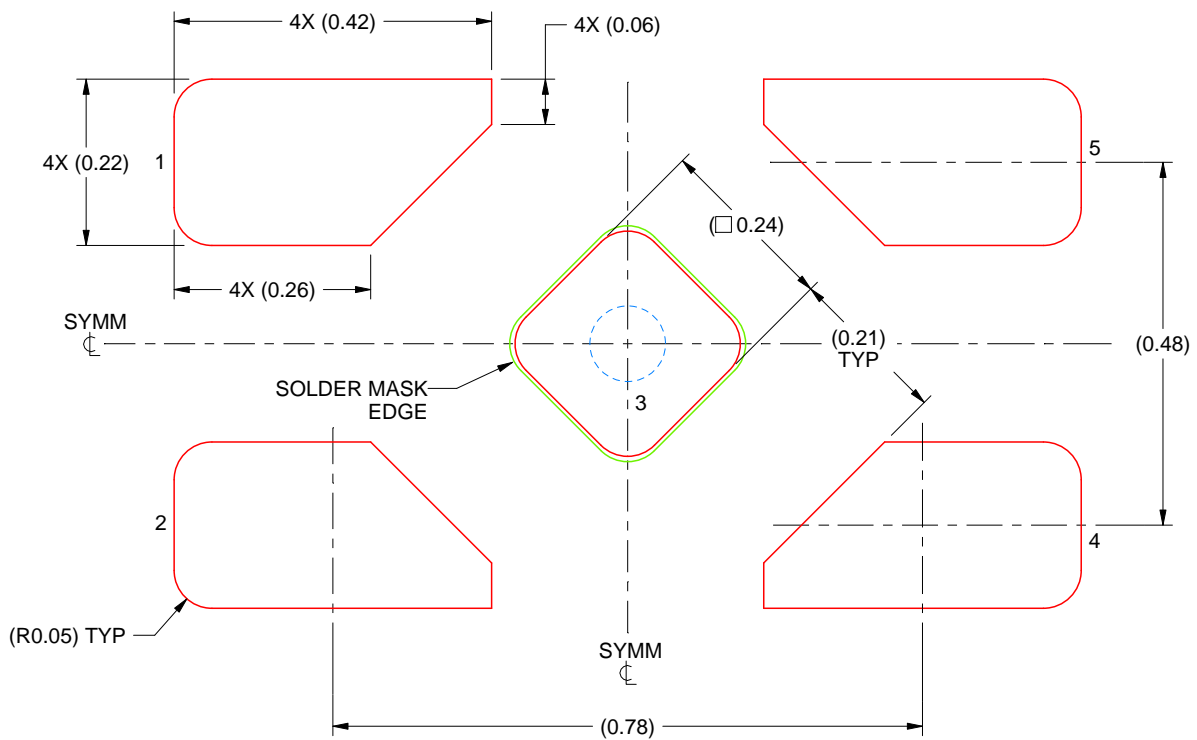
LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

4223102/D   03/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).

4X (0.42)

4X (0.06)

4X (0.22)

1

4X (0.26)

SYMM

SOLDER MASK
EDGE

(□ 0.24)

5

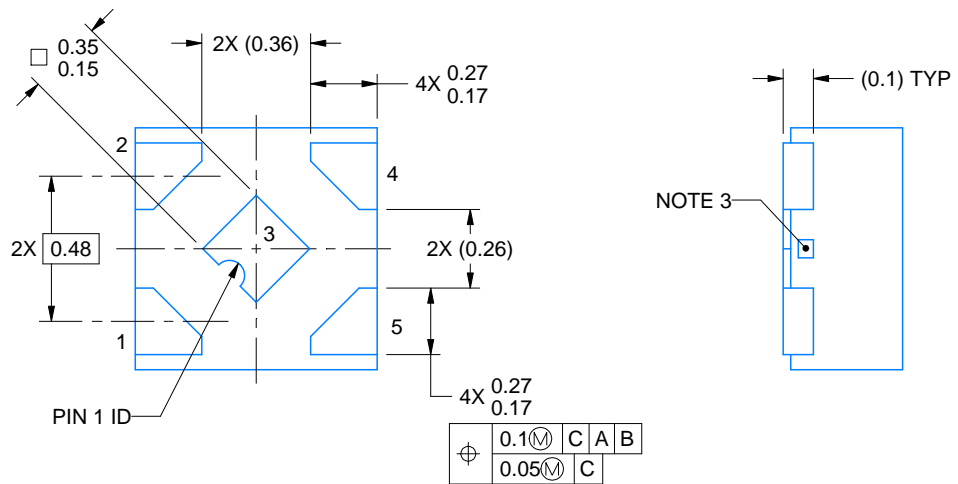(0.21)
TYP

(0.48)

3

2

4

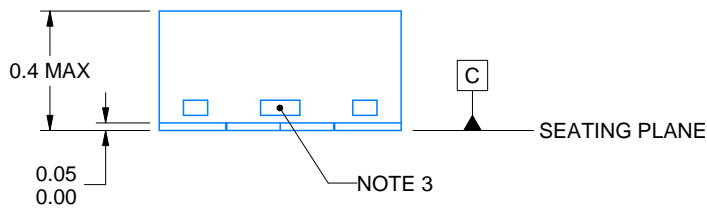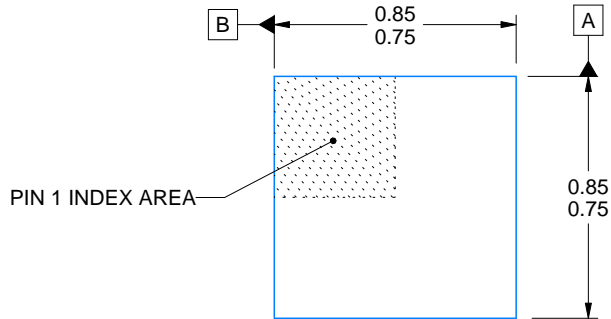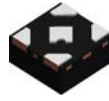(R0.05) TYP

SYMM

(0.78)

SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 3
92% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:100X

4223102/D   03/2022

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
design recommendations.

B | 0.85 / 0.75 | A

PIN 1 INDEX AREA

0.85 / 0.75

0.4 MAX

C

SEATING PLANE

0.05 / 0.00

NOTE 3

□ 0.35 / 0.15

2X (0.36)

4X 0.27 / 0.17

2

4

3

2X 0.48

2X (0.26)

1

5

PIN 1 ID

4X 0.27 / 0.17

⌖ | 0.1 Ⓜ | C | A | B
0.05 Ⓜ | C
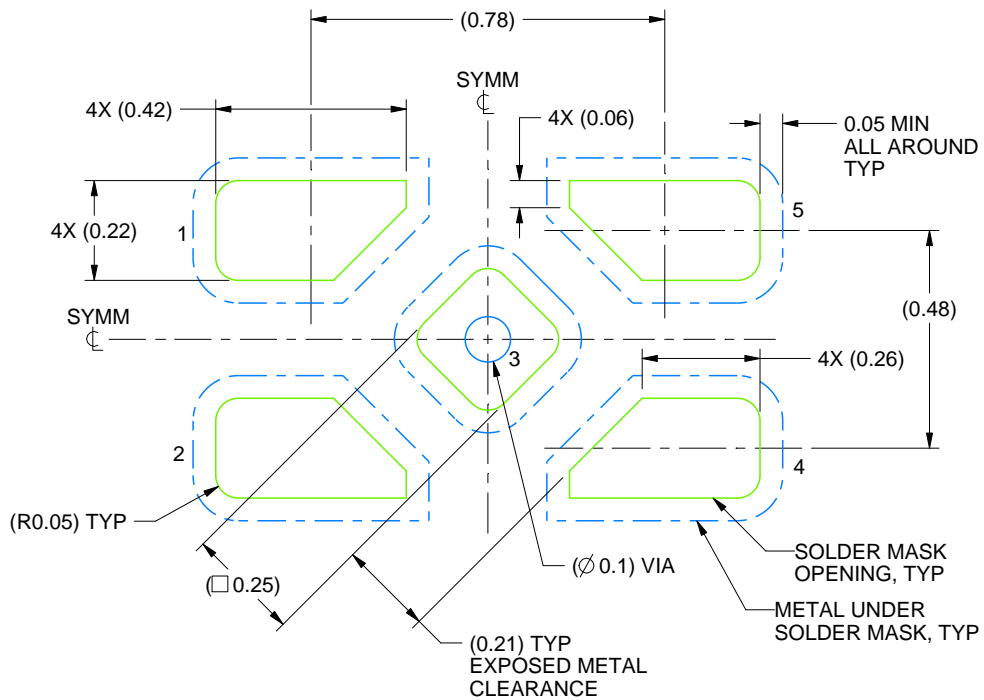
(0.1) TYP

NOTE 3

4228233/D   09/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.

(0.78)

SYMM

4X (0.42)

4X (0.06)

0.05 MIN
ALL AROUND
TYP

4X (0.22)

1

5

SYMM

3

(0.48)

4X (0.26)

2

4

(R0.05) TYP

(Ø 0.1) VIA

SOLDER MASK
OPENING, TYP

(□ 0.25)

METAL UNDER
SOLDER MASK, TYP

(0.21) TYP
EXPOSED METAL
CLEARANCE

LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X
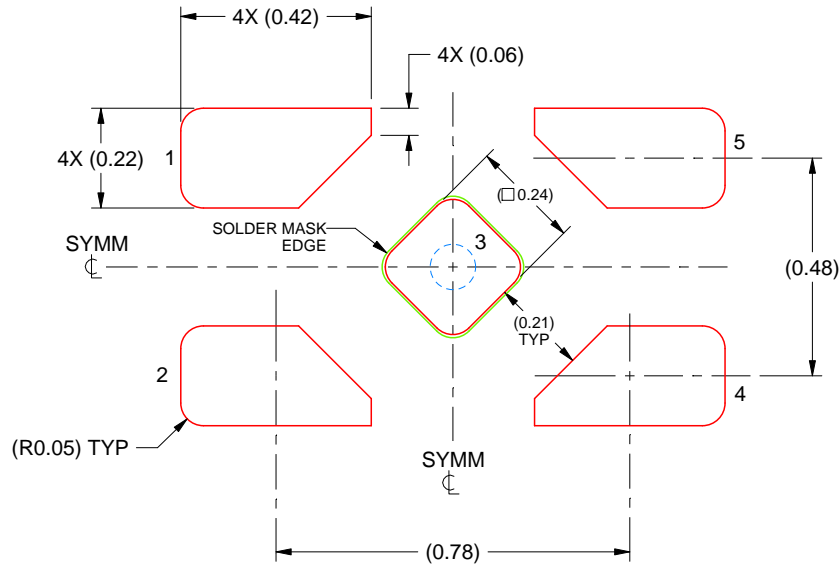
4228233/D   09/2023

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).

TEXAS INSTRUMENTS
www.ti.com

4X (0.42)

4X (0.06)

4X (0.22) 1

5

SYMM

SOLDER MASK EDGE

(□0.24)

3

(0.48)

(0.21) TYP

2

4

(R0.05) TYP

SYMM

(0.78)

SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 5
92% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:60X

4228233/D   09/2023

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
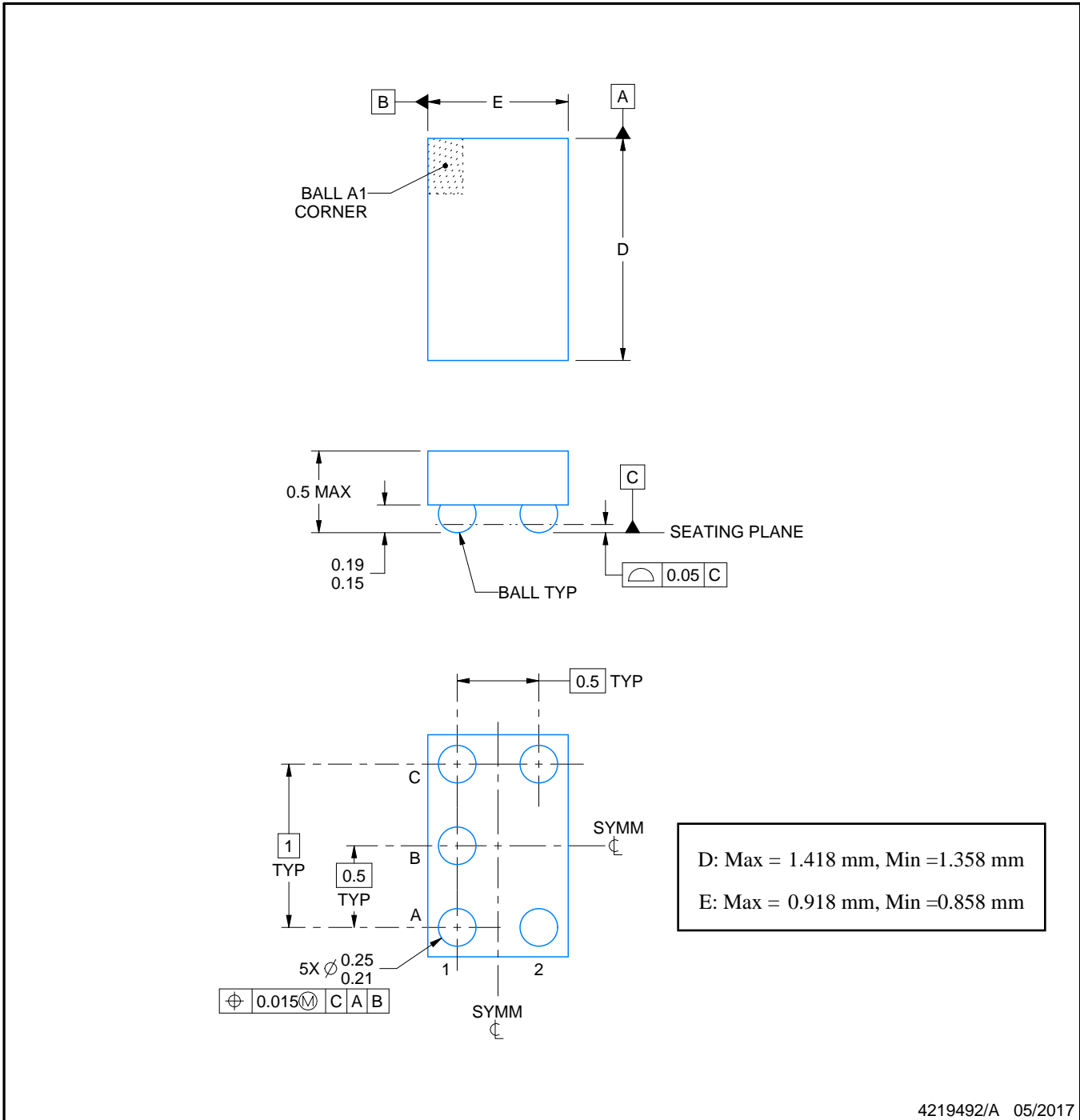
BALL A1
CORNER

B E A

D

0.5 MAX

0.19
0.15

SEATING PLANE

C

⌒ 0.05 C

BALL TYP

0.5 TYP

C

1
TYP

B

0.5
TYP

A

SYMM
℄

D: Max = 1.418 mm, Min =1.358 mm

E: Max = 0.918 mm, Min =0.858 mm

5X ∅ 0.25
0.21

1 2

⊕ 0.015Ⓜ C A B

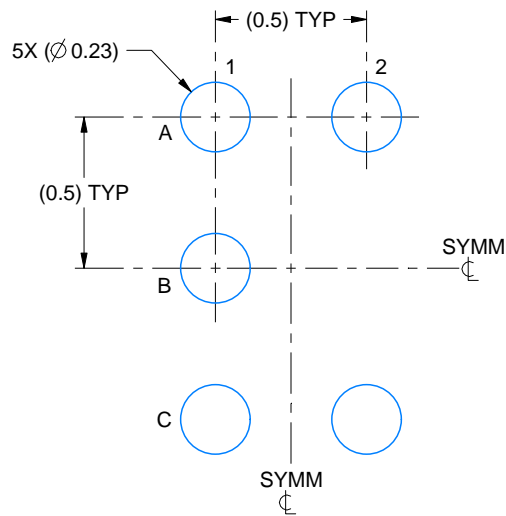SYMM
℄

4219492/A 05/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing
   per ASME Y14.5M.
2. This drawing is subject to change without notice.

LAND PATTERN EXAMPLE
SCALE:40X

5X ($\varnothing$ 0.23)

(0.5) TYP

(0.5) TYP

SYMM

SYMM

SOLDER MASK OPENING

0.05 MAX

($\varnothing$ 0.23) METAL

NON-SOLDER MASK DEFINED (PREFERRED)

0.05 MIN

($\varnothing$ 0.23) SOLDER MASK OPENING

METAL UNDER SOLDER MASK

SOLDER MASK DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4219492/A   05/2017

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

YZP0005

(0.5) TYP

5X (□ 0.25)

(R0.05) TYP

1   2

A

(0.5) TYP

B   SYMM ℄
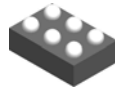
SYMM ℄

C

METAL TYP

SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219492/A   05/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.
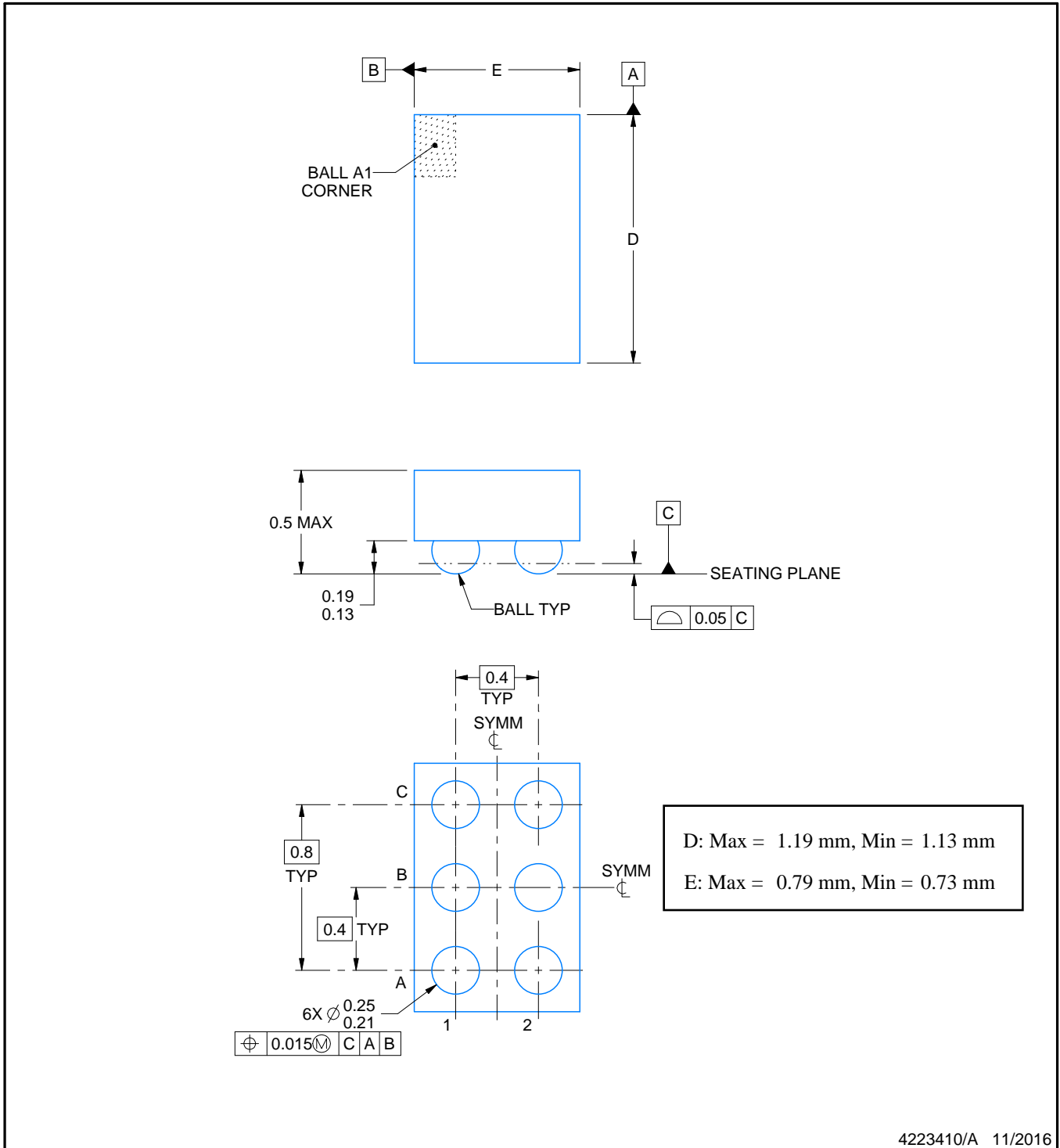
B ◄────── E ──────► A

BALL A1
CORNER

D

0.5 MAX

0.19
0.13

BALL TYP

SEATING PLANE

C

◯ 0.05 C

0.4
TYP

SYMM
℄

C

0.8
TYP

B

SYMM
℄

0.4 TYP

A

D: Max = 1.19 mm, Min = 1.13 mm

E: Max = 0.79 mm, Min = 0.73 mm

6X ∅ 0.25
     0.21

1   2

⊕ 0.015Ⓜ C A B
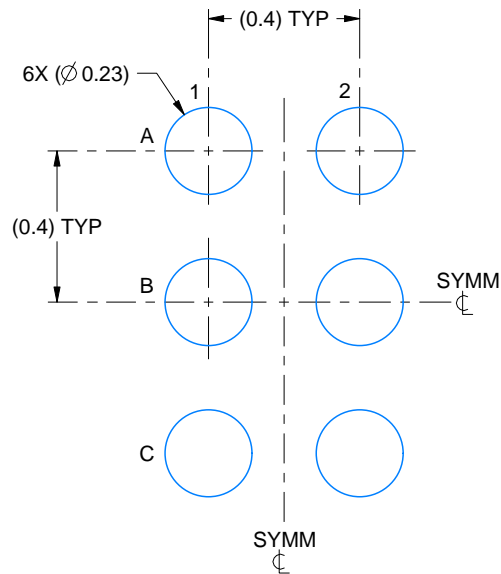
4223410/A   11/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

(0.4) TYP

6X (⌀ 0.23)
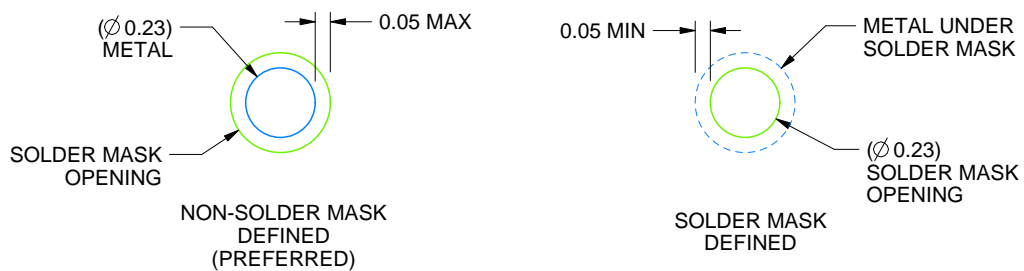
1   2

A

(0.4) TYP

B   SYMM
                     ℄

C

SYMM
℄

LAND PATTERN EXAMPLE
SCALE:50X

(⌀ 0.23)
METAL

0.05 MAX

0.05 MIN

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

(⌀ 0.23)
SOLDER MASK
OPENING

NON-SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS
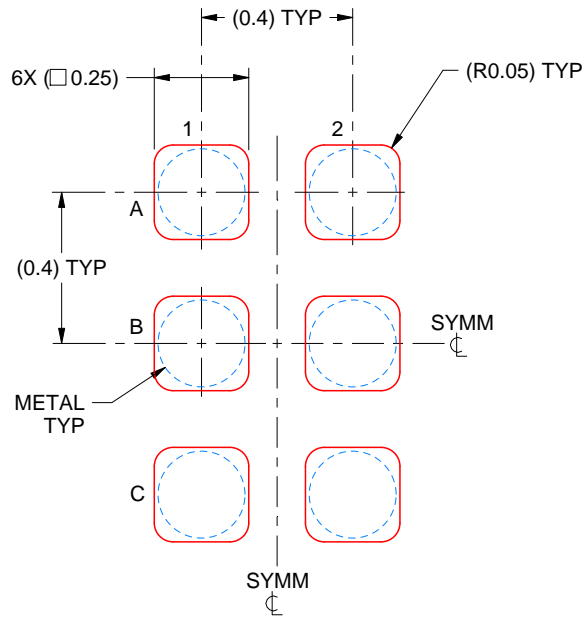NOT TO SCALE

4223410/A   11/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).
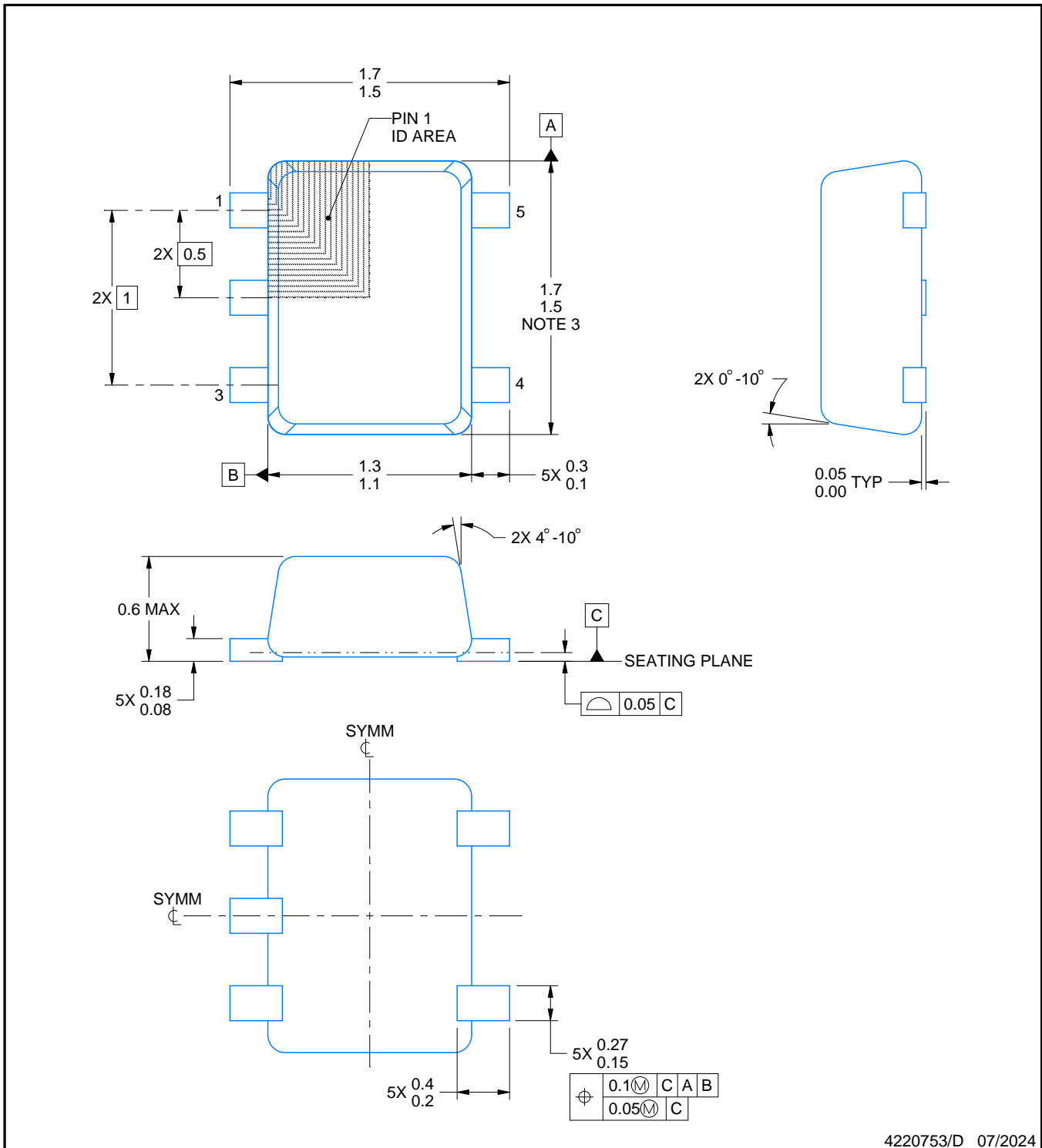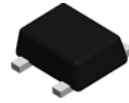
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

4223410/A   11/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

1.7
1.5

PIN 1
ID AREA

A

1

2X 0.5

2X 1

3

5

1.7
1.5
NOTE 3

4

B

1.3
1.1

5X 0.3
0.1

2X 0° -10°

0.05 TYP
0.00

2X 4° -10°

0.6 MAX

C

SEATING PLANE

5X 0.18
0.08

0.05 C

SYMM

SYMM

5X 0.27
0.15

5X 0.4
0.2

0.1 M C A B

0.05 M C

4220753/D   07/2024

NOTES:

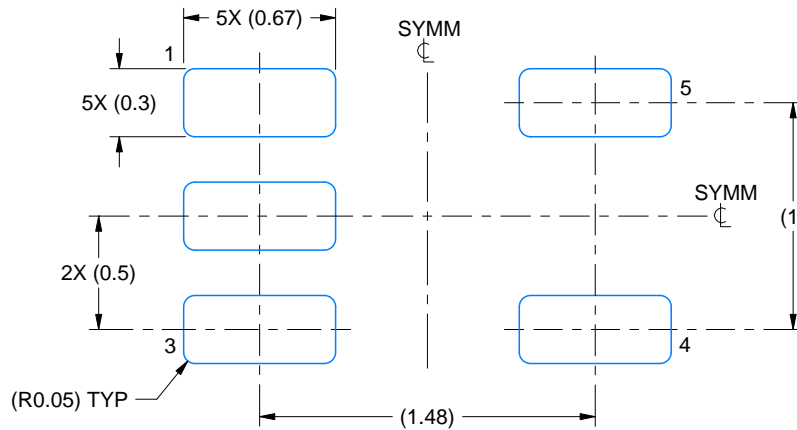1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD-1

5X (0.67)

SYMM

1

5X (0.3)

5

SYMM

(1)

2X (0.5)

3

4

(R0.05) TYP

(1.48)

LAND PATTERN EXAMPLE
SCALE:30X

0.05 MAX
AROUND

0.05 MIN
AROUND

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED
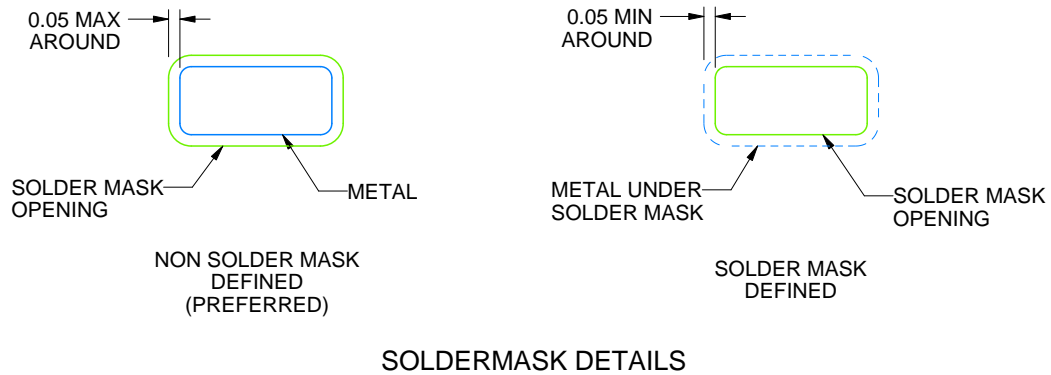
SOLDERMASK DETAILS

4220753/D   07/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

DRL0005A

5X (0.67)

SYMM

1

5X (0.3)

5

SYMM

(1)

2X (0.5)

3

4

(R0.05) TYP

(1.48)
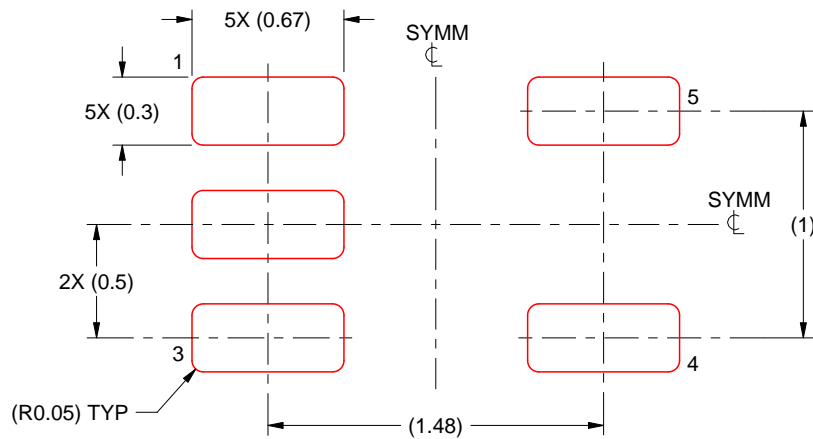
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4220753/D   07/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

YEP (R−XBGA−N5)   DIE−SIZE BALL GRID ARRAY

Pin A1 Index Area

5X ⌀ 0,25 / 0,20

⌖ ⌀ 0,05 Ⓜ C A B
⌀ 0,05 Ⓜ C

0,50 Max

0,20 / 0,15

Seating Plane
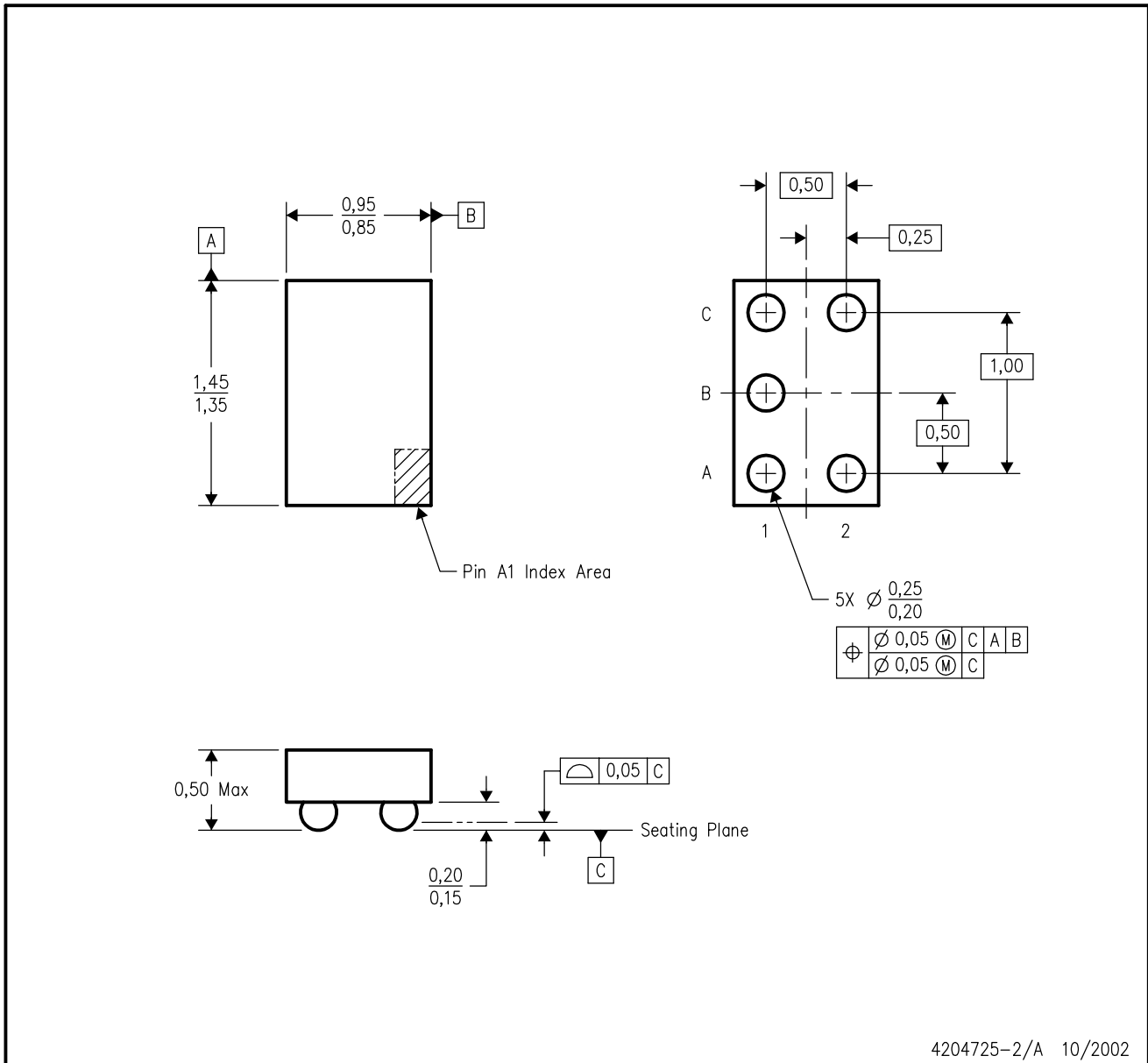
4204725−2/A 10/2002

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. NanoStar™ package configuration.
        D. This package is tin−lead (SnPb). Refer to the 5 YZP package (drawing 4204741) for lead−free.

NanoStar is a trademark of Texas Instruments.

TEXAS INSTRUMENTS
www.ti.com

PIN 1
INDEX AREA

2.4
1.8

1.4
1.1

B

A

1.1 MAX

0.1 C

1

5

2X 0.65

NOTE 4

(0.15)

1.3

2

1.3

2.15
1.85

(0.1)

5X 0.33
0.15

3

4

0.1 C A B
NOTE 5

4X 0°-12°

(0.9)

0.1
0.0 TYP

4X 4°-14°

0.15

GAGE PLANE

0.22
0.08 TYP

8°
0° TYP

0.46
0.26 TYP

SEATING PLANE

4214834/F 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

DCK0005A

5X (0.95)

PKG ₵

1

5X (0.4)

2

2X (0.65)

3

(R0.05) TYP

5

SYMM ₵

(1.3)

4

(2.2)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.07 MAX
ARROUND

NON SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.07 MIN
ARROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214834/F   08/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/F   08/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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