

# Quad 2-Input NAND Gate with Schmitt-Trigger Inputs

## High-Performance Silicon-Gate CMOS

### MC74HC132A, MC74HCT132A

The MC74HC132A, MC74HCT132A are identical in pinout to the LS132. The device inputs are compatible with standard CMOS outputs; with pull-up resistors, they are compatible with LSTTL outputs. The MC74HCT132A device inputs are compatible with Standard CMOS or TTL outputs.

The HC132A can be used to enhance noise immunity or to square up slowly changing waveforms.

#### Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V (HC), 4.5 to 5.5 V (HCT)
- Low Input Current: 1.0  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements as Defined by JEDEC Standard No. 7A
- Chip Complexity: 72 FETs or 18 Equivalent Gates
- -Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

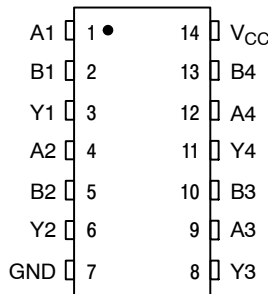
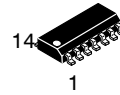


Figure 1. Pinout Diagram

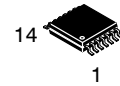
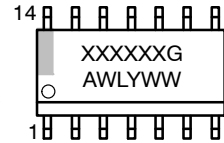
#### FUNCTION TABLE

Inputs		Output Y
A	B	
L	L	H
L	H	H
H	L	H
H	H	L

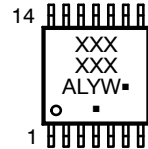
#### MARKING DIAGRAMS



SOIC-14  
D SUFFIX  
CASE 751A



TSSOP-14  
DT SUFFIX  
CASE 948G



XXX = Specific Device Code  
A = Assembly Location  
WL, L = Wafer Lot  
Y = Year  
WW, W = Work Week  
G or ■ = Pb-Free Package  
(Note: Microdot may be in either location)

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

# MC74HC132A, MC74HCT132A

## MAXIMUM RATINGS

Symbol	Parameter	Value	Unit	
V <sub>CC</sub>	DC Supply Voltage	-0.5 to +6.5	V	
V <sub>IN</sub>	DC Input Voltage	-0.5 to V <sub>CC</sub> + 0.5	V	
V <sub>OUT</sub>	DC Output Voltage	-0.5 to V <sub>CC</sub> + 0.5	V	
I <sub>IN</sub>	DC Input Current, per Pin	±20	mA	
I <sub>OUT</sub>	DC Output Current, per Pin	±25	mA	
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA	
I <sub>IK</sub>	Input Clamp Current (V <sub>IN</sub> < 0 or V <sub>IN</sub> > V <sub>CC</sub> )	±20	mA	
I <sub>OK</sub>	Output Clamp Current (V <sub>OUT</sub> < 0 or V <sub>OUT</sub> > V <sub>CC</sub> )	±20	mA	
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C	
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C	
T <sub>J</sub>	Junction Temperature Under Bias	±150	°C	
θ <sub>JA</sub>	Thermal Resistance (Note 1)	SOIC-14 TSSOP-14	116 150	°C/W
P <sub>D</sub>	Power Dissipation in Still Air at 25°C	SOIC-14 TSSOP-14	1077 833	mW
MSL	Moisture Sensitivity		Level 1	-
F <sub>R</sub>	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	-
V <sub>ESD</sub>	ESD Withstand Voltage (Note 2)	Human Body Model Charged Device Model	>2000 N/A	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 76mm-by-114mm, 2-ounce copper trace no air flow per JESD51-7.
2. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
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### MC74HC

V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V <sub>IN</sub> , V <sub>OUT</sub>	DC Input Voltage, Output Voltage (Referenced to GND) (Note 3)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Free-Air Temperature	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise or Fall Time	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 1000 500 400	ns

### MC74HCT

V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V <sub>IN</sub> , V <sub>OUT</sub>	DC Input Voltage, DC Output Voltage (Referenced to GND) (Note 3)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Free-Air Temperature	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise or Fall Time	0	500	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

# MC74HC132A, MC74HCT132A

## DC ELECTRICAL CHARACTERISTICS (MC74HC132A)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				-55°C to 25°C	≤ 85°C	≤ 125°C	
V <sub>T+</sub> max	Maximum Positive-Going Input Threshold Voltage (Figure 5)	V <sub>OUT</sub> = 0.1 V  I <sub>OUT</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>T+</sub> min	Minimum Positive-Going Input Threshold Voltage (Figure 5)	V <sub>OUT</sub> = 0.1 V  I <sub>OUT</sub>   ≤ 20 μA	2.0	1.0	0.95	0.95	V
			4.5	2.3	2.25	2.25	
			6.0	3.0	2.95	2.95	
V <sub>T-</sub> max	Maximum Negative-Going Input Threshold Voltage (Figure 5)	V <sub>OUT</sub> = V <sub>CC</sub> - 0.1 V  I <sub>OUT</sub>   ≤ 20 μA	2.0	0.9	0.95	0.95	V
			4.5	2.0	2.05	2.05	
			6.0	2.6	2.65	2.65	
V <sub>T-</sub> min	Minimum Negative-Going Input Threshold Voltage (Figure 5)	V <sub>OUT</sub> = V <sub>CC</sub> - 0.1 V  I <sub>OUT</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>H</sub> max (Note 4)	Maximum Hysteresis Voltage (Figure 5)	V <sub>OUT</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>OUT</sub>   ≤ 20 μA	2.0	1.2	1.2	1.2	V
			4.5	2.25	2.25	2.25	
			6.0	3.0	3.0	3.0	
V <sub>H</sub> min (Note 4)	Minimum Hysteresis Voltage (Figure 5)	V <sub>OUT</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>OUT</sub>   ≤ 20 μA	2.0	0.2	0.2	0.2	V
			4.5	0.4	0.4	0.4	
			6.0	0.5	0.5	0.5	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>IN</sub> ≤ V <sub>T-</sub> min or V <sub>T+</sub> max  I <sub>OUT</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
		V <sub>IN</sub> ≤ -V <sub>T-</sub> min or V <sub>T+</sub> max  I <sub>OUT</sub>   ≤ 4.0 mA  I <sub>OUT</sub>   ≤ 5.2 mA	4.5	3.98	3.84	3.7	
			6.0	5.48	5.34	5.2	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>IN</sub> ≥ V <sub>T+</sub> max  I <sub>OUT</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
		V <sub>IN</sub> ≥ V <sub>T+</sub> max  I <sub>OUT</sub>   ≤ 4.0 mA  I <sub>OUT</sub>   ≤ 5.2 mA	4.5	0.26	0.33	0.4	
			6.0	0.26	0.33	0.4	
I <sub>IN</sub>	Maximum Input Leakage Current	V <sub>IN</sub> = V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>IN</sub> = V <sub>CC</sub> or GND I <sub>OUT</sub> = 0 μA	6.0	1.0	10	40	μA

4. V<sub>H</sub>min > (V<sub>T+</sub>min) - (V<sub>T-</sub>max); V<sub>H</sub>max = (V<sub>T+</sub>max) + (V<sub>T-</sub>min).

## AC ELECTRICAL CHARACTERISTICS (MC74HC132A)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			-55°C to 25°C	≤ 85°C	≤ 125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, (A or B) to Y (Figures 2 and 3)	2.0	125	155	190	ns
		4.5	25	31	38	
		6.0	21	26	32	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 2 and 3)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF
C <sub>PD</sub>	Power Dissipation Capacitance (per Gate) (Note 5)	Typical @ 25°C, V <sub>CC</sub> = 5.0 V			pF	
		24				

5. Used to determine the no-load dynamic power consumption: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup>f + I<sub>CC</sub> V<sub>CC</sub>.

# MC74HC132A, MC74HCT132A

## DC ELECTRICAL CHARACTERISTICS (MC74HCT132A)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				-55°C to 25°C	≤ 85°C	≤ 125°C	
V <sub>T+</sub> max	Maximum Positive-Going Input Threshold Voltage	V <sub>OUT</sub> = 0.1 V  I <sub>OUT</sub>   ≤ 20 μA	4.5 5.5	1.9 2.1	1.9 2.1	1.9 2.1	V
V <sub>T+</sub> min	Minimum Positive-Going Input Threshold Voltage	V <sub>OUT</sub> = 0.1 V  I <sub>OUT</sub>   ≤ 20 μA	4.5 5.5	1.2 1.4	1.2 1.4	1.2 1.4	V
V <sub>T-</sub> max	Maximum Negative-Going Input Threshold Voltage	V <sub>OUT</sub> = V <sub>CC</sub> - 0.1 V  I <sub>OUT</sub>   ≤ 20 μA	4.5 5.5	1.2 1.4	1.2 1.4	1.2 1.4	V
V <sub>T-</sub> min	Minimum Negative-Going Input Threshold Voltage	V <sub>OUT</sub> = V <sub>CC</sub> - 0.1 V  I <sub>OUT</sub>   ≤ 20 μA	4.5 5.5	0.5 0.6	0.5 0.6	0.5 0.6	V
V <sub>H</sub> min (Note 4)	Minimum Hysteresis Voltage	V <sub>OUT</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>OUT</sub>   ≤ 20 μA	4.5 5.5	0.4 0.4	0.4 0.4	0.4 0.4	V
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>IN</sub> ≤ V <sub>T-</sub> min or V <sub>T+</sub> max  I <sub>OUT</sub>   ≤ 20 μA	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		V <sub>IN</sub> ≤ -V <sub>T-</sub> min or V <sub>T+</sub> max  I <sub>OUT</sub>   ≤ 4.0 mA	4.5	3.98	3.84	3.7	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>IN</sub> ≥ V <sub>T+</sub> max  I <sub>OUT</sub>   ≤ 20 μA	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		V <sub>IN</sub> ≥ V <sub>T+</sub> max  I <sub>OUT</sub>   ≤ 4.0 mA	4.5	0.26	0.33	0.4	
I <sub>IN</sub>	Maximum Input Leakage Current	V <sub>IN</sub> = V <sub>CC</sub> or GND	5.5	±0.1	±1.0	±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>IN</sub> = V <sub>CC</sub> or GND I <sub>OUT</sub> = 0 μA	5.5	1.0	10	40	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

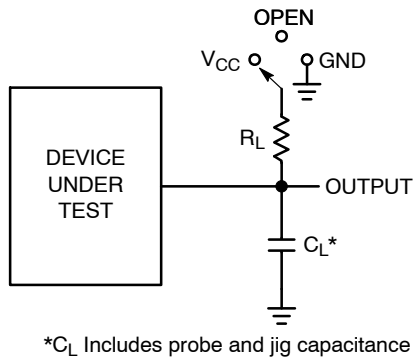
6. V<sub>H</sub>min > (V<sub>T+</sub>min) - (V<sub>T-</sub>max); V<sub>H</sub>max = (V<sub>T+</sub>max) + (V<sub>T-</sub>min).

## AC ELECTRICAL CHARACTERISTICS (MC74HCT132A)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			-55°C to 25°C	≤ 85°C	≤ 125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, (A or B) to Y (Figures 2 and 3)	5.0	25	31	38	ns
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 2 and 3)	5.0	15	19	22	ns
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF
C <sub>PD</sub>	Power Dissipation Capacitance (per Gate) (Note 5)	<b>Typical @ 25°C, V<sub>CC</sub> = 5.0 V</b>			pF	
		24				

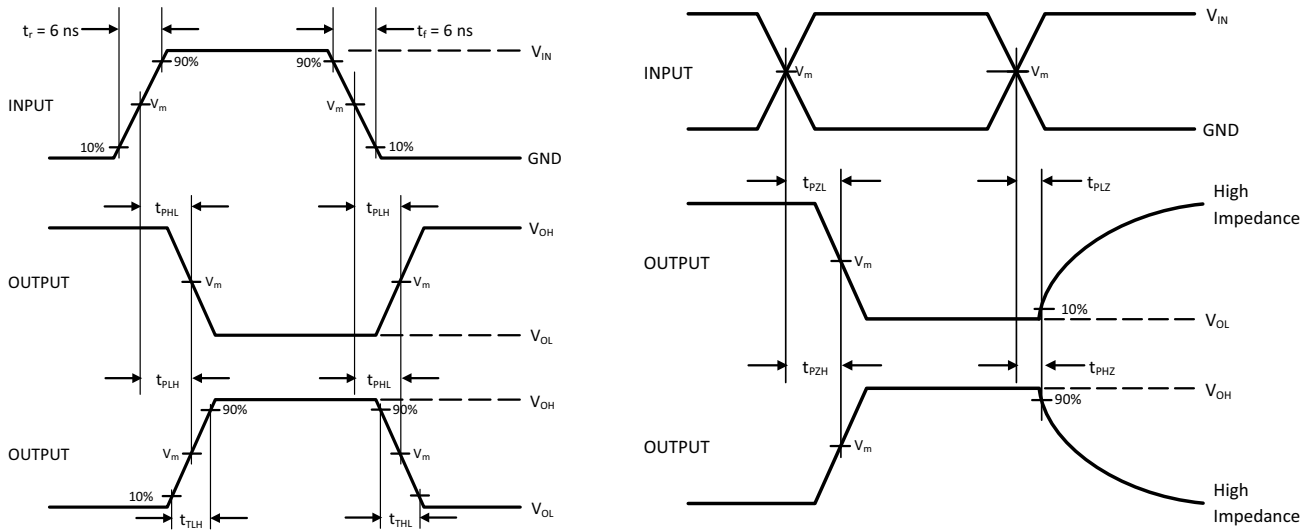
7. Used to determine the no-load dynamic power consumption: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup>f + I<sub>CC</sub> V<sub>CC</sub>.

# MC74HC132A, MC74HCT132A



Test	Switch Position	C <sub>L</sub>	R <sub>L</sub>
t <sub>PLH</sub> / t <sub>PHL</sub>	Open	50 pF	1 kΩ
t <sub>PLZ</sub> / t <sub>PZL</sub>	V <sub>CC</sub>		
t <sub>PHZ</sub> / t <sub>PZH</sub>	GND		

Figure 2. Test Circuit



Device	V <sub>IN</sub> , V	V <sub>m</sub> , V
MC74HC132A	V <sub>CC</sub>	50% x V <sub>CC</sub>
MC74HCT132A	3 V	1.3 V

Figure 3. Switching Waveforms

# MC74HC132A, MC74HCT132A

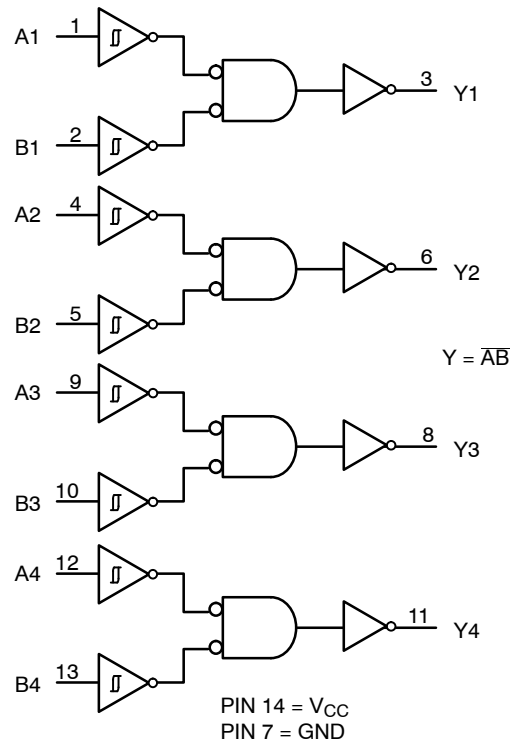


Figure 4. Logic Diagram

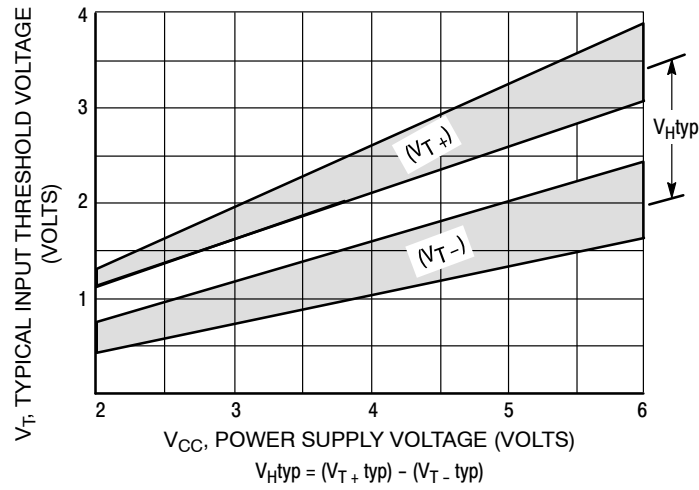
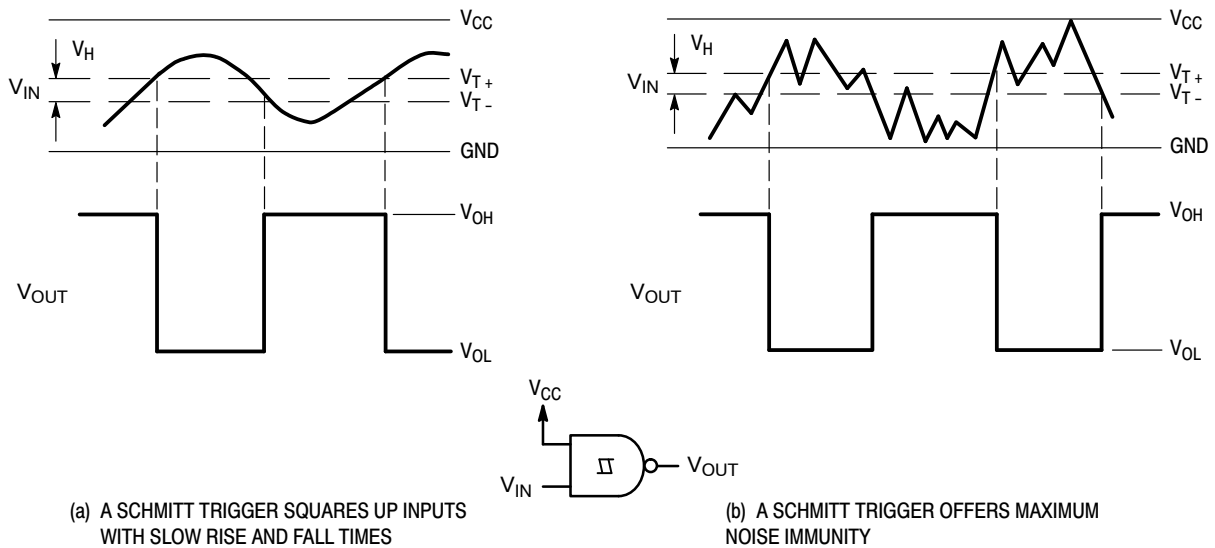


Figure 5. Typical Input Threshold,  $V_{T+}$ ,  $V_{T-}$  Versus Power Supply Voltage

## MC74HC132A, MC74HCT132A



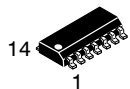
**Figure 6. Typical Schmitt-Trigger Applications**

### ORDERING INFORMATION

Device	Marking	Package	Shipping <sup>†</sup>
MC74HC132ADG	HC132A	SOIC-14	55 Units / Rail
MC74HC132ADR2G	HC132A	SOIC-14	2500 / Tape & Reel
MC74HC132ADTG	HC 132A	TSSOP-14	96 Units / Rail
MC74HC132ADTR2G	HC 132A	TSSOP-14	2500 / Tape & Reel
MC74HC132ADG-Q*	HC132A	SOIC-14	55 Units / Rail
MC74HC132ADR2G-Q*	HC132A	SOIC-14	2500 / Tape & Reel
MC74HC132ADTG-Q*	HC 132A	TSSOP-14	96 Units / Rail
MC74HC132ADTR2G-Q*	HC 132A	TSSOP-14	2500 / Tape & Reel
MC74HCT132ADR2G	HCT132A	SOIC-14	2500 / Tape & Reel
MC74HCT132ADR2G-Q*	HCT132A	SOIC-14	2500 / Tape & Reel
MC74HCT132ADTR2G	HCT 132A	TSSOP-14	2500 / Tape & Reel
MC74HCT132ADTR2G-Q*	HCT 132A	TSSOP-14	2500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

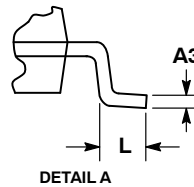
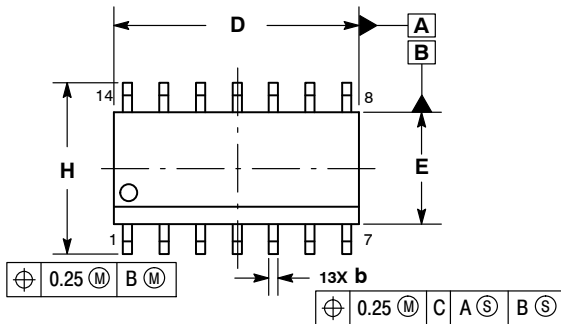
\*-Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable



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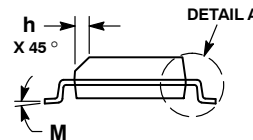
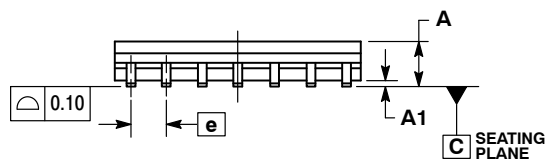
SOIC-14 NB  
CASE 751A-03  
ISSUE L

DATE 03 FEB 2016

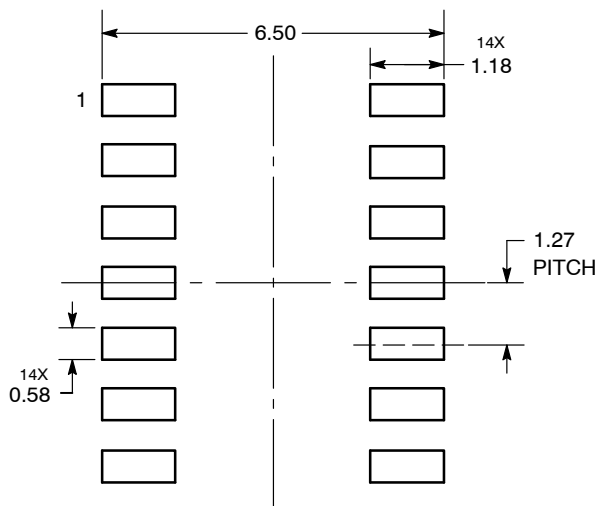


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETERS.
  3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
  4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
  5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0°	7°	0°	7°



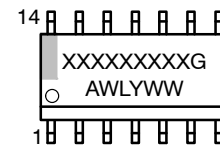
SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM\*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42565B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-14 NB	PAGE 1 OF 2

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**SOIC-14**  
**CASE 751A-03**  
**ISSUE L**

DATE 03 FEB 2016

STYLE 1:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. NO CONNECTION  
 5. ANODE/CATHODE  
 6. NO CONNECTION  
 7. ANODE/CATHODE  
 8. ANODE/CATHODE  
 9. ANODE/CATHODE  
 10. NO CONNECTION  
 11. ANODE/CATHODE  
 12. ANODE/CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 2:  
 CANCELLED

STYLE 3:  
 PIN 1. NO CONNECTION  
 2. ANODE  
 3. ANODE  
 4. NO CONNECTION  
 5. ANODE  
 6. NO CONNECTION  
 7. ANODE  
 8. ANODE  
 9. ANODE  
 10. NO CONNECTION  
 11. ANODE  
 12. ANODE  
 13. NO CONNECTION  
 14. COMMON CATHODE

STYLE 4:  
 PIN 1. NO CONNECTION  
 2. CATHODE  
 3. CATHODE  
 4. NO CONNECTION  
 5. CATHODE  
 6. NO CONNECTION  
 7. CATHODE  
 8. CATHODE  
 9. CATHODE  
 10. NO CONNECTION  
 11. CATHODE  
 12. CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 5:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. ANODE/CATHODE  
 5. ANODE/CATHODE  
 6. NO CONNECTION  
 7. COMMON ANODE  
 8. COMMON CATHODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. ANODE/CATHODE  
 12. ANODE/CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

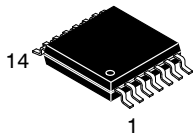
STYLE 6:  
 PIN 1. CATHODE  
 2. CATHODE  
 3. CATHODE  
 4. CATHODE  
 5. CATHODE  
 6. CATHODE  
 7. CATHODE  
 8. ANODE  
 9. ANODE  
 10. ANODE  
 11. ANODE  
 12. ANODE  
 13. ANODE  
 14. ANODE

STYLE 7:  
 PIN 1. ANODE/CATHODE  
 2. COMMON ANODE  
 3. COMMON CATHODE  
 4. ANODE/CATHODE  
 5. ANODE/CATHODE  
 6. ANODE/CATHODE  
 7. ANODE/CATHODE  
 8. ANODE/CATHODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. COMMON CATHODE  
 12. COMMON ANODE  
 13. ANODE/CATHODE  
 14. ANODE/CATHODE

STYLE 8:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. NO CONNECTION  
 5. ANODE/CATHODE  
 6. ANODE/CATHODE  
 7. COMMON ANODE  
 8. COMMON ANODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. NO CONNECTION  
 12. ANODE/CATHODE  
 13. ANODE/CATHODE  
 14. COMMON CATHODE

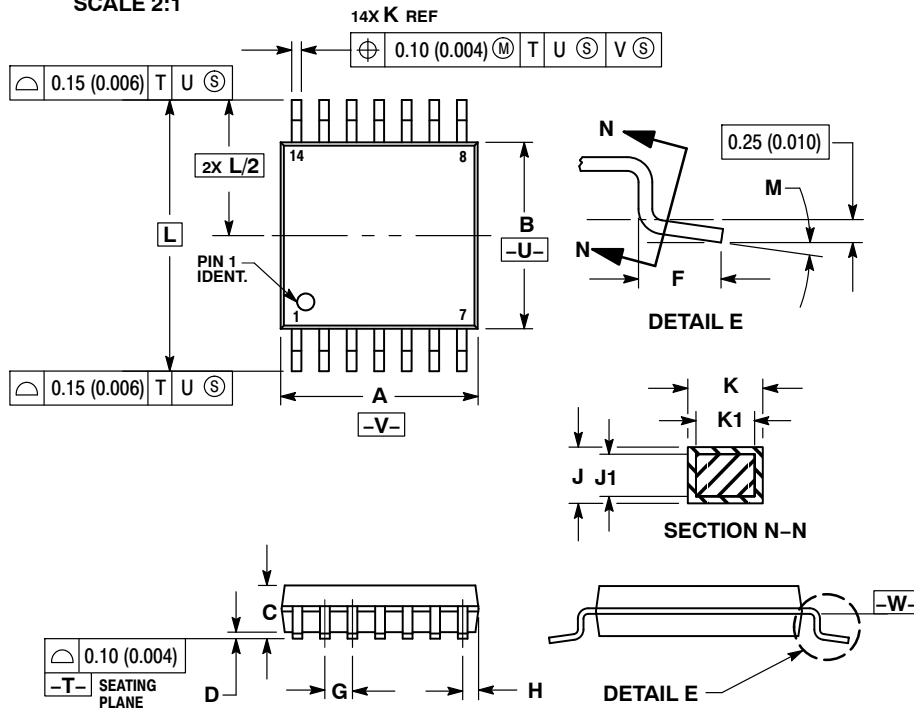
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<b>DESCRIPTION:</b>	<b>SOIC-14 NB</b>	<b>PAGE 2 OF 2</b>

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TSSOP-14 WB  
CASE 948G  
ISSUE C

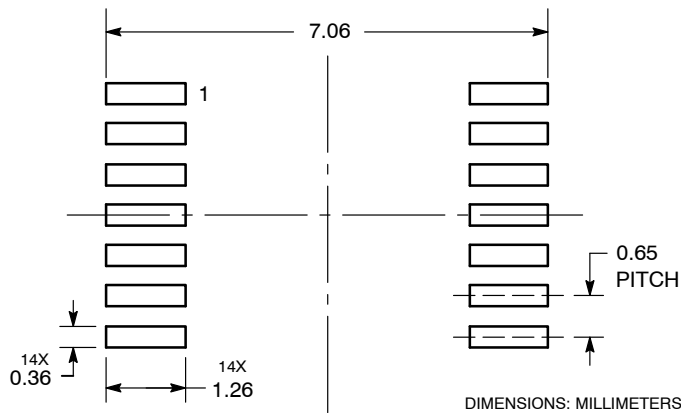
DATE 17 FEB 2016



- NOTES:
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  - CONTROLLING DIMENSION: MILLIMETER.
  - DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
  - DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
  - DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
  - TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
  - DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

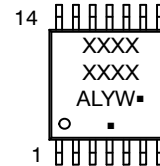
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

RECOMMENDED  
SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC  
MARKING DIAGRAM\*



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	TSSOP-14 WB	PAGE 1 OF 1

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