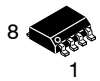
# 5 V ECL D Flip-Flop with Set and Reset

# MC10EL31, MC100EL31




**SOIC−8 NB**
**D SUFFIX**
**CASE 751−07**

## Description

The MC10EL/100EL31 is a D flip-flop with set and reset. The device is functionally equivalent to the E131 device with higher performance capabilities. With propagation delays and output transition times significantly faster than the E131, the EL31 is ideally suited for those applications which require the ultimate in AC performance.

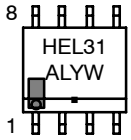
Both set and reset inputs are asynchronous, level triggered signals. Data enters the master portion of the flip-flop when clock is LOW and is transferred to the slave, and thus the outputs, upon a positive transition of the clock.

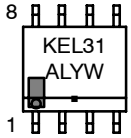
The 100 Series contains temperature compensation.

## Features

- 475 ps Propagation Delay
- 2.8 GHz Toggle Frequency
- ESD Protection:
  - ♦ > 1 kV Human Body Model
  - ♦ > 100 V Machine Model
- PECL Mode Operating Range: $V_{CC}$ = 4.2 V to 5.7 V with $V_{EE}$ = 0 V
- NECL Mode Operating Range: $V_{CC}$ = 0 V with $V_{EE}$ = −4.2 V to −5.7 V
- Internal Input Pulldown Resistors on D, CLK, S, and R
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity:
  - ♦ Level 1 for SOIC−8 NB
  - ♦ For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL 94 V−0 @ 0.125 in, Oxygen Index: 28 to 34
- Metastability 125 ps (see Application Note AN1504)
- Transistor Count = 79 Devices
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

## MARKING DIAGRAMS*




H = MC10
K = MC100
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

## ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| MC10EL31DG | SOIC−8 NB (Pb-Free) | 98 Units / Tube |
| MC10EL31DR2G | SOIC−8 NB (Pb-Free) | 2,500 / Tape & Reel |
| MC100EL31DG | SOIC−8 NB (Pb-Free) | 98 Units / Tube |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

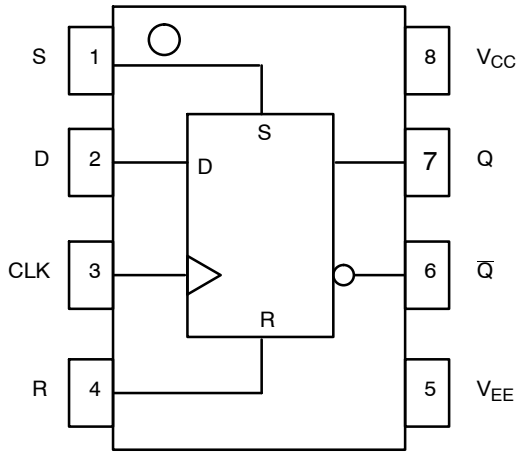



**Figure 1. Logic Diagram and Pinout Assignment**

**Table 1. TRUTH TABLE**

| D | S* | R* | CLK | Q |
|---|---|---|---|---|
| L | L | L | Z | L |
| H | L | L | Z | H |
| X | H | L | X | H |
| X | L | H | X | L |
| X | H | **H** | X | Undef |

Z = LOW to HIGH Transition

* Pins will default low when left open.

**Table 2. PIN DESCRIPTION**

| PIN | FUNCTION |
|---|---|
| S | ECL Set Input |
| D | ECL Data Input |
| R | ECL Reset Input |
| CLK | ECL Clock Input |
| Q, $\overline{Q}$ | ECL Data Outputs |
| $V_{CC}$ | Positive Supply |
| $V_{EE}$ | Negative Supply |

**Table 3. MAXIMUM RATINGS**

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | PECL Mode Power Supply- | $V_{EE}$ = 0 V | | 8 | V |
| $V_{EE}$ | NECL Mode Power Supply | $V_{CC}$ = 0 V | | −8 | V |
| $V_I$ | PECL Mode Input Voltage<br>NECL Mode Input Voltage | $V_{EE}$ = 0 V<br>$V_{CC}$ = 0 V | $V_I \le V_{CC}$<br>$V_I \ge V_{EE}$ | 6<br>−6 | V |
| $I_{out}$ | Output Current | Continuous<br>Surge | | 50<br>100 | mA |
| $T_A$ | Operating Temperature Range | | | −40 to +85 | °C |
| $T_{stg}$ | Storage Temperature Range | | | −65 to +150 | °C |
| $\theta_{JA}$ | Thermal Resistance (Junction-to-Ambient) | 0 lfpm<br>500 lfpm | SOIC−8 NB<br>SOIC−8 NB | 190<br>130 | °C/W |
| $\theta_{JC}$ | Thermal Resistance (Junction-to-Case) | Standard Board | SOIC−8 NB | 41 to 44 | °C/W |
| $T_{sol}$ | Wave Solder (Pb-Free) | < 2 to 3 sec @ 260°C | | 265 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**Table 4. 10EL SERIES PECL DC CHARACTERISTICS** ($V_{CC}$ = 5.0 V; $V_{EE}$ = 0 V) (Note 1)

| Symbol | Characteristic | −40°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $I_{EE}$ | Power Supply Current | | 27 | 32 | | 27 | 32 | | 27 | 32 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 2) | 3920 | 4010 | 4110 | 4020 | 4105 | 4190 | 4090 | 4185 | 4280 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 2) | 3050 | 3200 | 3350 | 3050 | 3210 | 3370 | 3050 | 3227 | 3405 | mV |
| $V_{IH}$ | Input HIGH Voltage | 3770 | | 4110 | 3870 | | 4190 | 3940 | | 4280 | mV |
| $V_{IL}$ | Input LOW Voltage | 3050 | | 3500 | 3050 | | 3520 | 3050 | | 3555 | mV |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current | 0.5 | | | 0.5 | | | 0.3 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

1. Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary +0.25 V / −0.5 V.
2. Outputs are terminated through a 50 ohm resistor to $V_{CC}$−2 volts.

**Table 5. 10EL SERIES NECL DC CHARACTERISTICS** ($V_{CC}$ = 0 V; $V_{EE}$ = −5.0 V) (Note 1)

| Symbol | Characteristic | −40°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $I_{EE}$ | Power Supply Current | | 27 | 32 | | 27 | 32 | | 27 | 32 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 2) | −1080 | −990 | −890 | −980 | −895 | −810 | −910 | −815 | −720 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 2) | −1950 | −1800 | −1650 | −1950 | −1790 | −1630 | −1950 | −1773 | −1595 | mV |
| $V_{IH}$ | Input HIGH Voltage | −1230 | | −890 | −1130 | | −810 | −1060 | | −720 | mV |
| $V_{IL}$ | Input LOW Voltage | −1950 | | −1500 | −1950 | | −1480 | −1950 | | −1445 | mV |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current | 0.5 | | | 0.5 | | | 0.3 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

1. Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary +0.25 V / −0.5 V.
2. Outputs are terminated through a 50 ohm resistor to $V_{CC}$−2 volts.

**Table 6. 100EL SERIES PECL DC CHARACTERISTICS** ($V_{CC}$ = 5.0 V; $V_{EE}$ = 0 V) (Note 1)

| Symbol | Characteristic | −40°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $I_{EE}$ | Power Supply Current | | 27 | 32 | | 27 | 32 | | 31 | 37 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 2) | 3915 | 3995 | 4120 | 3975 | 4045 | 4120 | 3975 | 4050 | 4120 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 2) | 3170 | 3305 | 3445 | 3190 | 3295 | 3380 | 3190 | 3295 | 3380 | mV |
| $V_{IH}$ | Input HIGH Voltage | 3835 | | 4120 | 3835 | | 4120 | 3835 | | 4120 | mV |
| $V_{IL}$ | Input LOW Voltage | 3190 | | 3525 | 3190 | | 3525 | 3190 | | 3525 | mV |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current | 0.5 | | | 0.5 | | | 0.5 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

1. Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary +0.8 V / −0.5 V.
2. Outputs are terminated through a 50 ohm resistor to $V_{CC}$−2 volts.

**Table 7. 100EL SERIES NECL DC CHARACTERISTICS** ($V_{CC}$ = 0 V; $V_{EE}$ = −5.0 V) (Note 1)

| Symbol | Characteristic | −40°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $I_{EE}$ | Power Supply Current | | 27 | 32 | | 27 | 32 | | 31 | 37 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 2) | −1085 | −1005 | −880 | −1025 | −955 | −880 | −1025 | −955 | −880 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 2) | −1830 | −1695 | −1555 | −1810 | −1705 | −1620 | −1810 | −1705 | −1620 | mV |
| $V_{IH}$ | Input HIGH Voltage | −1165 | | −880 | −1165 | | −880 | −1165 | | −880 | mV |
| $V_{IL}$ | Input LOW Voltage | −1810 | | −1475 | −1810 | | −1475 | −1810 | | −1475 | mV |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current | 0.5 | | | 0.5 | | | 0.5 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

1. Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary +0.8 V / −0.5 V.
2. Outputs are terminated through a 50 ohm resistor to $V_{CC}$−2 volts.

**Table 8. AC CHARACTERISTICS** ($V_{CC}$ = 5.0 V; $V_{EE}$ = 0 V or $V_{CC}$ = 0 V; $V_{EE}$ = −5.0 V) (Note 1)

| Symbol | Characteristic | | −40°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| fmax | Maximum Toggle Frequency | | 2.0 | 2.5 | | 2.2 | 2.8 | | 2.2 | 2.8 | | GHz |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>to Output | CLK<br>S, R | 315<br>295 | 465<br>455 | 630<br>630 | 375<br>355 | 475<br>465 | 590<br>590 | 430<br>400 | 530<br>510 | 645<br>645 | ps |
| $t_S$<br>$t_H$ | Setup Time<br>Hold Time | | 150<br>250 | 0<br>100 | | 150<br>250 | 0<br>100 | | 150<br>250 | 0<br>100 | | ps |
| $t_{RR}$ | Set/Reset Recovery | | 400 | 200 | | 400 | 200 | | 400 | 200 | | ps |
| $t_{PW}$ | Minimum Pulse Width<br>CLK, Set, Reset | | 400 | | | 400 | | | 400 | | | ps |
| tJITTER | Cycle-to-Cycle Jitter | | | TBD | | | TBD | | | TBD | | ps |
| $t_r$<br>$t_f$ | Output Rise/Fall Times Q<br>(20% − 80%) | | 100 | 225 | 350 | 100 | 225 | 350 | 100 | 225 | 350 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

1. 10 Series: $V_{EE}$ can vary +0.25 V / −0.5 V.
   100 Series: $V_{EE}$ can vary +0.8 V / −0.5 V.

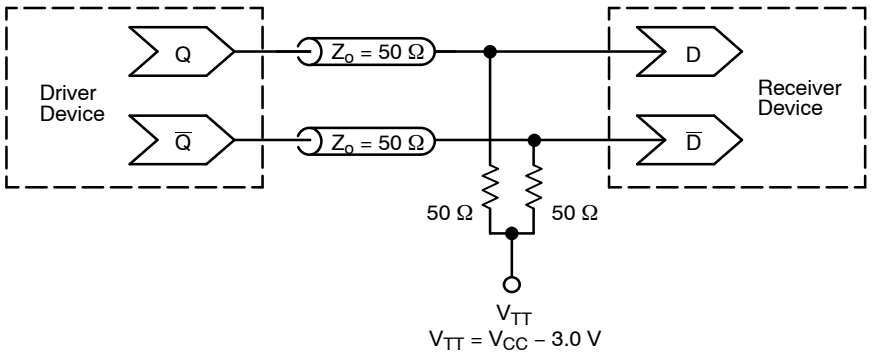



**Figure 2. Typical Termination for Output Driver and Device Evaluation**
**(See Application Note AND8020/D – Termination of ECL Logic Devices)**

### Resource Reference of Application Notes

**AN1405/D** – ECL Clock Distribution Techniques

**AN1406/D** – Designing with PECL (ECL at +5.0 V)

**AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit

**AN1504/D** – Metastability and the ECLinPS Family

**AN1568/D** – Interfacing Between LVDS and ECL

**AN1672/D** – The ECL Translator Guide

**AND8001/D** – Odd Number Counters Design

**AND8002/D** – Marking and Date Codes

**AND8020/D** – Termination of ECL Logic Devices

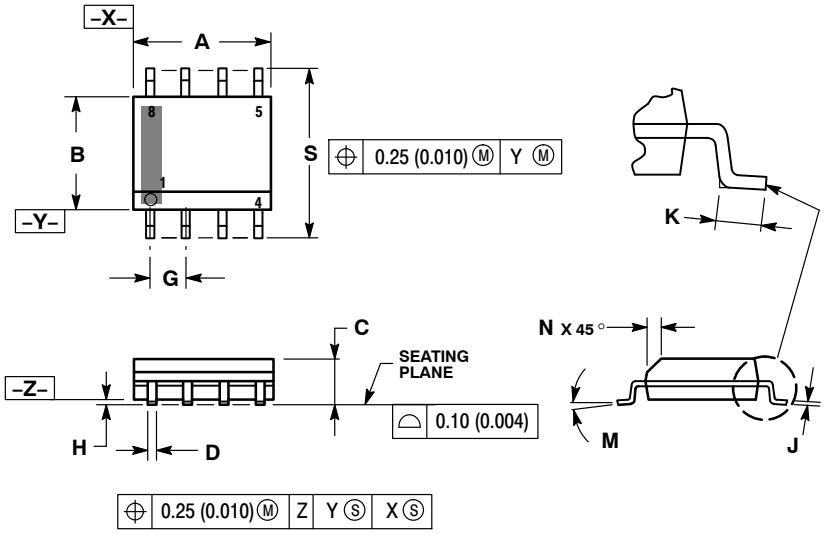
**AND8066/D** – Interfacing with ECLinPS

**AND8090/D** – AC Characteristics of ECL Devices

**SCALE 1:1**

**SOIC−8 NB**
CASE 751−07
ISSUE AK

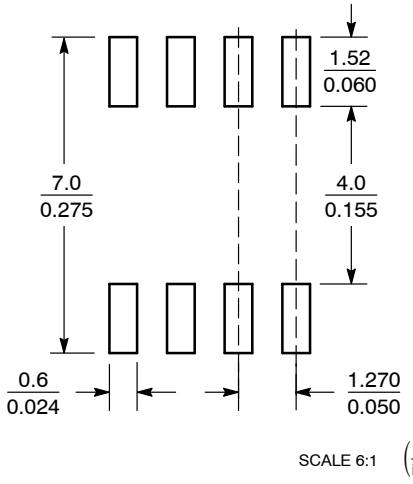
DATE 16 FEB 2011




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 4.80 | 5.00 | 0.189 | 0.197 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.33 | 0.51 | 0.013 | 0.020 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | 0.10 | 0.25 | 0.004 | 0.010 |
| J | 0.19 | 0.25 | 0.007 | 0.010 |
| K | 0.40 | 1.27 | 0.016 | 0.050 |
| M | 0° | 8° | 0° | 8° |
| N | 0.25 | 0.50 | 0.010 | 0.020 |
| S | 5.80 | 6.20 | 0.228 | 0.244 |

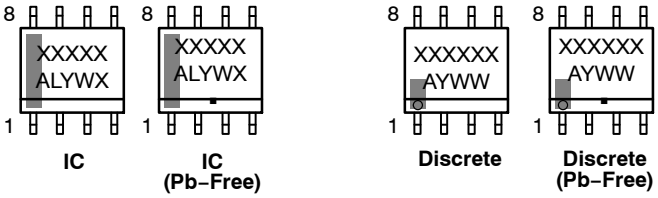
## SOLDERING FOOTPRINT*




SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## GENERIC MARKING DIAGRAM*




XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

**STYLES ON PAGE 2**

| | | | |
|---|---|---|---|
| **DOCUMENT NUMBER:** | **98ASB42564B** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. | |
| **DESCRIPTION:** | **SOIC−8 NB** | | **PAGE 1 OF 2** |

**SOIC−8 NB**
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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