

SN74AHCT273 Octal D-Type Flip-Flops With Clear

1 Features

- Inputs are TTL-voltage compatible
- Contain eight flip-flops with single-rail outputs
- Direct clear input
- Individual data input to each flip-flop
- Latch-up performance exceeds 250mA per JESD 17
- ESD protection exceeds JESD 22
 - 2000V human-body model (A114-A)
 - 200V machine model (A115-A)
 - 1000V charged-device model (C101)

2 Applications

- Buffers and Storage Registers
- Shift Registers
- Pattern Generators
- Servers
- PCs and Notebooks
- Network Switches
- Memory Systems
- Databases

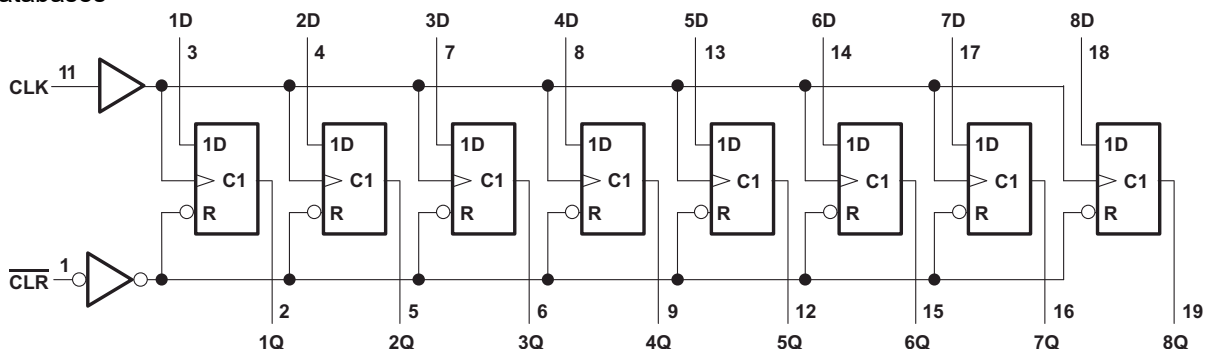
3 Description

These devices are positive-edge-triggered D-type flip-flops with a direct clear ($\overline{\text{CLR}}$) input.

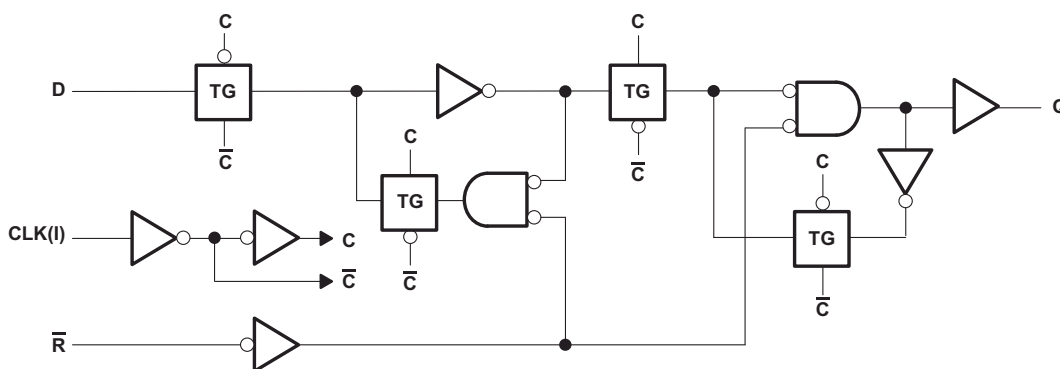
Device Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾	BODY SIZE ⁽³⁾
SN74AHCT273	DB (SSOP, 20)	7.2mm × 7.8mm	7.2mm × 5.30mm
	DW (SOIC, 20)	12.80mm × 10.3mm	12.8mm × 7.5mm
	N (PDIP, 20)	24.33mm × 9.4mm	24.33mm × 6.35mm
	PW (TSSOP, 20)	6.50mm × 6.4mm	6.50mm × 4.40mm
	NS (SOP, 20)	12.6mm × 7.8mm	12.6mm × 5.3mm

- (1) For more information, see [Section 11](#).
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.
- (3) The body size (length × width) is a nominal value and does not include pins.



Simplified Schematic



Simplified Schematic



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4 Pin Configuration and Functions

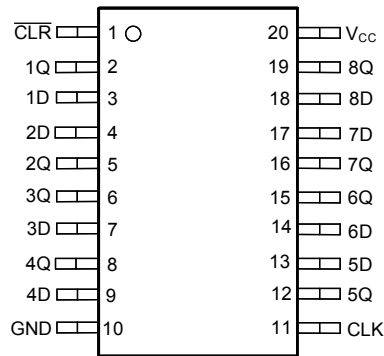


Figure 4-1. SN74AHCT273 DB, DW, N, NS, or PW Packages; 20-Pin SSOP, SOIC, PDIP, SOP, or TSSOP

Table 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	$\overline{\text{CLR}}$	I	Clear Pin
2	1Q	O	1Q Output
3	1D	I	1D Input
4	2D	I	2D Input
5	2Q	O	2Q Output
6	3Q	O	3Q Output
7	3D	I	3D Input
8	4D	I	4D Input
9	4Q	O	4Q Output
10	GND	—	Ground Pin
11	CLK	I	Clock Pin
12	5Q	O	5Q Output
13	5D	I	5D Input
14	6D	I	6D Input
15	6Q	O	6Q Output
16	7Q	O	7Q Output
17	7D	I	7D Input
18	8D	I	8D Input
19	8Q	O	8Q Output
20	V _{CC}	—	Power Pin

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT	
V _{CC}	Supply voltage range	-0.5	7	V	
V _I	Input voltage range ⁽²⁾	-0.5	7	V	
V _O	Output voltage range ⁽²⁾	-0.5	V _{CC} + 0.5	V	
I _{IK}	Input clamp current	V _I < 0		-20	mA
I _{OK}	Output clamp current	V _O < 0 or V _O > V _{CC}		±20	mA
I _O	Continuous output current	V _O = 0 to V _{CC}		±25	mA
Continuous current through V _{CC} or GND				±75	mA

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 Handling Ratings

		MIN	MAX	UNIT
T _{stg}	Storage temperature range	-65	150	°C
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾		V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾		
		0	2000	
		0	1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		SN74AHCT273		UNIT
		MIN	MAX	
V _{CC}	Supply voltage	4.5	5.5	V
V _{IH}	High-level input voltage	2		V
V _{IL}	Low-level input voltage		0.8	V
V _I	Input voltage	0	5.5	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current		-8	mA
I _{OL}	Low-level output current		8	mA
Δt/Δv	Input transition rise or fall rate		20	ns/V
T _A	Operating free-air temperature	-40	125	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI Application Report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74AHCT273						UNIT
		DB (SSOP)	DW (SOIC)	DGV (TVSOP)	N (PDIP)	NS (SOP)	PW (TSSOP)	
		20 PINS						
R _{θJA}	Junction-to-ambient thermal resistance	87.2	81.1	118.1	53.9	77.6	116.8	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	49.1	48.9	33.4	38.8	42.7	58.5	
R _{θJB}	Junction-to-board thermal resistance	51.8	53.8	59.6	34.7	45.7	78.7	
ψ _{JT}	Junction-to-top characterization parameter	11.6	19.5	1.1	26.9	10.2	12.6	
ψ _{JB}	Junction-to-board characterization parameter	51.2	53.1	58.9	34.7	45.2	77.9	
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, (SPRA953).

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN74AHCT273		UNIT
			MIN	TYP	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	4.5 V	4.4	4.5		4.4	V	
	I _{OH} = -8 mA		3.94		3.8			
V _{OL}	I _{OL} = 50 μA	4.5 V			0.1	0.1	V	
	I _{OL} = 8 mA				0.36	0.44		
I _I	V _I = 5.5 V or GND	0 V to 5.5 V			±0.1	±1	μA	
I _{CC}	V _I = V _{CC} or GND I _O = 0	5.5 V			4	40	μA	
ΔI _{CC} ⁽¹⁾	One input at 3.4 V, Other inputs at V _{CC} or GND	5.5 V			1.35	1.5	mA	
C _i	V _I = V _{CC} or GND	5 V		2.5	10	10	pF	

(1) This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

5.6 Timing Requirements

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

			T _A = 25°C		SN74AHCT273		UNIT
			MIN	MAX	MIN	MAX	
t _w	Pulse duration	CLR low	5		6	ns	
		CLK high or low	5		6.5		
t _{su}	Setup time	Data before CLK↑	5		5	ns	
		CLR before CLK↑	2.5		2.5		
t _h	Hold time, data after CLK↑		0		0	ns	

5.7 Switching Characteristics

over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN74AHCT273		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{max}			$C_L = 15\text{ pF}$	75 ⁽¹⁾	120 ⁽¹⁾		65		MHz
			$C_L = 50\text{ pF}$	50	75		45		
t_{PHL}	$\overline{\text{CLR}}$	Q	$C_L = 15\text{ pF}$		7.5 ⁽¹⁾	10 ⁽¹⁾	1	11.6	ns
t_{PLH}	CLK	Q	$C_L = 15\text{ pF}$		5.5 ⁽¹⁾	7.5 ⁽¹⁾	1	8.8	ns
t_{PHL}					5.8 ⁽¹⁾	8.2 ⁽¹⁾	1	10	
t_{PHL}	$\overline{\text{CLR}}$	Q	$C_L = 50\text{ pF}$		8.5	11	1	12.6	ns
t_{PLH}	CLK	Q	$C_L = 50\text{ pF}$		6.5	8.5	1	9.8	ns
t_{PHL}					6.8	9.2	1	11	
$t_{\text{sk(o)}}$			$C_L = 50\text{ pF}$			1 ⁽²⁾		1	ns

- (1) On products compliant to MIL-PRF-38535, this parameter is not production tested.
- (2) On products compliant to MIL-PRF-38535, this parameter does not apply.

5.8 Noise Characteristics

$V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ ⁽¹⁾

PARAMETER	DESCRIPTION	SN74AHCT273			UNIT
		MIN	TYP	MAX	
$V_{\text{OL(P)}}$	Quiet output, maximum dynamic V_{OL}		7.6		V
$V_{\text{OL(V)}}$	Quiet output, minimum dynamic V_{OL}		-0.48		V
$V_{\text{OH(V)}}$	Quiet output, minimum dynamic V_{OH}	4.4			V
$V_{\text{IH(D)}}$	High-level dynamic input voltage		2		V
$V_{\text{IL(D)}}$	Low-level dynamic input voltage			0.8	V

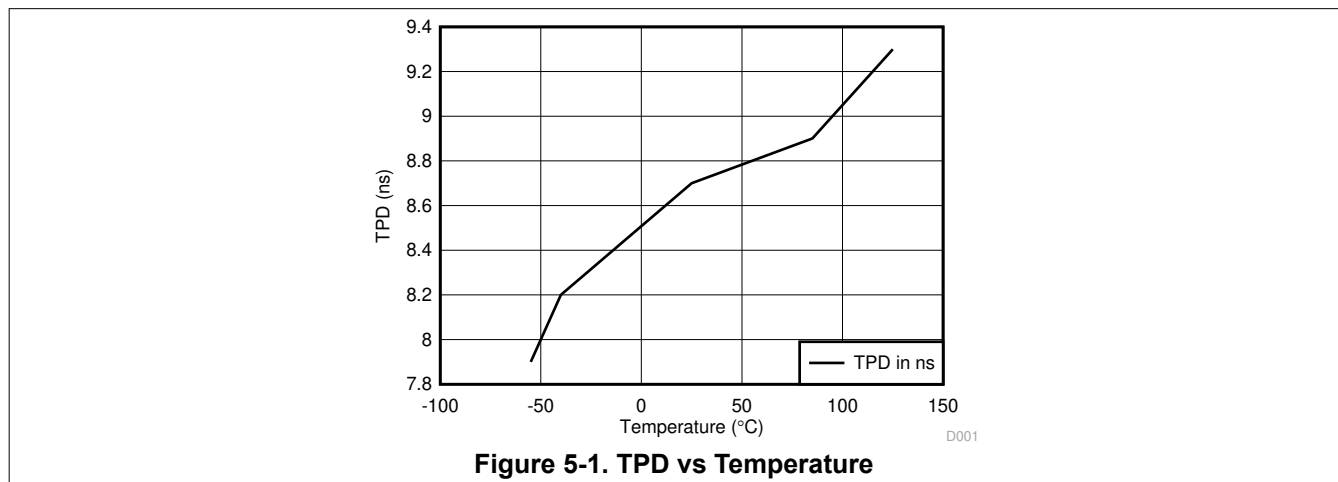
- (1) Characteristics are for surface-mount packages only.

5.9 Operating Characteristics

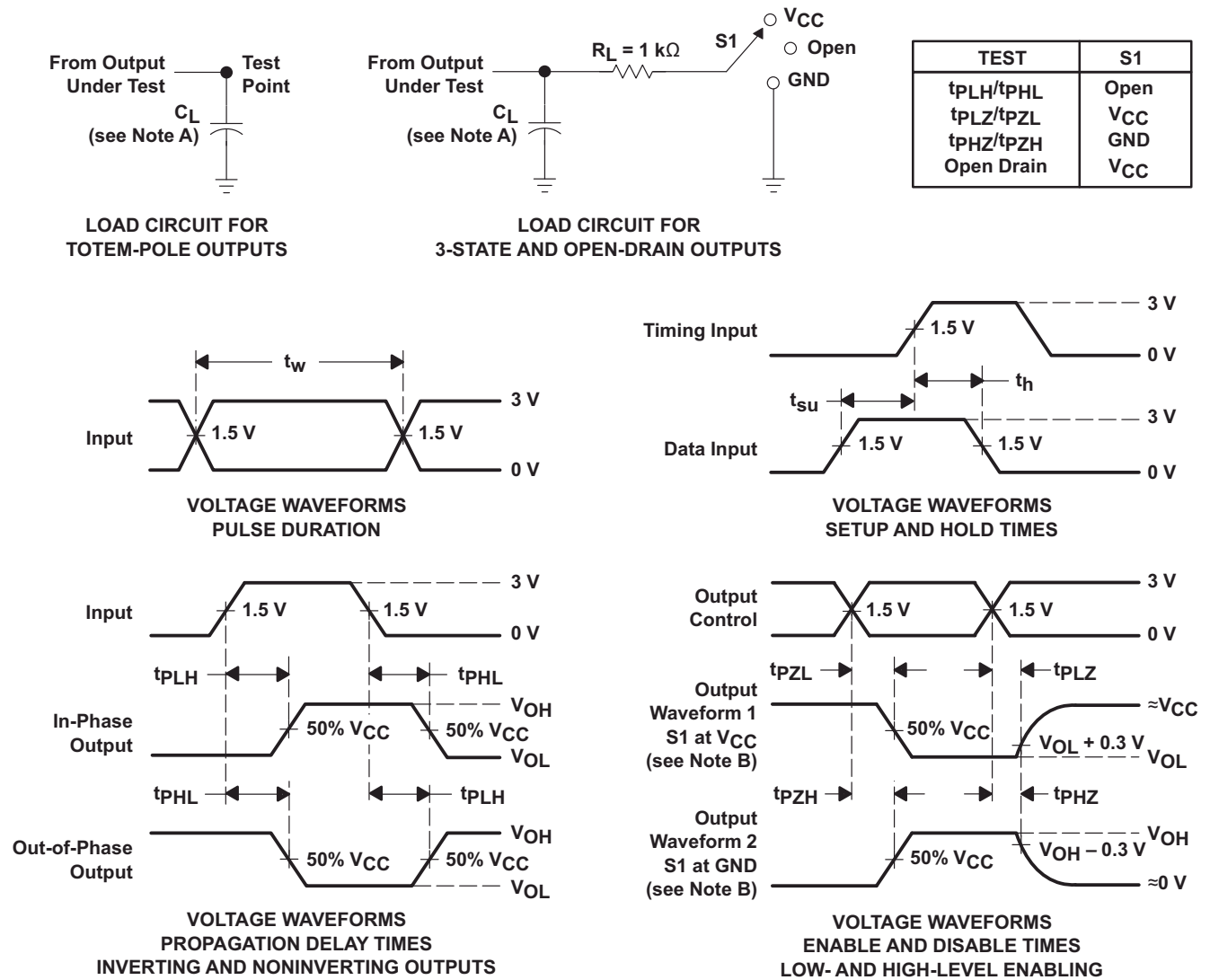
$T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd}	No load, $f = 1\text{ MHz}$	27	pF

5.10 Typical Characteristics



6 Parameter Measurement Information



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 6-1. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

These circuits are positive-edge-triggered D-type flip-flops with a direct clear ($\overline{\text{CLR}}$) input. Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When CLK is at either the high or low level, the D input has no effect at the output.

The inputs are TTL compatible with V_{IL} at 0.8 V and V_{IH} at 2 V. This feature allows the use of these devices as up translators in a mixed 3.3 V to 5 V system environment.

7.2 Functional Block Diagrams

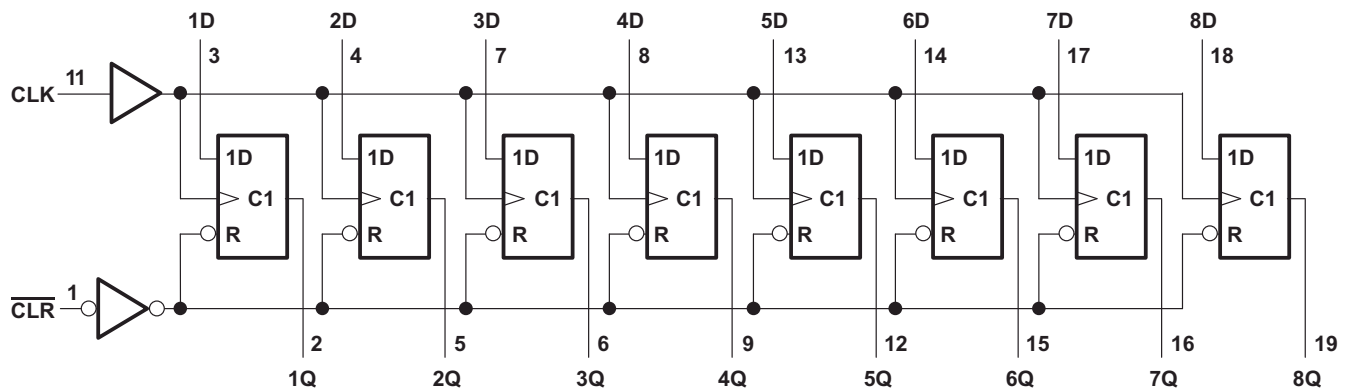


Figure 7-1. Logic Diagram (Positive Logic)

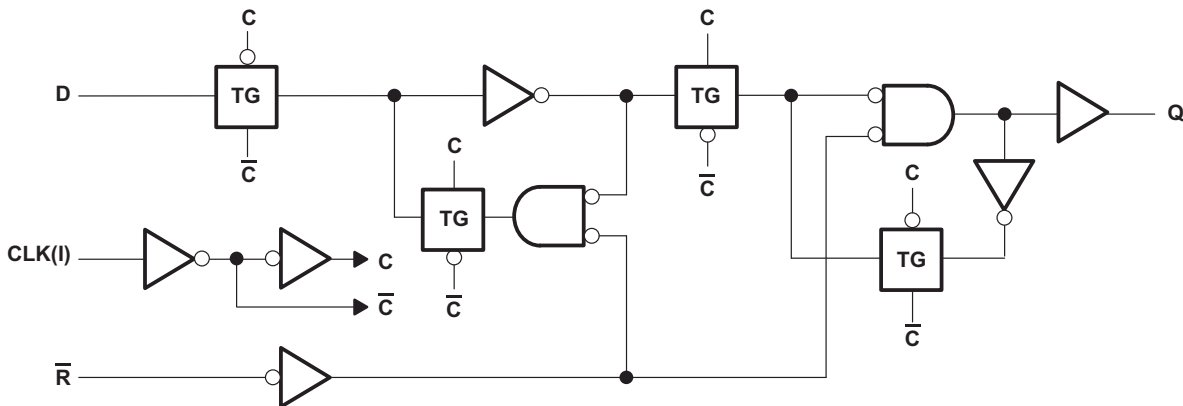


Figure 7-2. Logic Diagram, Each Flip-flop (Positive Logic)

7.3 Feature Description

- Allow up voltage translation from 3.3 V to 5 V
 - Inputs accept TTL voltage levels
- Slow edge rates minimize output ringing

7.4 Device Functional Modes

**Table 7-1. Function Table
(Each Flip-flop)**

INPUTS			OUTPUT Q
CLR	CLK	D	
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q ₀

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The SNx4AHCT273 is a low-drive CMOS device that can be used for a multitude of applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs are TTL compatible. This feature makes it ideal for translating up from 3.3 V to 5 V. [Figure 8-2](#) shows the reduction in ringing compared to higher drive parts such as AC.

8.2 Typical Application

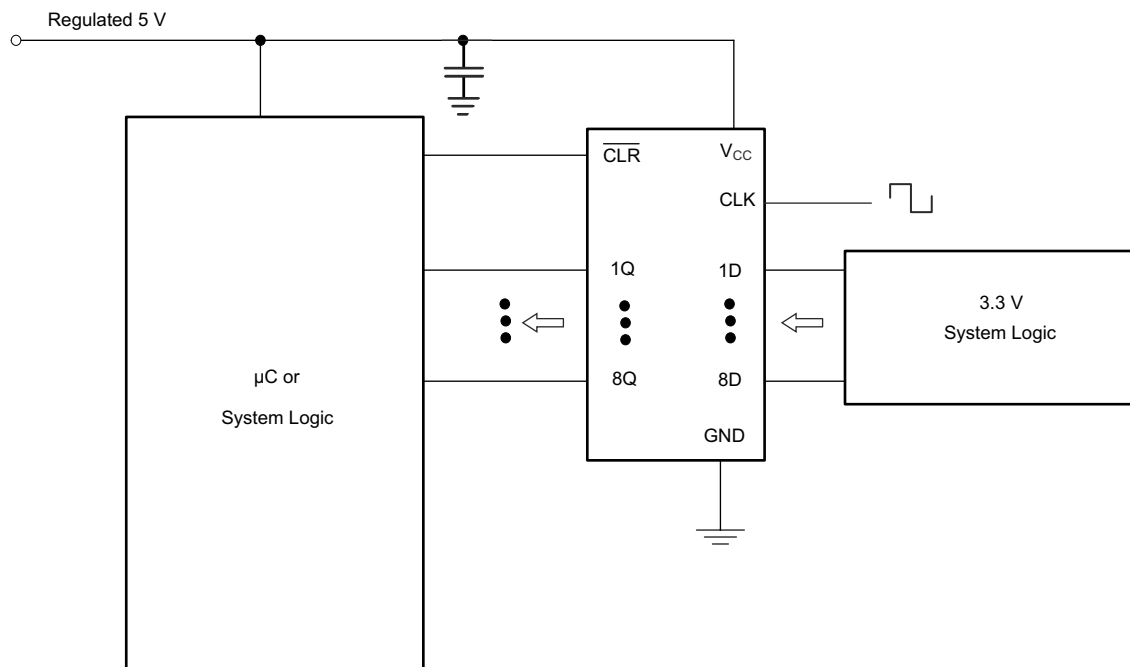


Figure 8-1. Typical Application Schematic

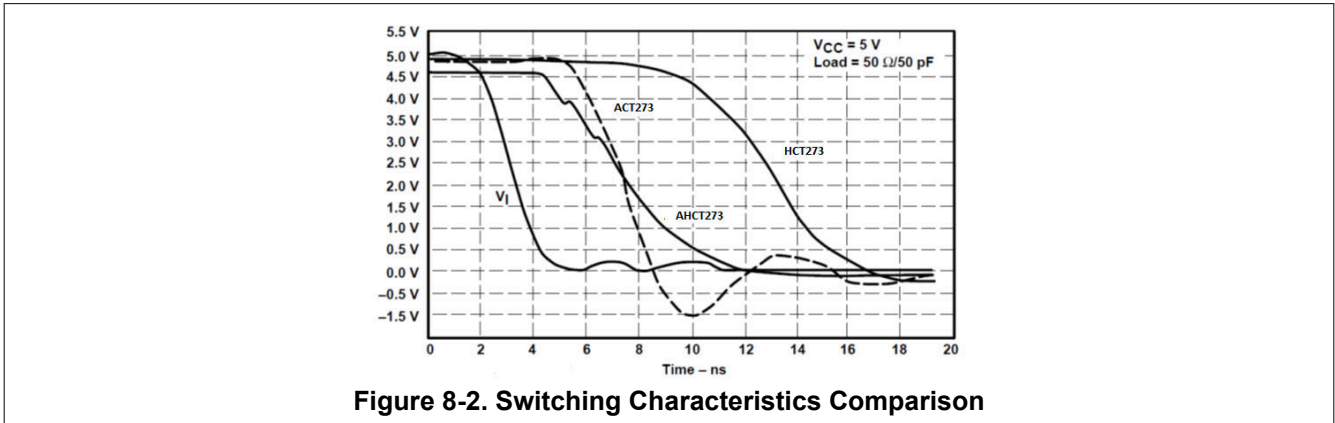
8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

8.2.2 Detailed Design Procedure

- Recommended input conditions
 - Rise time and fall time specs: See $(\Delta t/\Delta V)$ in the [Section 5.3](#) table.
 - Specified High and low levels: See $(V_{IH}$ and $V_{IL})$ in the [Section 5.3](#) table.
 - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}
- Recommend output conditions
 - Load currents should not exceed 25 mA per output and 75 mA total for the part
 - Outputs should not be pulled above V_{CC}

8.2.3 Application Curves



8.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Section 5.3](#) table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μF is recommended. If there are multiple V_{CC} pins, 0.01 μF or 0.022 μF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified in [Figure 8-3](#) are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally inputs will be tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is generally acceptable to float outputs unless the part is a transceiver.

8.4.2 Layout Example

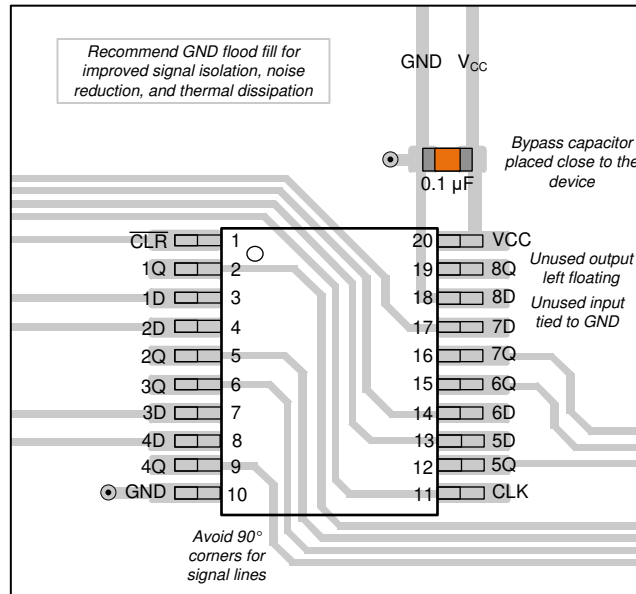


Figure 8-3. Layout Diagram

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 9-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74AHCT273	Click here	Click here	Click here	Click here	Click here

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

Changes from Revision F (July 2014) to Revision G (August 2024)	Page
• Added package size to <i>Package Information</i> table.....	1
• Deleted references to military device throughout data sheet.....	1
• Updated RθJA values: PW = 104.7 to 116.8, DB = 98.7 to 87.2, DW = 81.8 to 81.1, NS = 79.4 to 77.6; Updated PW, DB, DW, and NS packages for RθJC(top), RθJB, ΨJT, ΨJB, and RθJC(bot), all values in °C/ W	5
• Updated <i>Layout Example</i> image.....	12

Changes from Revision E (April 2002) to Revision F (July 2014)	Page
• Updated document to new TI data sheet standards.....	1
• Deleted Ordering Information table.....	1

- Added Applications..... 1
- Added Handling Ratings table.4
- Changed MAX operating temperature to 125°C in Recommended Operating Conditions table.4
- Added Typical Characteristics section.6
- Added Application and Implementation section.10

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHCT273DBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB273	Samples
SN74AHCT273DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	-40 to 125	AHCT273	
SN74AHCT273DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT273	Samples
SN74AHCT273N	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	SN74AHCT273N	Samples
SN74AHCT273NSR	ACTIVE	SOP	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT273	Samples
SN74AHCT273PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB273	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHCT273DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74AHCT273DWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
SN74AHCT273DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74AHCT273NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74AHCT273PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHCT273DBR	SSOP	DB	20	2000	356.0	356.0	35.0
SN74AHCT273DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74AHCT273DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74AHCT273NSR	SOP	NS	20	2000	367.0	367.0	45.0
SN74AHCT273PWR	TSSOP	PW	20	2000	356.0	356.0	35.0

TUBE

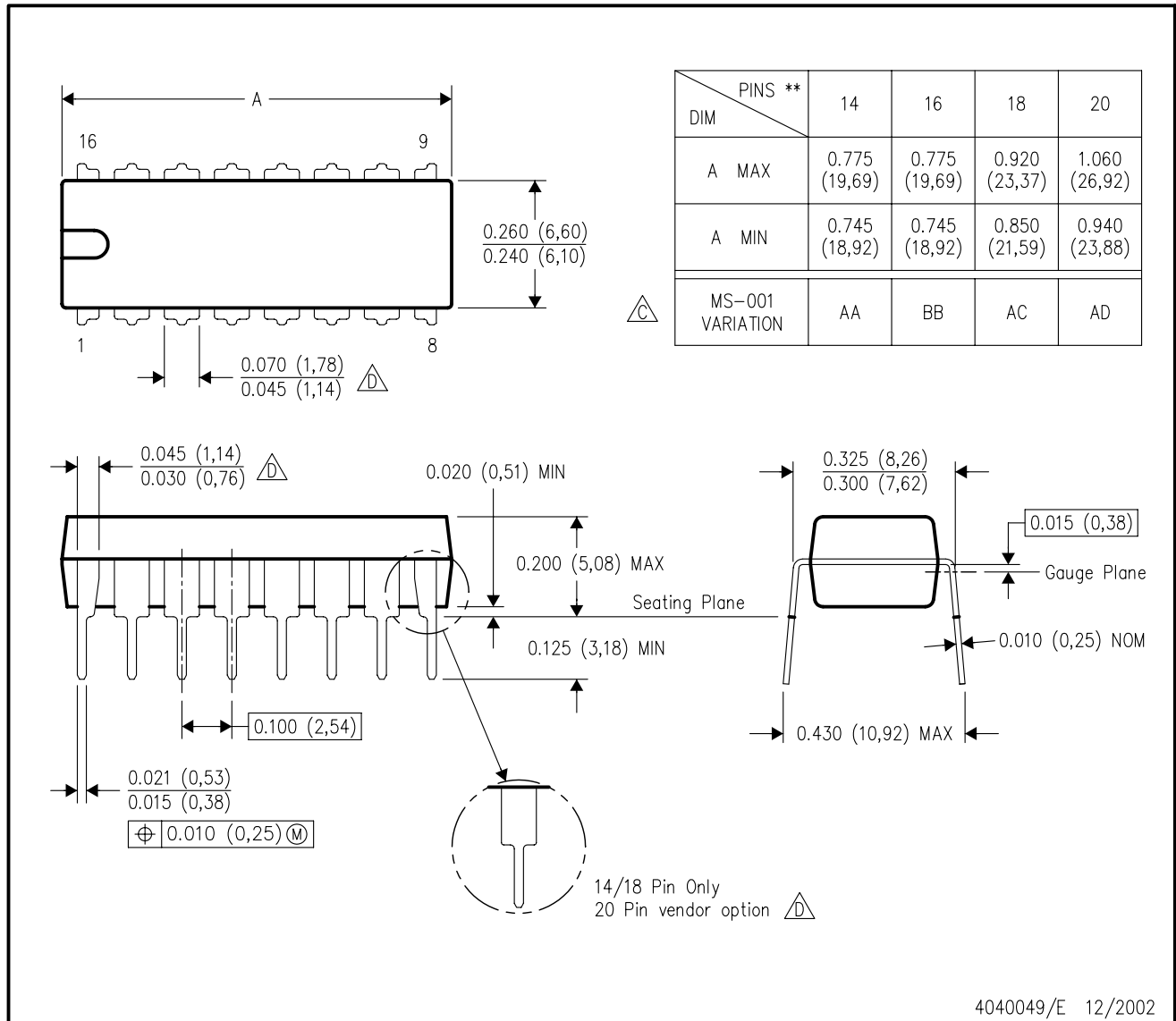

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74AHCT273N	N	PDIP	20	20	506	13.97	11230	4.32

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

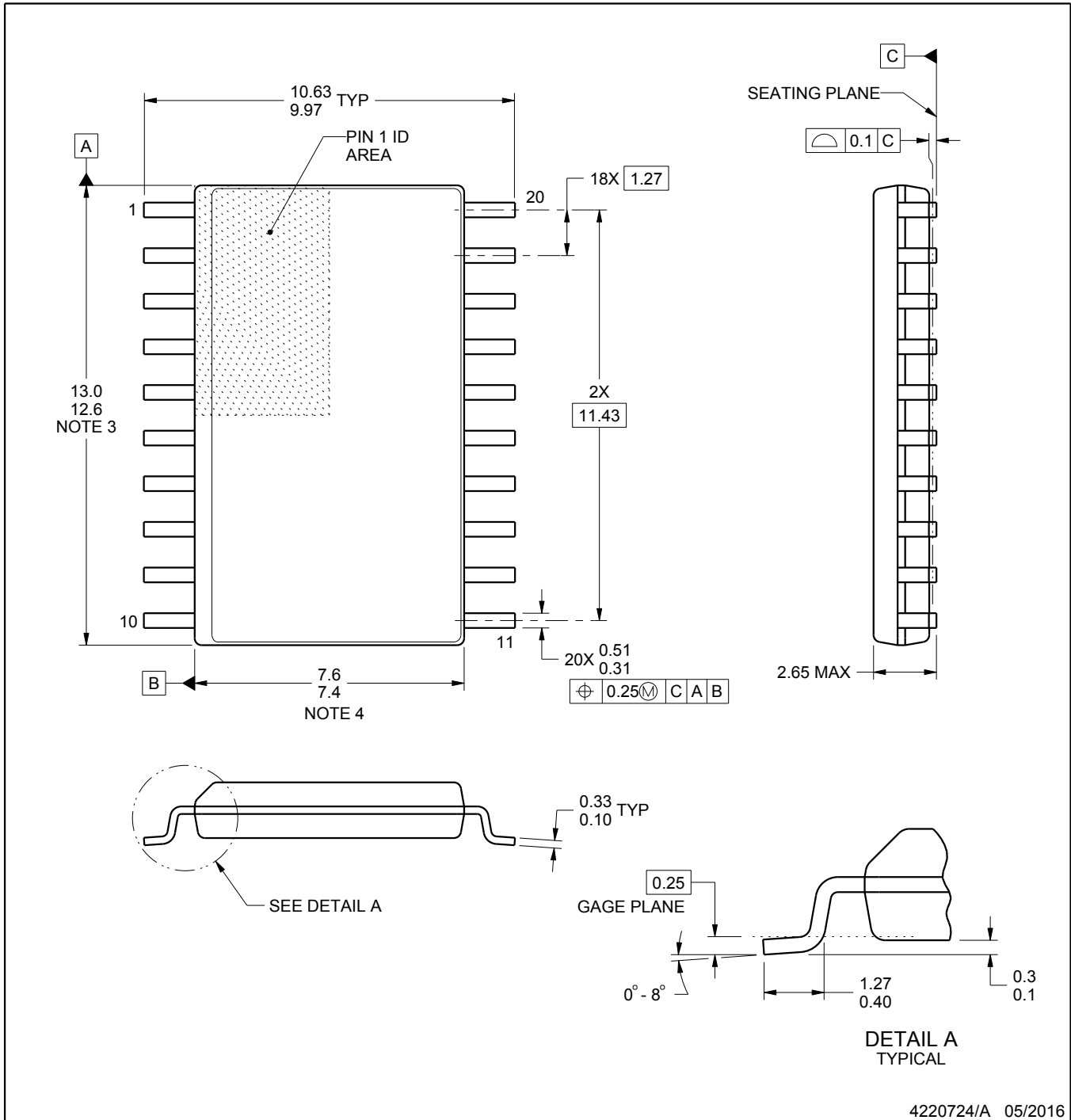
DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES:

- All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
- Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

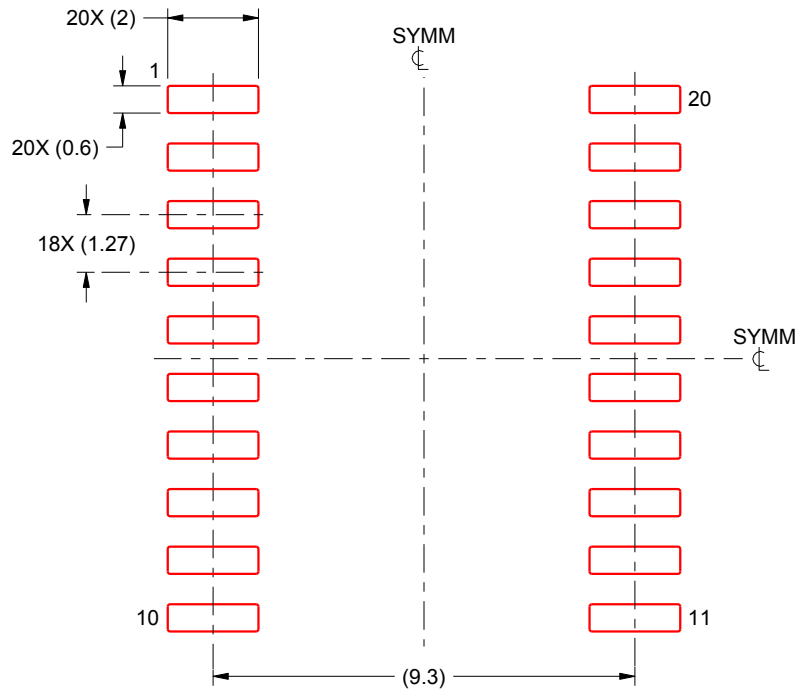
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



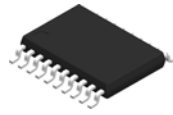
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

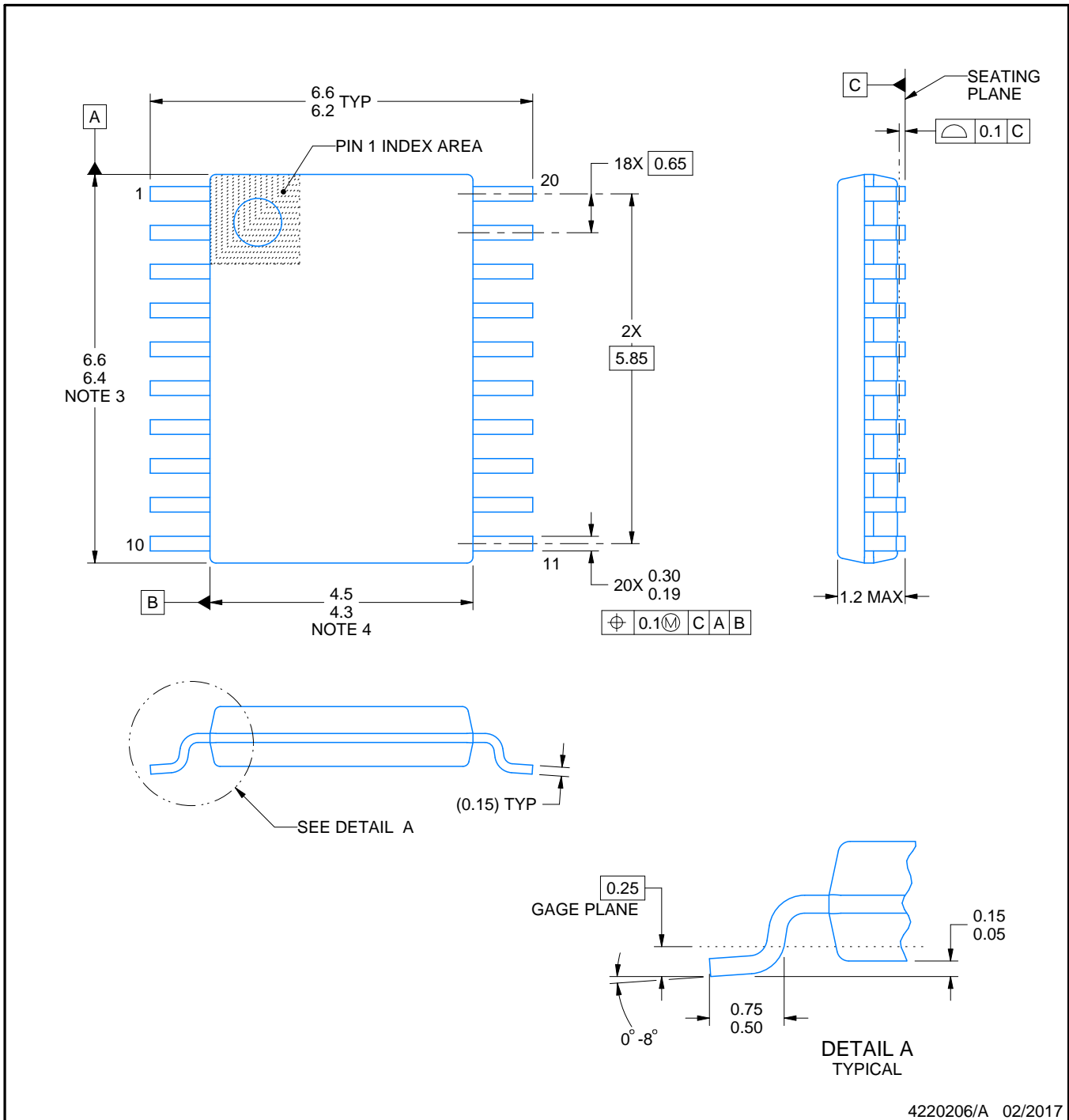
PW0020A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220206/A 02/2017

NOTES:

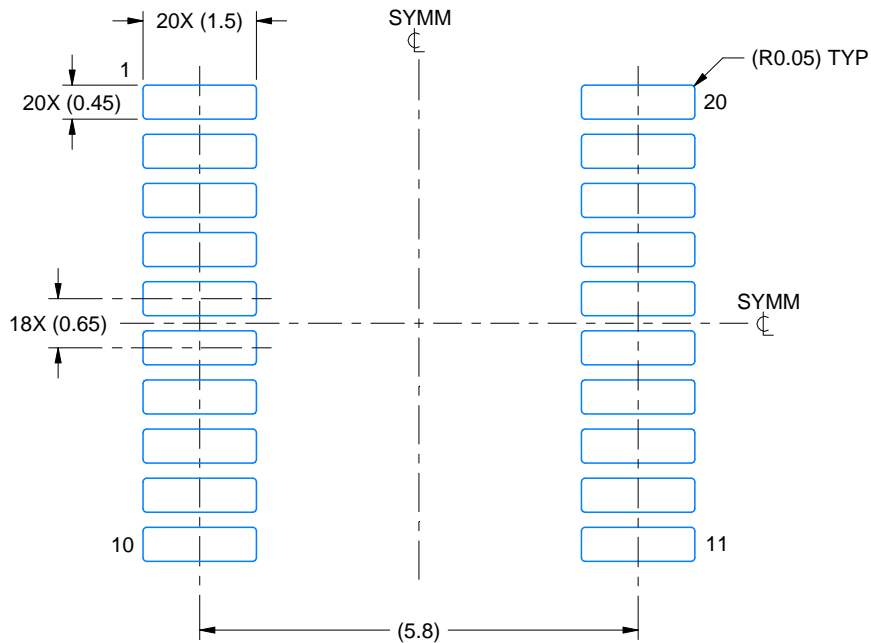
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

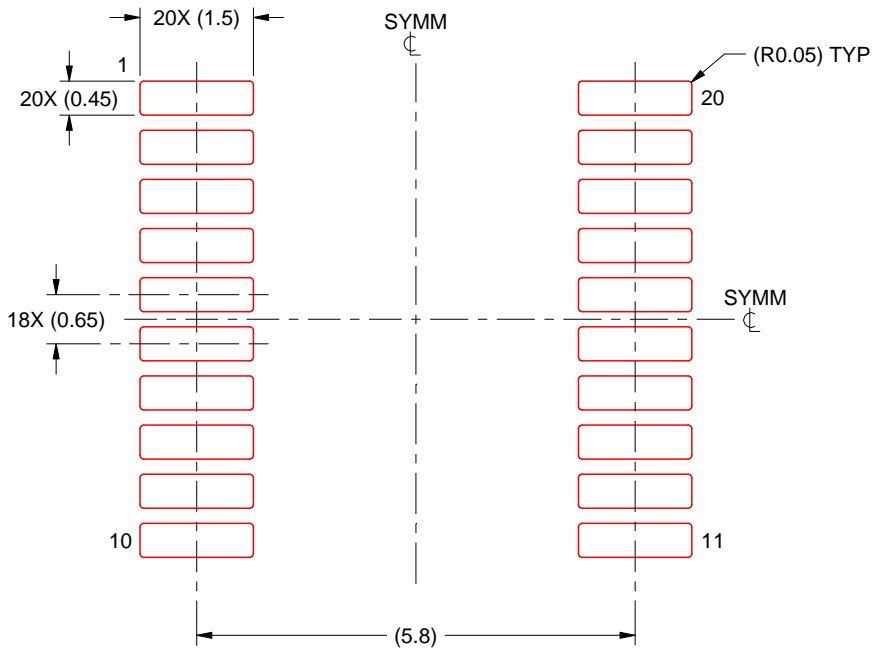
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



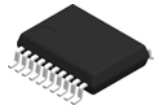
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

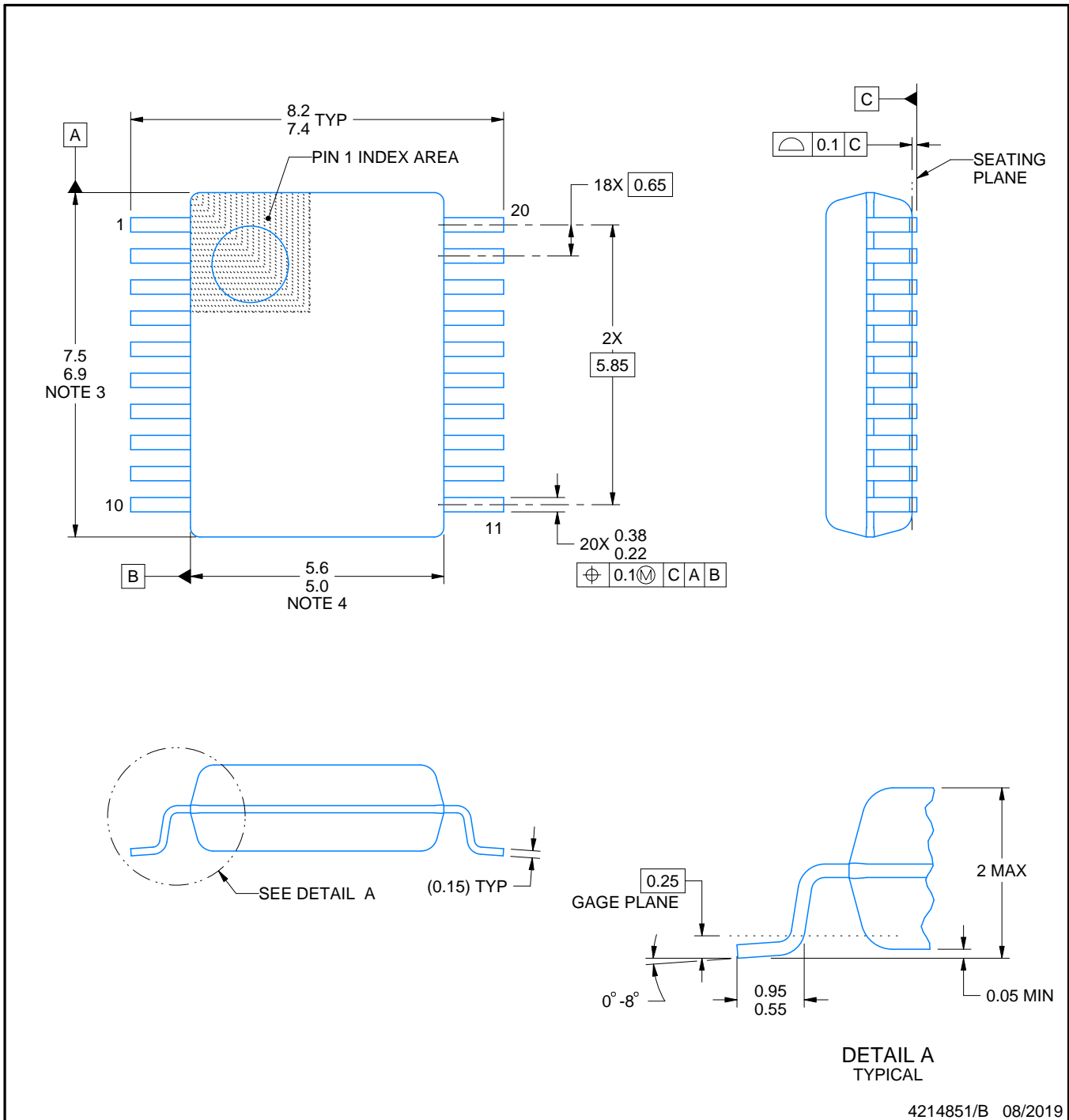
DB0020A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

NOTES:

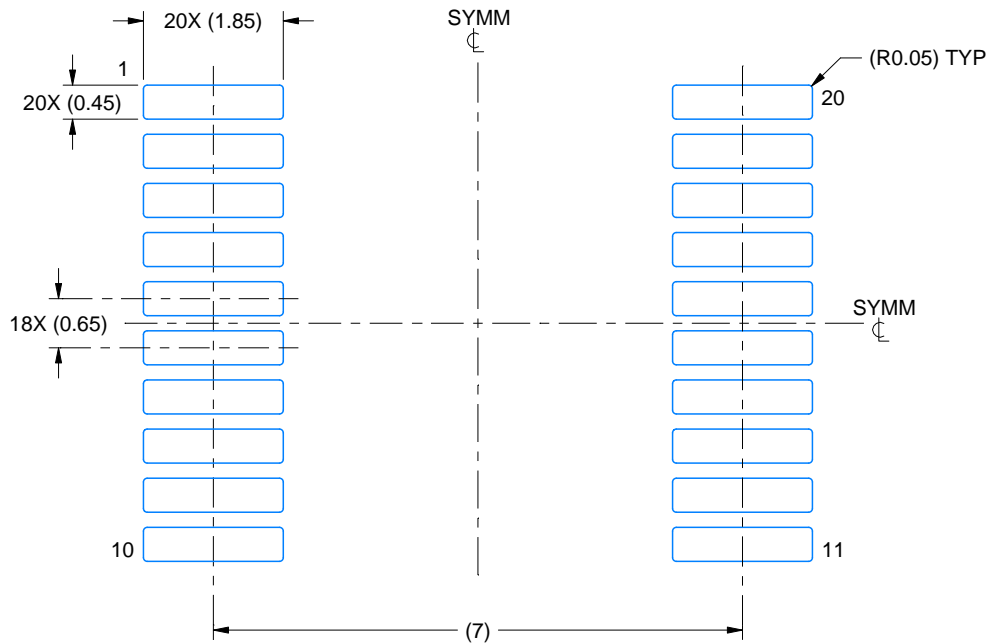
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

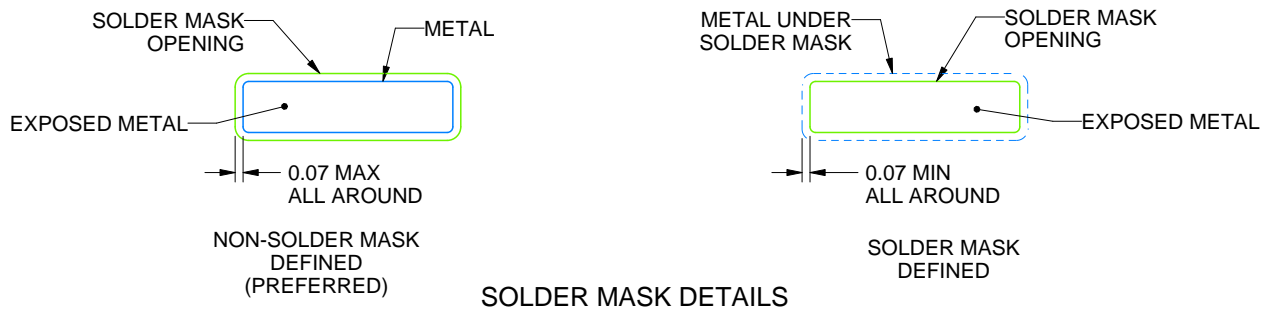
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

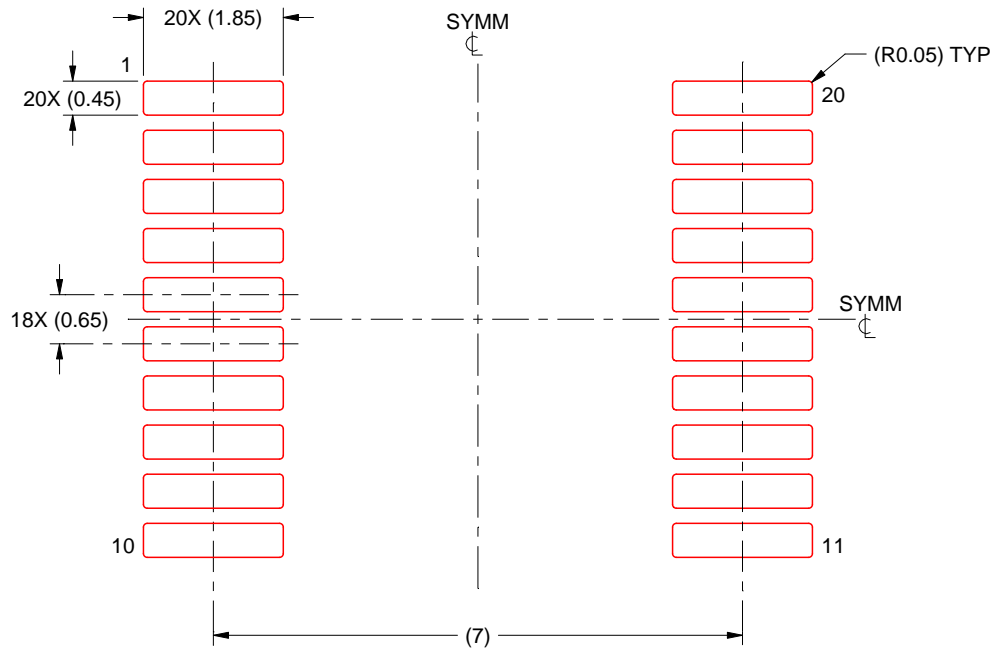
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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