

# Octal D-Type Flip-Flop with 3-State Output

## MC74VHC574, MC74VHCT574A

The MC74VHC574/MC74VHCT574A is an advanced high speed CMOS octal flip-flop with 3-state output fabricated with silicon gate CMOS technology. The device achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

This 8-bit D-type flip-flop is controlled by a clock input and an output enable input. When the output enable input is high, the eight outputs are in a high impedance state.

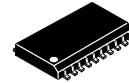
The MC74VHC574 inputs are compatible with standard CMOS levels while the MC74VHCT574A inputs are compatible with TTL levels. The MC74VHCT574A can be used as a level converter for interfacing 3.3 V to 5.0 V, because it has full 5.0 V CMOS level output swings.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The MC74VHC574 and MC74VHCT574A input structures tolerate voltages up to 5.5 V, allowing the interface of 5 V systems to 3 V systems.

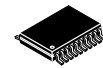
The MC74VHCT574A output structures provide protection when  $V_{CC} = 0$  V. These output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

### Features

- High Speed:  $f_{max} = 180$  MHz (Typ) at  $V_{CC} = 5.0$  V  
 $f_{max} = 140$  MHz (Typ) at  $V_{CC} = 5.0$  V
- Low Power Dissipation:  $I_{CC} = 4.0$   $\mu$ A (Max) at  $T_A = 25^\circ$ C
- High Noise Immunity:  $V_{NIH} = V_{NIL} = 28\%$
- Power Down Protection Provided
- Balanced Propagation Delays
- Designed for: 2.0 V to 5.5 V (VHC)  
4.5 V to 5.5 V (VHCT)
- Low Noise:  $V_{OLP} = 1.2$  V (Max) (VHC)  
 $V_{OLP} = 1.6$  V (Max) (VHCT)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 100 mA
- ESD Performance: Human Body Model > 2000 V;
- Chip Complexity: 286 FETs or 71.5 Equivalent Gates
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

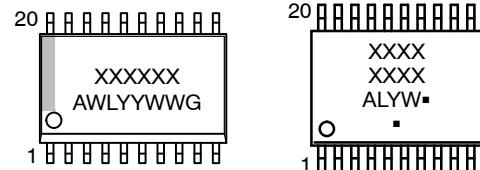


SOIC-20  
DW SUFFIX  
CASE 751D



TSSOP-20  
DT SUFFIX  
CASE 948E

### MARKING DIAGRAMS



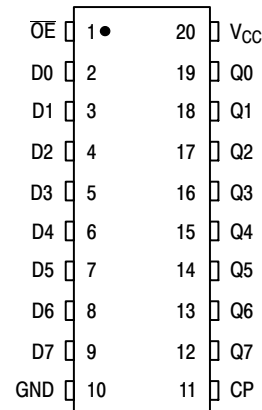
SOIC-20

TSSOP-20

- A = Assembly Location
- WL, L = Wafer Lot
- YY, Y = Year
- WW, W = Work Week
- G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

### PIN ASSIGNMENT



### FUNCTION TABLE

INPUTS			OUTPUT
OE	CP	D	Q
L		H	H
L		L	L
L	L, H,	X	No Change
H	X	X	Z

### ORDERING INFORMATION

See detailed ordering and shipping information on page 10 of this data sheet.

# MC74VHC574, MC74VHCT574A

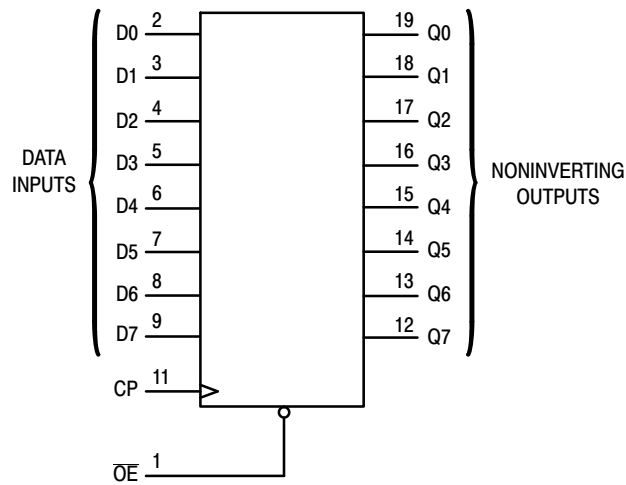


Figure 1. Logic Diagram

## MAXIMUM RATINGS

Symbol	Parameter	Value	Unit	
$V_{CC}$	DC Supply Voltage	-0.5 to +6.5	V	
$V_{IN}$	DC Input Voltage	-0.5 to +6.5	V	
$V_{OUT}$	DC Output Voltage (MC74VHC)	-0.5 to $V_{CC} + 0.5$	V	
	DC Output Voltage (MC74VHCT)	Active Mode (High or Low State)		-0.5 to $V_{CC} + 0.5$
		Tristate Mode (Note 1)		-0.5 to +6.5
	Power-Off Mode ( $V_{CC} = 0$ V)	-0.5 to +6.5		
$I_{IN}$	DC Input Current, per Pin	$\pm 20$	mA	
$I_{OUT}$	DC Output Current, Per Pin	$\pm 25$	mA	
$I_{CC}$	DC Supply Current, $V_{CC}$ and GND Pins	$\pm 75$	mA	
$I_{IK}$	Input Clamp Current	-20	mA	
$I_{OK}$	Output Clamp Current	MC74VHC574	$\pm 20$	mA
		MC74VHCT574A	-20	
$T_{STG}$	Storage Temperature Range	-65 to +150	$^{\circ}$ C	
$T_L$	Lead Temperature, 1 mm from Case for 10 secs	260	$^{\circ}$ C	
$T_J$	Junction Temperature Under Bias	+150	$^{\circ}$ C	
$\theta_{JA}$	Thermal Resistance (Note 2)	SOIC-20W	96	$^{\circ}$ C/W
		TSSOP-20	150	
$P_D$	Power Dissipation in Still Air at 25 $^{\circ}$ C	SOIC-20W	1302	mW
		TSSOP-20	833	
MSL	Moisture Sensitivity	Level 1	-	
$F_R$	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.574 in	-
$V_{ESD}$	ESD Withstand Voltage (Note 3)	Human Body Model	2000	V
		Charged Device Model	N/A	
$I_{LATCHUP}$	Latchup Performance (Note 4)	$\pm 100$	mA	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri-stated.
2. Measured with minimum pad spacing on an FR4 board, using 76 mm-by-114 mm, 2-ounce copper trace no air flow per JESD51-7.
3. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.
4. Tested to EIA/JESD78 Class II.

# MC74VHC574, MC74VHCT574A

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
<b>MC74VHC</b>				
$V_{CC}$	DC Supply Voltage	2.0	5.5	V
$V_{IN}$	DC Input Voltage (Note 5)	0	5.5	V
$V_{OUT}$	DC Output Voltage (Note 5)	0	$V_{CC}$	V
$T_A$	Operating Temperature	-40	+85	°C
$t_r, t_f$	Input Rise or Fall Rate	$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ $V_{CC} = 4.5\text{ V to }5.5\text{ V}$	0 100	ns/V

## MC74VHCT

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	DC Supply Voltage	4.5	5.5	V
$V_{IN}$	DC Input Voltage (Note 5)	0	5.5	V
$V_{OUT}$	DC Output Voltage (Note 5)	0	$V_{CC}$	V
	Active Mode (High or Low State)	0	$V_{CC}$	V
	Tristate Mode	0	5.5	V
	Power-Off Mode ( $V_{CC} = 0\text{ V}$ )	0	5.5	V
$T_A$	Operating Temperature	-40	+85	°C
$t_r, t_f$	Input Rise or Fall Rate	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	0	20

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

5. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

## DC ELECTRICAL CHARACTERISTICS (MC74VHC574)

Symbol	Parameter	Test Conditions	$V_{CC}$ V	$T_A = 25^\circ\text{C}$			$T_A = -40\text{ to }85^\circ\text{C}$		Unit
				Min	Typ	Max	Min	Max	
$V_{IH}$	Minimum High-Level Input Voltage		2.0 3.0 to 5.5	1.50 $V_{CC} \times 0.7$			1.50 $V_{CC} \times 0.7$		V
$V_{IL}$	Maximum Low-Level Input Voltage		2.0 3.0 to 5.5			0.50 $V_{CC} \times 0.3$		0.50 $V_{CC} \times 0.3$	V
$V_{OH}$	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ or $V_{IL}$ $I_{OH} = -50\ \mu\text{A}$	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V
		$V_{in} = V_{IH}$ or $V_{IL}$ $I_{OH} = -4\text{ mA}$ $I_{OH} = -8\text{ mA}$	3.0 4.5	2.58 3.94			2.48 3.80		V
$V_{OL}$	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or $V_{IL}$ $I_{OL} = 50\ \mu\text{A}$	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or $V_{IL}$ $I_{OL} = 4\text{ mA}$ $I_{OL} = 8\text{ mA}$	3.0 4.5			0.36 0.36		0.44 0.44	V
$I_{in}$	Maximum Input Leakage Current	$V_{in} = 5.5\text{ V}$ or GND	0 to 5.5			$\pm 0.1$		$\pm 1.0$	$\mu\text{A}$
$I_{OZ}$	Maximum Three-State Leakage Current	$V_{in} = V_{IL}$ or $V_{IH}$ $V_{out} = V_{CC}$ or GND	5.5			$\pm 0.25$		$\pm 2.5$	$\mu\text{A}$
$I_{CC}$	Maximum Quiescent Supply Current	$V_{in} = V_{CC}$ or GND	5.5			4.0		40.0	$\mu\text{A}$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

# MC74VHC574, MC74VHCT574A

## AC ELECTRICAL CHARACTERISTICS (MC74VHC574)

Symbol	Parameter	Test Conditions	T <sub>A</sub> = 25°C			T <sub>A</sub> = - 40 to 85°C		Unit
			Min	Typ	Max	Min	Max	
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle)	V <sub>CC</sub> = 3.3 ± 0.3 V C <sub>L</sub> = 15 pF	80	125	-	65	-	ns
		C <sub>L</sub> = 50 pF	50	75	-	45	-	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, CP to Q	V <sub>CC</sub> = 3.3 ± 0.3 V C <sub>L</sub> = 15 pF	-	8.5	13.2	1.0	15.5	ns
		C <sub>L</sub> = 50 pF	-	11.0	16.7	1.0	19.0	
t <sub>PZL</sub> , t <sub>PZH</sub>	Output Enable Time, OE to Q	V <sub>CC</sub> = 5.0 ± 0.5 V C <sub>L</sub> = 15 pF	-	5.6	8.6	1.0	10.0	ns
		C <sub>L</sub> = 50 pF	-	7.1	10.6	1.0	12.0	
t <sub>PZL</sub> , t <sub>PZH</sub>	Output Enable Time, OE to Q	V <sub>CC</sub> = 3.3 ± 0.3 V C <sub>L</sub> = 15 pF	-	8.2	12.8	1.0	15.0	ns
		C <sub>L</sub> = 50 pF	-	10.7	16.3	1.0	18.5	
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Output Disable Time, OE to Q	V <sub>CC</sub> = 5.0 ± 0.5 V C <sub>L</sub> = 15 pF	-	5.9	9.0	1.0	10.5	ns
		C <sub>L</sub> = 50 pF	-	7.4	11.0	1.0	12.5	
t <sub>OSLH</sub> , t <sub>OSHL</sub>	Output to Output Skew	V <sub>CC</sub> = 3.3 ± 0.3 V C <sub>L</sub> = 50 pF (Note 6)	-	-	1.5	-	1.5	ns
		V <sub>CC</sub> = 5.0 ± 0.5 V C <sub>L</sub> = 50 pF (Note 6)	-	-	1.0	-	1.0	ns
C <sub>in</sub>	Maximum Input Capacitance		-	4	10	-	10	pF
C <sub>out</sub>	Maximum Three-State Output Capacitance, Output in High-Impedance State		-	6	-	-	-	pF

C <sub>PD</sub>	Power Dissipation Capacitance (Note 7)	Typical @ 25°C, V <sub>CC</sub> = 5.0 V		pF
		28		

6. Parameter guaranteed by design. t<sub>OSLH</sub> = |t<sub>PLHm</sub> - t<sub>PLHn</sub>|, t<sub>OSHL</sub> = |t<sub>PHLm</sub> - t<sub>PHLn</sub>|.

7. C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I<sub>CC(OPR)</sub> = C<sub>PD</sub> • V<sub>CC</sub> • f<sub>in</sub> + I<sub>CC</sub>/8 (per flip-flop). C<sub>PD</sub> is used to determine the no-load dynamic power consumption; P<sub>D</sub> = C<sub>PD</sub> • V<sub>CC</sub><sup>2</sup> • f<sub>in</sub> + I<sub>CC</sub> • V<sub>CC</sub>.

## MC74VHC574, MC74VHCT574A

### NOISE CHARACTERISTICS (MC74VHC574) ( $C_L = 50 \text{ pF}$ , $V_{CC} = 5.0 \text{ V}$ )

Symbol	Parameter	$T_A = 25^\circ\text{C}$		Unit
		Typ	Max	
$V_{OLP}$	Quiet Output Maximum Dynamic $V_{OL}$	0.9	1.2	V
$V_{OLV}$	Quiet Output Minimum Dynamic $V_{OL}$	-0.9	-1.2	V
$V_{IHD}$	Minimum High Level Dynamic Input Voltage	-	3.5	V
$V_{ILD}$	Maximum Low Level Dynamic Input Voltage	-	1.5	V

### TIMING REQUIREMENTS (MC74VHC574)

Symbol	Parameter	Test Conditions	$T_A = 25^\circ\text{C}$		$T_A = -40$ to $85^\circ\text{C}$	Unit
			Typ	Limit	Limit	
$t_{su}$	Minimum Setup Time, D to CP	$V_{CC} = 3.3 \pm 0.3 \text{ V}$ $V_{CC} = 5.0 \pm 0.5 \text{ V}$	-	3.5	3.5	ns
$t_h$	Minimum Hold Time, CP to D	$V_{CC} = 3.3 \pm 0.3 \text{ V}$ $V_{CC} = 5.0 \pm 0.5 \text{ V}$	-	1.5	1.5	ns
$t_w$	Minimum Pulse Width, CP	$V_{CC} = 3.3 \pm 0.3 \text{ V}$ $V_{CC} = 5.0 \pm 0.5 \text{ V}$	-	5.0	5.5	ns

# MC74VHC574, MC74VHCT574A

## DC ELECTRICAL CHARACTERISTICS (MC74VHCT574A)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	T <sub>A</sub> = 25°C			T <sub>A</sub> = - 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V <sub>IH</sub>	Minimum High-Level Input Voltage		4.5 to 5.5	2.0			2.0		V
V <sub>IL</sub>	Maximum Low-Level Input Voltage		4.5 to 5.5			0.8		0.8	V
V <sub>OH</sub>	Minimum High-Level Output Voltage V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = - 50 μA	4.5	4.4	4.5		4.4		V
		I <sub>OH</sub> = - 8 mA	4.5	3.94			3.80		
V <sub>OL</sub>	Maximum Low-Level Output Voltage V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 50 μA	4.5		0.0	0.1		0.1	V
		I <sub>OL</sub> = 8 mA	4.5			0.36		0.44	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = 5.5 V or GND	0 to 5.5			±0.1		±1.0	μA
I <sub>OZ</sub>	Maximum 3-State Leakage Current	V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>out</sub> = V <sub>CC</sub> or GND	5.5			±0.25		±2.5	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current	V <sub>in</sub> = V <sub>CC</sub> or GND	5.5			4.0		40.0	μA
I <sub>CCT</sub>	Quiescent Supply Current	Per Input: V <sub>IN</sub> = 3.4 V Other Input: V <sub>CC</sub> or GND	5.5			1.35		1.50	mA
I <sub>OPD</sub>	Output Leakage Current	V <sub>OUT</sub> = 5.5 V	0			0.5		5.0	μA

## AC ELECTRICAL CHARACTERISTICS (MC74VHCT574A)

Symbol	Parameter	Test Conditions	T <sub>A</sub> = 25°C			T <sub>A</sub> = - 40 to 85°C		Unit
			Min	Typ	Max	Min	Max	
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle)	V <sub>CC</sub> = 5.0 ± 0.5 V C <sub>L</sub> = 15 pF C <sub>L</sub> = 50 pF	90 85	140 130		80 95		MHz
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, CP to Q	V <sub>CC</sub> = 5.0 ± 0.5 V C <sub>L</sub> = 15 pF C <sub>L</sub> = 50 pF		4.1 5.6	9.4 10.4	1.0 1.0	10.5 11.5	ns
t <sub>PZL</sub> , t <sub>PZH</sub>	Output Enable Time, OE to Q	V <sub>CC</sub> = 5.0 ± 0.5 V C <sub>L</sub> = 15 pF C <sub>L</sub> = 50 pF		6.5 7.3	10.2 11.2	1.0 1.0	11.5 12.5	ns
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Output Disable Time, OE to Q	V <sub>CC</sub> = 5.0 ± 0.5 V C <sub>L</sub> = 50 pF		7.0	11.2	1.0	12.0	ns
t <sub>OSLH</sub> , t <sub>OSHL</sub>	Output to Output Skew	V <sub>CC</sub> = 5.0 ± 0.5 V C <sub>L</sub> = 50 pF (Note 8)			1.0		1.0	ns
C <sub>in</sub>	Maximum Input Capacitance			4	10		10	pF
C <sub>out</sub>	Maximum Three-State Output Capacitance, Output in High-Impedance State			9				pF

C <sub>PD</sub>	Power Dissipation Capacitance (Note 9)	Typical @ 25°C, V <sub>CC</sub> = 5.0 V		pF
		25		

8. Parameter guaranteed by design. t<sub>OSLH</sub> = |t<sub>PLHm</sub> - t<sub>PLHn</sub>|, t<sub>OSHL</sub> = |t<sub>PHLm</sub> - t<sub>PHLn</sub>|.
9. C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I<sub>CC(OPR)</sub> = C<sub>PD</sub> • V<sub>CC</sub> • f<sub>in</sub> + I<sub>CC</sub>/8 (per flip-flop). C<sub>PD</sub> is used to determine the no-load dynamic power consumption; P<sub>D</sub> = C<sub>PD</sub> • V<sub>CC</sub><sup>2</sup> • f<sub>in</sub> + I<sub>CC</sub> • V<sub>CC</sub>.

## MC74VHC574, MC74VHCT574A

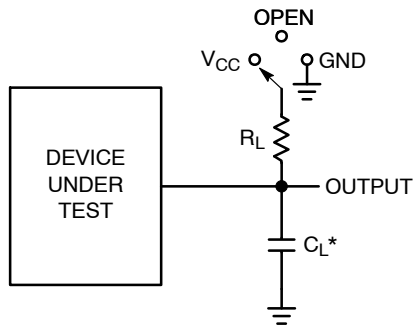
### NOISE CHARACTERISTICS (MC74VHCT574A) ( $C_L = 50 \text{ pF}$ , $V_{CC} = 5.0 \text{ V}$ )

Symbol	Parameter	$T_A = 25^\circ\text{C}$		Unit
		Typ	Max	
$V_{OLP}$	Quiet Output Maximum Dynamic $V_{OL}$	1.2	1.6	V
$V_{OLV}$	Quiet Output Minimum Dynamic $V_{OL}$	-1.2	-1.6	V
$V_{IHD}$	Minimum High Level Dynamic Input Voltage		2.0	V
$V_{ILD}$	Maximum Low Level Dynamic Input Voltage		0.8	V

### TIMING REQUIREMENTS (MC74VHCT574A)

Symbol	Parameter	Test Conditions	$T_A = 25^\circ\text{C}$		$T_A = -40 \text{ to } 85^\circ\text{C}$	Unit
			Typ	Limit	Limit	
$t_{su}$	Minimum Setup Time, D to CP	$V_{CC} = 5.0 \pm 0.5 \text{ V}$		6.5	8.5	ns
$t_h$	Minimum Hold Time, CP to D	$V_{CC} = 5.0 \pm 0.5 \text{ V}$		2.5	2.5	ns
$t_w$	Minimum Pulse Width, CP	$V_{CC} = 5.0 \pm 0.5 \text{ V}$		2.5	2.5	ns

# MC74VHC574, MC74VHCT574A



\*C<sub>L</sub> Includes probe and jig capacitance  
Input signal t<sub>R</sub> = t<sub>F</sub> = 3 ns

Test	Switch Position	C <sub>L</sub>	R <sub>L</sub>
t <sub>PLH</sub> / t <sub>PHL</sub>	Open	See AC Characteristics Table	1 kΩ
t <sub>PLZ</sub> / t <sub>PZL</sub>	V <sub>CC</sub>		
t <sub>PHZ</sub> / t <sub>PZH</sub>	GND		

Figure 2. Test Circuits

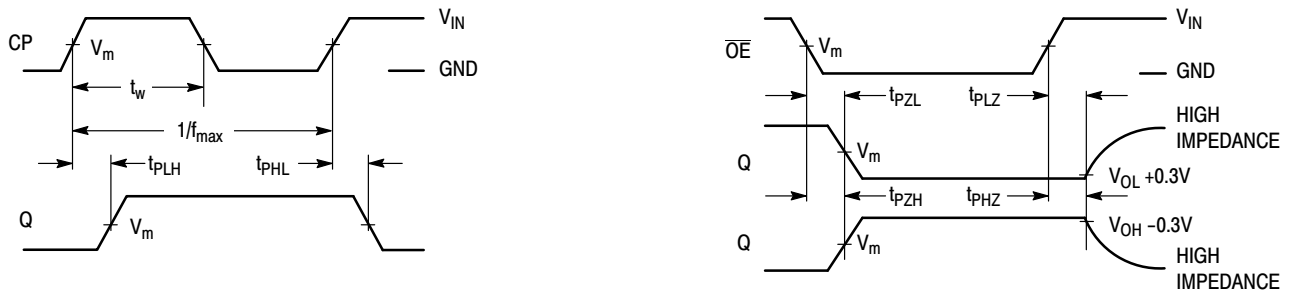


Figure 3. Switching Waveforms

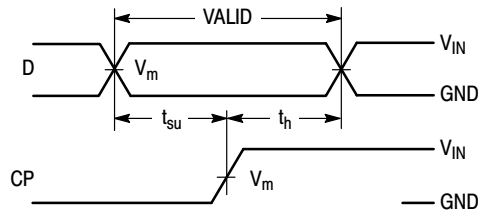


Figure 4.

Device	V <sub>IN</sub> , V	V <sub>m</sub> , V
MC74VHC574	V <sub>CC</sub>	50% x V <sub>CC</sub>
MC74VHCT574A	3 V	1.5 V





## MC74VHC574, MC74VHCT574A

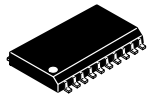
### ORDERING INFORMATION

Device	Marking	Package	Shipping <sup>†</sup>
MC74VHC574DWG	VHC574G	SOIC-20W	38 Units / Rail
MC74VHC574DWR2G	VHC574G	SOIC-20W	1000 / Tape & Reel
MC74VHC574DTG	VHC 574	TSSOP-20	75 Units / Rail
MC74VHC574DTR2G	VHC 574	TSSOP-20	2500 / Tape & Reel
MC74VHCT574ADWR2G	VHCT574AG	SOIC-20W	1000 / Tape & Reel
MC74VHCT574ADTR2G	VHCT 574A	TSSOP-20	2500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*-Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable

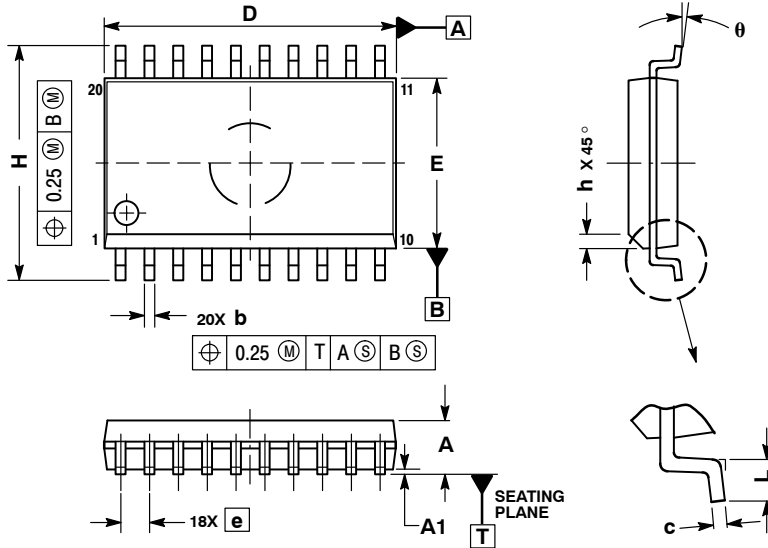
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-20 WB  
CASE 751D-05  
ISSUE H

DATE 22 APR 2015

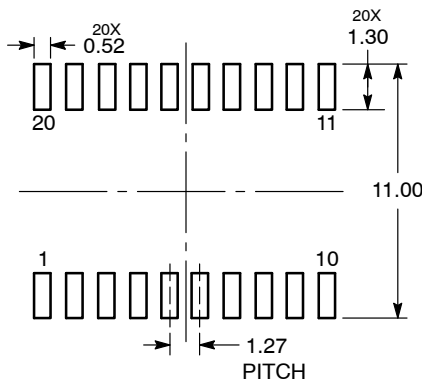


NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

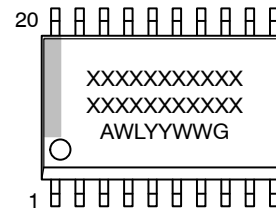
RECOMMENDED  
SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC  
MARKING DIAGRAM\*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

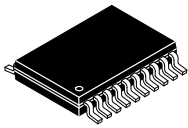
DOCUMENT NUMBER:	98ASB42343B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-20 WB	PAGE 1 OF 1

onsemi and ONSEMI are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

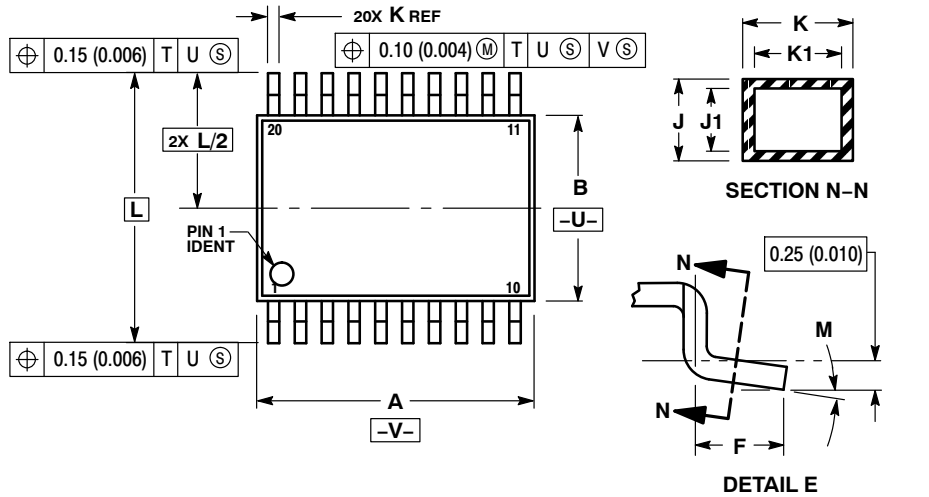
ON Semiconductor®



TSSOP-20 WB  
CASE 948E  
ISSUE D

DATE 17 FEB 2016

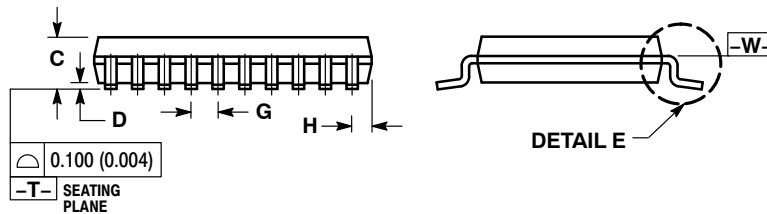
SCALE 2:1



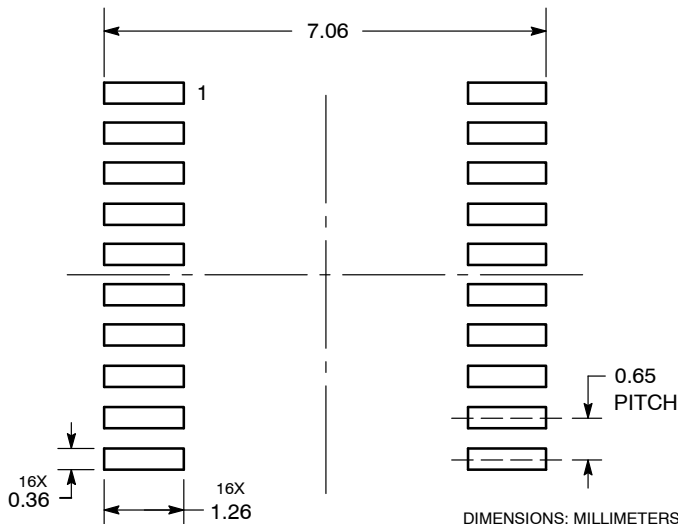
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

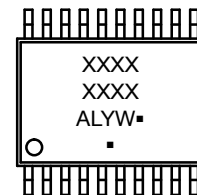
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°



SOLDERING FOOTPRINT



GENERIC MARKING DIAGRAM\*



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

DOCUMENT NUMBER:	98ASH70169A	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	TSSOP-20 WB	PAGE 1 OF 1

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## ADDITIONAL INFORMATION

### TECHNICAL PUBLICATIONS:

Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
onsemi Website: [www.onsemi.com](http://www.onsemi.com)

### ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)

For additional information, please contact your local Sales Representative at [www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)