# SNx4AHC273 Octal D-Type Flip-Flops With Clear

## 1 Features

- Operating range 2V to 5.5V $V_{CC}$
- Contain eight flip-flops with single-rail outputs
- Direct clear input
- Individual data input to each flip-flop
- Latch-up performance exceeds 250mA per JESD 17
- ESD protection exceeds JESD 22
  - 2000V human-body model (A114-A)
  - 1000V charged-device model (C101)
- On products compliant to MIL-PRF-38535, All parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

## 2 Applications

- Buffers and Storage Registers
- Shift Registers
- Pattern Generators
- Servers
- PCs and Notebooks
- Network Switches
- Memory Systems
- Databases

## 3 Description

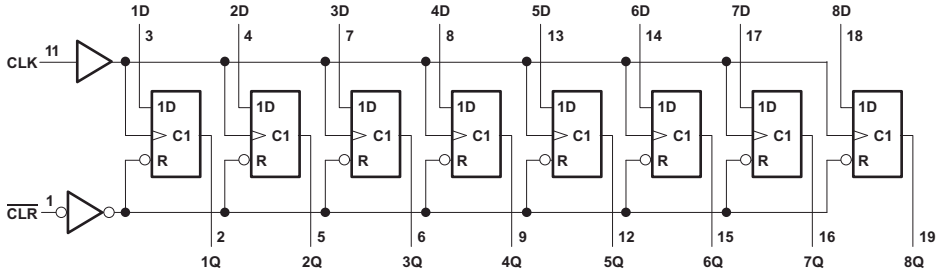
These devices are positive-edge-triggered D-type flip-flops with a direct clear ( $\overline{CLR}$) input.

Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When CLK is at either the high or low level, the D input has no effect at the output.

**Device Information**

| PART NUMBER | PACKAGE(1) | PACKAGE SIZE(2) | BODY SIZE(3) |
|---|---|---|---|
| SNx4AHC273 | N (PDIP, 20) | 24.33mm x 9.4mm | 25.40mm x 6.35mm |
| | DB (SSOP, 20) | 7.2mm × 7.8mm | 7.50mm x 5.30mm |
| | NS (SOP, 20) | 12.60mm x 7.8mm | 12.6mm x 5.30mm |
| | PW (TSSOP, 20) | 6.50mm × 6.4mm | 6.50mm x 4.40mm |
| | DGV (TVSOP, 20) | 5.00mm x 6.4mm | 5.00mm x 4.40mm |
| | DW (SOIC, 20) | 12.80mm × 10.3mm | 12.8mm x 7.5mm |

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.




**Simplified Schematics**

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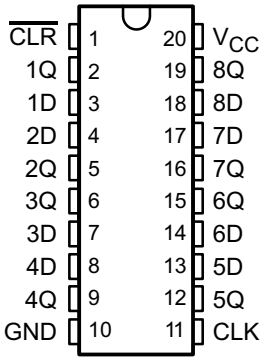
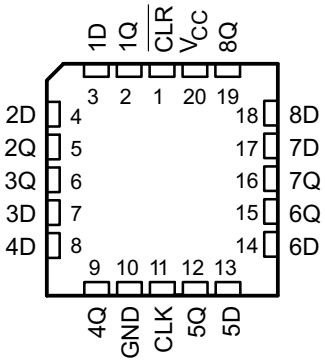
# 4 Pin Configuration and Functions

**SN54AHC273 . . . J OR W PACKAGE**
**SN74AHC273 . . . DB, DGV, DW, N, NS, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHC273 . . . FK PACKAGE**
**(TOP VIEW)**




| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | $\overline{CLR}$ | I | Clear Pin |
| 2 | 1Q | O | 1Q Output |
| 3 | 1D | I | 1D Input |
| 4 | 2D | I | 2D Input |
| 5 | 2Q | O | 2Q Output |
| 6 | 3Q | O | 3Q Output |
| 7 | 3D | I | 3D Input |
| 8 | 4D | I | 4D Input |
| 9 | 4Q | O | 4Q Output |
| 10 | GND | — | Ground Pin |
| 11 | CLK | I | Clock Pin |
| 12 | 5Q | O | 5Q Output |
| 13 | 5D | I | 5D Input |
| 14 | 6D | I | 6D Input |
| 15 | 6Q | O | 6Q Output |
| 16 | 7Q | O | 7Q Output |
| 17 | 7D | I | 7D Input |
| 18 | 8D | I | 8D Input |
| 19 | 8Q | O | 8Q Output |
| 20 | VCC | — | Power Pin |

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | –0.5 | 7 | V |
| $V_I$ | Input voltage range(2) | | –0.5 | 7 | V |
| $V_O$ | Output voltage range(2) | | –0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | $V_I$ < 0 | | –20 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < 0 or $V_O$ > $V_{CC}$ | | ±20 | mA |
| $I_O$ | Continuous output current | $V_O$ = 0 to $V_{CC}$ | | ±25 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±75 | mA |
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | ±2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

| | | | SN54AHC273 | | SN74AHC273 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | 1.5 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | | 0.5 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | | 1.65 | |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | | –50 | µA |
| | | $V_{CC}$ = 3 V ± 0.3 V | | –4 | | –4 | mA |
| | | $V_{CC}$ = 5.5 V ± 0.5 V | | –8 | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | | 50 | µA |
| | | $V_{CC}$ = 3 V ± 0.3 V | | 4 | | 4 | mA |
| | | $V_{CC}$ = 5.5 V ± 0.5 V | | 8 | | 8 | |
| Δt/Δv | Input transition rise and fall time | $V_{CC}$ = 3 V ± 0.3 V | | 100 | | 100 | ns/V |
| | | $V_{CC}$ = 5.5 V ± 0.5 V | | 20 | | 20 | |

over operating free-air temperature range (unless otherwise noted)(1)

| | | SN54AHC273 | | SN74AHC273 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 125 | °C |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, (SCBA004).

## 5.4 Thermal Information

| THERMAL METRIC(1) | | SN74AHC273 | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | N | DW | NS | DB | PW | DGV | |
| | | 20 PINS | | | | | | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 53.9 | 81.1 | 79.4 | 98.7 | 116.8 | 118.1 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 38.8 | 48.9 | 45.9 | 60.4 | 58.5 | 33.4 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 34.7 | 53.8 | 46.9 | 56.9 | 78.7 | 59.6 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 26.9 | 19.5 | 19.1 | 21.6 | 12.6 | 1.1 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 34.7 | 53.1 | 46.5 | 53.5 | 77.9 | 58.9 | |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | N/A | N/A | N/A | N/A | |

(1) For more information about traditional and new thermal metrics, see the TI application report *IC Package Thermal Metrics* (SPRA953).

## 5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHC273 | | SN74AHC273 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 µA | 2 V | 1.9 | | | 1.9 | | 1.9 | | V |
| | | 3 V | 2.9 | | | 2.9 | | 2.9 | | |
| | | 4.5 V | 4.4 | | | 4.4 | | 4.4 | | |
| | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | 2.48 | | |
| | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 µA | 2 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | 3 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.5 | | 0.44 | |
| | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| $I_I$ | $V_I$ = 5.5 V or GND | 0 to 5.5 V | | | ±0.1 | | ±1(1) | | ±1 | µA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | µA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 2.5 | 10 | | | | 10 | pF |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at $V_{CC}$ = 0 V.

## 5.6 Timing Requirements, $V_{CC}$ = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

| | | | SN54AHC273 | | | SN74AHC273 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | $T_A$ = 25°C | | MIN MAX | $T_A$ = 25°C | | MIN MAX | |
| | | | MIN | MAX | | MIN | MAX | | |
| $t_w$ | Pulse Duration | $\overline{CLR}$ low | 5 | | 6 | 5 | | 6 | ns |
| | | CLK high or low | 5 | | 6.5 | 5 | | 6.5 | |

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

| | | | SN54AHC273 | | | SN74AHC273 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | $T_A$ = 25°C | | MIN MAX | $T_A$ = 25°C | | MIN MAX | |
| | | | MIN | MAX | | MIN | MAX | | |
| $t_{su}$ | Setup time | Data before CLK↑ | 5.5 | | 6.5 | 5.5 | | 6.5 | ns |
| | | CLR before CLK↑ | 2.5 | | 2.5 | 2.5 | | 2.5 | |
| $t_h$ | Hold time, data after CLK↑ | | 1.5 | | 2 | 1 | | 1 | ns |

## 5.7 Timing Requirements, $V_{CC}$ = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

| | | | SN54AHC273 | | | SN74AHC273 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | $T_A$ = 25°C | | MIN MAX | $T_A$ = 25°C | | MIN MAX | |
| | | | MIN | MAX | | MIN | MAX | | |
| $t_w$ | Pulse Duration | $\overline{CLR}$ low | 5 | | 5 | 5 | | 5 | ns |
| | | CLK high or low | 5 | | 5 | 5 | | 5 | |
| $t_{su}$ | Setup time | Data before CLK↑ | 4.5 | | 4.5 | 4.5 | | 4.5 | ns |
| | | CLR before CLK↑ | 2 | | 2 | 2 | | 2 | |
| $t_h$ | Hold time, data after CLK↑ | | 1.5 | | 2 | 1 | | 1 | ns |

## 5.8 Switching Characteristics, $V_{CC}$ = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN54AHC273 | | SN74AHC273 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | $C_L$ = 15 pF | 75[1] | 120[1] | | 65[1] | | 65 | | MHz |
| | | | $C_L$ = 50 pF | 50 | 75 | | 45 | | 45 | | |
| $t_{PHL}$ | $\overline{CLR}$ | Q | $C_L$ = 15 pF | | 8.9[1] | 13.6[1] | 1[1] | 16[1] | 1 | 16 | ns |
| $t_{PLH}$ | CKL | Q | $C_L$ = 15 pF | | 8.7[1] | 13.6[1] | 1[1] | 16[1] | 1 | 16 | ns |
| $t_{PHL}$ | | | | | 8.7[1] | 13.6[1] | 1[1] | 16[1] | 1 | 16 | |
| $t_{PHL}$ | $\overline{CLR}$ | Q | $C_L$ = 50 pF | | 11.4 | 17.1 | 1 | 19.5 | 1 | 19.5 | ns |
| $t_{PLH}$ | CLK | Q | $C_L$ = 50 pF | | 11.2 | 17.1 | 1 | 19.5 | 1 | 19.5 | ns |
| $t_{PHL}$ | | | | | 11.2 | 17.1 | 1 | 19.5 | 1 | 19.5 | ns |
| $t_{sk(o)}$ | | | $C_L$ = 50 pF | | | 1.5[2] | | | | 1.5 | ns |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

## 5.9 Switching Characteristics, $V_{CC}$ = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN54AHC273 | | SN74AHC273 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | $C_L$ = 15 pF | 120[1] | 165[1] | | 100[1] | | 100 | | MHz |
| | | | $C_L$ = 50 pF | 80 | 110 | | 70 | | 70 | | |
| $t_{PHL}$ | $\overline{CLR}$ | Q | $C_L$ = 15 pF | | 5.2[1] | 8.5[1] | 1[1] | 10[1] | 1 | 10 | ns |
| $t_{PLH}$ | CKL | Q | $C_L$ = 15 pF | | 5.8[1] | 9[1] | 1[1] | 10.5[1] | 1 | 10.5 | ns |
| $t_{PHL}$ | | | | | 5.8[1] | 9[1] | 1[1] | 10.5[1] | 1 | 10.5 | |
| $t_{PHL}$ | $\overline{CLR}$ | Q | $C_L$ = 50 pF | | 6.7 | 10.5 | 1 | 12 | 1 | 12 | ns |
| $t_{PLH}$ | CLK | Q | $C_L$ = 50 pF | | 7.3 | 11 | 1 | 12.5 | 1 | 12.5 | ns |
| $t_{PHL}$ | | | | | 7.3 | 11 | 1 | 12.5 | 1 | 12.5 | ns |

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN54AHC273 | | SN74AHC273 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{sk(o)}$ | | | $C_L$ = 50 pF | | | 1(2) | | | | 1 | ns |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

## 5.10 Noise Characteristics

$V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C

| PARAMETER | | SN74AHC273 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.7 | | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.7 | | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | 4.7 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 3.5 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 1.5 | V |

## 5.11 Operating Characteristics

$T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 31 | pF |

## 5.12 Typical Characteristics

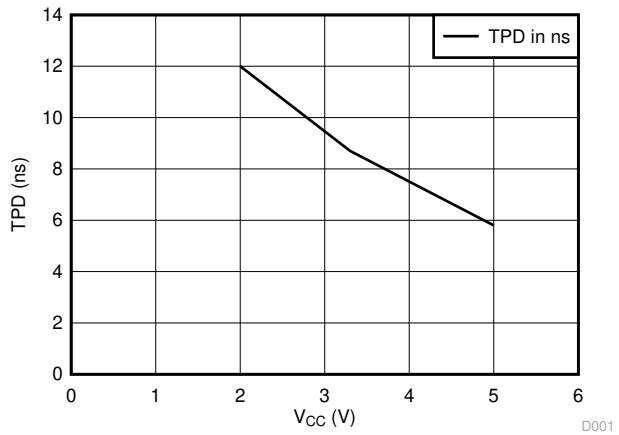



Figure 5-1. TPD vs $V_{CC}$

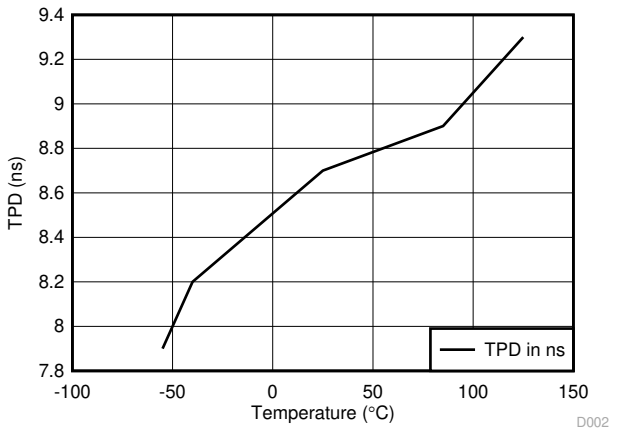
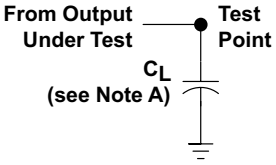
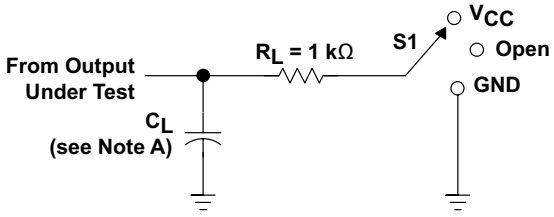



Figure 5-2. TPD vs Temperature

## 6 Parameter Measurement Information

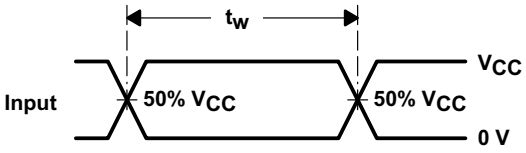



LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

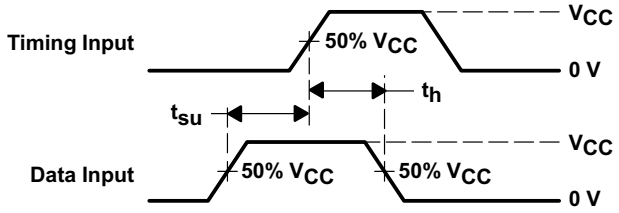



LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

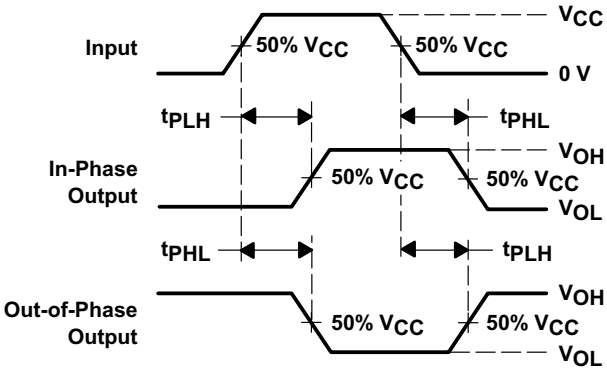
| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |
| Open Drain | $V_{CC}$ |



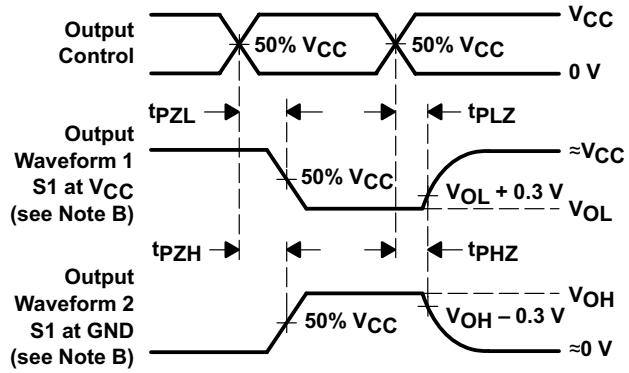

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 3 ns, $t_f$ ≤ 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

**Figure 6-1. Load Circuit and Voltage Waveforms**

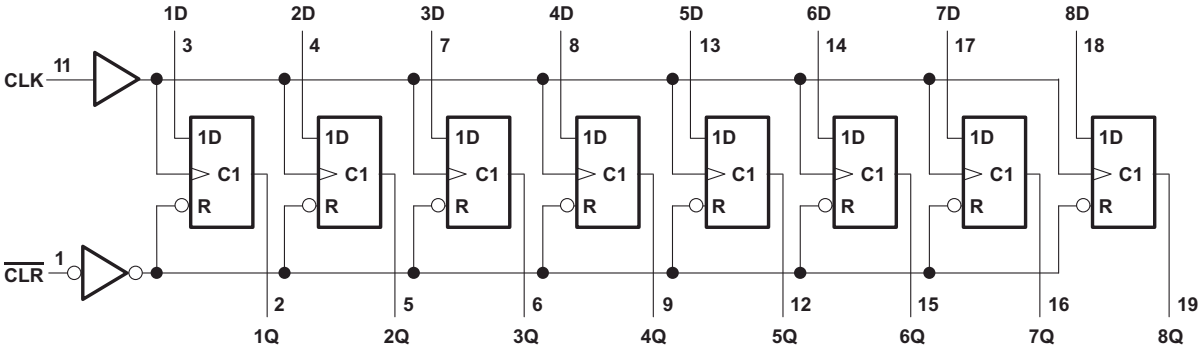
# 7 Detailed Description

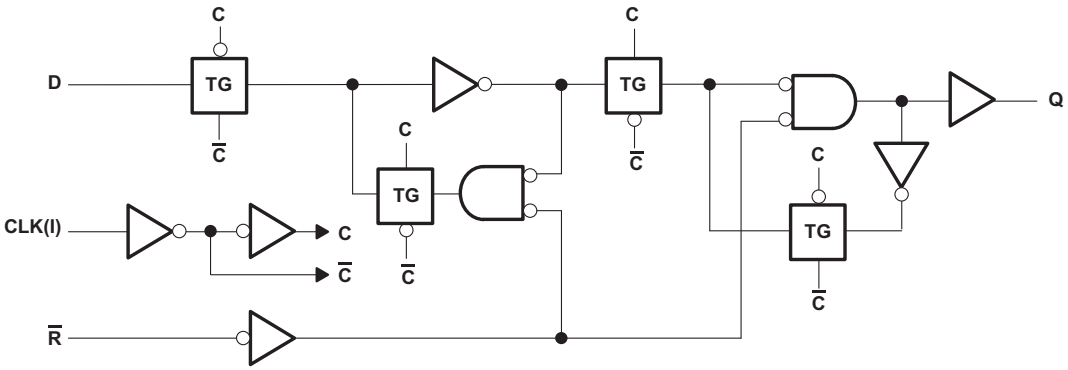
## 7.1 Overview

These circuits are positive-edge-triggered D-type flip-flops with a direct clear ( $\overline{CLR}$) input. Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When CLK is at either the high or low level, the D input has no effect at the output.

The inputs are 5 V tolerant and can be driven from 5-V devices. This feature allows the use of these devices as down translators in a mixed 5-V to 3.3-V system environment.

## 7.2 Functional Block Diagrams




## 7.3 Feature Description

- Wide operating voltage range
  - Operates from 2 V to 5.5 V
- Allows down voltage translation
  - Inputs accept voltages to 5.5 V
- Slow edge rates minimize output ringing

## 7.4 Device Functional Modes

**Table 7-1. Function Table**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{CLR}$ | CLK | D | Y |
| L | X | X | L |
| H | ↑ | H | H |
| H | ↑ | L | L |
| H | L | X | $Q_0$ |

# 8 Application and Implementation

## 8.1 Application Information

The SNx4AHC273 is a low-drive CMOS device that can be used for a multitude of applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs are tolerant to 5.5 V at any valid $V_{CC}$. This feature makes the device ideal for translating down to the $V_{CC}$ level. Figure 8-2 shows the reduction in ringing compared to higher drive parts such as AC.

## 8.2 Typical Application

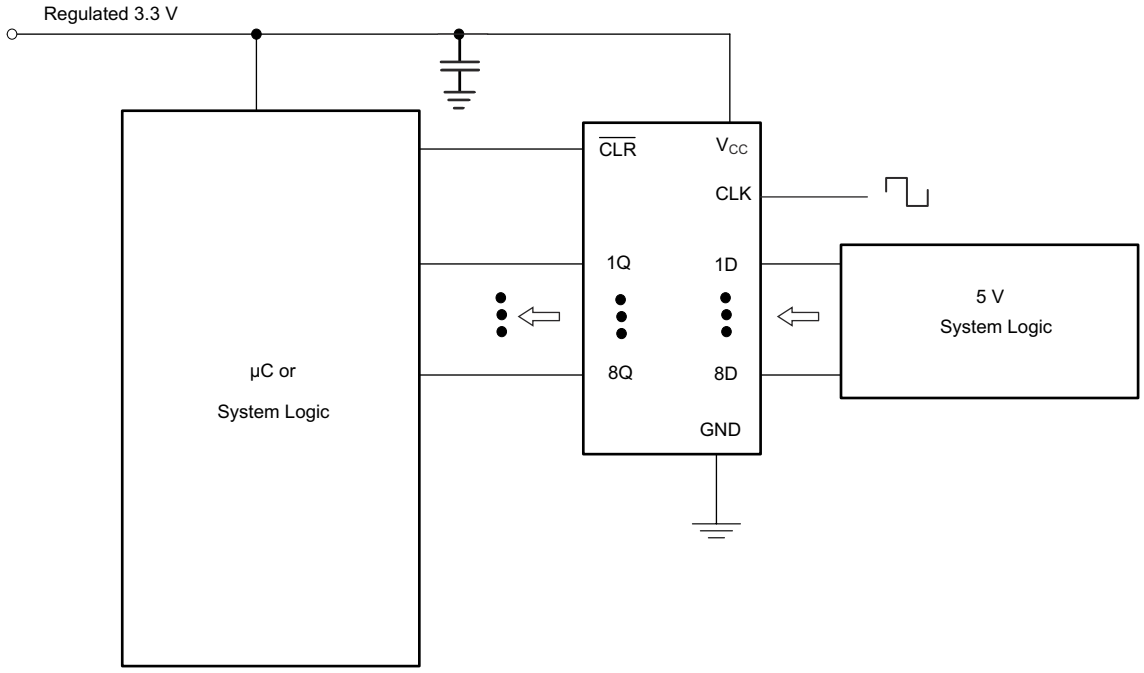



**Figure 8-1. Specific Application Schematic**

### *8.2.1 Design Requirements*

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

### *8.2.2 Detailed Design Procedure*

1. Recommended input conditions
   - Rise time and fall time specs: See (Δt/ΔV) in the *Section 5.3* table.
   - Specified High and low levels: See ($V_{IH}$ and $V_{IL}$) in the *Section 5.3* table.
   - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid $V_{CC}$
2. Recommend output conditions
   - Load currents should not exceed 25 mA per output and 75 mA total for the part
   - Outputs should not be pulled above $V_{CC}$

### 8.2.3 Application Curves

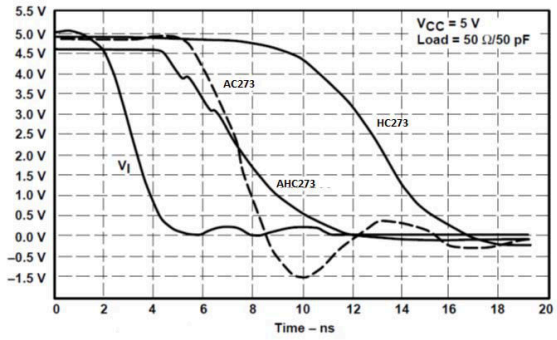



**Figure 8-2. Switching Characteristics Comparison**

## 8.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Recommended Operating Conditions* table.

Each VCC pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 µf is recommended; if there are multiple VCC pins, then 0.01 µf or 0.022 µf is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 µf and a 1 µf are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

## 8.4 Layout

### 8.4.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified in Figure 8-3 are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally inputs will be tied to GND or $V_{CC}$, whichever makes more sense or is more convenient. It is generally acceptable to float outputs unless the part is a transceiver.

### 8.4.2 Layout Example

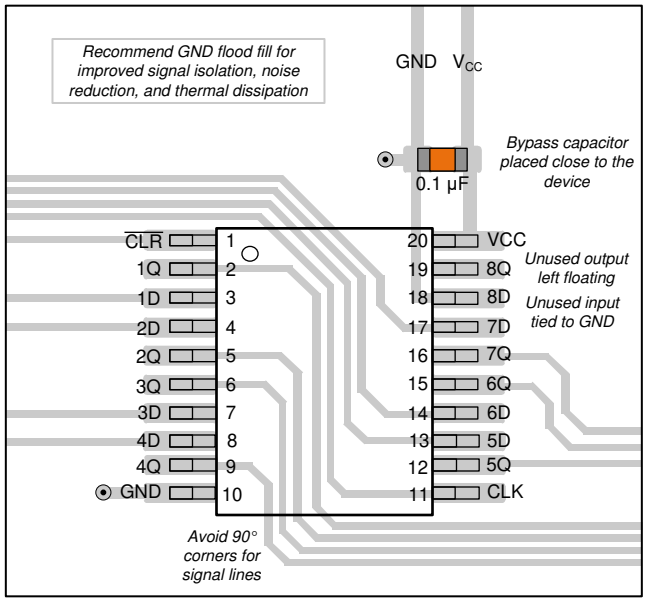



**Figure 8-3. Layout Diagram**

# 9 Device and Documentation Support

## 9.1 Documentation Support

### *9.1.1 Related Links*

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 9-1. Related Links**

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| SN54AHC273 | Click here | Click here | Click here | Click here | Click here |
| SN74AHC273 | Click here | Click here | Click here | Click here | Click here |

## 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

# 10 Revision History

| Changes from Revision I (March 2015) to Revision J (July 2024) | Page |
|---|---|
| • Added NS package to *Device Information* table | 1 |
| • Updated RθJA values: PW = 104.7 to 116.8, DW = 81.8 to 81.1; Updated PW and DW packages for RθJC(top), RθJB, ΨJT, ΨJB, and RθJC(bot), all values in °C/W | 5 |
| • Updated *Layout Example* image | 12 |

| Changes from Revision H (July 2014) to Revision I (March 2015) | Page |
|---|---|
| • Changed $I_{OH}$ test conditions for $V_{OH}$ from mA to µA to fix typographical error. | 5 |

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 5962-9853001Q2A | ACTIVE | LCCC | FK | 20 | 55 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9853001Q2A SNJ54AHC 273FK | Samples |
| 5962-9853001QRA | ACTIVE | CDIP | J | 20 | 20 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9853001QRA SNJ54AHC273J | Samples |
| 5962-9853001QSA | ACTIVE | CFP | W | 20 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9853001QSA SNJ54AHC273W | Samples |
| SN74AHC273DBR | ACTIVE | SSOP | DB | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HA273 | Samples |
| SN74AHC273DGVR | ACTIVE | TVSOP | DGV | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HA273 | Samples |
| SN74AHC273DW | OBSOLETE | SOIC | DW | 20 | | TBD | Call TI | Call TI | -40 to 125 | AHC273 | |
| SN74AHC273DWR | ACTIVE | SOIC | DW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHC273 | Samples |
| SN74AHC273N | ACTIVE | PDIP | N | 20 | 20 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 125 | SN74AHC273N | Samples |
| SN74AHC273NSR | ACTIVE | SOP | NS | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHC273 | Samples |
| SN74AHC273PW | OBSOLETE | TSSOP | PW | 20 | | TBD | Call TI | Call TI | -40 to 125 | HA273 | |
| SN74AHC273PWR | ACTIVE | TSSOP | PW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HA273 | Samples |
| SNJ54AHC273FK | ACTIVE | LCCC | FK | 20 | 55 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9853001Q2A SNJ54AHC 273FK | Samples |
| SNJ54AHC273J | ACTIVE | CDIP | J | 20 | 20 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9853001QRA SNJ54AHC273J | Samples |
| SNJ54AHC273W | ACTIVE | CFP | W | 20 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9853001QSA SNJ54AHC273W | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.



**OTHER QUALIFIED VERSIONS OF SN54AHC273, SN74AHC273 :**

- Catalog : SN74AHC273
- Military : SN54AHC273

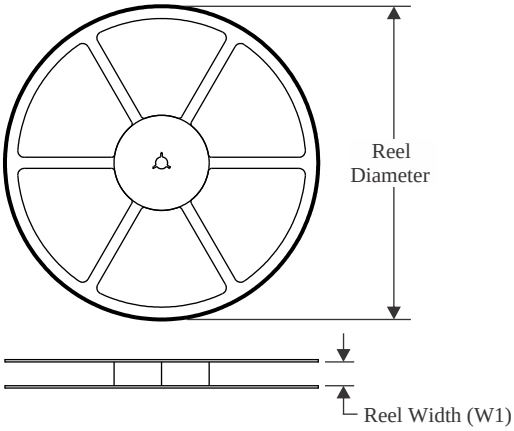
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

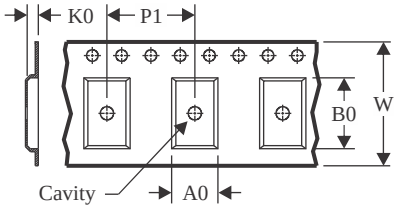
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

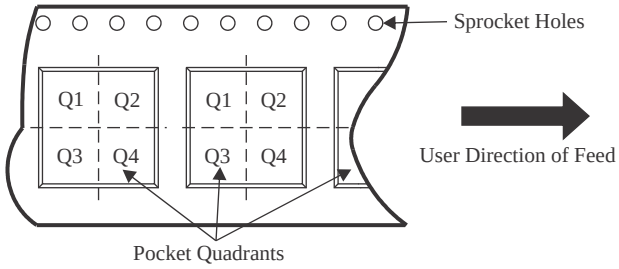



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

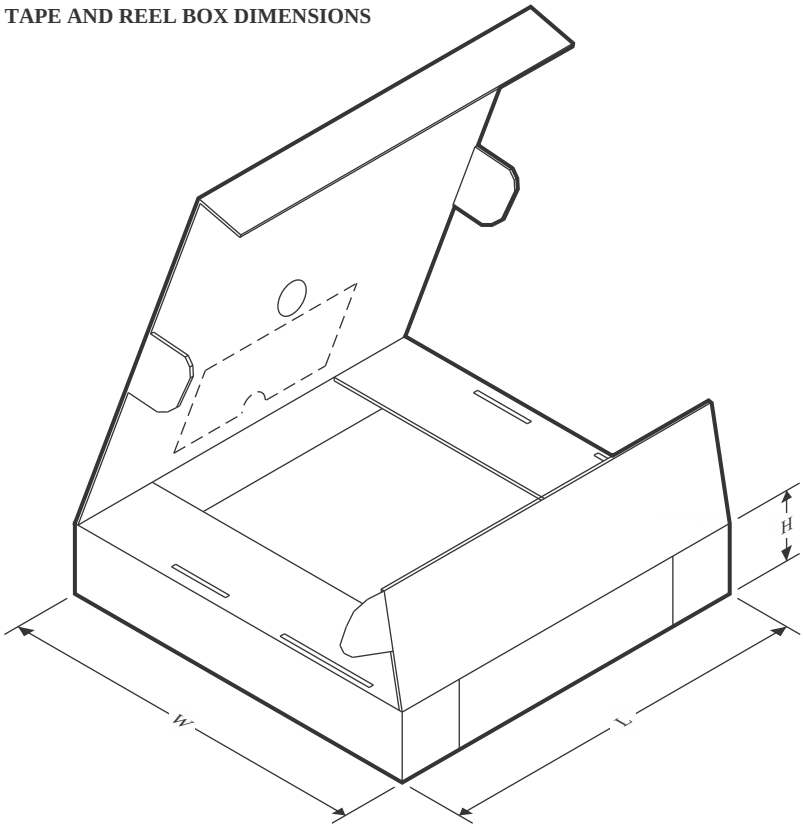
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74AHC273DBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74AHC273DGVR | TVSOP | DGV | 20 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74AHC273DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.9 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74AHC273NSR | SOP | NS | 20 | 2000 | 330.0 | 24.4 | 8.4 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |
| SN74AHC273PWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |

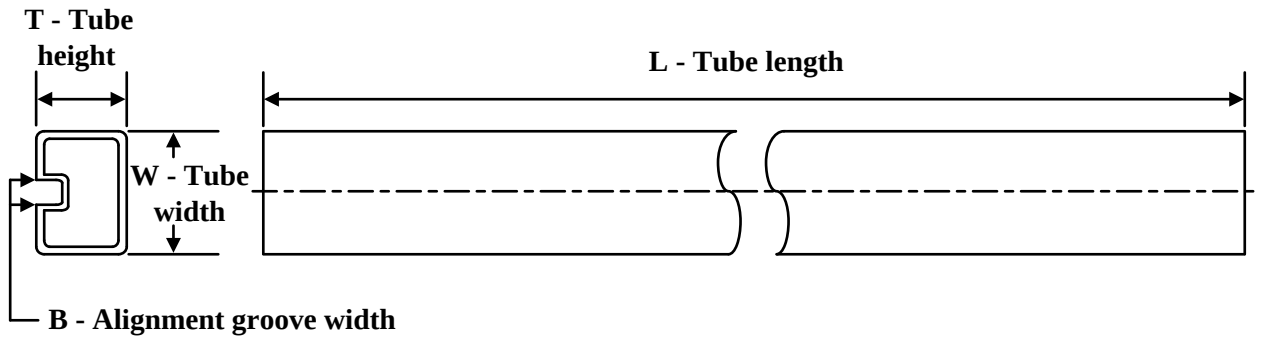
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74AHC273DBR | SSOP | DB | 20 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74AHC273DGVR | TVSOP | DGV | 20 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74AHC273DWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74AHC273NSR | SOP | NS | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74AHC273PWR | TSSOP | PW | 20 | 2000 | 356.0 | 356.0 | 35.0 |

## TUBE



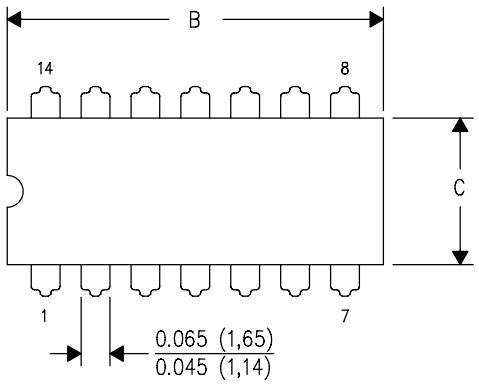

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| 5962-9853001Q2A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| 5962-9853001QSA | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |
| SN74AHC273N | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SNJ54AHC273FK | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SNJ54AHC273W | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |

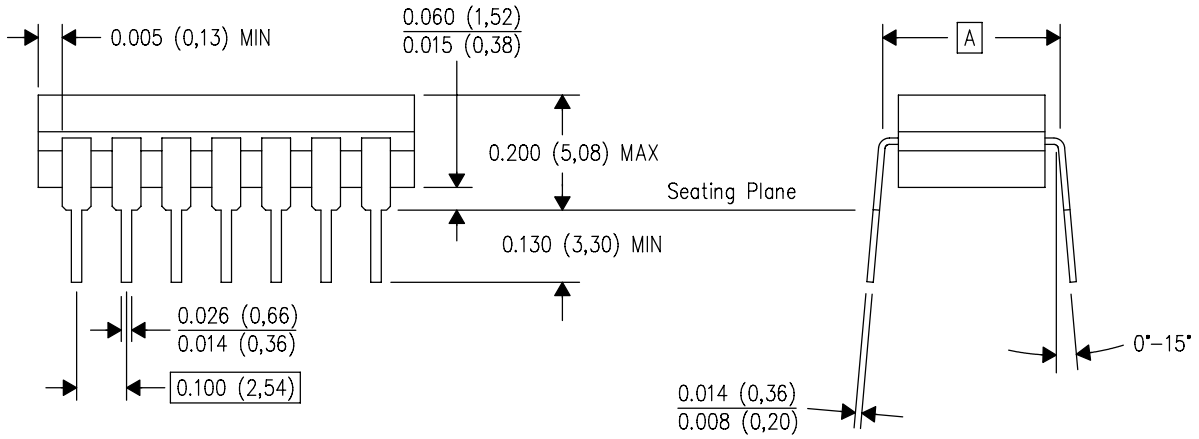
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |

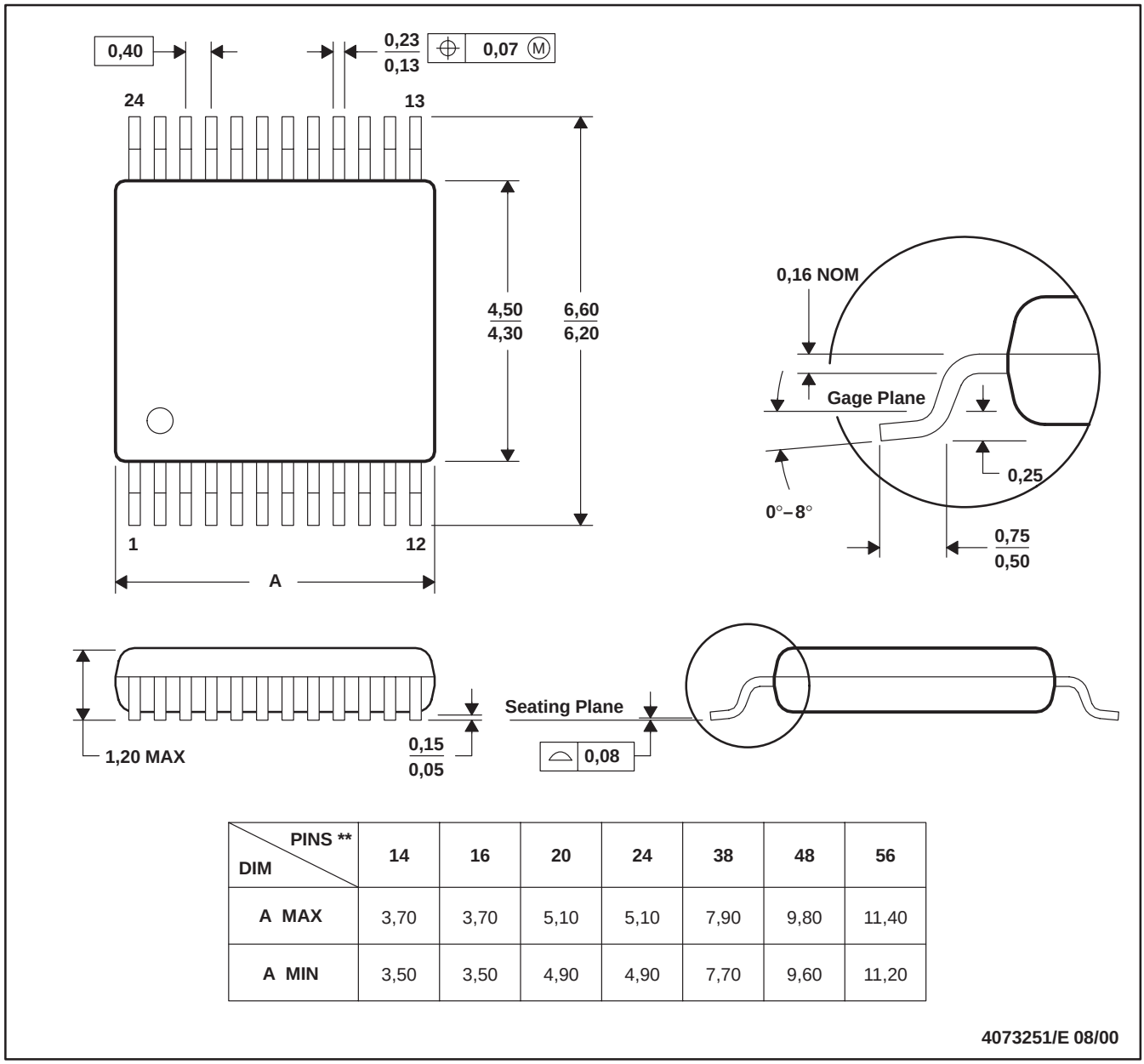



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

**DGV (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**24 PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 | 38 | 48 | 56 |
|---|---|---|---|---|---|---|---|
| A MAX | 3,70 | 3,70 | 5,10 | 5,10 | 7,90 | 9,80 | 11,40 |
| A MIN | 3,50 | 3,50 | 4,90 | 4,90 | 7,70 | 9,60 | 11,20 |

**4073251/E 08/00**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

# GENERIC PACKAGE VIEW

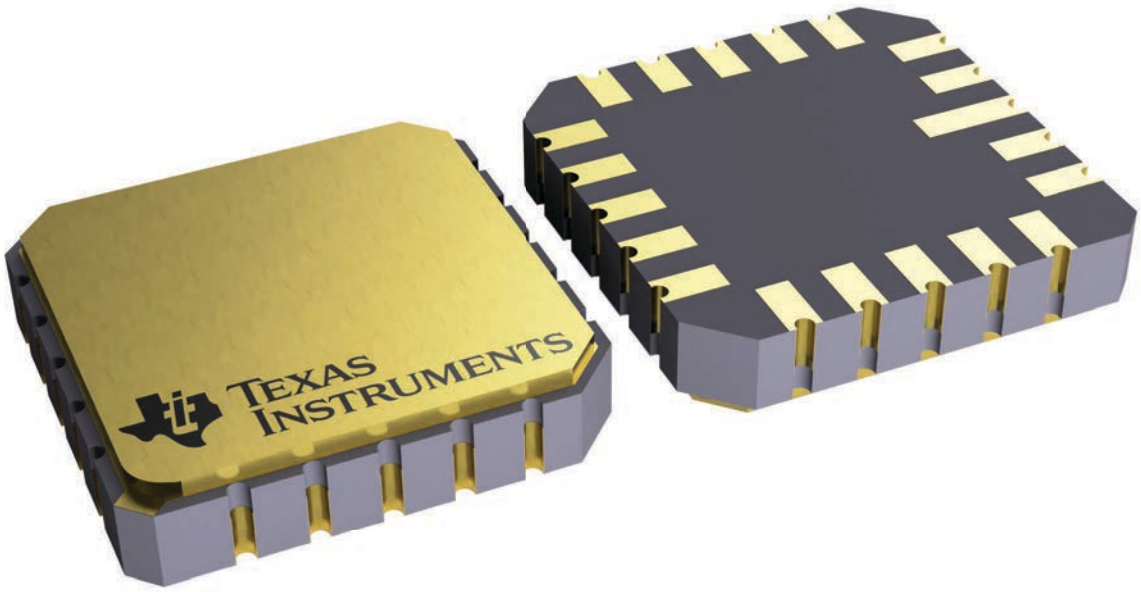
## FK 20

## LCCC - 2.03 mm max height

**8.89 x 8.89, 1.27 mm pitch**

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

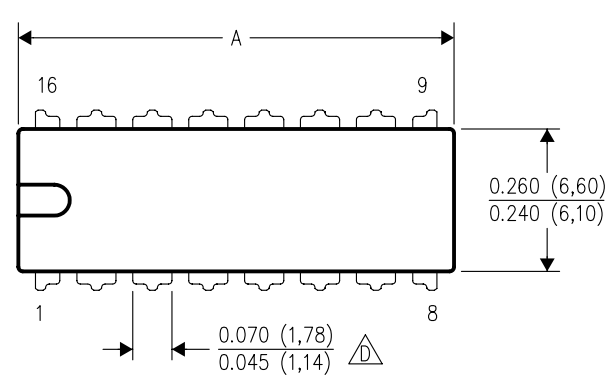



4229370VA\

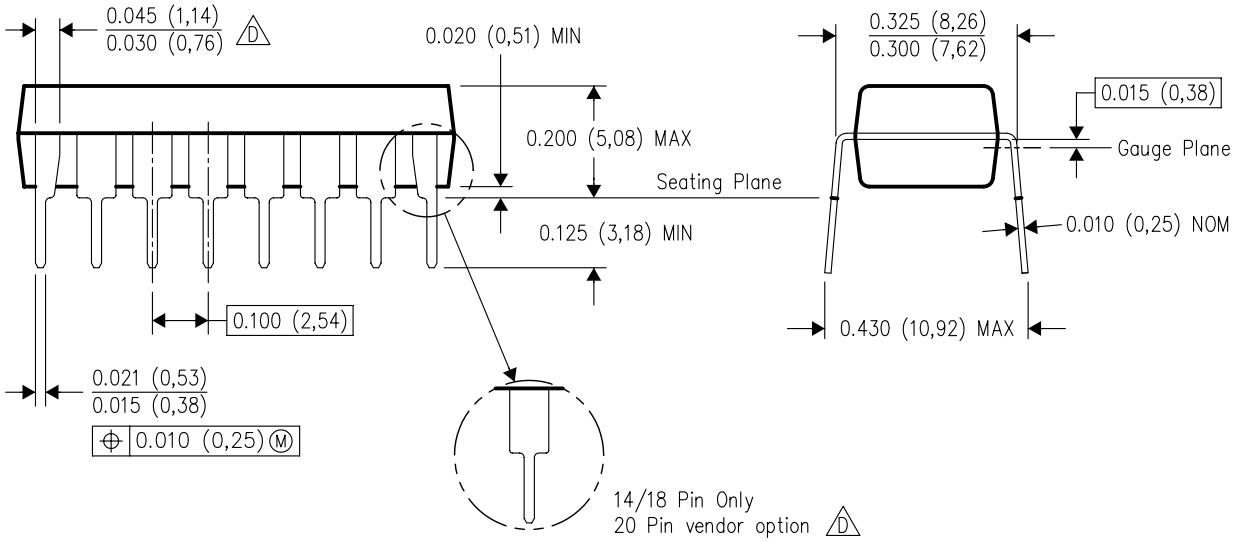
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

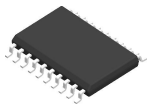



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

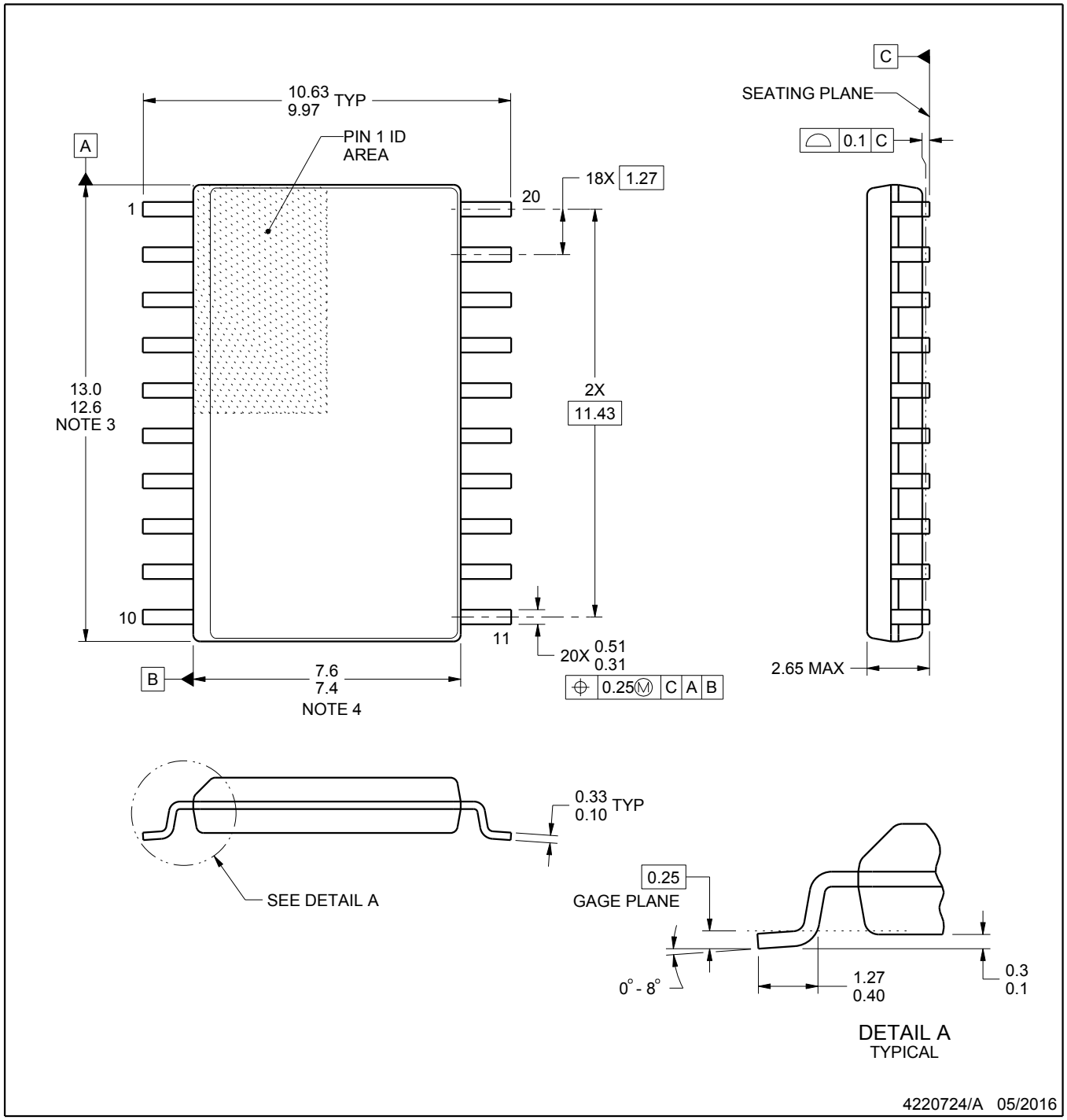


# PACKAGE OUTLINE

## DW0020A

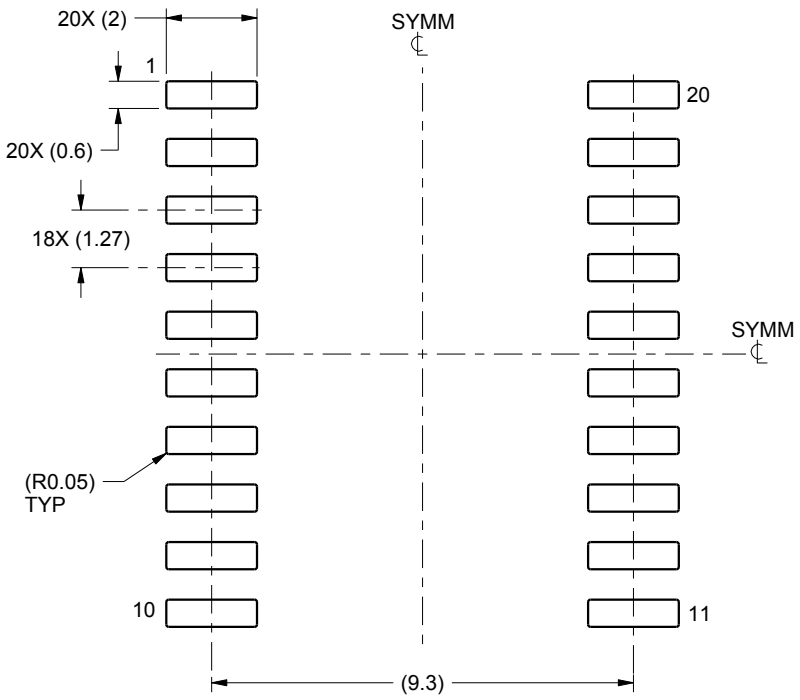
## SOIC - 2.65 mm max height

SOIC

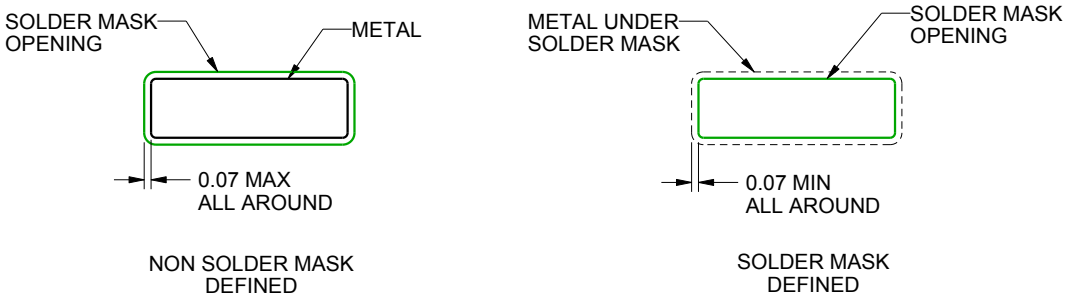



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.




LAND PATTERN EXAMPLE
SCALE:6X

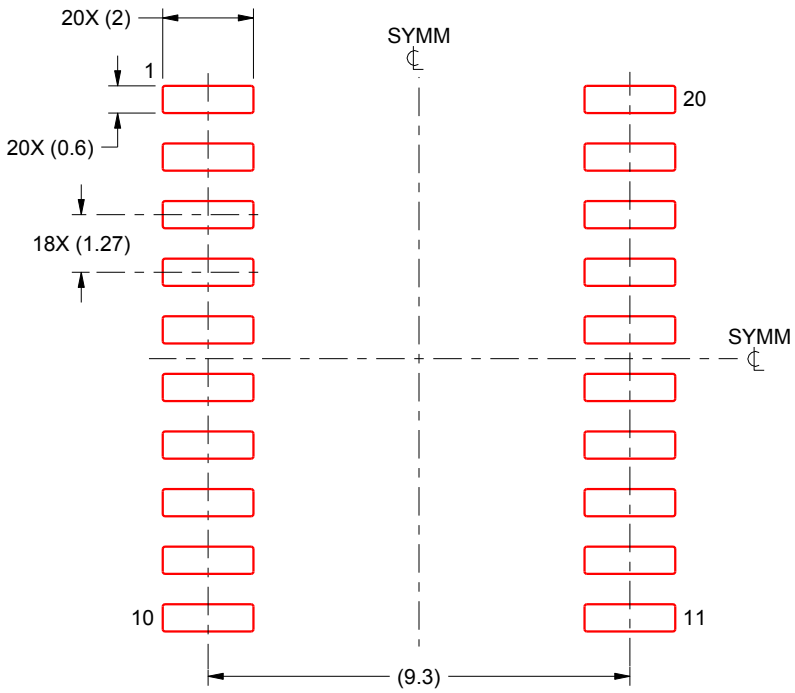



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



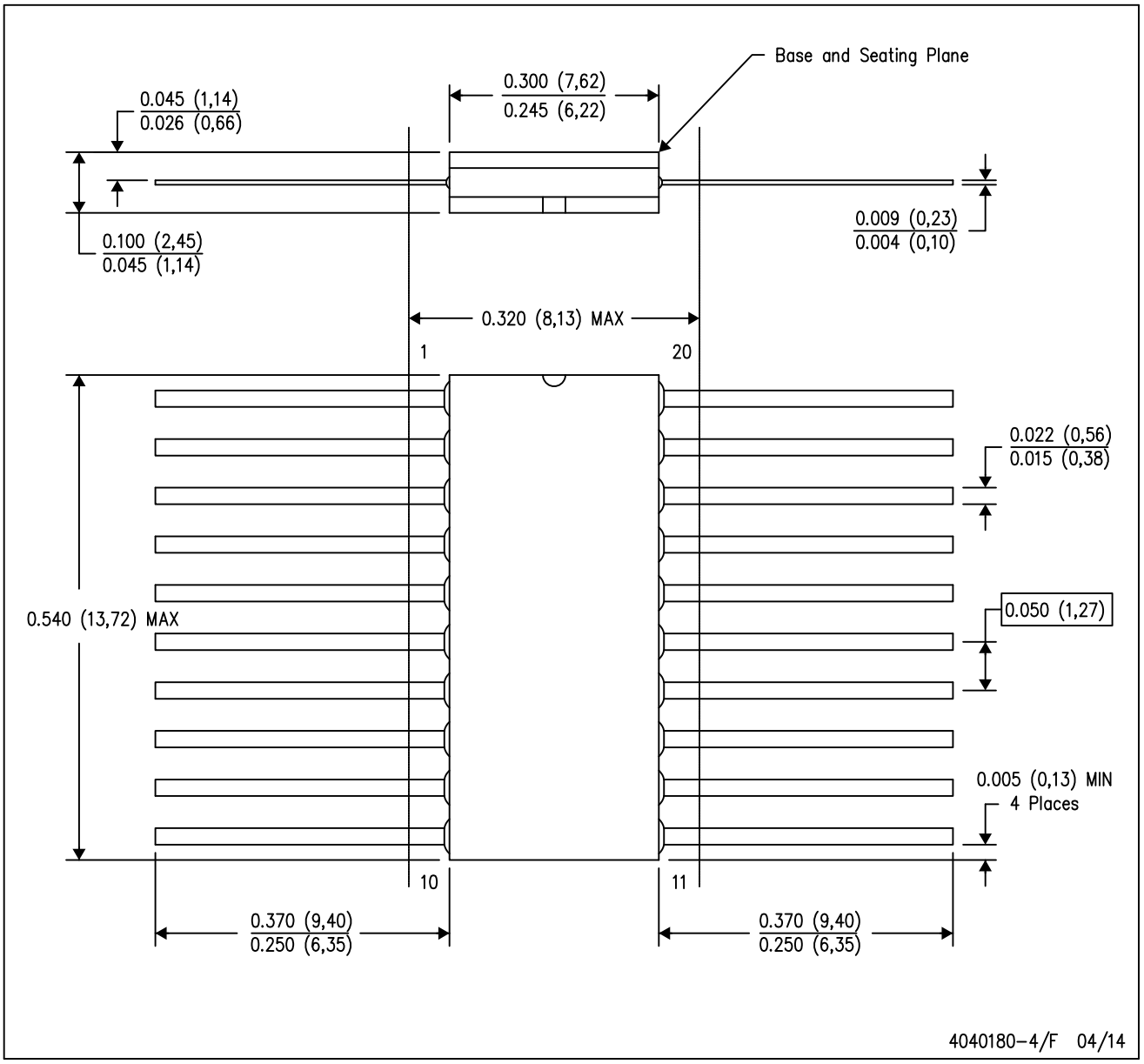

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R–GDFP–F20) CERAMIC DUAL FLATPACK



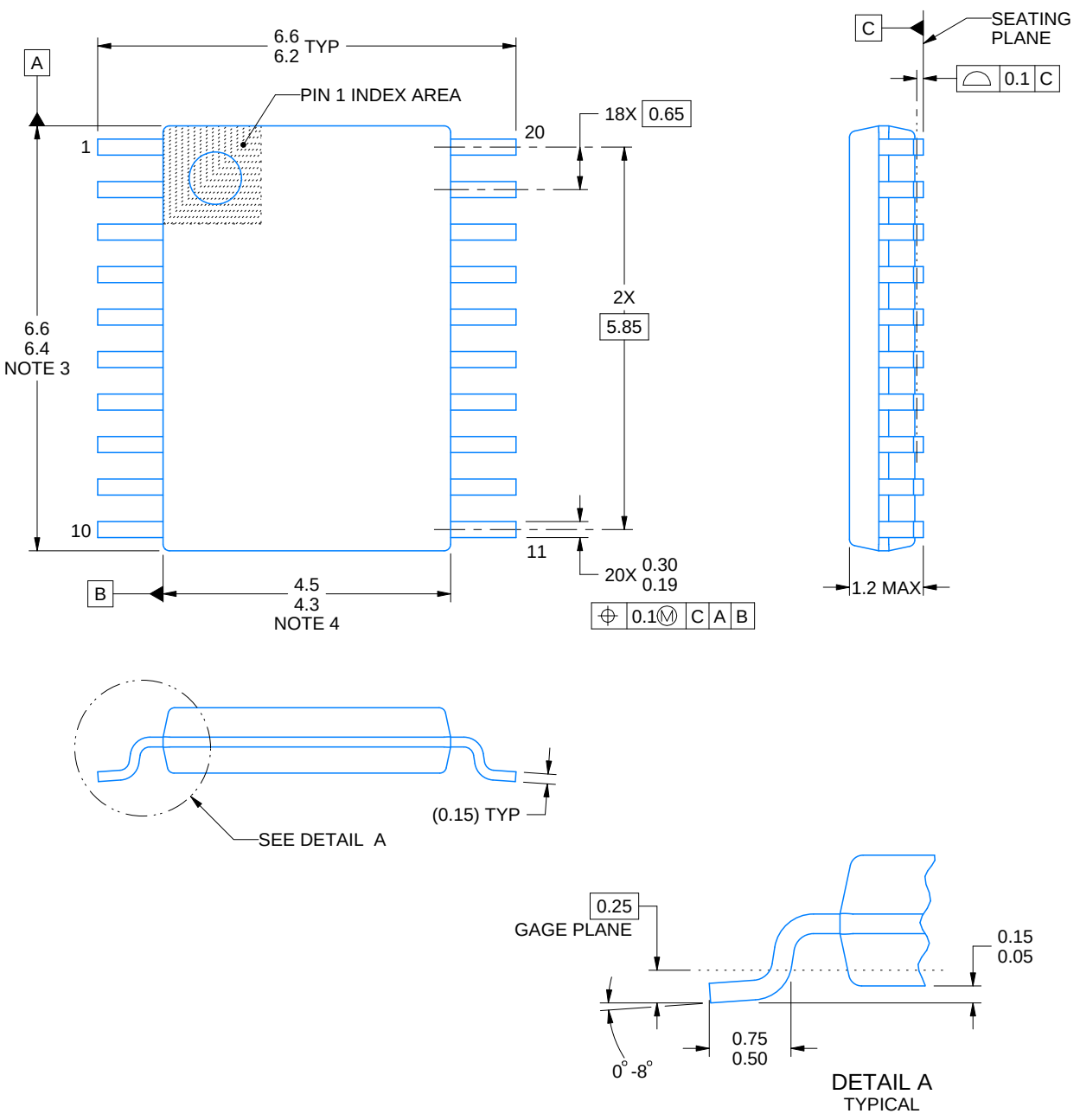

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil–Std 1835 GDFP2–F20

# PACKAGE OUTLINE

## PW0020A

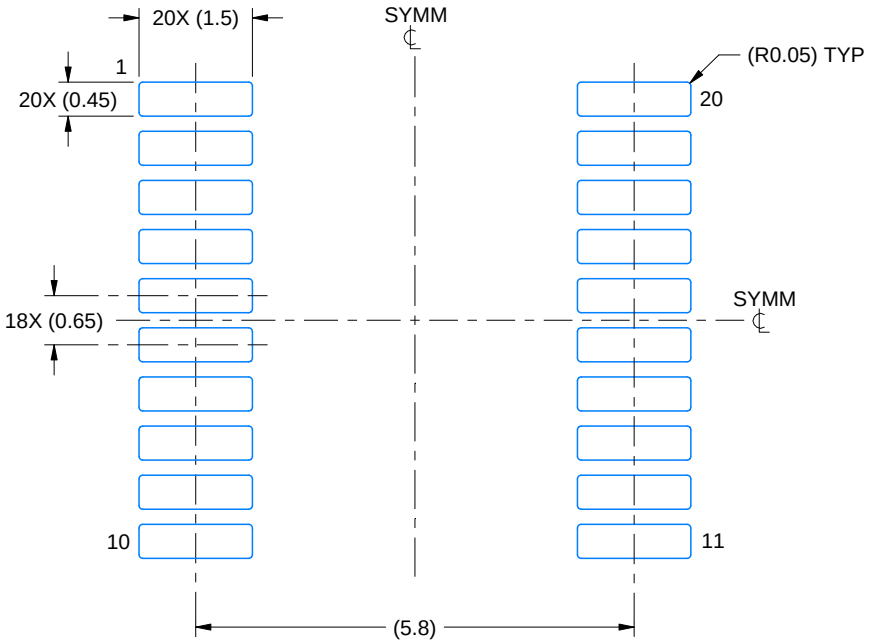
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE




NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



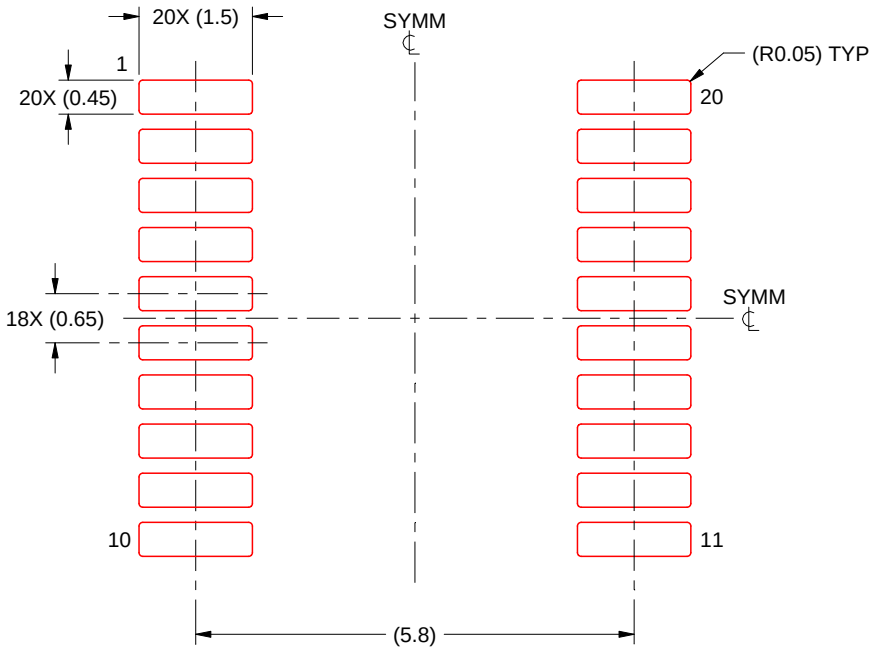

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X


SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

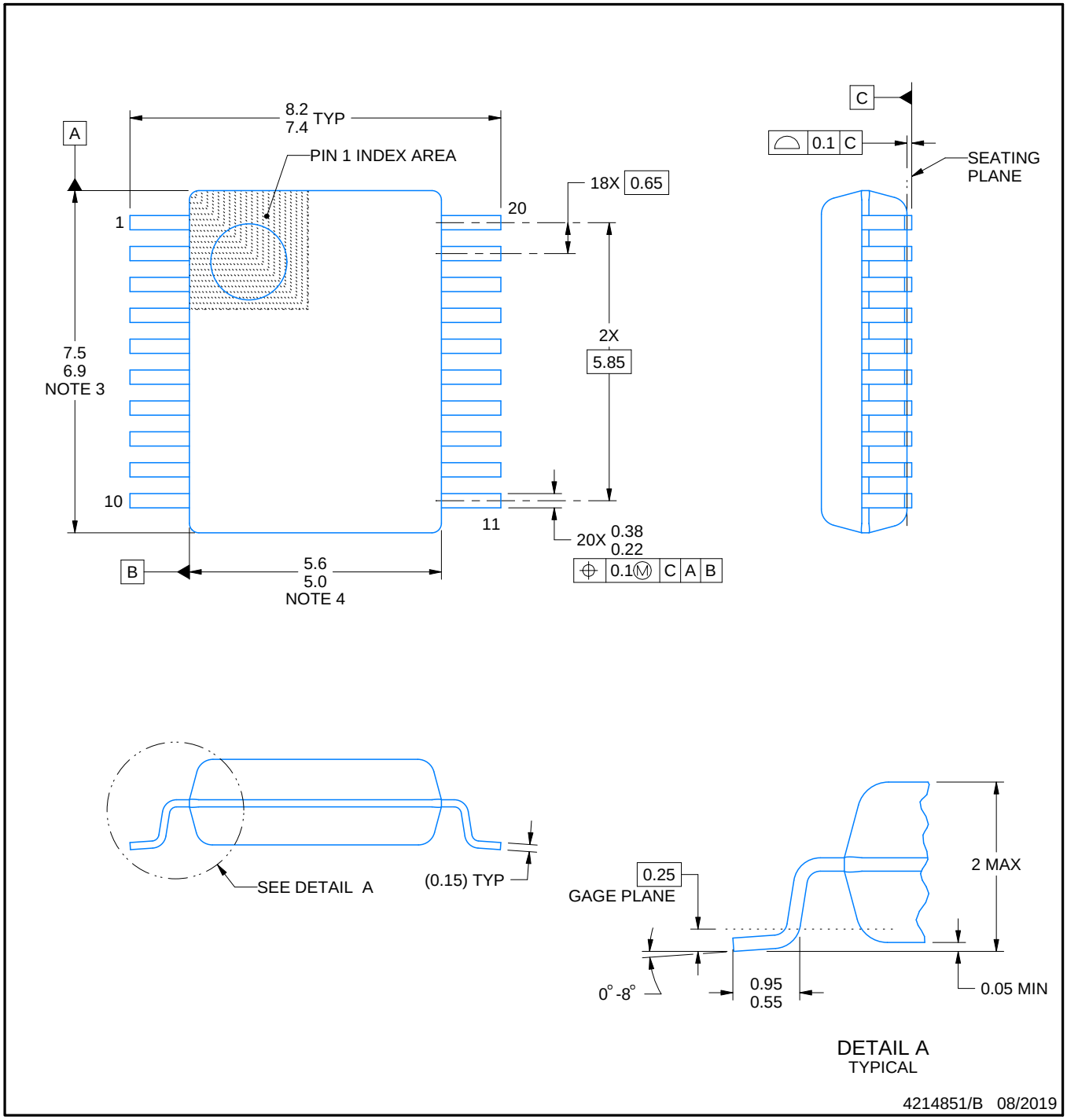
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## DB0020A

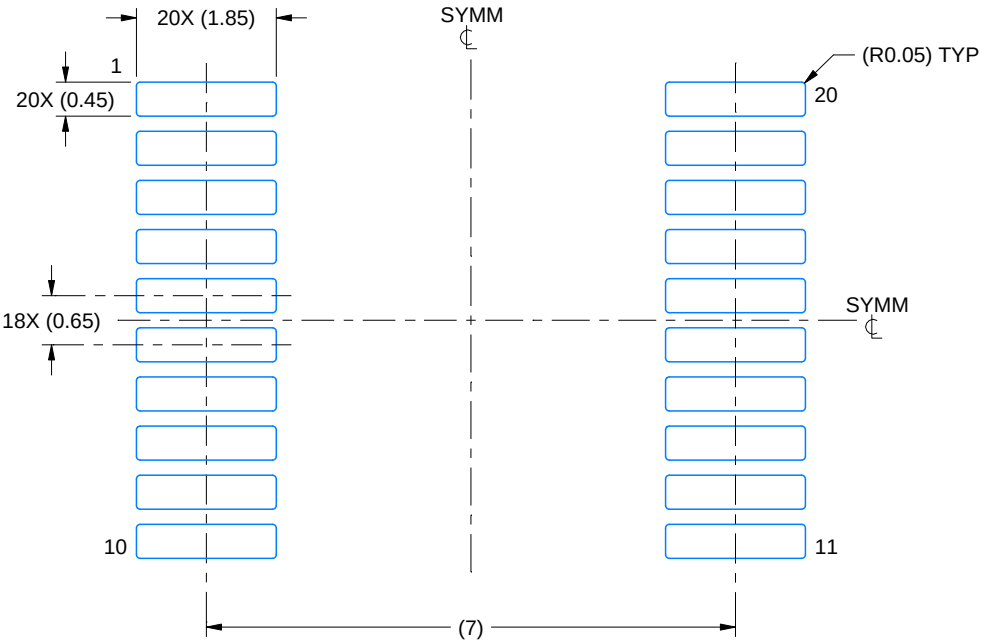
## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

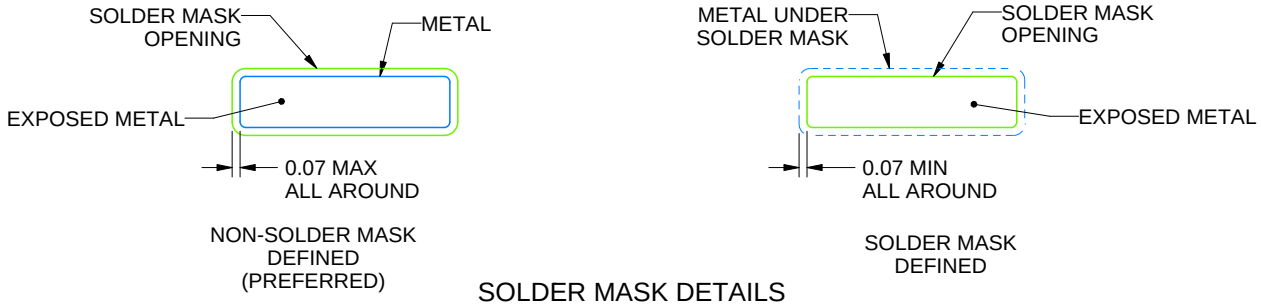



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X




SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

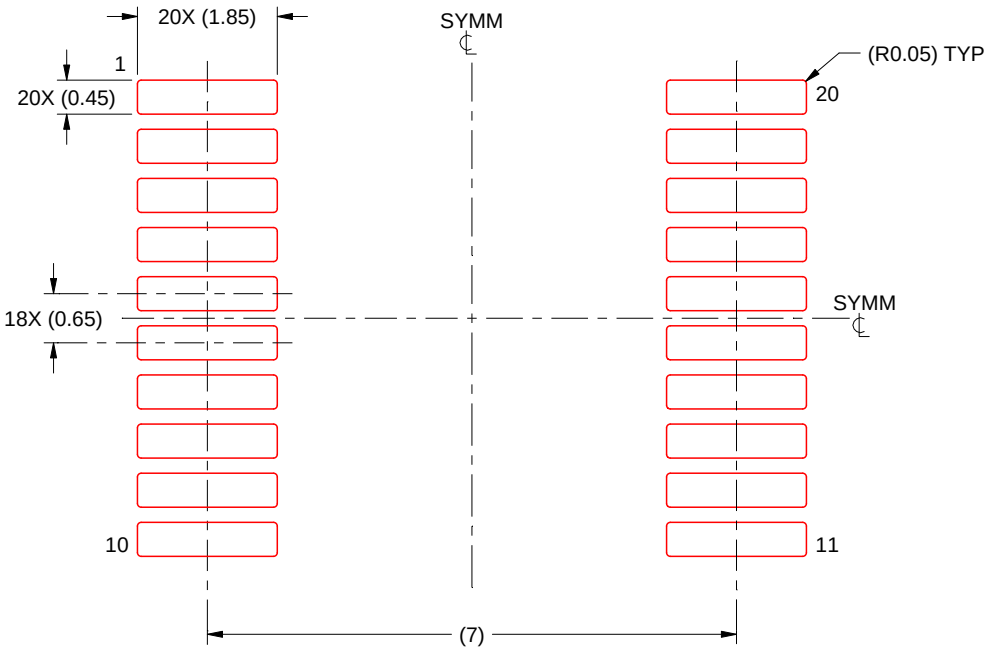
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## DB0020A

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

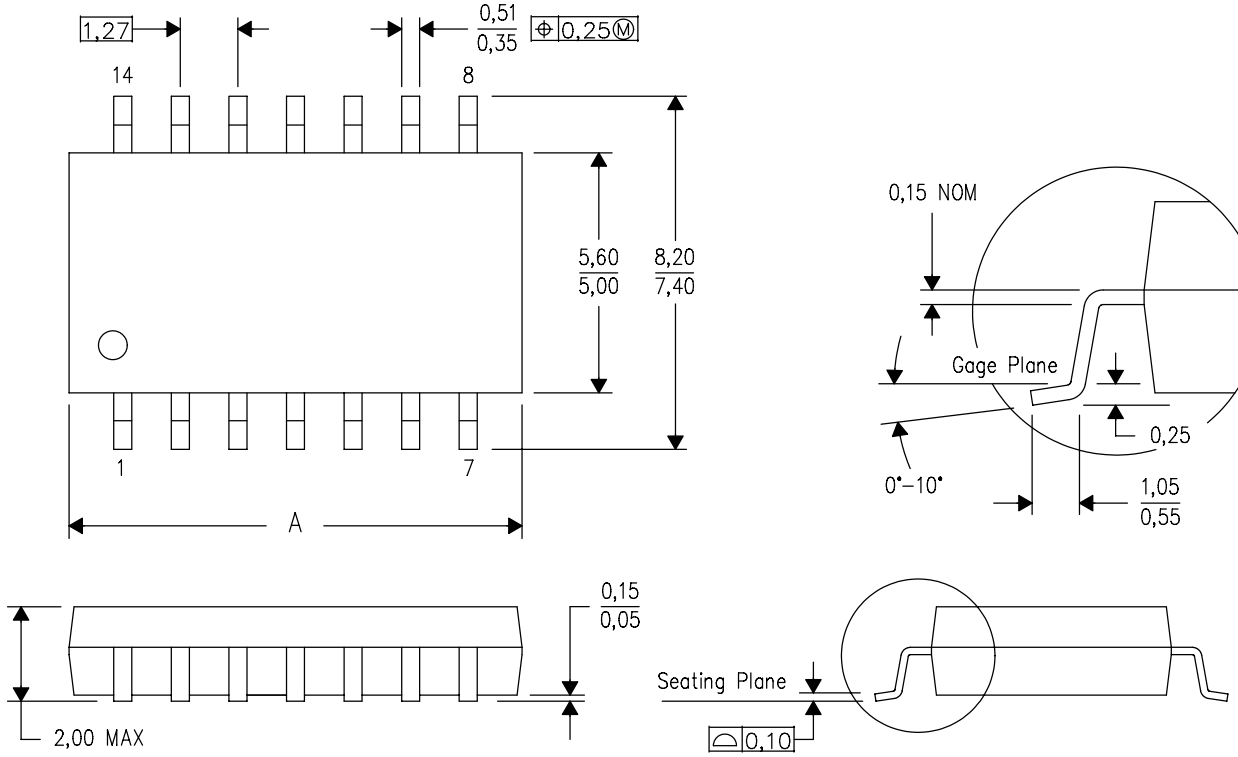
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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