

# MC74LCX74

## Low-Voltage CMOS Dual D-Type Flip-Flop

### With 5 V-Tolerant Inputs

The MC74LCX74 is a high performance, dual D-type flip-flop with asynchronous clear and set inputs and complementary (O,  $\bar{O}$ ) outputs. It operates from a 2.3 to 3.6 V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A  $V_I$  specification of 5.5 V allows MC74LCX74 inputs to be safely driven from 5.0 V devices.

The MC74LCX74 consists of 2 edge-triggered flip-flops with individual D-type inputs. The flip-flop will store the state of individual D inputs, that meet the setup and hold time requirements, on the LOW-to-HIGH Clock (CP) transition.

#### Features

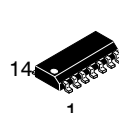
- Designed for 2.3 V to 3.6 V  $V_{CC}$  Operation
- 5.0 V Tolerant Inputs – Interface Capability With 5.0 V TTL Logic
- LVTTTL Compatible
- LVC MOS Compatible
- 24 mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (10  $\mu$ A) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500 mA
- ESD Performance: Human Body Model >2000 V  
Machine Model >200 V
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



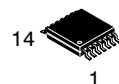
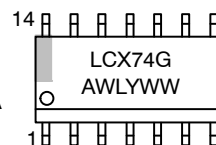
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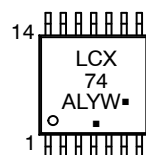
#### MARKING DIAGRAMS



SOIC-14  
D SUFFIX  
CASE 751A



TSSOP-14  
DT SUFFIX  
CASE 948G



A = Assembly Location  
L, WL = Wafer Lot  
Y, YY = Year  
W, WW = Work Week  
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

# MC74LCX74

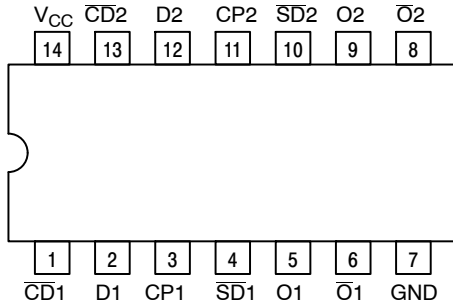


Figure 1. Pinout: 14-Lead (Top View)

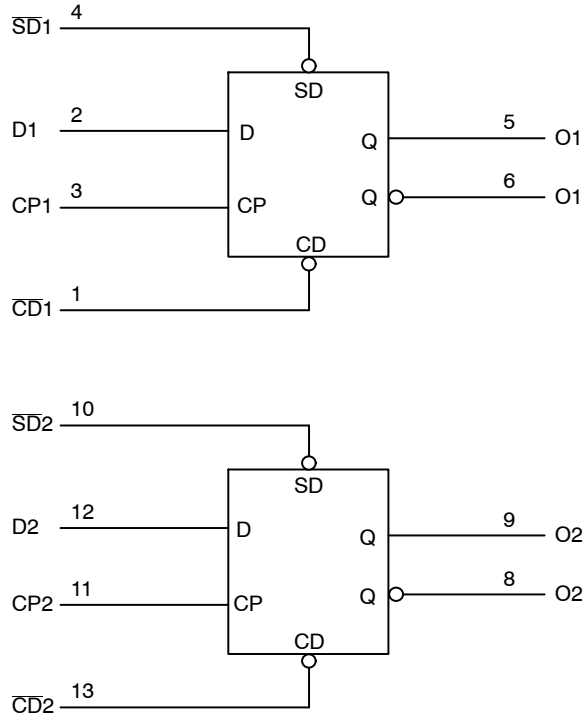


Figure 2. Logic Diagram

## PIN NAMES

Pins	Function
CP1, CP2	Clock Pulse Inputs
D1-D2	Data Inputs
$\overline{CD}1$ , $\overline{CD}2$	Direct Clear Inputs
$\overline{SD}1$ , $\overline{SD}2$	Direct Set Inputs
O <sub>n</sub> - $\overline{O}$ <sub>n</sub>	Outputs

## TRUTH TABLE

Inputs				Outputs		Operating Mode
$\overline{SD}n$	$\overline{CD}n$	CP <sub>n</sub>	D <sub>n</sub>	O <sub>n</sub>	$\overline{O}n$	
L	H	X	X	H	L	Asynchronous Set Asynchronous Clear Undetermined
H	L	X	X	L	H	
L	L	X	X	H	H	
H	H	↑	h	H	L	Load and Read Register
H	H	↑	l	L	H	
H	H	⊠	X	NC	NC	Hold

H = High Voltage Level

h = High Voltage Level One Setup Time Prior to the Low-to-High Clock Transition

L = Low Voltage Level

l = Low Voltage Level One Setup Time Prior to the Low-to-High Clock Transition

NC = No Change

X = High or Low Voltage Level and Transitions are Acceptable

↑ = Low-to-High Transition

⊠ = Not a Low-to-High Transition

For I<sub>CC</sub> reasons, DO NOT FLOAT Inputs

# MC74LCX74

## MAXIMUM RATINGS

Symbol	Parameter	Value	Condition	Units
$V_{CC}$	DC Supply Voltage	-0.5 to +7.0		V
$V_I$	DC Input Voltage	$-0.5 \leq V_I \leq +7.0$		V
$V_O$	DC Output Voltage	$-0.5 \leq V_O \leq V_{CC} + 0.5$	Output in HIGH or LOW State (Note 1)	V
$I_{IK}$	DC Input Diode Current	-50	$V_I < GND$	mA
$I_{OK}$	DC Output Diode Current	-50	$V_O < GND$	mA
		+50	$V_O > V_{CC}$	mA
$I_O$	DC Output Source/Sink Current	$\pm 50$		mA
$I_{CC}$	DC Supply Current Per Supply Pin	$\pm 100$		mA
$I_{GND}$	DC Ground Current Per Ground Pin	$\pm 100$		mA
$T_{STG}$	Storage Temperature Range	-65 to +150		°C
MSL	Moisture Sensitivity		Level 1	

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1.  $I_O$  absolute maximum rating must be observed.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Type	Max	Units
$V_{CC}$	Supply Voltage Operating Data Retention Only	2.0 1.5	2.5, 3.3 2.5, 3.3	3.6 3.6	V
$V_I$	Input Voltage	0		5.5	V
$V_O$	Output Voltage (HIGH or LOW State)	0		$V_{CC}$	V
$I_{OH}$	HIGH Level Output Current $V_{CC} = 3.0\text{ V} - 3.6\text{ V}$ $V_{CC} = 2.7\text{ V} - 3.0\text{ V}$ $V_{CC} = 2.3\text{ V} - 2.7\text{ V}$			-24 -12 -8	mA
$I_{OL}$	LOW Level Output Current $V_{CC} = 3.0\text{ V} - 3.6\text{ V}$ $V_{CC} = 2.7\text{ V} - 3.0\text{ V}$ $V_{CC} = 2.3\text{ V} - 2.7\text{ V}$			+24 +12 +8	mA
$T_A$	Operating Free-Air Temperature	-40		+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate, $V_{IN}$ from 0.8 V to 2.0 V, $V_{CC} = 3.0\text{ V}$	0		10	ns/V

## ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
MC74LCX74DG	SOIC-14 (Pb-Free)	55 Units / Rail
MC74LCX74DR2G	SOIC-14 (Pb-Free)	2500 Tape & Reel
MC74LCX74DTG	TSSOP-14 (Pb-Free)	96 Units / Rail
MC74LCX74DTR2G	TSSOP-14 (Pb-Free)	2500 Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MC74LCX74

## DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T <sub>A</sub> = -40°C to +85°C		Units
			Min	Max	
V <sub>IH</sub>	HIGH Level Input Voltage (Note 2)	2.3 V ≤ V <sub>CC</sub> ≤ 2.7 V	1.7		V
		2.7 V ≤ V <sub>CC</sub> ≤ 3.6 V	2.0		
V <sub>IL</sub>	LOW Level Input Voltage (Note 2)	2.3 V ≤ V <sub>CC</sub> ≤ 2.7 V		0.7	V
		2.7 V ≤ V <sub>CC</sub> ≤ 3.6 V		0.8	
V <sub>OH</sub>	HIGH Level Output Voltage	2.3 V ≤ V <sub>CC</sub> ≤ 3.6 V; I <sub>OH</sub> = -100 μA	V <sub>CC</sub> - 0.2		V
		V <sub>CC</sub> = 2.3 V; I <sub>OH</sub> = -8 mA	1.8		
		V <sub>CC</sub> = 2.7 V; I <sub>OH</sub> = -12 mA	2.2		
		V <sub>CC</sub> = 3.0 V; I <sub>OH</sub> = -18 mA	2.4		
		V <sub>CC</sub> = 3.0 V; I <sub>OH</sub> = -24 mA	2.2		
V <sub>OL</sub>	LOW Level Output Voltage	2.3 V ≤ V <sub>CC</sub> ≤ 3.6 V; I <sub>OL</sub> = 100 μA		0.2	V
		V <sub>CC</sub> = 2.3 V; I <sub>OL</sub> = 8 mA		0.6	
		V <sub>CC</sub> = 2.7 V; I <sub>OL</sub> = 12 mA		0.4	
		V <sub>CC</sub> = 3.0 V; I <sub>OL</sub> = 16 mA		0.4	
		V <sub>CC</sub> = 3.0 V; I <sub>OL</sub> = 24 mA		0.55	
I <sub>OFF</sub>	Power Off Leakage Current	V <sub>CC</sub> = 0, V <sub>IN</sub> = 5.5 V or V <sub>OUT</sub> = 5.5 V		10	μA
I <sub>IN</sub>	Input Leakage Current	V <sub>CC</sub> = 3.6 V, V <sub>IN</sub> = 5.5 V or GND		±5	μA
I <sub>CC</sub>	Quiescent Supply Current	V <sub>CC</sub> = 3.6 V, V <sub>IN</sub> = 5.5 V or GND		10	μA
ΔI <sub>CC</sub>	Increase in I <sub>CC</sub> per Input	2.3 ≤ V <sub>CC</sub> ≤ 3.6 V; V <sub>IH</sub> = V <sub>CC</sub> - 0.6 V		500	μA

2. These values of V<sub>I</sub> are used to test DC electrical characteristics only.

## AC CHARACTERISTICS (t<sub>R</sub> = t<sub>F</sub> = 2.5 ns; R<sub>L</sub> = 500 Ω)

Symbol	Parameter	Waveform	Limits						Units
			T <sub>A</sub> = −40°C to +85°C						
			V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		
			C <sub>L</sub> = 50 pF		C <sub>L</sub> = 50 pF		C <sub>L</sub> = 30 pF		
			Min	Max	Min	Max	Min	Max	
f <sub>max</sub>	Clock Pulse Frequency	1	150		150		150		MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CPn to On or On	1	1.5 1.5	7.0 7.0	1.5 1.5	8.0 8.0	1.5 1.5	8.4 8.4	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay SDn or CDn to On or On	2	1.5 1.5	7.0 7.0	1.5 1.5	8.0 8.0	1.5 1.5	8.4 8.4	ns
t <sub>s</sub>	Setup Time, HIGH or LOW Dn to CPn	1	2.5		2.5		4.0		ns
t <sub>h</sub>	Hold Time, HIGH or LOW Dn to CPn	1	1.5		1.5		2.0		ns
t <sub>w</sub>	CPn Pulse Width, HIGH or LOW SDn or CDn Pulse Width, LOW	4	3.3 3.3		3.3 3.6		4.0 4.0		ns
t <sub>rec</sub>	Recovery Time SDn or CDn to CPn	3	2.5		3.0		4.5		ns
t <sub>OSHL</sub> t <sub>OSLH</sub>	Output–to–Output Skew (Note 3)			1.0 1.0					ns

3. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t<sub>OSHL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>); parameter guaranteed by design.

# MC74LCX74

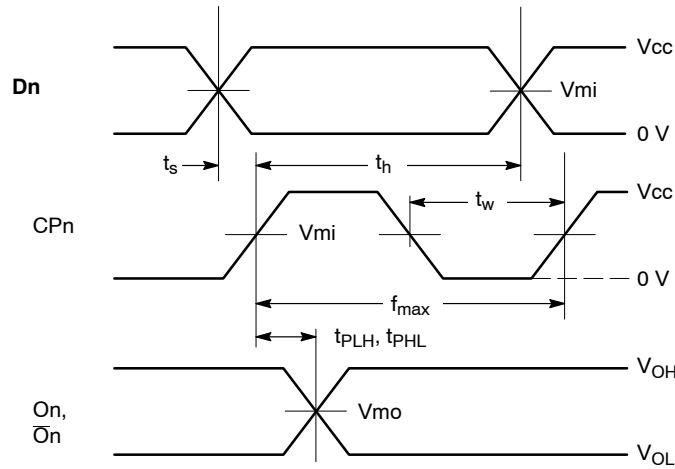
## DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	$T_A = +25^\circ\text{C}$			Units
			Min	Typ	Max	
$V_{OLP}$	Dynamic LOW Peak Voltage (Note 4)	$V_{CC} = 3.3\text{ V}, C_L = 50\text{ pF}, V_{IH} = 3.3\text{ V}, V_{IL} = 0\text{ V}$ $V_{CC} = 2.5\text{ V}, C_L = 30\text{ pF}, V_{IH} = 2.5\text{ V}, V_{IL} = 0\text{ V}$		0.8 0.6		V V
$V_{OLV}$	Dynamic LOW Valley Voltage (Note 4)	$V_{CC} = 3.3\text{ V}, C_L = 50\text{ pF}, V_{IH} = 3.3\text{ V}, V_{IL} = 0\text{ V}$ $V_{CC} = 2.5\text{ V}, C_L = 30\text{ pF}, V_{IH} = 2.5\text{ V}, V_{IL} = 0\text{ V}$		-0.8 -0.6		V V

4. Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.

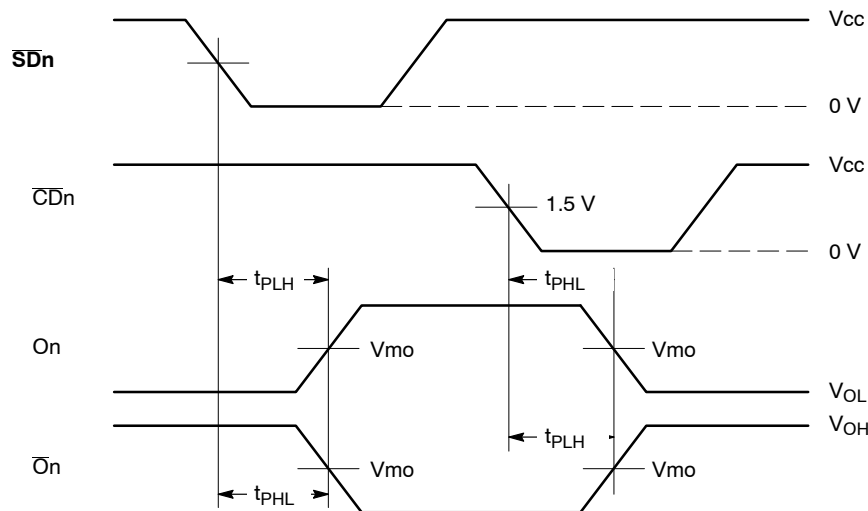
## CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Units
$C_{IN}$	Input Capacitance	$V_{CC} = 3.3\text{ V}, V_I = 0\text{ V or } V_{CC}$	7	pF
$C_{OUT}$	Output Capacitance	$V_{CC} = 3.3\text{ V}, V_I = 0\text{ V or } V_{CC}$	8	pF
$C_{PD}$	Power Dissipation Capacitance	10 MHz, $V_{CC} = 3.3\text{ V}, V_I = 0\text{ V or } V_{CC}$	25	pF



**WAVEFORM 1 – PROPAGATION DELAYS, SETUP AND HOLD TIMES**

$t_R = t_F = 2.5\text{ ns}$ , 10% to 90%;  $f = 1\text{ MHz}$ ;  $t_W = 500\text{ ns}$

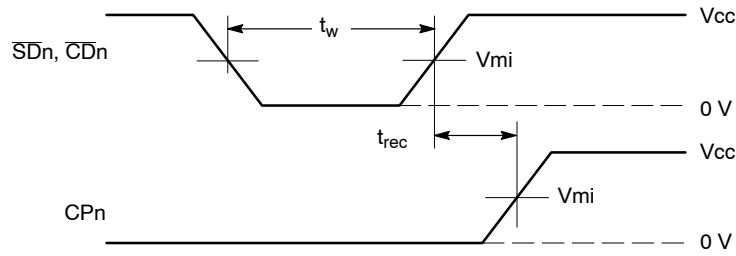


**WAVEFORM 2 – PROPAGATION DELAYS**

$t_R = t_F = 2.5\text{ ns}$ , 10% to 90%;  $f = 1\text{ MHz}$ ;  $t_W = 500\text{ ns}$

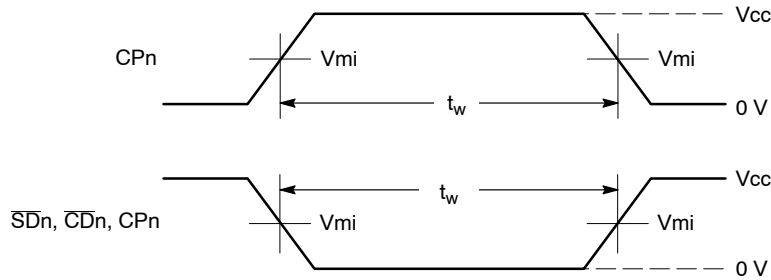
**Figure 3. AC Waveforms**

## MC74LCX74



**WAVEFORM 3 - RECOVERY TIME**

$t_R = t_F = 2.5 \text{ ns}$  from 10% to 90%;  $f = 1 \text{ MHz}$ ;  $t_w = 500 \text{ ns}$

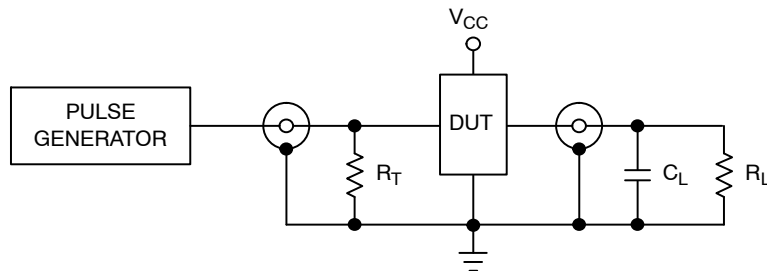


**WAVEFORM 4 - PULSE WIDTH**

$t_R = t_F = 2.5 \text{ ns}$  (or fast as required) from 10% to 90%;  
Output requirements:  $V_{OL} \leq 0.8 \text{ V}$ ,  $V_{OH} \geq 2.0 \text{ V}$

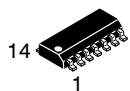
Symbol	Vcc		
	3.3 V $\pm$ 0.3 V	2.7 V	2.5 V $\pm$ 0.2 V
Vmi	1.5 V	1.5 V	$V_{CC}/2$
Vmo	1.5 V	1.5 V	$V_{CC}/2$

**Figure 3. AC Waveforms (Continued)**



$C_L = 50 \text{ pF}$  at  $V_{CC} = 3.3 \pm 0.3 \text{ V}$  or equivalent (includes jig and probe capacitance)  
 $C_L = 30 \text{ pF}$  at  $V_{CC} = 2.5 \pm 0.2 \text{ V}$  or equivalent (includes jig and probe capacitance)  
 $R_L = R_1 = 500 \Omega$  or equivalent  
 $R_T = Z_{OUT}$  of pulse generator (typically  $50 \Omega$ )

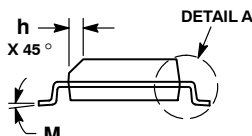
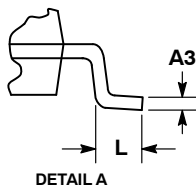
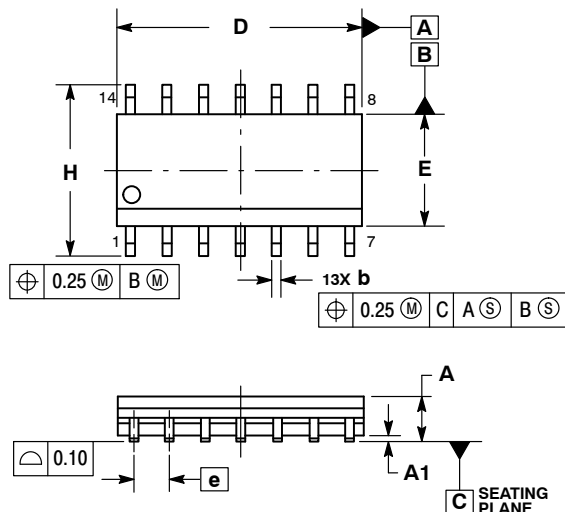
**Figure 4. Test Circuit**



SCALE 1:1

SOIC-14 NB  
CASE 751A-03  
ISSUE L

DATE 03 FEB 2016

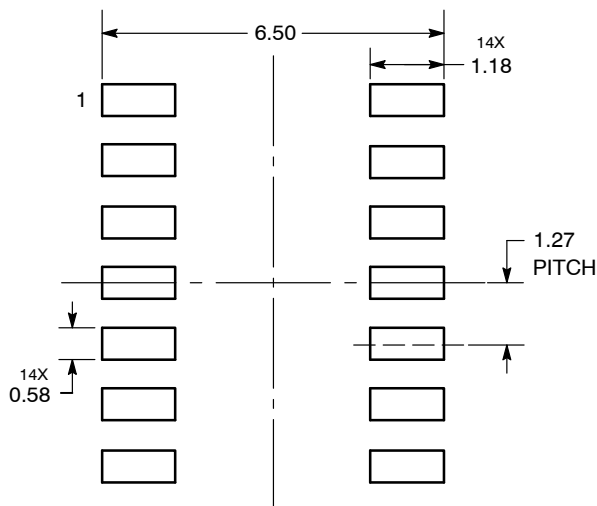


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0°	7°	0°	7°

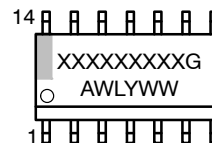
SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC  
MARKING DIAGRAM\*



XXXXXX = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
Y = Year  
WW = Work Week  
G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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CASE 751A-03  
ISSUE L

DATE 03 FEB 2016

STYLE 1:  
PIN 1. COMMON CATHODE  
2. ANODE/CATHODE  
3. ANODE/CATHODE  
4. NO CONNECTION  
5. ANODE/CATHODE  
6. NO CONNECTION  
7. ANODE/CATHODE  
8. ANODE/CATHODE  
9. ANODE/CATHODE  
10. NO CONNECTION  
11. ANODE/CATHODE  
12. ANODE/CATHODE  
13. NO CONNECTION  
14. COMMON ANODE

STYLE 2:  
CANCELLED

STYLE 3:  
PIN 1. NO CONNECTION  
2. ANODE  
3. ANODE  
4. NO CONNECTION  
5. ANODE  
6. NO CONNECTION  
7. ANODE  
8. ANODE  
9. ANODE  
10. NO CONNECTION  
11. ANODE  
12. ANODE  
13. NO CONNECTION  
14. COMMON CATHODE

STYLE 4:  
PIN 1. NO CONNECTION  
2. CATHODE  
3. CATHODE  
4. NO CONNECTION  
5. CATHODE  
6. NO CONNECTION  
7. CATHODE  
8. CATHODE  
9. CATHODE  
10. NO CONNECTION  
11. CATHODE  
12. CATHODE  
13. NO CONNECTION  
14. COMMON ANODE

STYLE 5:  
PIN 1. COMMON CATHODE  
2. ANODE/CATHODE  
3. ANODE/CATHODE  
4. ANODE/CATHODE  
5. ANODE/CATHODE  
6. NO CONNECTION  
7. COMMON ANODE  
8. COMMON CATHODE  
9. ANODE/CATHODE  
10. ANODE/CATHODE  
11. ANODE/CATHODE  
12. ANODE/CATHODE  
13. NO CONNECTION  
14. COMMON ANODE

STYLE 6:  
PIN 1. CATHODE  
2. CATHODE  
3. CATHODE  
4. CATHODE  
5. CATHODE  
6. CATHODE  
7. CATHODE  
8. ANODE  
9. ANODE  
10. ANODE  
11. ANODE  
12. ANODE  
13. ANODE  
14. ANODE

STYLE 7:  
PIN 1. ANODE/CATHODE  
2. COMMON ANODE  
3. COMMON CATHODE  
4. ANODE/CATHODE  
5. ANODE/CATHODE  
6. ANODE/CATHODE  
7. ANODE/CATHODE  
8. ANODE/CATHODE  
9. ANODE/CATHODE  
10. ANODE/CATHODE  
11. COMMON CATHODE  
12. COMMON ANODE  
13. ANODE/CATHODE  
14. ANODE/CATHODE

STYLE 8:  
PIN 1. COMMON CATHODE  
2. ANODE/CATHODE  
3. ANODE/CATHODE  
4. NO CONNECTION  
5. ANODE/CATHODE  
6. ANODE/CATHODE  
7. COMMON ANODE  
8. COMMON ANODE  
9. ANODE/CATHODE  
10. ANODE/CATHODE  
11. NO CONNECTION  
12. ANODE/CATHODE  
13. ANODE/CATHODE  
14. COMMON CATHODE

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