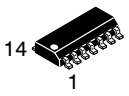
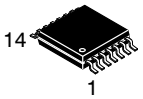
Dual D-Type Flip-Flop with Preset and Clear

MM74HCT74



SOIC−14 NB
CASE 751A−03



TSSOP−14 WB
CASE 948G

General Description

The MM74HCT74 utilizes advanced silicon−gate CMOS technology to achieve operation speeds similar to the equivalent LS−TTL part. It possesses the high noise immunity and low power consumption of standard CMOS integrated circuits, along with the ability to drive 10 LS−TTL loads.

This flip−flop has independent data, preset, clear, and clock inputs and Q and $\overline{Q}$ outputs. The logic level present at the data input is transferred to the output during the positive−going transition of the clock pulse. Preset and clear are independent of the clock and accomplished by a low level at the appropriate input.

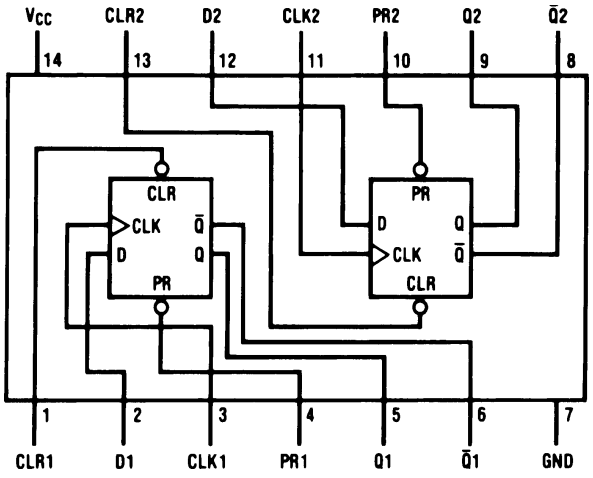
The 74HCT logic family is functionally and pin−out compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to VCC and ground.

MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug−in replacements for LS−TTL devices and can be used to reduce power consumption in existing designs.

Features

- Typical Propagation Delay: 18 ns
- Low Quiescent Current: 80 μA Maximum (74HCT Series)
- Low Input Current: 1 μA Maximum
- Fanout of 10 LS−TTL Loads
- Meta−stable Hardened
- These Devices are Pb−Free, Halide Free and are RoHS Compliant

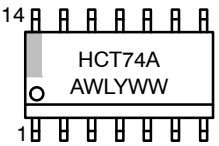
Connection Diagram



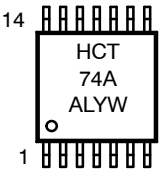
Top View

Figure 1. Pin Assignments for SOIC and TSSOP

MARKING DIAGRAM



SOIC−14 NB



TSSOP−14

HCT74A = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
Y = Year
WW, W = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

TRUTH TABLE

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H (Note 1)	H (Note 1)
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	$\overline{Q}$0

Q0 = the level of Q before the indicated input conditions were established.

1. This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (HIGH) level.

Logic Diagram

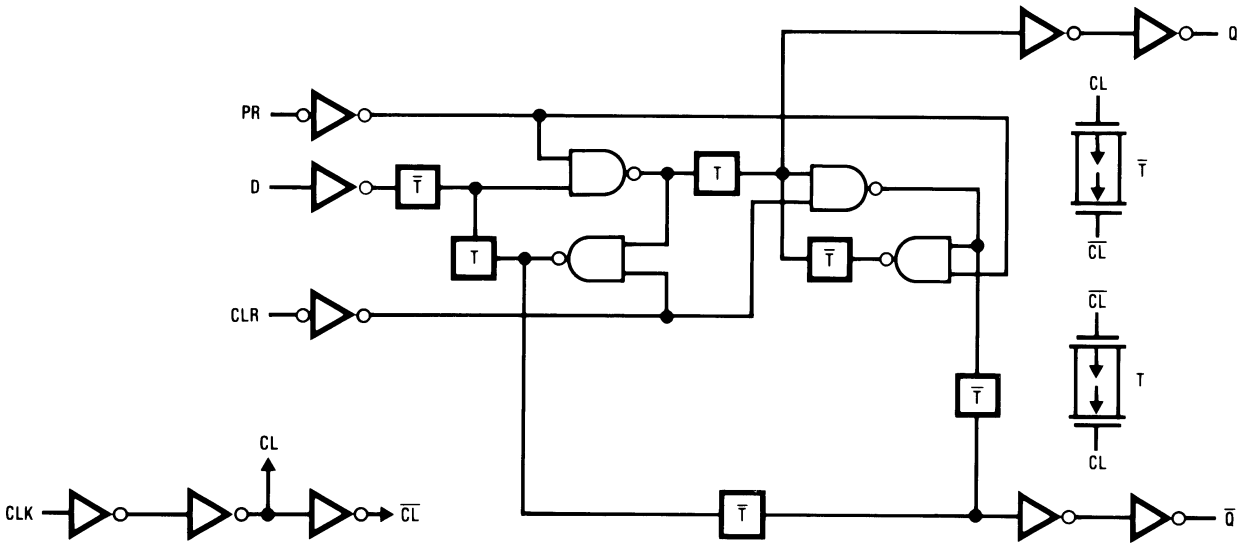


Figure 2. Logic Diagram

ABSOLUTE MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	−0.5 to +6.5 V
V_{IN}	DC Input Voltage	−0.5 to V_{CC} + 0.5 V
V_{OUT}	DC Output Voltage	−0.5 to V_{CC} + 0.5 V
I_{IK}, I_{OK}	Clamp Diode Current	±20 mA
I_{OUT}	DC Output Current, per Pin	±25 mA
I_{CC}	DC V_{CC} or GND Current, per Pin	±50 mA
T_{STG}	Storage Temperature Range	−65°C to +150°C
P_D	Power Dissipation SOIC−14 TSSOP−14	1077 mW 833 mW
T_L	Lead Temperature (Soldering 10 Seconds)	260°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Unless otherwise specified all voltages are referenced to ground.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IN}, V_{OUT}	DC Input or Output Voltage	0	V_{CC}	V
T_A	Operating Temperature Range	−55	+125	°C
t_r, t_f	Input Rise or Fall Times	–	500	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC CHARACTERISTICS (V_{CC} = 5 V ±10% (unless otherwise specified))

Symbol	Parameter	Conditions	T_A = 25°C	T_A = −40°C to 85°C	T_A = −55°C to 125°C	Unit
			Typ	Guaranteed Limits		
V_{IH}	Minimum HIGH Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum LOW Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum HIGH Level Output Voltage	V_{IN} = V_{IH} or V_{IL}, $\|I_{OUT}\|$ = 20 μA	VCC	V_{CC} − 0.1	V_{CC} − 0.1	V_{CC} − 0.1	V
		V_{IN} = V_{IH} or V_{IL}, $\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5 V	4.2	3.98	3.84	3.7	
		V_{IN} = V_{IH} or V_{IL}, $\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5 V	5.2	4.98	4.84	4.7	
V_{OL}	Maximum LOW Level Voltage	V_{IN} = V_{IH} or V_{IL}, $\|I_{OUT}\|$ = 20 μA	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL}, $\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5 V	0.2	0.26	0.33	0.4	
		V_{IN} = V_{IH} or V_{IL}, $\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5 V	0.2	0.26	0.33	0.4	
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND, V_{IH} or V_{IL}	–	±0.5	±0.5	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND, I_{OUT} = 0 μA	–	2.0	20	80	μA
		V_{IN} = 2.4 V or 0.5 V (Note 3)	–	0.3	0.4	0.5	mA

3. This is measured per input with all other inputs held at V_{CC} or ground.

AC CHARACTERISTICS (V_{CC} = 5.0 V, t_r = t_f = 6 ns, C_L = 15 pF, T_A = 25°C (unless otherwise noted))

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Unit
f_{MAX}	Maximum Operating Frequency from Clock to Q or $\overline{Q}$		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q or $\overline{Q}$		18	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Preset or Clear to Q or $\overline{Q}$		18	30	ns
t_{REM}	Minimum Removal Time, Preset or Clear to Clock		–	20	ns
t_S	Minimum Setup Time Data to Clock		–	20	ns
t_H	Minimum Hold Time Clock to Data		−3	0	ns
t_W	Minimum Pulse Width Clock, Preset or Clear		8	16	ns

AC CHARACTERISTICS (V_{CC} = 5.0 V ±10%, C_L = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise noted))

Symbol	Parameter	Conditions	T_A = 25°C	T_A = −40°C to 85°C		Unit
			Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		–	27	21	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clock to Q or $\overline{Q}$		21	35	44	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Preset or Clear to Q or $\overline{Q}$		21	35	44	ns
t_{REM}	Minimum Removal Time Preset or Clear to Clock		–	20	25	ns
t_S	Minimum Setup Time Data to Clock		–	20	25	ns
t_H	Minimum Hold Time Clock to Data		–3	0	0	ns
t_W	Minimum Pulse Width Clock, Preset or Clear		9	16	20	ns
t_r, t_f	Maximum Clock Input Rise and Fall Time		–	500	500	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		–	15	19	ns
C_{PD}	Power Dissipation Capacitance (Note 4)	(per flip−flop)	10	–	–	pF
C_{IN}	Maximum Input Capacitance		5	10	10	pF

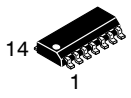
4. C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

ORDERING INFORMATION

Part Number	Package	Shipping†
MM74HCT74M	SOIC−14, Case 751A−03 (Pb−Free, Halide−Free)	55 Units / Tube
MM74HCT74MX	SOIC−14, Case 751A−03 (Pb−Free, Halide−Free)	2500 Units / Tape & Reel
MM74HCT74MTCX	TSSOP−14, Case 948G−01 (Pb−Free, Halide Free)	2500 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



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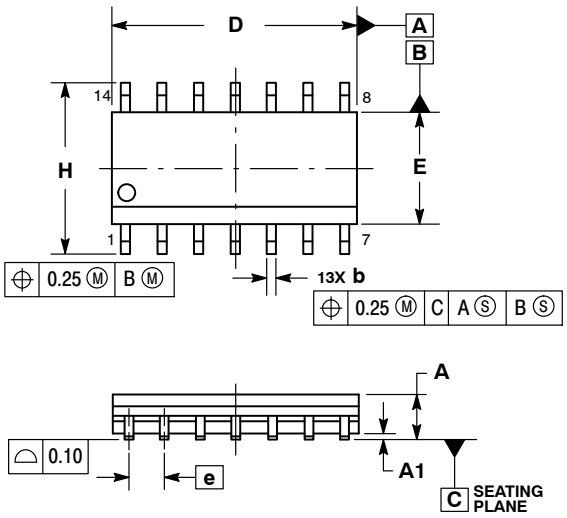
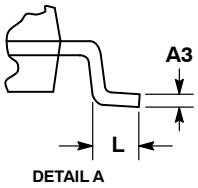
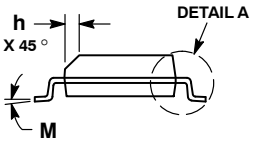
SOIC−14 NB
CASE 751A−03
ISSUE L

DATE 03 FEB 2016



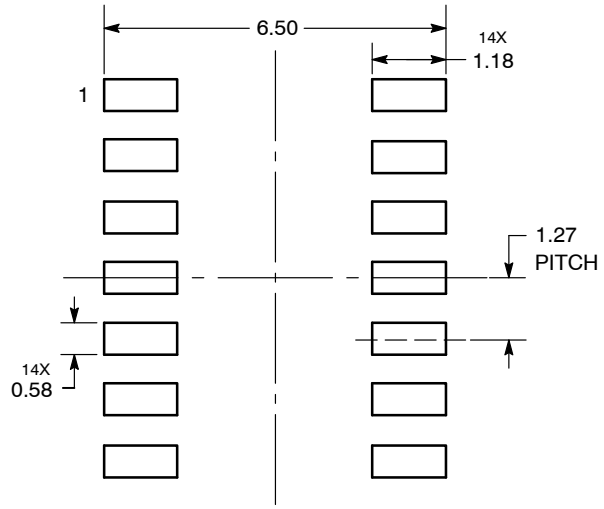




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

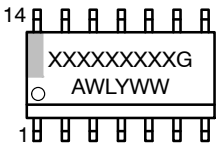
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42565B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**SOIC−14 NB**		**PAGE 1 OF 2**

SOIC−14
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

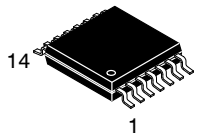
STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

TSSOP−14 WB
CASE 948G
ISSUE C

DATE 17 FEB 2016



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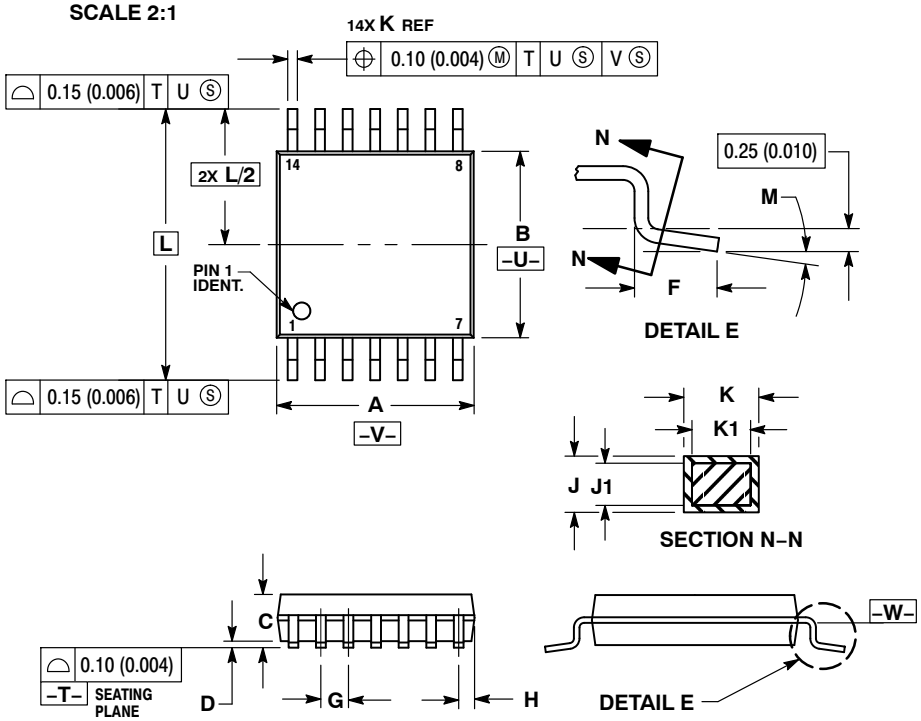
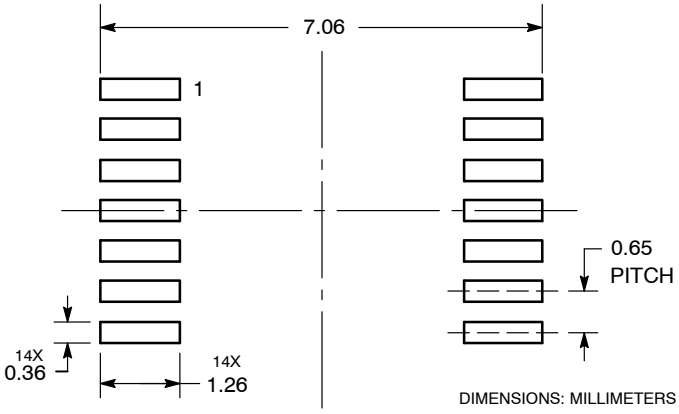


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

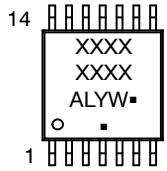
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98ASH70246A**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**TSSOP−14 WB**	**PAGE 1 OF 1**

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