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Octal D-Type Flip-Flop with 3-STATE Outputs

74VHC374



The VHC374 is an advanced high speed CMOS octal flip–flop with 3–STATE output fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. This 8–bit D–type flip–flop is controlled by a clock input (CP) and an output enable input (\overline{OE}). When the \overline{OE} input is HIGH, the eight outputs are in a HIGH impedance state.

An input protection circuit ensures that 0 V to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

- High Speed: $t_{PD} = 5.4 \text{ ns}$ (Typ) at $V_{CC} = 5 \text{ V}$
- High Noise Immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (Min)
- Power Down Protection is Provided on All Inputs
- Low Power Dissipation: $I_{CC} = 4 \mu A (Max) @ T_A = 25 °C$
- Pin and Function Compatible with 74HC374
- This is a Pb–Free Device

Logic Symbol

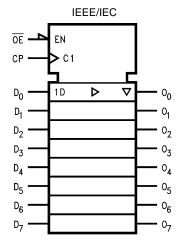
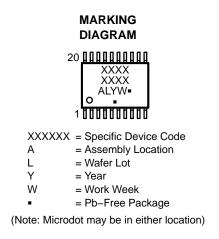


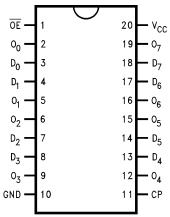
Figure 1. Logic Symbol



TSSOP20, 4.4x6.5 CASE 948AQ







PIN DESCRIPTION

Pin Names	Description
D ₀ –D ₇	Data Inputs
CP	Clock Pulse Input
ŌE	3-STATE Output Enable Input
O ₀ –O ₇	3–STATE Outputs

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

TRUTH TABLE

	Outputs		
D _n	СР	ŌĒ	O _n
Н	\ \	L	Н
L	~	L	L
Х	Х	Н	Z

H = HIGH Voltage Level

L = LOW Voltage Level

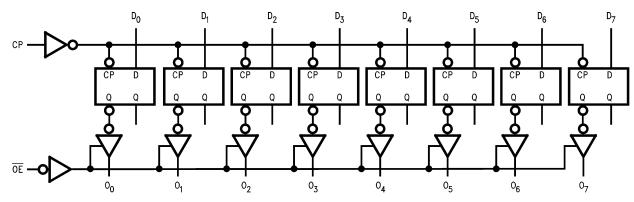
- X = Immaterial
- Z = High Impedance

 \checkmark = LOW-to-HIGH Transition

Logic Diagram

Functional Description

The VHC374 consists of eight edge–triggered flip–flops with individual D–type inputs and 3–STATE true outputs. The buffered clock and buffered Output Enable are common to all flip–flops. The eight flip–flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW–to–HIGH Clock (CP) transition. With the Output Enable (\overline{OE}) LOW, the con– tents of the eight flip–flops are available at the outputs. When the \overline{OE} is HIGH, the outputs go to the high impedance state. Operation of the \overline{OE} input does not affect the state of the flip–flops.



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 2. Logic Diagram

MAXIMUM RATINGS

Symbol	Р	Value	Unit	
V _{CC}	DC Supply Voltage	-0.5 to +6.5	V	
V _{IN}	DC Input Voltage		-0.5 to +6.5	V
V _{OUT}	DC Output Voltage		–0.5 to V _{CC} + 0.5	V
I _{IN}	DC Input Current		±20	mA
I _{OUT}	DC Output Current	±25	mA	
I _{CC}	DC Supply Current, V _{CC} and GND Pi	±75	mA	
I _{IK}	Input Clamp Current	-20	mA	
Ι _{ΟΚ}	Output Clamp Current	±20	mA	
T _{STG}	Storage Temperature Range	-65 to +150	°C	
ΤL	Lead Temperature, 1 mm from Case	for 10 Seconds	260	°C
TJ	Junction Temperature under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 2)		150	°C/W
PD	Power Dissipation in Still Air at 25 °C		833	mW
MSL	Moisture Sensitivity		Level 1	
F _R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V–0 @ 0.574 in	
V _{ESD}	ESD Withstand Voltage (Note 3)	Human Body Model	2000	V
		Charged Device Model	N/A	1

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality Applicable to devices with outputs that may be tri-stated.
 Measured with minimum pad spacing on an FR4 board, using 76 mm-by-114 mm, 2-ounce copper trace no air flow per JESD51-7.

3. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.

RECOMMENDED OPERATING CONDITIONS

Symbol		Parameter					
V _{CC}	DC Supply Voltage			2.0	5.5	V	
V _{IN}	DC Input Voltage (Note 4)				5.5	V	
V _{OUT}	DC Output Voltage (Note 4)				V _{CC}	V	
T _A	Operating Temperature	Operating Temperature				°C	
t _r , t _f	Input Rise or Fall Rate	$V_{CC} = 3.0 \text{ V} \text{ to } 3.6 \text{ V}$		0	100	ns/V	
		$V_{CC} = 4.5 \text{ V} \text{ to } 5.5 \text{ V}$		0	20		

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

74VHC374

DC ELECTRICAL CHARACTERISTICS

								$T_A = 25 \ ^{\circ}C$ $T_A = -40 \ ^{\circ}C \ to +85$			C to +85 °C	0
Symbol	Parameter	Conditions		V _{CC} (V)	Min	Тур	Max	Min	Max	Unit		
V _{IH}	HIGH Level			2.0	1.50	-	-	1.50	-	V		
	Input Voltage			3.0–5.5	0.7 x V _{CC}	-	-	$0.7 \mathrm{x} \mathrm{V}_{\mathrm{CC}}$	-			
V _{IL}	LOW Level			2.0	-	-	0.50	-	0.50	V		
	Input Voltage			3.0-5.5	-	-	$0.3 \times V_{CC}$	-	$0.3 \times V_{CC}$			
V _{OH}	HIGH Level	$V_{IN} = V_{IH}$	$I_{OH} = -50 \ \mu A$	2.0	1.9	2.0	-	1.9	-	V		
	Output Voltage	or V _{IL}		3.0	2.9	3.0	-	2.9	-			
				4.5	4.4	4.5	-	4.4	-			
			$I_{OH} = -4 \text{ mA}$	3.0	2.58	-	-	2.48	-			
			I _{OH} = -8 mA	4.5	3.94	-	-	3.80	-			
V _{OL}	LOW Level	$V_{IN} = V_{IH}$	I _{OL} = 50 μA	2.0	-	0.0	0.1	-	0.1	V		
	Output Voltage	or V _{IL}		3.0	-	0.0	0.1	-	0.1			
				4.5	-	0.0	0.1	-	0.1			
			I _{OL} = 4 mA	3.0	-	-	0.36	-	0.44			
			I _{OL} = 8 mA	4.5	-	-	0.36	-	0.44			
I _{OZ}	3–STATE Output Off–State Current	$V_{IN} = V_{IH} \text{ or } V_{IL};$ $V_{OUT} = V_{CC} \text{ or } GND$		5.5	-	_	±0.25	-	±2.5	μΑ		
I _{IN}	Input Leakage Current	V_{IN} = 5.5 V or GND		0–5.5	-	-	±0.1	_	±1.0	μA		
I _{CC}	Quiescent Supply Current	$V_{IN} = V_{CC}$	or GND	5.5	-	-	4.0	-	40.0	μA		

NOISE CHARACTERISTICS

				T _A = 25 °C		
Symbol	Parameter	Conditions	V _{CC} (V)	Тур	Limits	Unit
V _{OLP} (Note 5)	Quiet Output Maximum Dynamic V _{OL}	C _L = 50 pF	5.0	0.6	0.9	V
V _{OLV} (Note 5)	Quiet Output Minimum Dynamic V _{OL}	C _L = 50 pF	5.0	-0.6	-0.9	V
V _{IHD} (Note 5)	Minimum HIGH Level Dynamic Input Voltage	C _L = 50 pF	5.0	-	3.5	V
V _{ILD} (Note 5)	Maximum LOW Level Dynamic Input Voltage	C _L = 50 pF	5.0	-	1.5	V

5. Parameter guaranteed by design.

AC ELECTRICAL CHARACTERISTICS

						$T_A = 25 \ ^{\circ}C$ $T_A = -40 \ ^{\circ}C \ to \ +85 \ ^{\circ}$				C to +85 °C	
Symbol	Parameter	Con	ditions	V _{CC} (V)	Min	Тур	Max	Min	Max	Unit	
t _{PLH} , t _{PHL}	Propagation		C _L = 15 pF	3.3 ±0.3	_	8.1	12.7	1.0	15.0	ns	
	Delay Time (CP to O _n)		C _L = 50 pF		-	10.6	16.2	1.0	18.5		
			C _L = 15 pF	5.0 ±0.5	-	5.4	8.1	1.0	9.5	ns	
			C _L = 50 pF		-	6.9	10.1	1.0	11.5		
t _{PZL} , t _{PZH}	3-STATE	$R_L = 1 \ k\Omega$	C _L = 15 pF	3.3 ±0.3	-	7.1	11.0	1.0	13.0	ns	
	Output Enable Time		C _L = 50 pF		-	9.6	14.5	1.0	16.5		
			C _L = 15 pF	5.0 ±0.5	-	5.1	7.6	1.0	9.0	ns	
			C _L = 50 pF		-	6.6	9.6	1.0	11.0		
t _{PLZ} , t _{PHZ}	3-STATE	$R_L = 1 \ k\Omega$	C _L = 50 pF	3.3 ±0.3	-	10.2	14.0	1.0	16.0	ns	
Output Disab	Output Disable Time		C _L = 50 pF	5.0 ±0.5	_	6.1	8.8	1.0	10.0		
t _{OSLH} ,	Output to	(Note 6)	C _L = 50 pF	3.3 ±0.3	_	-	1.5	-	1.5	ns	
t _{OSHL}	Output Skew		C _L = 50 pF	5.0 ±0.5	_	-	1.0	-	1.0		
f _{MAX}	Maximum Clock		C _L = 15 pF	3.3 ±0.3	80	130	-	70	-	MHz	
	Frequency		C _L = 50 pF		55	85	-	50	-		
			C _L = 15 pF	5.0 ±0.5	130	185	-	110	-		
			C _L = 50 pF		85	120	-	75	-		
C _{IN}	Input Capacitance	V _{CC} = Ope	n		_	4	10	-	10	pF	
C _{OUT}	Output Capacitance	V _{CC} = 5.0 V			_	6	-	-	-	pF	
C _{PD}	Power Dissipation Capacitance	(Note 7)			-	32	-	-	-	pF	

6. Parameter guaranteed by design. t_{OSLH} = |t_{PLH max} - t_{PLH min}|; t_{OSHL} = |t_{PHL max} - t_{PHL min}|
7. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC} (opr.) = C_{PD} · V_{CC} · f_{IN} + I_{CC}/8 (per F/F). The total C_{PD} when n pcs. of the Octal D Flip–Flop operates can be calculated by the equation: C_{PD} (total) = 20 + 12n.

AC OPERATING REQUIREMENTS

			T _A = 25 °C		T _A = -40 °C to +85 °C			
Symbol	Parameter	V _{CC} (V)	Min	Тур	Max	Min	Max	Unit
t _W (H),	Minimum Pulse Width (CP)	3.3 ±0.3	5.0	-	-	5.5	-	ns
t _W (L)		5.0 ±0.5	5.0	-	-	5.0	-	
t _S	Minimum Set–Up Time	3.3 ±0.3	4.5	-	-	4.5	-	ns
		5.0 ±0.5	3.0	-	-	3.0	-	
t _H	Minimum Hold Time	3.3 ±0.3	2.0	-	-	2.0	-	ns
		5.0 ±0.5	2.0	-	-	2.0	-	

ORDERING INFORMATION

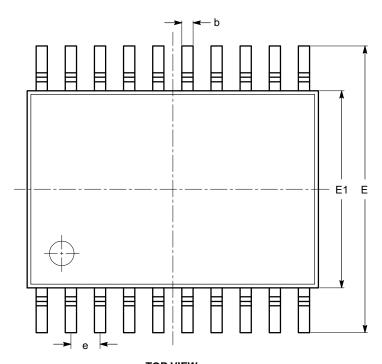
Device	Marking	Package	Shipping [†]
74VHC374MTCX	VHC 374	TSSOP20 (Pb–Free)	2500 Units / Tape & Reel

+For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



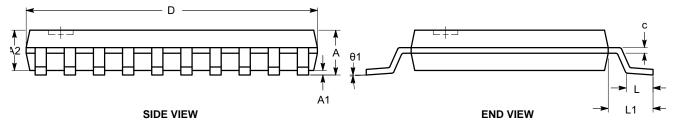
TSSOP20, 4.4x6.5 CASE 948AQ ISSUE A

DATE 19 MAR 2009



SYMBOL	MIN	NOM	MAX
А			1.20
A1	0.05		0.15
A2	0.80		1.05
b	0.19		0.30
С	0.09		0.20
D	6.40	6.50	6.60
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
е		0.65 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
θ	0°		8°





Notes:

All dimensions are in millimeters. Angles in degrees.
 Complies with JEDEC MO-153.

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