SNx4AHC240 Octal Buffers/Drivers With 3-State Outputs

1 Features

- Low delay, 4.3ns typ. (25°C, 5V)
- Latch-up performance exceeds 250mA per JESD 17

2 Applications

- Handset: smartphone
- Network switch
- Health fitness and wearables

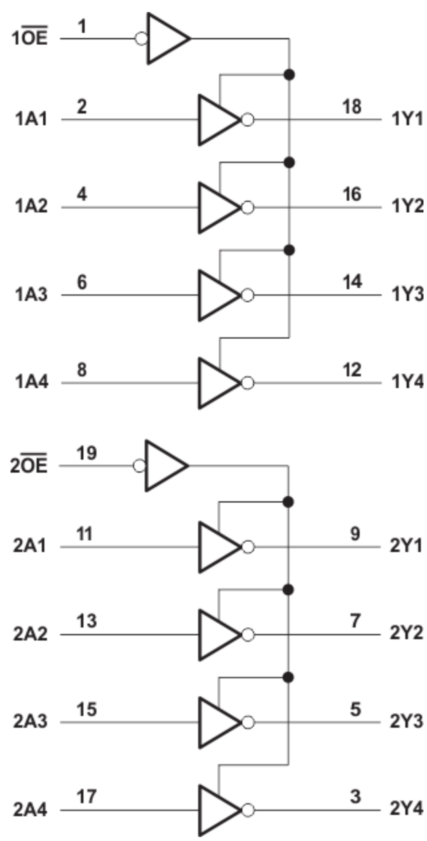
3 Description

These octal buffers/drivers are designed specifically to improve the performance and density of 3-state memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

Device Information

PART NUMBER	PACKAGE[1]	PACKAGE SIZE[2]	BODY SIZE[3]
SN54AHC240	J (CDIP, 20)	24.2mm x 7.62mm	24.2mm x 6.92mm
	W (CFP, 20)	13.09mm x 8.13mm	13.09mm x 6.92mm
	FK (LCCC, 20)	8.89 mm × 8.89 mm	8.89 mm × 8.89 mm
SN74AHC240	N (PDIP, 20)	24.33mm x 9.4mm	25.40mm x 6.35mm
	DW (SOIC, 20)	12.80mm × 10.3mm	12.8mm x 7.5mm
	NS (SOP, 20)	12.60mm x 7.8mm	12.6mm x 5.30mm
	PW (TSSOP, 20)	6.50mm × 6.4mm	6.50mm x 4.40mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins..



Logic Diagram (Positive Logic)

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4 Pin Configuration and Functions

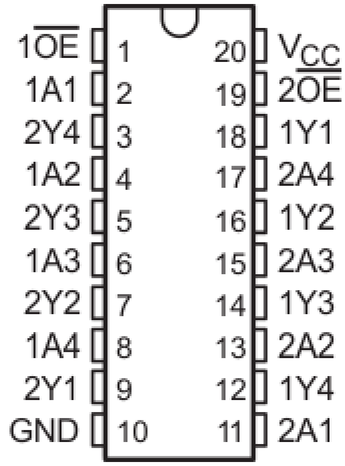


Figure 4-1. SN74AHC240-Q1 PW Package (Top View)

PIN		TYPE[(1)]	DESCRIPTION
NAME	NO.		
1OE	1	O	Output enable 1
1A1	2	I	1A1 input
2Y4	3	O	2Y4 output
1A2	4	I	1A2 input
2Y3	5	O	2Y3 output
1A3	6	I	1A3 input
2Y2	7	O	2Y2 output
1A4	8	I	1A4 input
2Y1	9	O	2Y1 output
GND	10	G	Ground pin
2A1	11	I	2A1 input
1Y4	12	O	1Y4 output
2A2	13	I	2A2 input
1Y3	14	O	1Y3 output
2A3	15	I	2A3 input
1Y2	16	O	1Y2 output
2A4	17	I	2A4 input
1Y1	18	O	1Y1 output
2OE	19	O	Output enable 2
VCC	20	P	Power pin

(1) Signal Types: I = Input, O = Output, I/O = Input or Output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
V_I	Input voltage range(2)		–0.5	7	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		–0.5	7	V
V_O	Output voltage range(2)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < -0.5V		-20	mA
I_{OK}	Output clamp current	V_O < -0.5V or V_O > V_{CC} + 0.5V		±20	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±25	mA
	Continuous output current through V_{CC} or GND			±75	mA
T_{stg}	Storage temperature		-65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Specification	Description	Condition	MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2V	1.5		V
		V_{CC} = 3V	2.1		
		V_{CC} = 5.5V	3.85		
V_{IL}	Low-Level input voltage	V_{CC} = 2V		0.5	V
	Low-Level input voltage	V_{CC} = 3V		0.9	
	Low-Level input voltage	V_{CC} = 5.5V		1.65	
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2V		-50	µA
		V_{CC} = 3.3V ± 0.3V		-4	mA
		V_{CC} = 5V ± 0.5V		-8	mA
I_{OL}	Low-level output current	V_{CC} = 2V		50	µA
		V_{CC} = 3.3V ± 0.3V		4	mA
		V_{CC} = 5V ± 0.5V		8	mA
Δt/Δv	Input transition rise or fall rate	V_{CC} = 3.3V ± 0.3V		100	ns/V
		V_{CC} = 5V ± 0.5V		20	ns/V
T_A	Operating free-air temperature		–40	125	°C

5.4 Thermal Information

THERMAL METRIC[1]		DW	DB	DGV	N	NS	PW	UNIT
		20 PINS						
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2]	81.1	70	92	69	60	116.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The package thermal impedance is calculated in accordance with JESD 51-7.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C MIN	T_A = 25°C TYP	T_A = 25°C MAX	-40°C to 125°C MIN	-40°C to 125°C TYP	-40°C to 125°C MAX	UNIT
V_{OH}	I_{OH} = –50µA	2V to 5.5V	V_{CC}-0.1	V_{CC}		V_{CC}-0.1	V_{CC}		V
	I_{OH} = −4mA	3V	2.58			2.48			
	I_{OH} = −8mA	4.5V	3.94			3.8			
V_{OL}	I_{OL} = 50µA	2V to 5.5V			0.1			0.1	V
	I_{OL} = 4mA	3V			0.36			0.44	
	I_{OL} = 8mA	4.5V			0.36			0.44	
I_I	V_I = 5.5V or GND and V_{CC} = 0V to 5.5V	0V to 5.5V			±0.1			±1	µA
I_{OZ}	V_O = V_{CC} or GND and V_{CC} = 5.5V	5.5V			±0.25			±5	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0, and V_{CC} = 5.5V	5.5V			4			40	µA
C_I	V_I = V_{CC} or GND	5V		2	10			10	pF
C_O	Vo = V_{CC} or GND	5V		5					pF
C_{PD}	No load, F = 1MHz	5V		15					pF

5.6 Switching Characteristics

C_L = 50pF; over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	T_A = 25°C MIN	T_A = 25°C TYP	T_A = 25°C MAX	-40°C to 125°C MIN	-40°C to 125°C TYP	-40°C to 125°C MAX	UNIT
t_{PLH}	A	Y	C_L = 15pF	2V			19.5	1		23	ns
t_{PHL}							19.5	1		23	ns
t_{PZH}	$\overline{OE}$	Y	C_L = 15pF	2V			25.5	1		30	ns
t_{PZL}							25.5	1		30	ns
t_{PHZ}	$\overline{OE}$	Y	C_L = 15pF	2V			25.5	1		30	ns
t_{PLZ}							25.5	1		30	ns
t_{PLH}	A	Y	C_L = 15pF	3.3V		5.3	7.5	1		9	ns
t_{PHL}						5.3	7.5	1		9	ns
t_{PZH}	$\overline{OE}$	Y	C_L = 15pF	3.3V		6.6	10.6	1		12.5	ns
t_{PZL}						6.6	10.6	1		12.5	ns
t_{PHZ}	$\overline{OE}$	Y	C_L = 15pF	3.3V		7.8	11.5	1		12.5	ns
t_{PLZ}						7.8	11.5	1		12.5	ns
t_{PLH}	A	Y	C_L = 15pF	5V		3.6	5.5	1		6.5	ns
t_{PHL}						3.6	5.5	1		6.5	ns
t_{PZH}	$\overline{OE}$	Y	C_L = 15pF	5V		4.7	7.3	1		8.5	ns
t_{PZL}						4.7	7.3	1		8.5	ns

5.6 Switching Characteristics (continued)

C_L = 50pF; over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	T_A = 25°C			-40°C to 125°C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHZ}	$\overline{OE}$	Y	C_L = 15pF	5V		5.2	7.2	1		8.5	ns
t_{PLZ}						5.2	7.2	1		8.5	ns
t_{PLH}	A	Y	C_L = 50pF	2V			26.5	1		30	ns
t_{PHL}							26.5	1		30	ns
t_{PZH}	$\overline{OE}$	Y	C_L = 50pF	2V			32.5	1		36.5	ns
t_{PZL}							32.5	1		36.5	ns
t_{PHZ}	$\overline{OE}$	Y	C_L = 50pF	2V			32	1		36.5	ns
t_{PLZ}							32	1		36.5	ns
t_{PLH}	A	Y	C_L = 50pF	3.3V		7.8	11	1		12.5	ns
t_{PHL}						7.8	11	1		12.5	ns
t_{PZH}	$\overline{OE}$	Y	C_L = 50pF	3.3V		9.1	14.1	1		16	ns
t_{PZL}						9.1	14.1	1		16	ns
t_{PHZ}	$\overline{OE}$	Y	C_L = 50pF	3.3V		10.3	14	1		16	ns
t_{PLZ}						10.3	14	1		16	ns
t_{PLH}	A	Y	C_L = 50pF	5V		5.1	7.5	1		8.5	ns
t_{PHL}						5.1	7.5	1		8.5	ns
t_{PZH}	$\overline{OE}$	Y	C_L = 50pF	5V		6.2	9.3	1		10.5	ns
t_{PZL}						6.2	9.3	1		10.5	ns
t_{PHZ}	$\overline{OE}$	Y	C_L = 50pF	5V		6.7	9.2	1		10.5	ns
t_{PLZ}						6.7	9.2	1		10.5	ns
$t_{sk(o)}$			C_L = 50pF	2V			2			2	ns
$t_{sk(o)}$			C_L = 50pF	3.3V			1.5			1.5	ns
$t_{sk(o)}$			C_L = 50pF	5V			1			1	ns

5.7 Noise Characteristics

VCC = 5V, CL = 50pF, TA = 25°C

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}				V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}				V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}				V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

5.8 Typical Characteristics

T_A = 25°C (unless otherwise noted)

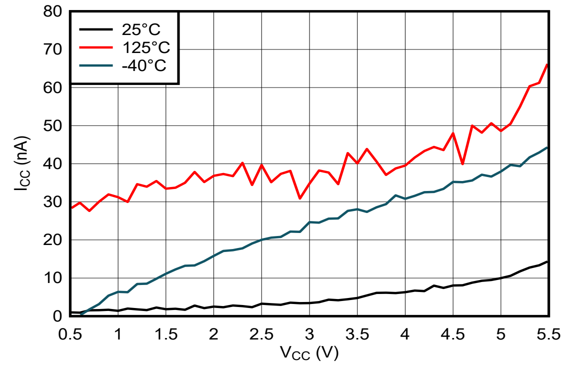


Figure 5-1. Supply Current Across Supply Voltage

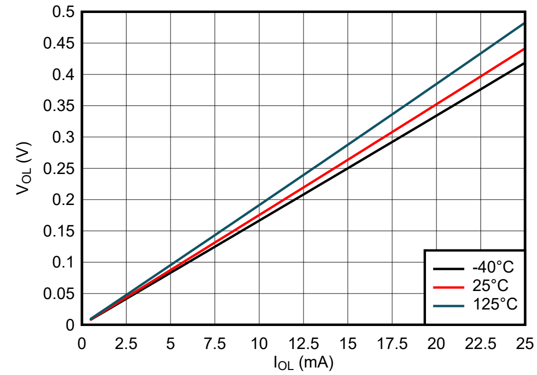


Figure 5-2. Output Voltage vs Current in LOW State; 5V Supply

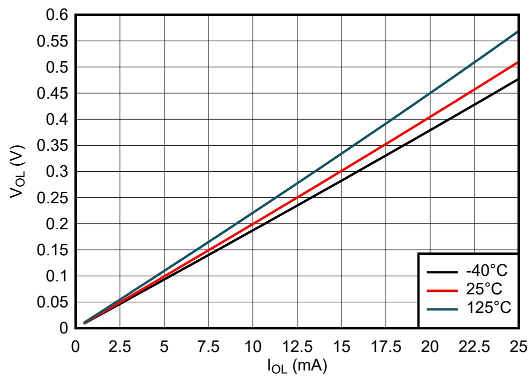


Figure 5-3. Output Voltage vs Current in LOW State; 3.3V Supply

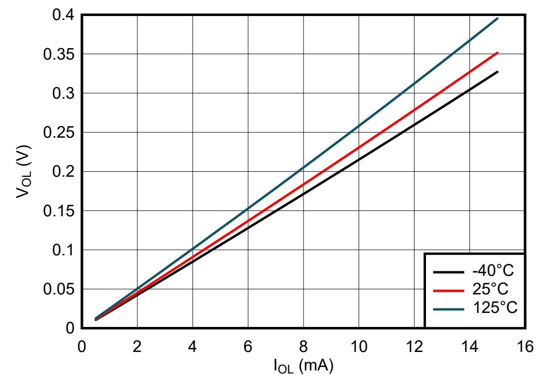
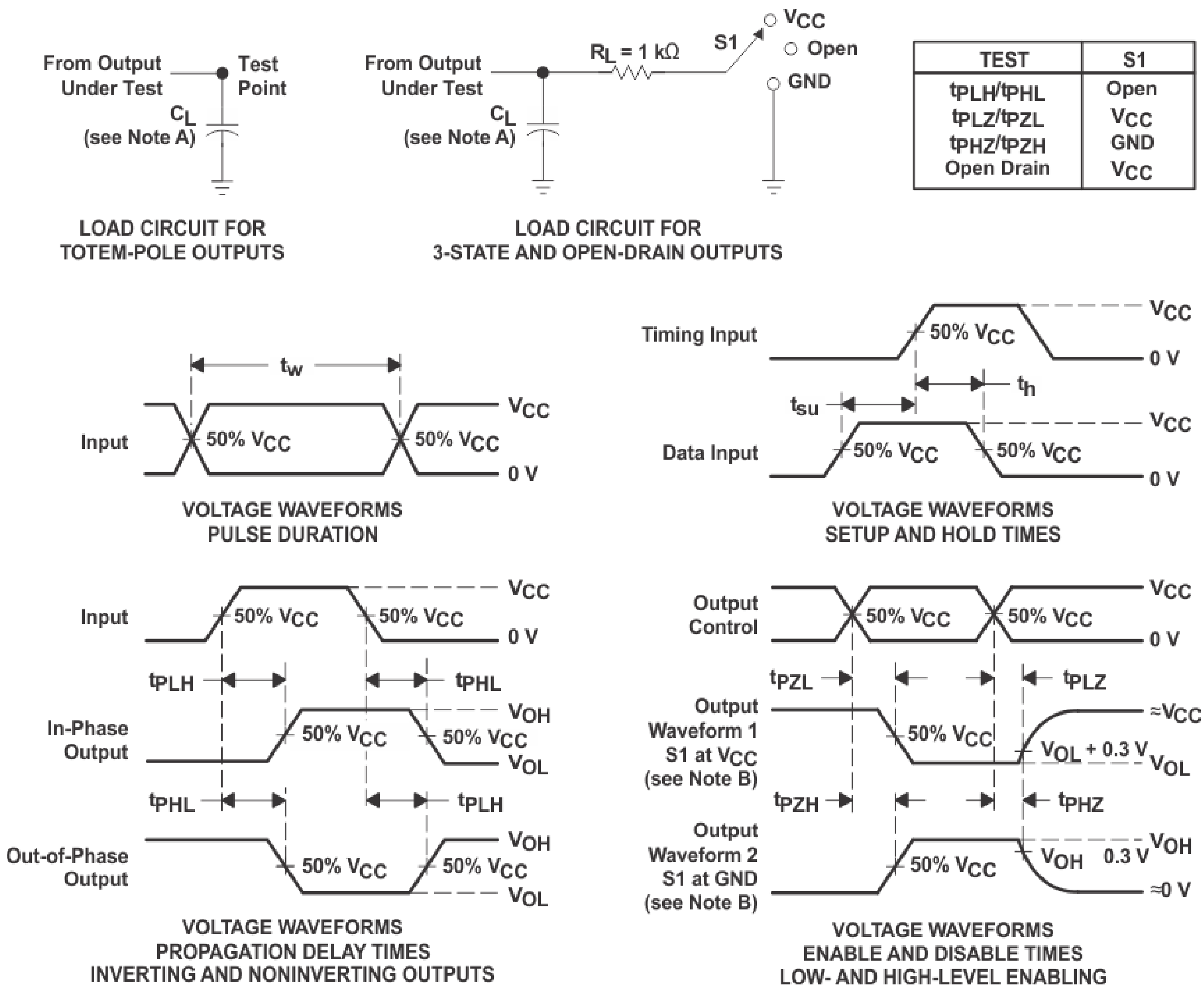


Figure 5-4. Output Voltage vs Current in LOW State; 2.5V Supply

6 Parameter Measurement Information



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

- A. C_L includes probe and jig capacitance
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_O = 50Ω, t_r ≤ 3ns, t_f ≤ 3ns.
- D. The outputs are measured one at a time with one input transition per measurement. E. All parameters and waveforms are not applicable to all devices.

Figure 6-1. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

The SNx4AHC240 devices are organized as two 4-bit buffers/line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

To place the device in the high-impedance state during power up or power down, tie $\overline{OE}$ to V_{CC} through a pullup resistor; the current-sinking capability of the driver determines the minimum value of the resistor.

7.2 Functional Block Diagram

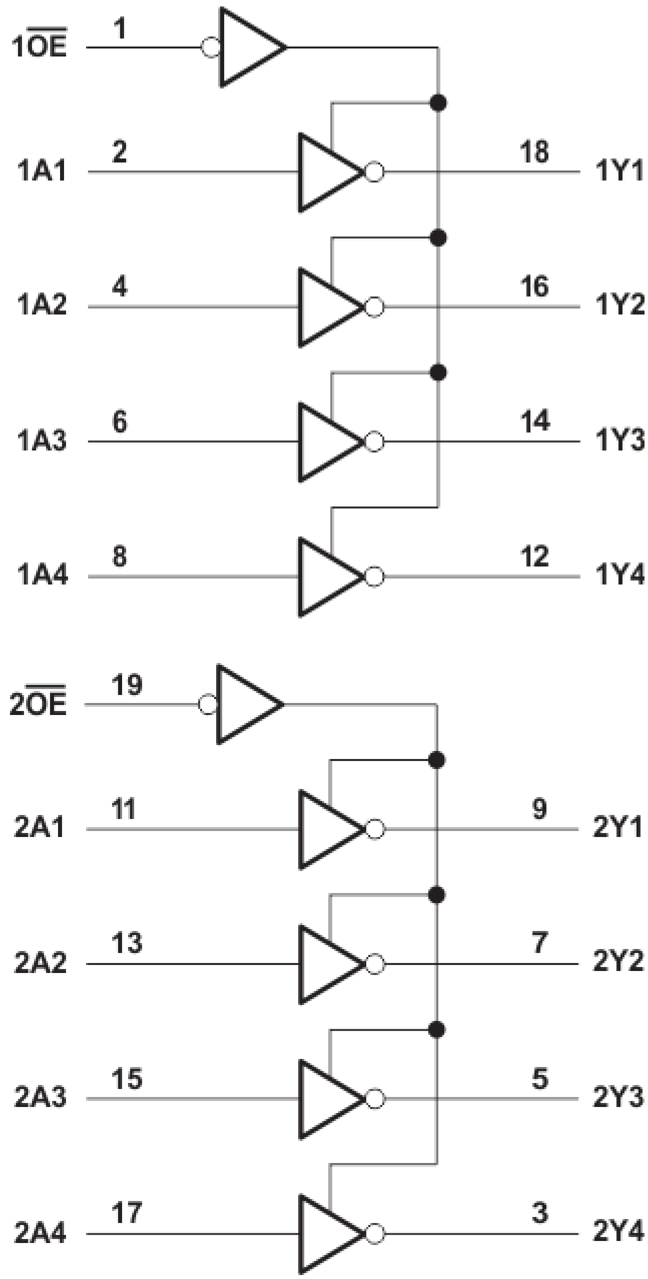


Figure 7-1. Logic Diagram (Positive Logic)

7.3 Feature Description

7.4 Device Functional Modes

Table 7-1. Function Table (Each Buffer)

INPUTS[1]		OUTPUT[2]
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care
(2) H = Driving High, L = Driving Low, Z = High Impedance State

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The SNx4AHC240 device is a high drive CMOS device that can be used for a multitude of bus-interface type applications where the data needs to be retained or latched. It can produce 24mA of drive current at 3.3V making it ideal for driving multiple outputs and also good for high-speed applications up to 100MHz. The inputs are 5.5V tolerant allowing it to translate down to V_{CC}.

8.2 Typical Application

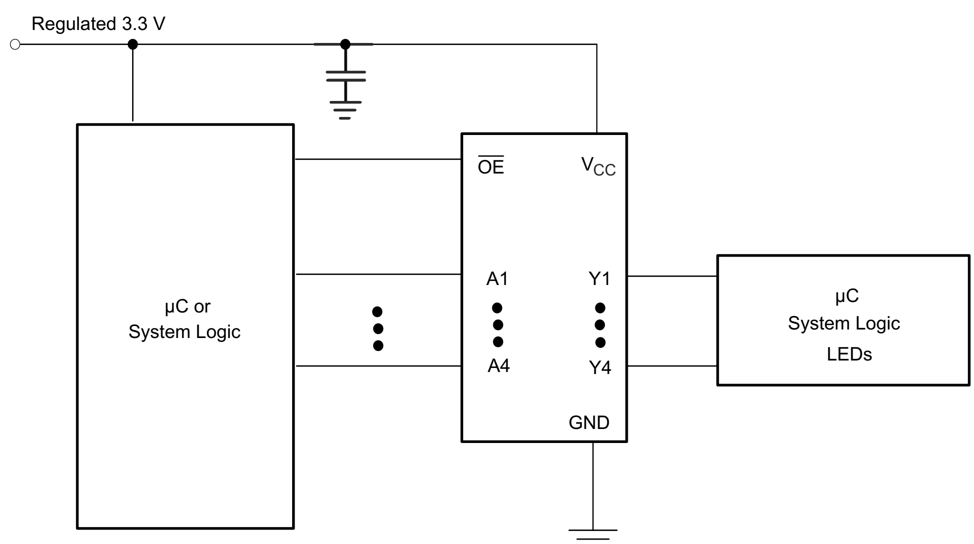


Figure 8-1. Typical Application Diagram

8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads; therefore, routing and load conditions should be considered to prevent ringing.

8.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   - Rise time and fall time specs: See (Δt/ΔV) in the *Recommended Operating Conditions* table.
   - Specified high and low levels: See (V_{IH} and V_{IL}) in the *Recommended Operating Conditions* table.
   - Inputs are overvoltage tolerant allowing them to go as high as 5.5V at any valid V_{CC}.
2. Recommend Output Conditions
   - Load currents should not exceed 25mA per output and 50mA total for the part.
   - Outputs should not be pulled above V_{CC}.

8.2.3 Application Curves

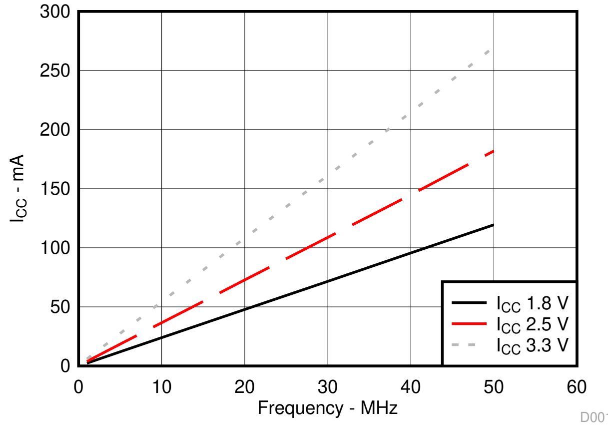


Figure 8-2. I_{CC} vs Frequency

8.3 Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in *Section 5.3* .

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends 0.1µF and if there are multiple V_{CC} terminals, then TI recommends .01µF or .022µF for each power terminal. It is okay to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1µF and 1µF are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple bit logic devices inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused (for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used). Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. The following rules specify what must be observed under all circumstances.

All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever makes more sense or is more convenient. It is generally okay to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, then it will disable the outputs section of the part when asserted. This does not disable the input section of the IOs, so they cannot float when disabled.

8.4.2 Layout Example

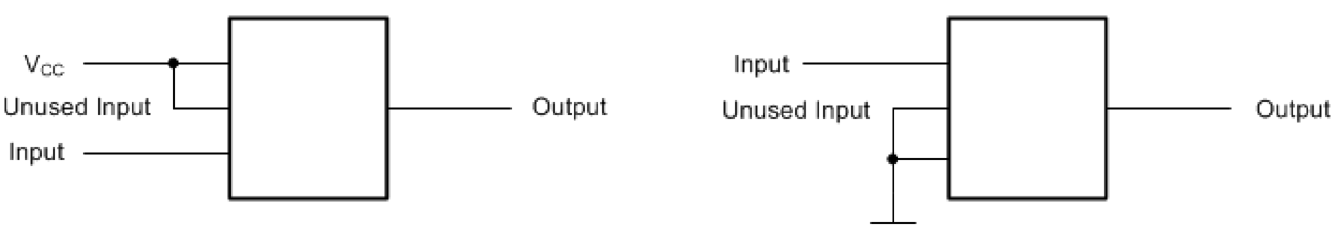


Figure 8-3. Layout Recommendation

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Implications of Slow or Floating CMOS Inputs*
- Texas Instruments, *Understanding Schmitt Triggers*

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

Changes from Revision I (April 2023) to Revision J (August 2024) **Page**

- Added package size and military packages to *Device Information* table....................1
- Updated RθJA values: PW = 83 to 116.8, DW = 58 to 81.1, all values in °C/W 5

Changes from Revision H (July 2003) to Revision I (April 2023) **Page**

- Added *Package Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Device Functional Modes,*Application and Implementation section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9680701Q2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9680701Q2A SNJ54AHC 240FK	Samples
5962-9680701QRA	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9680701QR A SNJ54AHC240J	Samples
5962-9680701QSA	ACTIVE	CFP	W	20	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9680701QS A SNJ54AHC240W	Samples
SN74AHC240DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	-40 to 85	AHC240	
SN74AHC240DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC240	Samples
SN74AHC240N	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74AHC240N	Samples
SN74AHC240NSR	ACTIVE	SOP	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC240	Samples
SN74AHC240PW	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI	-40 to 85	HA240	
SN74AHC240PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA240	Samples
SNJ54AHC240FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9680701Q2A SNJ54AHC 240FK	Samples
SNJ54AHC240J	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9680701QR A SNJ54AHC240J	Samples
SNJ54AHC240W	ACTIVE	CFP	W	20	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9680701QS A SNJ54AHC240W	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54AHC240, SN74AHC240 :

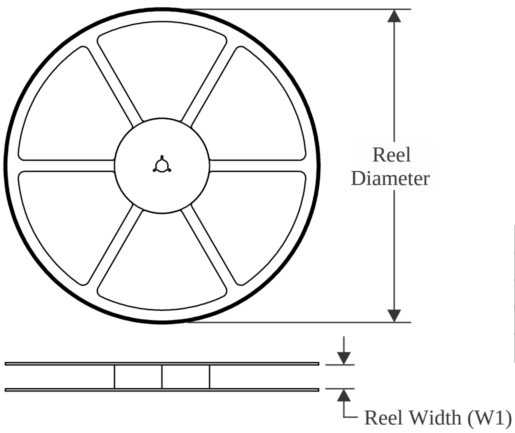
- Catalog : SN74AHC240
- Automotive : SN74AHC240-Q1, SN74AHC240-Q1
- Military : SN54AHC240

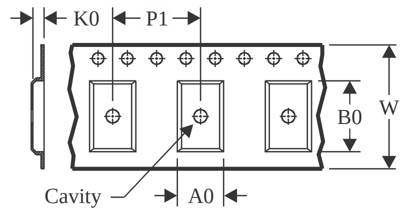
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

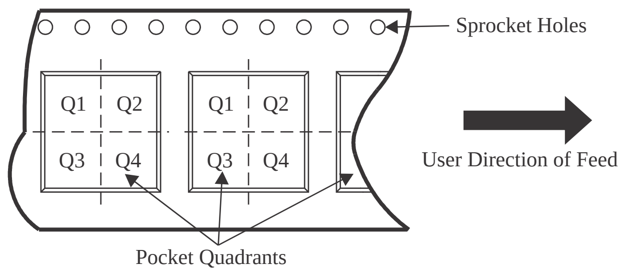
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION





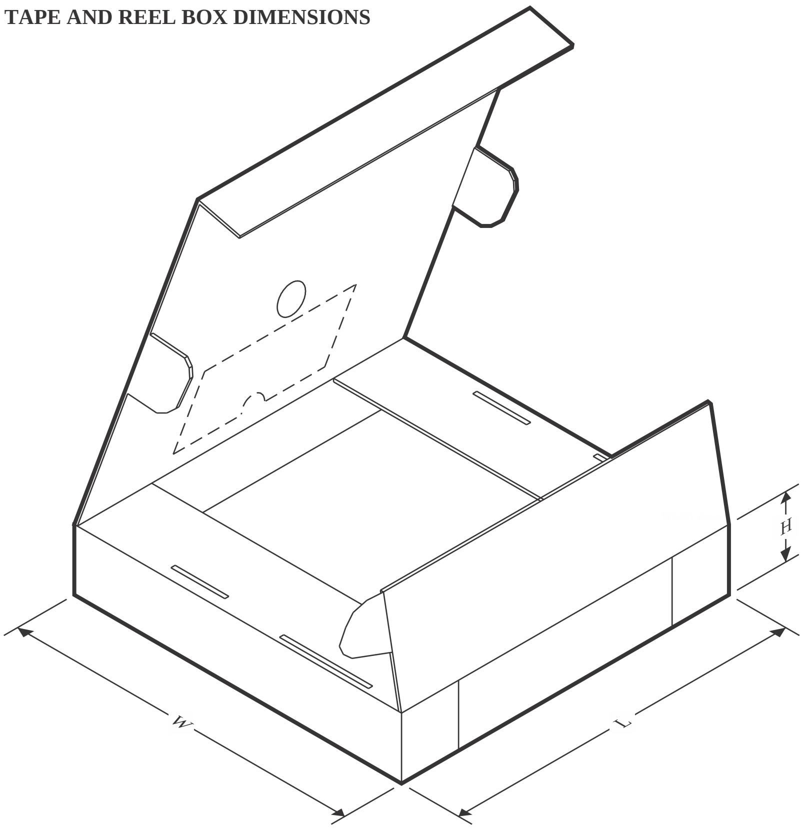
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC240DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74AHC240DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74AHC240NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74AHC240PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

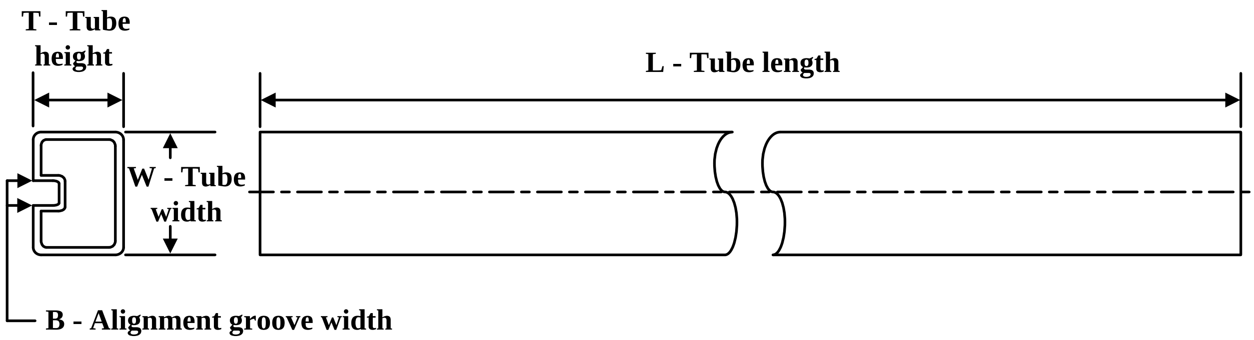
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC240DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74AHC240DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74AHC240NSR	SOP	NS	20	2000	367.0	367.0	45.0
SN74AHC240PWR	TSSOP	PW	20	2000	356.0	356.0	35.0

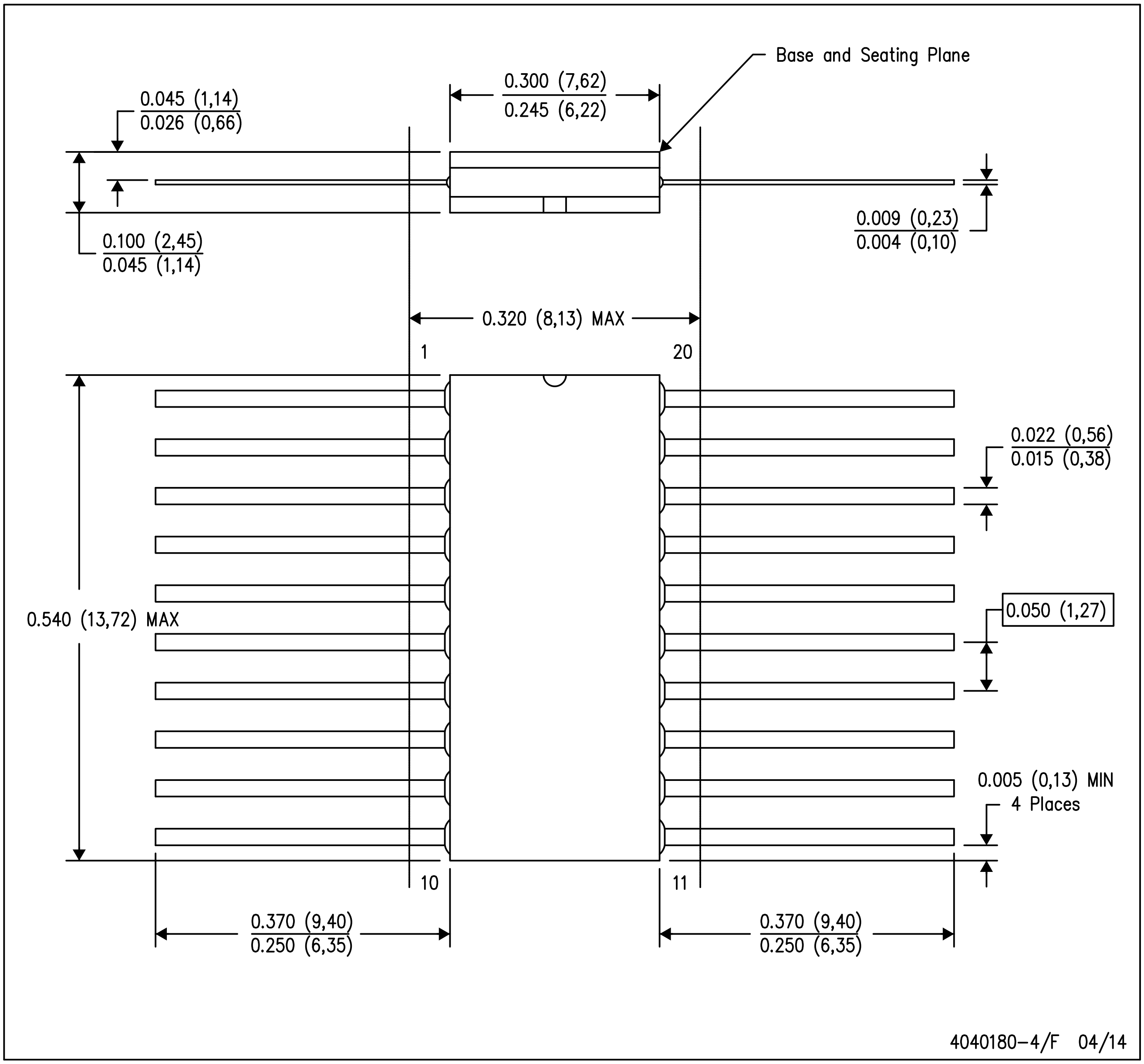
TUBE



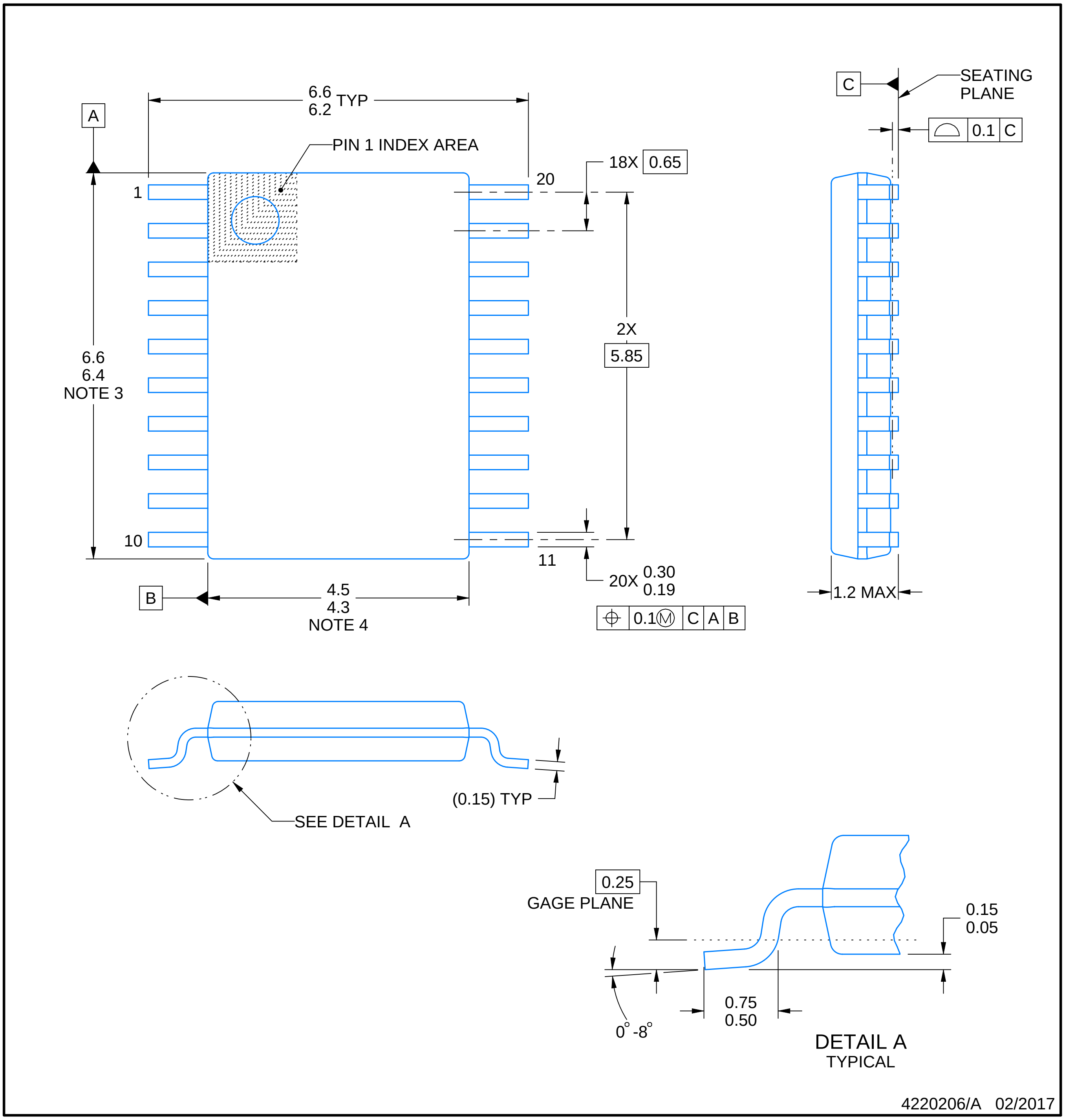
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9680701Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9680701QSA	W	CFP	20	25	506.98	26.16	6220	NA
SN74AHC240N	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54AHC240FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AHC240W	W	CFP	20	25	506.98	26.16	6220	NA

W (R–GDFP–F20) CERAMIC DUAL FLATPACK



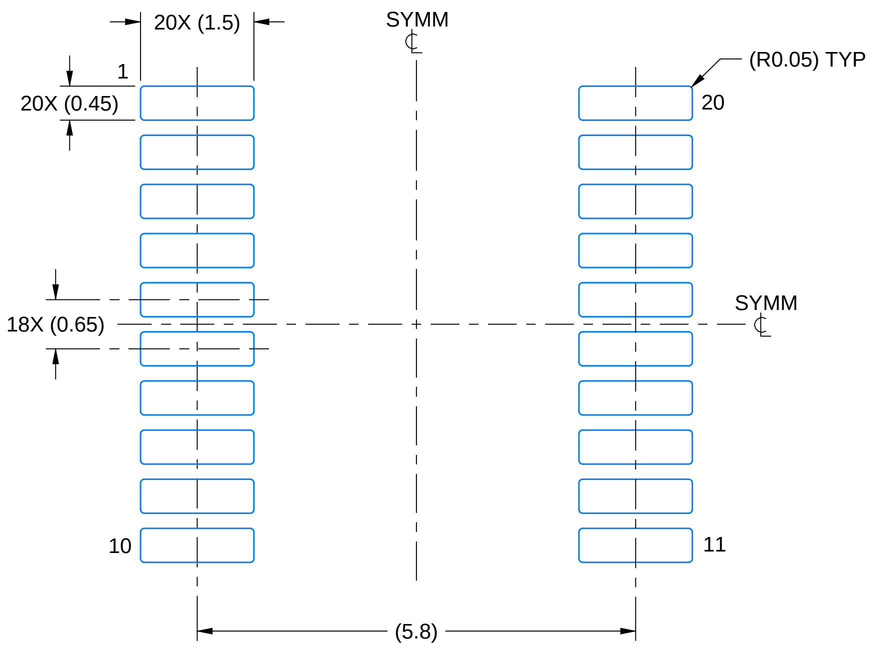
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil–Std 1835 GDFP2–F20



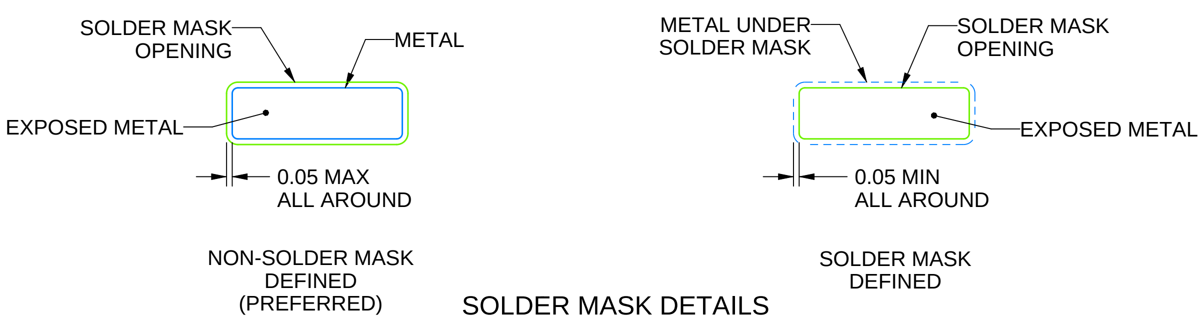
4220206/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

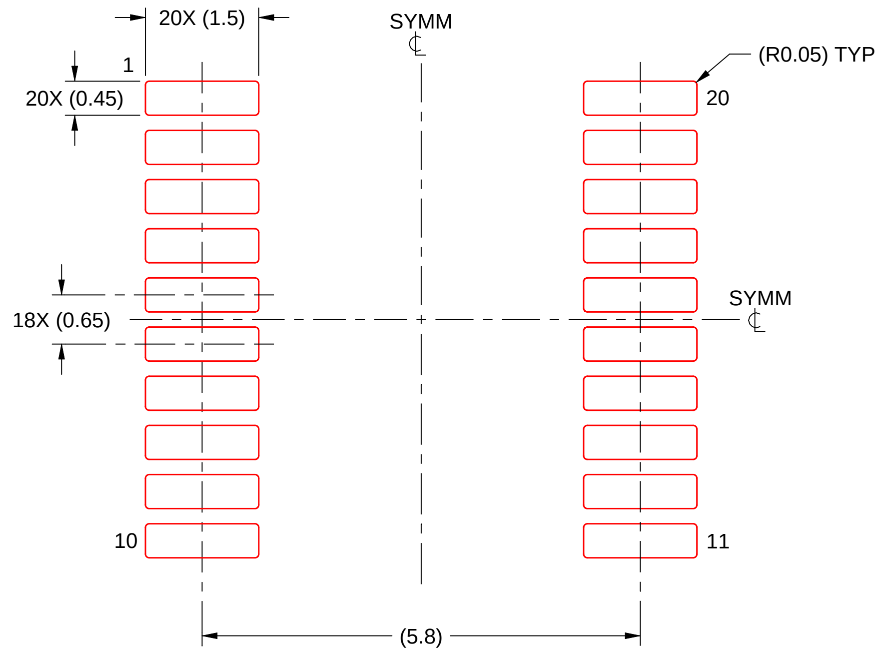


SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

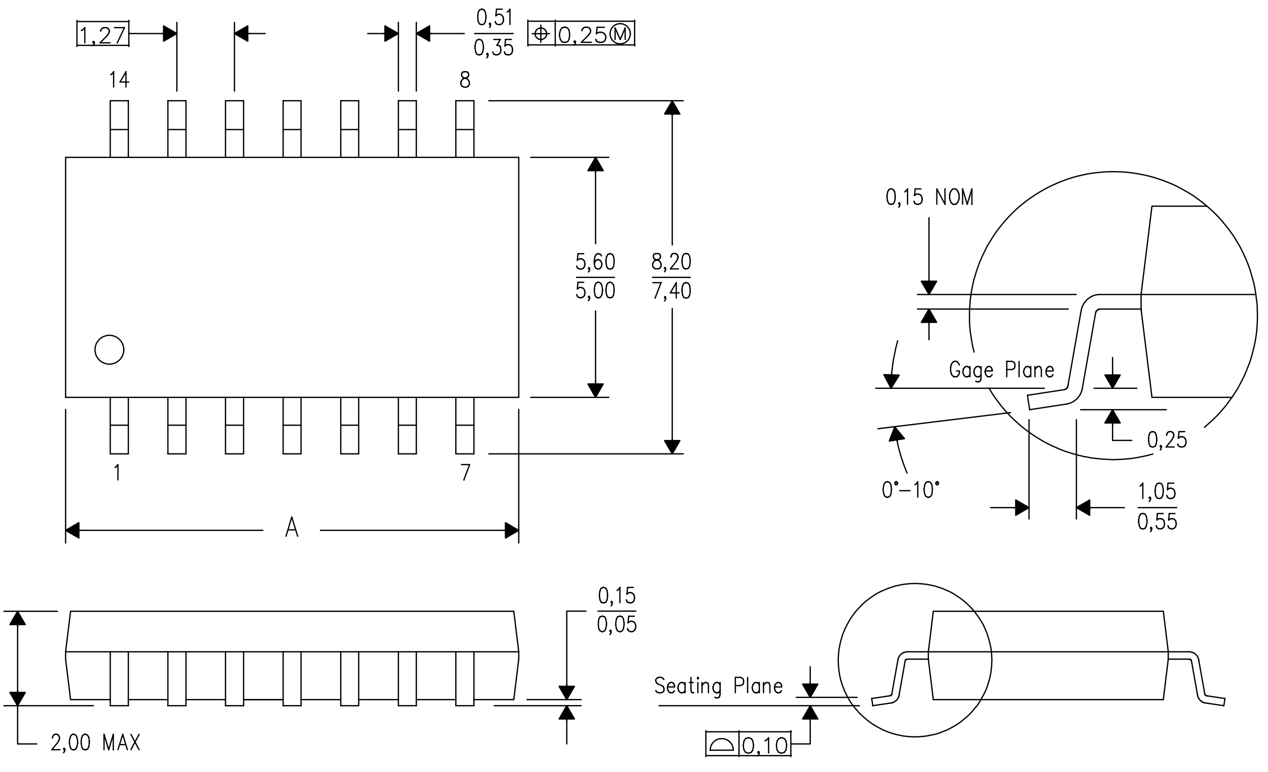
4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



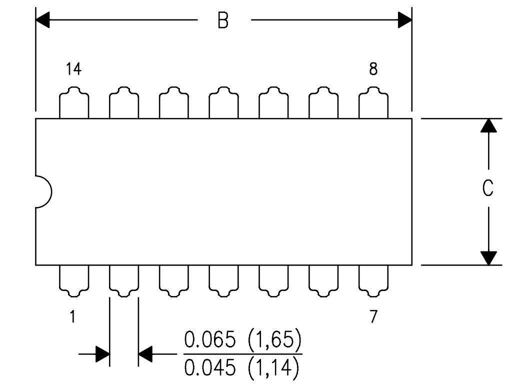
DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

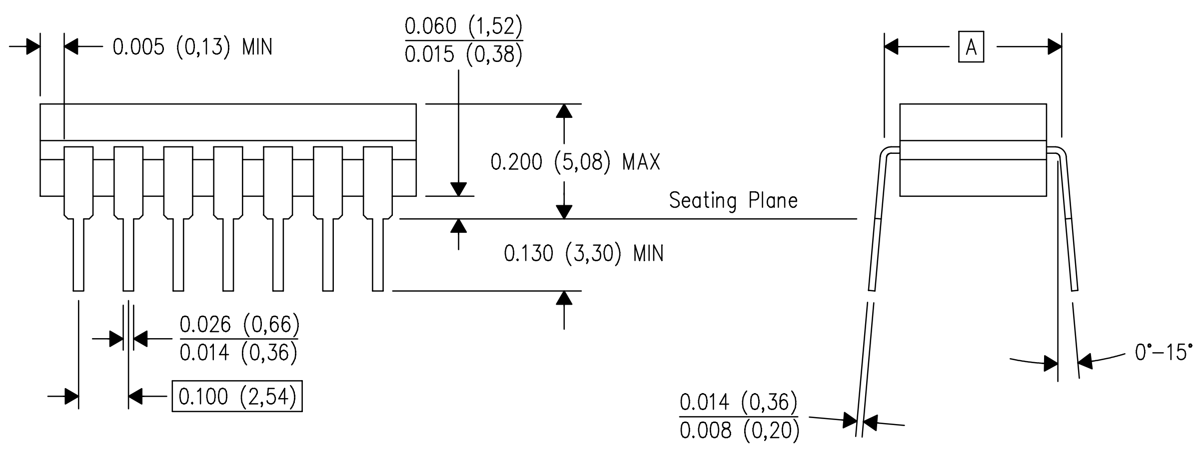
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R–GDIP–T**) CERAMIC DUAL IN–LINE PACKAGE

14 LEADS SHOWN



PINS ** / DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

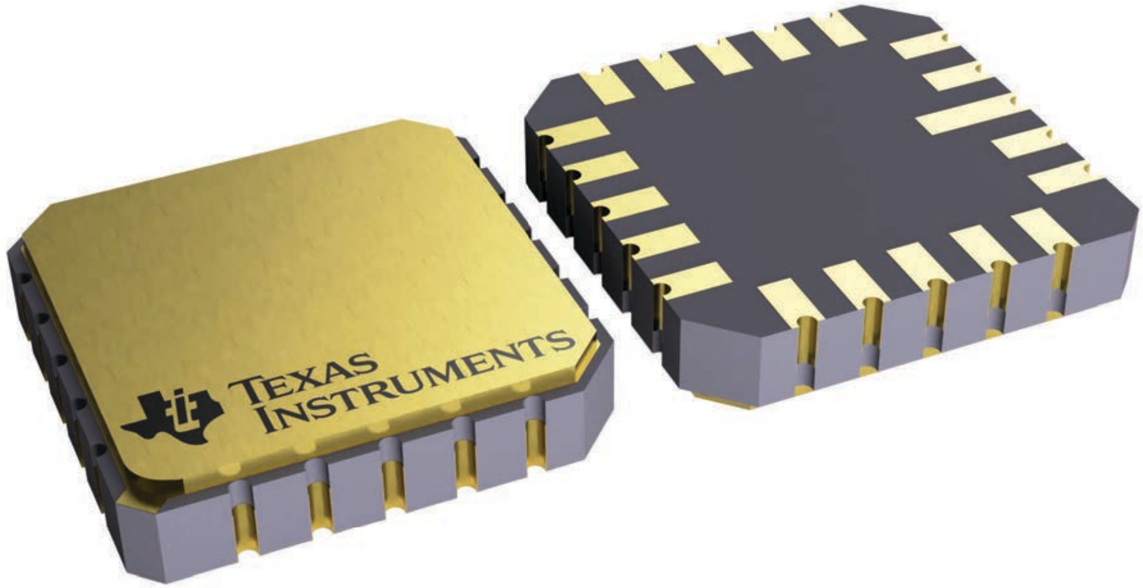
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

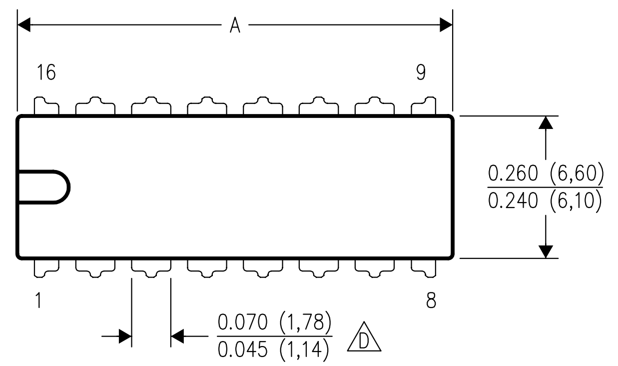
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



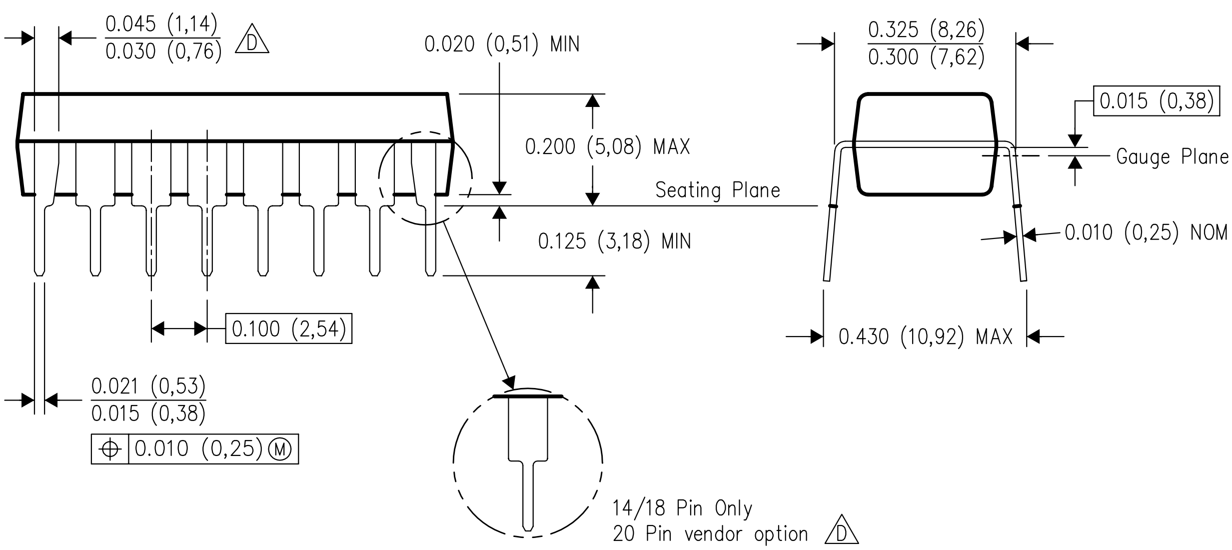
4229370\/A\

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

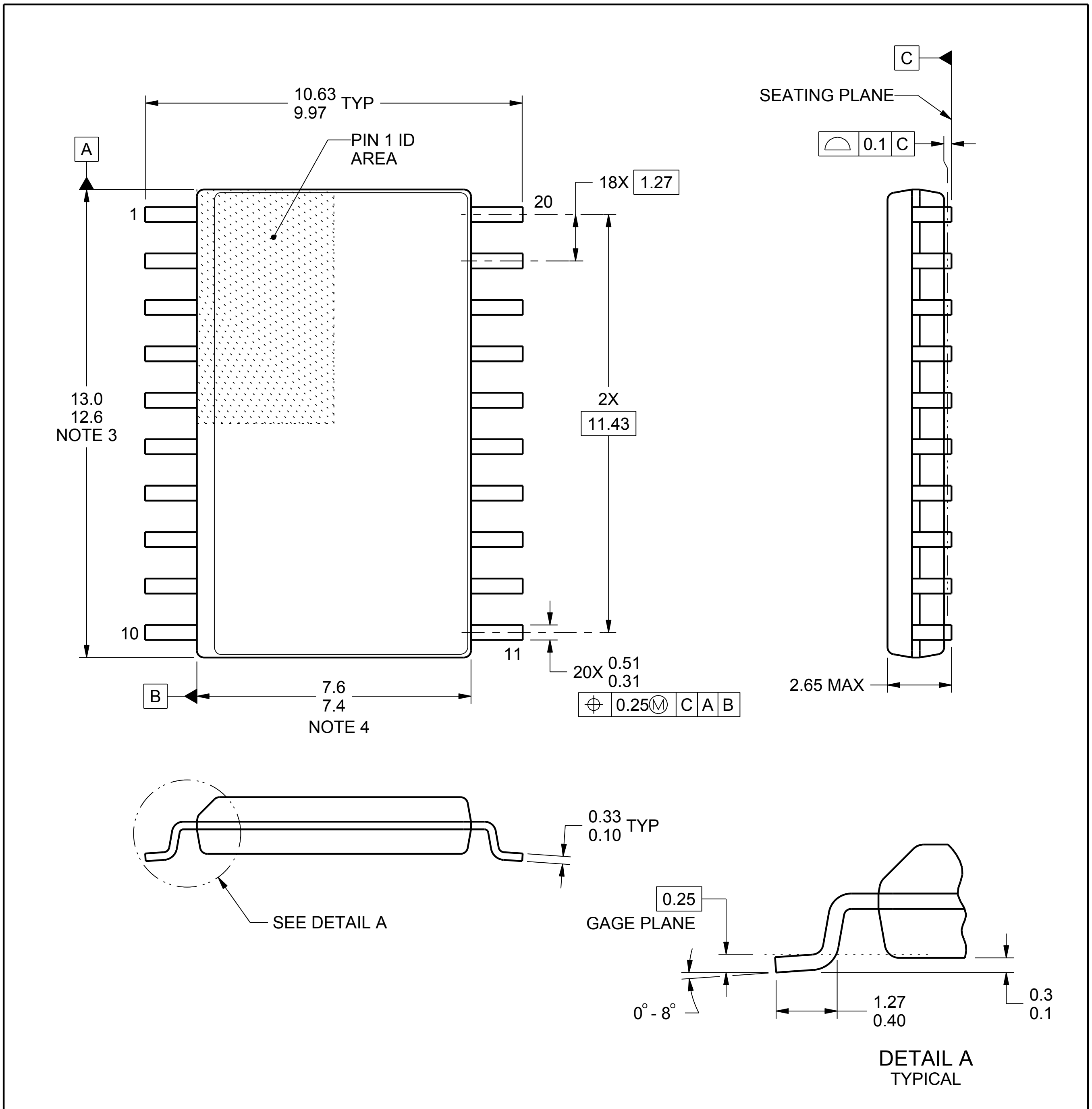


PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
(C) MS–001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

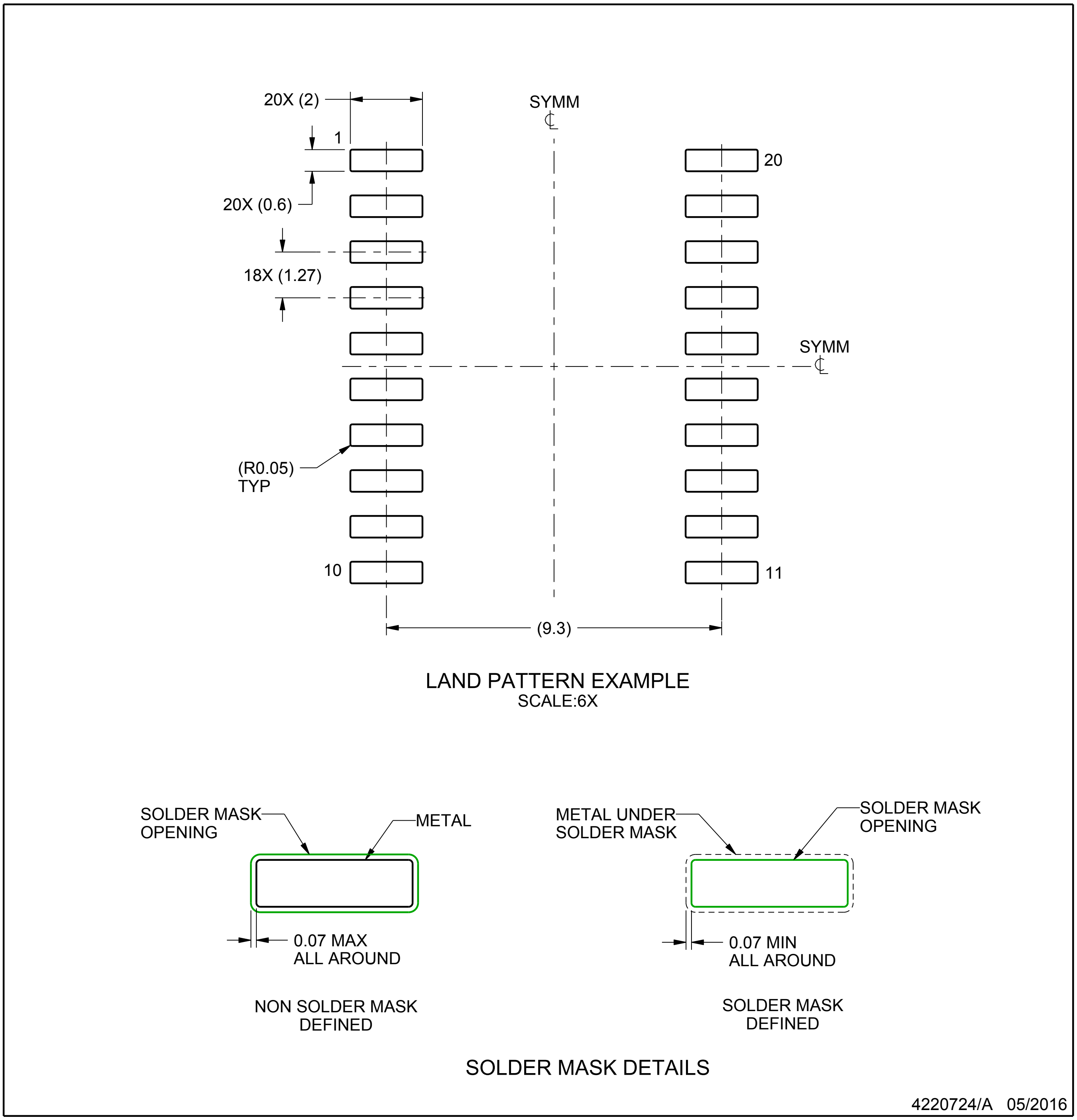
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- (C) Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
- (D) The 20 pin end lead shoulder width is a vendor option, either half or full width.



4220724/A 05/2016

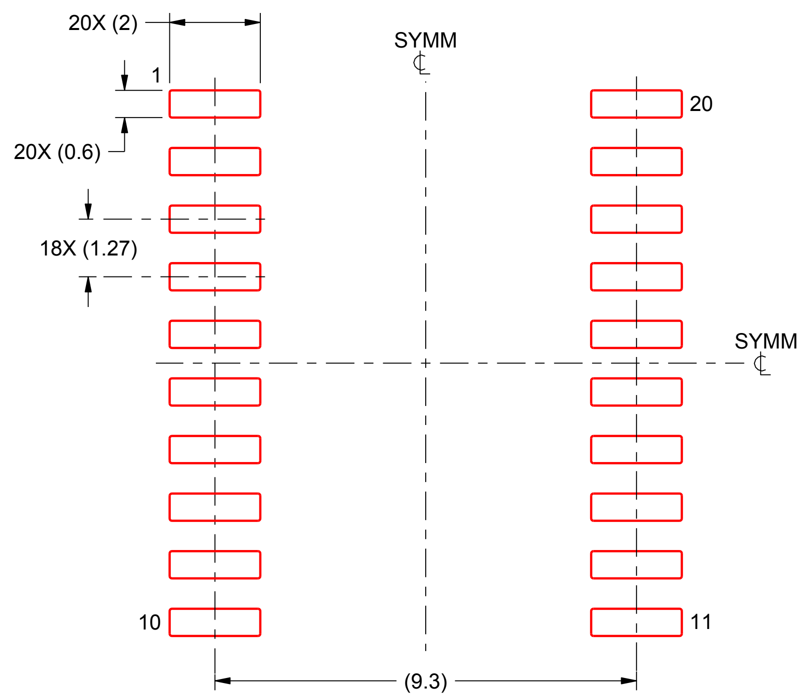
NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.