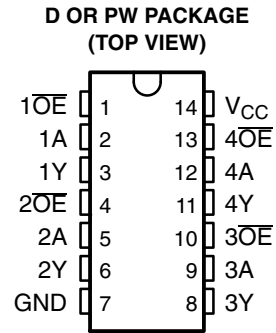


SN74AHC125Q QUADRUPLE BUS BUFFER GATE WITH 3-STATE OUTPUTS

SGDS015 – FEBRUARY 2002

- Q Devices Meet Automotive Performance Requirements
- Customer-Specific Configuration Control Can Be Supported Along With Major-Change Approval
- EPIC™ (Enhanced-Performance Implanted CMOS) Process
- Operating Range 2-V to 5.5-V V_{CC}
- Latch-Up Performance Exceeds 250 mA Per JESD 17



description

The SN74AHC125Q is a quadruple bus buffer gate featuring independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (\overline{OE}) input is high. When \overline{OE} is low, the respective gate passes the data from the A input to its Y output.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
	SOIC – D	Tape and reel		
–40°C to 125°C	SOIC – D	Tape and reel	SN74AHC125QDR	AHC125Q
	TSSOP – PW	Tape and reel	SN74AHC125QPWR	HA125Q

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (each buffer)

INPUTS		OUTPUT
\overline{OE}	A	Y
L	H	H
L	L	L
H	X	Z



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

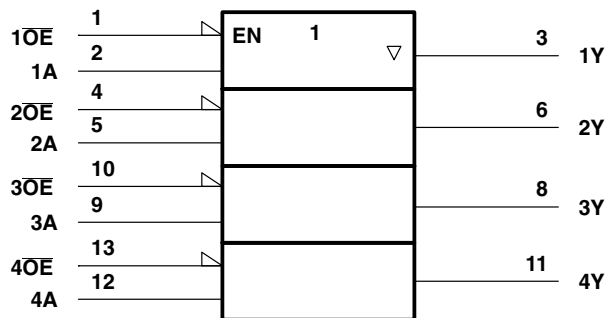
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SN74AHC125Q QUADRUPLE BUS BUFFER GATE WITH 3-STATE OUTPUTS

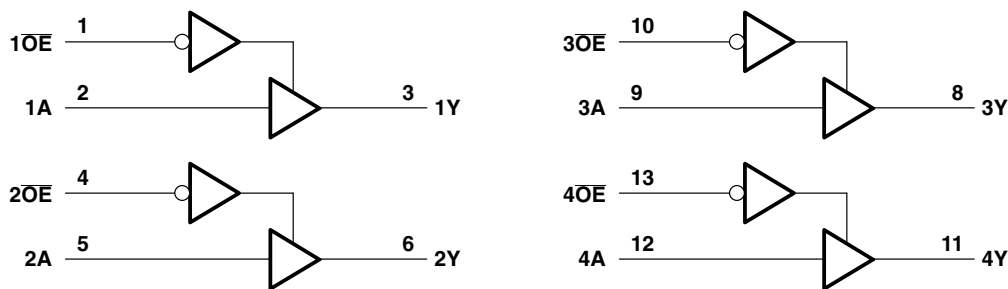
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Output voltage range, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND	± 50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package	86°C/W
PW package	113°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

SN74AHC125Q QUADRUPLE BUS BUFFER GATE WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V _{CC}	Supply voltage		2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		V
		V _{CC} = 3 V	2.1		
		V _{CC} = 5.5 V	3.85		
V _{IL}	Low-level input voltage	V _{CC} = 2 V		0.5	V
		V _{CC} = 3 V		0.9	
		V _{CC} = 5.5 V		1.65	
V _I	Input voltage		0	5.5	V
V _O	Output voltage		0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V		-50	μA
		V _{CC} = 3.3 V ± 0.3 V		-4	
		V _{CC} = 5 V ± 0.5 V		-8	
I _{OL}	Low-level output current	V _{CC} = 2 V		50	μA
		V _{CC} = 3.3 V ± 0.3 V		4	
		V _{CC} = 5 V ± 0.5 V		8	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 3.3 V ± 0.3 V		100	ns/V
		V _{CC} = 5 V ± 0.5 V		20	
T _A	Operating free-air temperature		-40	125	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V _{OH}	I _{OH} = -50 μA	2 V	1.9	2		1.9	V	
		3 V	2.9	3		2.9		
		4.5 V	4.4	4.5		4.4		
	I _{OH} = -4 mA	3 V	2.58			2.48		
	I _{OH} = -8 mA	4.5 V	3.94			3.8		
V _{OL}	I _{OL} = 50 μA	2 V			0.1	0.1	V	
		3 V			0.1	0.1		
		4.5 V			0.1	0.1		
	I _{OL} = 4 mA	3 V			0.36	0.5		
	I _{OL} = 8 mA	4.5 V			0.36	0.5		
I _I	V _I = 5.5 V or GND	0 V to 5.5 V			±0.1	±1	μA	
I _{OZ}	V _O = V _{CC} or GND	5.5 V			±0.25	±2.5	μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			4	40	μA	
C _i	V _I = V _{CC} or GND	5 V		4	10		pF	



SN74AHC125Q

QUADRUPLE BUS BUFFER GATE

WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A	Y	$C_L = 15\text{ pF}$	5.6	8	1	9.5	ns	
t_{PHL}				5.6	8	1	9.5		
t_{PZH}	\overline{OE}	Y	$C_L = 15\text{ pF}$	5.4	8	1	9.5	ns	
t_{PZL}				5.4	8	1	9.5		
t_{PHZ}	\overline{OE}	Y	$C_L = 15\text{ pF}$	7	9.7	1	11.5	ns	
t_{PLZ}				7	9.7	1	11.5		
t_{PLH}	A	Y	$C_L = 50\text{ pF}$	8.1	11.5	1	13	ns	
t_{PHL}				8.1	11.5	1	13		
t_{PZH}	\overline{OE}	Y	$C_L = 50\text{ pF}$	7.9	11.5	1	13	ns	
t_{PZL}				7.9	11.5	1	13		
t_{PHZ}	\overline{OE}	Y	$C_L = 50\text{ pF}$	9.5	13.2	1	15	ns	
t_{PLZ}				9.5	13.2	1	15		

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A	Y	$C_L = 15\text{ pF}$	3.8	5.5	1	6.5	ns	
t_{PHL}				3.8	5.5	1	6.5		
t_{PZH}	\overline{OE}	Y	$C_L = 15\text{ pF}$	3.6	5.1	1	6	ns	
t_{PZL}				3.6	5.1	1	6		
t_{PHZ}	\overline{OE}	Y	$C_L = 15\text{ pF}$	4.6	6.8	1	8	ns	
t_{PLZ}				4.6	6.8	1	8		
t_{PLH}	A	Y	$C_L = 50\text{ pF}$	5.3	7.5	1	8.5	ns	
t_{PHL}				5.3	7.5	1	8.5		
t_{PZH}	\overline{OE}	Y	$C_L = 50\text{ pF}$	5.1	7.1	1	8	ns	
t_{PZL}				5.1	7.1	1	8		
t_{PHZ}	\overline{OE}	Y	$C_L = 50\text{ pF}$	6.1	8.8	1	10	ns	
t_{PLZ}				6.1	8.8	1	10		

noise characteristics, $V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 4)

PARAMETER		MIN	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	4.4		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5		V
$V_{IL(D)}$	Low-level dynamic input voltage		1.5	V

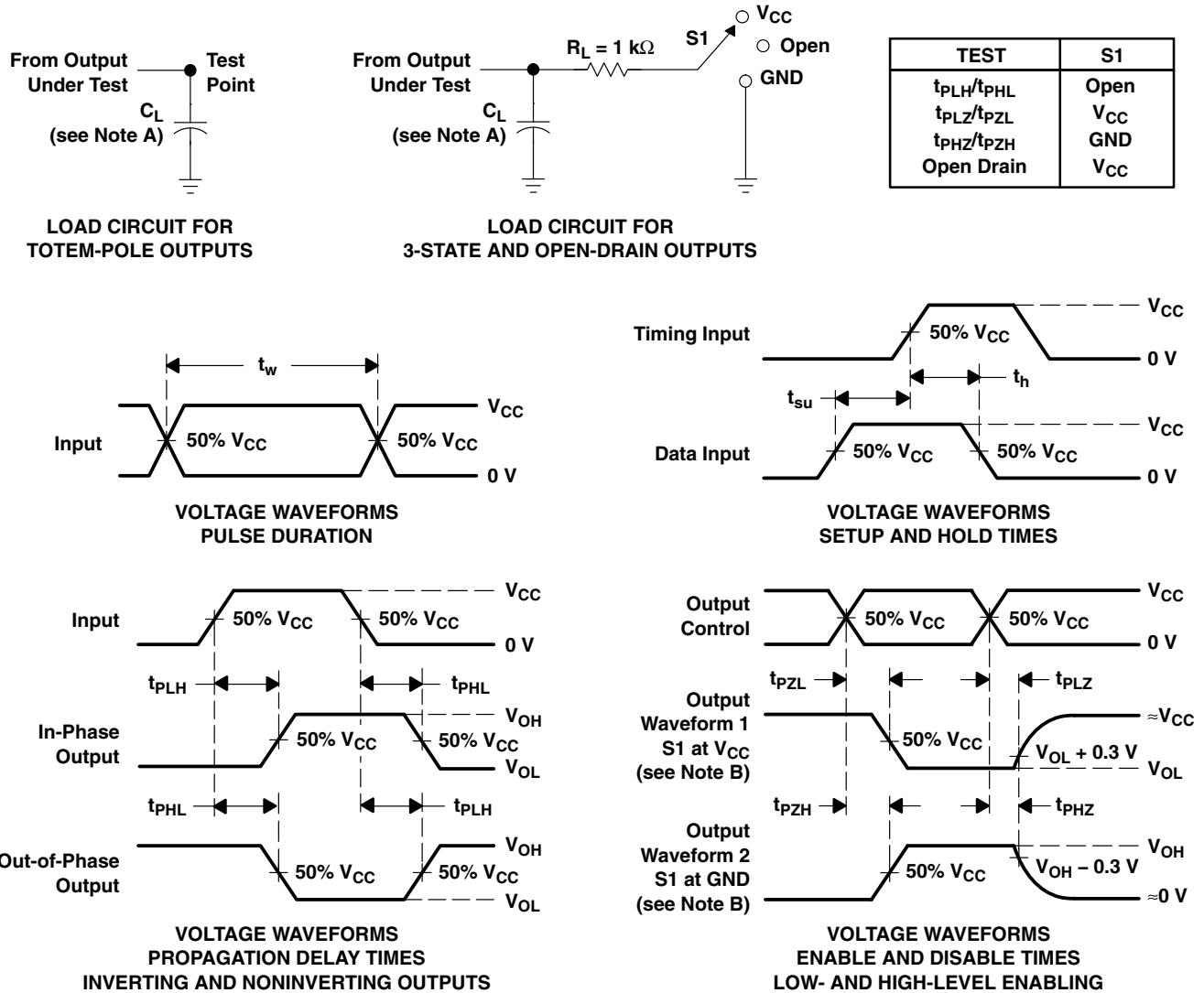
NOTE 4: Characteristics are for surface-mount packages only.

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, $f = 1\text{ MHz}$	14	pF



PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is high except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is low except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHC125QPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA125Q	Samples
SN74AHC125QPWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA125Q	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC125QPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC125QPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC125QPWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC125QPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74AHC125QPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74AHC125QPWRG4	TSSOP	PW	14	2000	356.0	356.0	35.0

PW0014A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

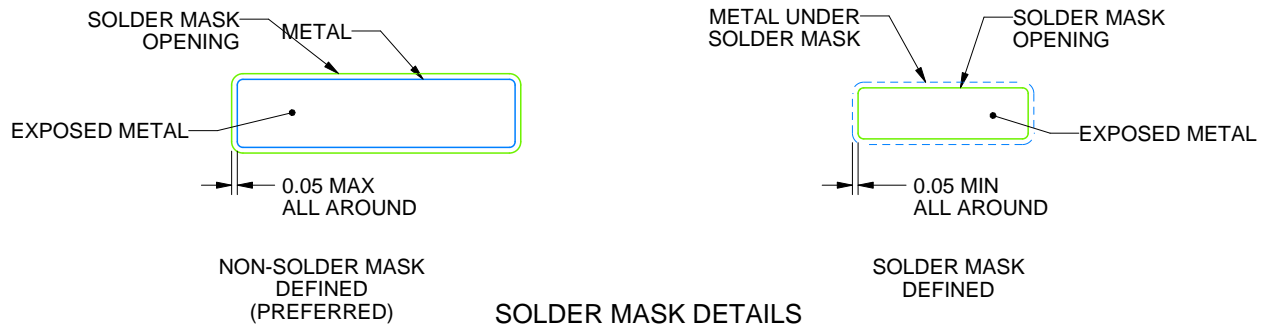
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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