Octal Bus Buffer

MC74LVX541

The MC74LVX541 is an advanced high speed CMOS octal bus buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The MC74LVX541 is a noninverting type. When either $\overline{OE1}$ or $\overline{OE2}$ are high, the terminal outputs are in the high impedance state.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 6.5 V, allowing the interface of 5.0 V systems to 3.0 V systems.

Features

- High Speed: t_{PD} = 5.0 ns (Typ) at V_{CC} = 3.3 V
- Low Power Dissipation: I_{CC} = 4 μA (Max) at T_A = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC}
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2 V to 3.6 V Operating Range
- Low Noise: V_{OLP} = 1.2 V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- Chip Complexity: 134 FETs or 33.5 Equivalent Gates
- ESD Performance:
  Human Body Model > 2000 V;
  Machine Model > 200 V
- These Devices are Pb−Free and are RoHS Compliant

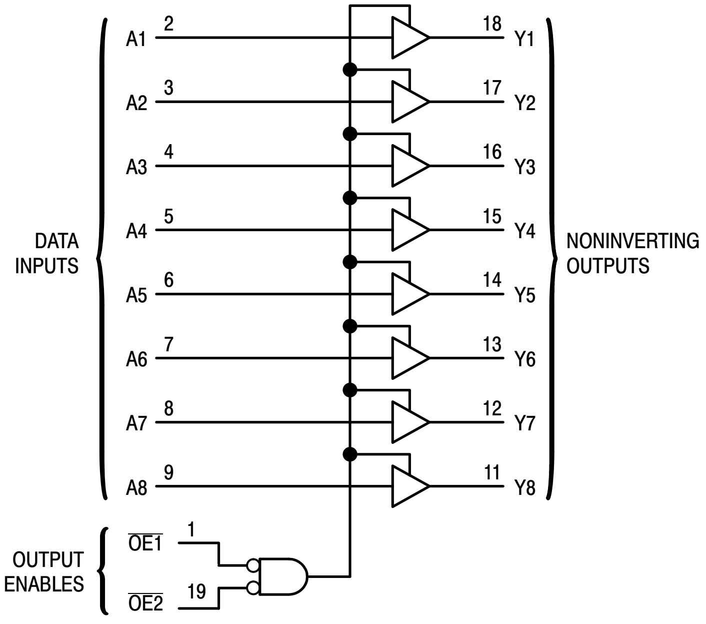
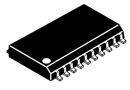
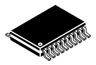


Figure 1. Logic Diagram

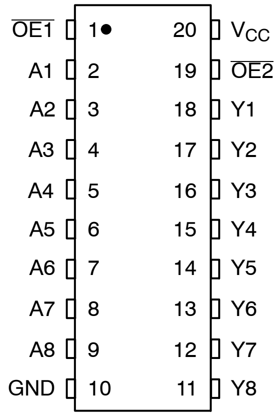


SOIC−20
DW SUFFIX
CASE 751D

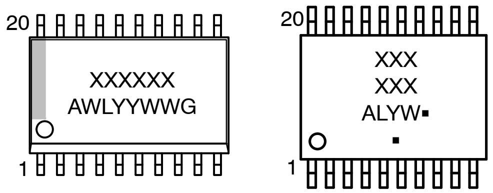


TSSOP−20
DT SUFFIX
CASE 948E

PIN ASSIGNMENT



MARKING DIAGRAMS



SOIC−20 TSSOP−20

XXXXXX = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
Y = Year
WW, W = Work Week
G or ▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

September, 2024 − Rev. 6

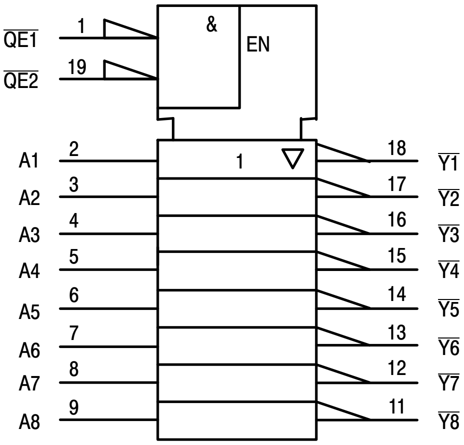


Figure 2. IEC Logic Diagram

FUNCTION TABLE

Inputs			Output Y
$\overline{OE1}$	$\overline{OE2}$	A	
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	– 0.5 to + 6.5	V
V_{in}	DC Input Voltage	– 0.5 to + 6.5	V
V_{out}	DC Output Voltage	– 0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current	– 20	mA
I_{OK}	Output Diode Current	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, SOIC TSSOP	1302 833	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	3.6	V
V_{in}	DC Input Voltage		0	5.5	V
V_{out}	DC Output Voltage		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		−40	+85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 3.3 V ± 0.3 V	0	100	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = −40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	Minimum High−Level Input Voltage		2.0 3.0 3.6	1.50 2.0 2.4			1.50 2.0 2.4		V
V_{IL}	Maximum Low−Level Input Voltage		2.0 3.0 3.6			0.50 0.80 0.80		0.50 0.80 0.80	V
V_{OH}	Minimum High−Level Output Voltage $V_{in} = V_{IH}$ or V_{IL}	I_{OH} = −50 μA I_{OH} = −50 μA I_{OH} = −4 mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V
V_{OL}	Maximum Low−Level Output Voltage $V_{in} = V_{IH}$ or V_{IL}	I_{OL} = 50 μA I_{OL} = 50 μA I_{OL} = 4 mA	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V
I_{in}	Maximum Input Leakage Current	V_{in} = 5.5 V or GND	0 to 3.6			±0.1		±1.0	μA
I_{OZ}	Maximum Three−State Leakage Current	$V_{in} = V_{IL}$ or V_{IH} $V_{out} = V_{CC}$ or GND	3.6			±0.25		±2.5	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{in} = V_{CC}$ or GND	3.6			4.0		40.0	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 3.0 ns)

Symbol	Parameter	Test Conditions		T_A = 25°C			T_A = −40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, A to Y	V_{CC} = 2.7 V	C_L = 15 pF C_L = 50 pF		5.0 7.5	7.0 10.5	1.0 1.0	8.5 12.0	ns
		V_{CC} = 3.3 ± 0.3 V	C_L = 15 pF C_L = 50 pF		3.5 5.0	5.0 7.0	1.0 1.0	6.0 8.0	
t_{PZL}, t_{PZH}	Output Enable TIme, $\overline{OE}$ to Y	V_{CC} = 2.7 V R_L = 1 kΩ	C_L = 15 pF C_L = 50 pF		6.8 9.3	10.5 14.0	1.0 1.0	12.5 16.0	ns
		V_{CC} = 3.3 ± 0.3 V R_L = 1 kΩ	C_L = 15 pF C_L = 50 pF		4.7 6.2	7.2 9.2	1.0 1.0	8.5 10.5	
t_{PLZ}, t_{PHZ}	Output Disable Time, $\overline{OE}$ to Y	V_{CC} = 2.7 V R_L = 1 kΩ	C_L = 50 pF		11.2	15.4	1.0	17.5	ns
		V_{CC} = 3.3 ± 0.3 V R_L = 1 kΩ	C_L = 50 pF		6.0	8.8	1.0	10.0	
t_{OSLH}, t_{OSHL}	Output to Output Skew	V_{CC} = 2.7 V (Note 1)	C_L = 50 pF			1.5		1.5	ns
		V_{CC} = 3.3 ± 0.3 V (Note 1)	C_L = 50 pF			1.0		1.0	ns
C_{in}	Maximum Input Capacitance				4.0	10		10	pF
C_{out}	Maximum Three−State Output Capacitance (Output in High Impedance State)				6.0				pF

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Note 2)	18	pF

1. Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.
2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/8$ (per bit). C_{PD} is used to determine the no−load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns, $C_L = 50$ pF, $V_{CC} = 3.3$ V)

Symbol	Parameter	$T_A = 25°C$		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.5	0.8	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	–0.5	–0.8	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

SWITCHING WAVEFORMS

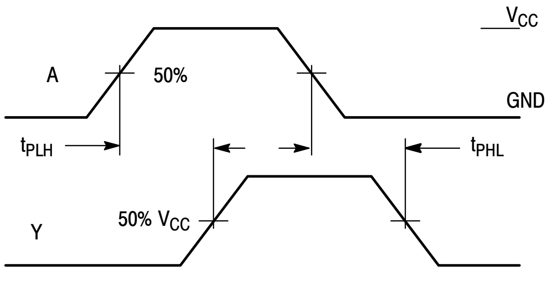


Figure 3.

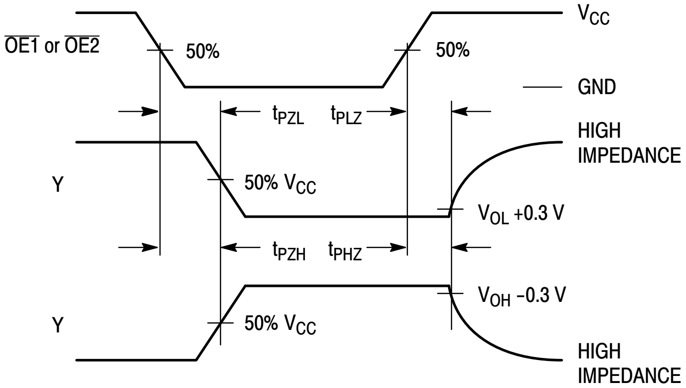
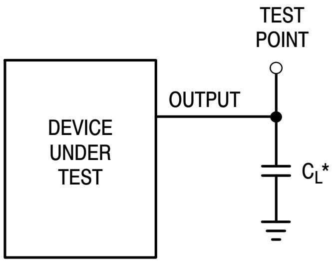


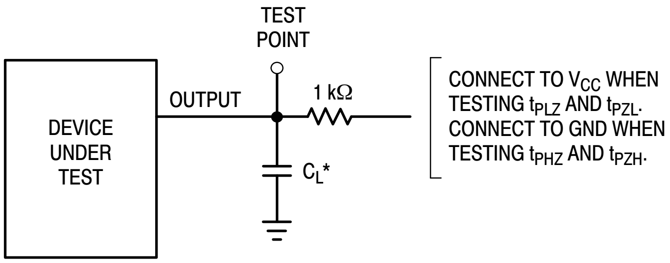
Figure 4.

TEST CIRCUITS



*Includes all probe and jig capacitance

Figure 5.



*Includes all probe and jig capacitance

Figure 6.

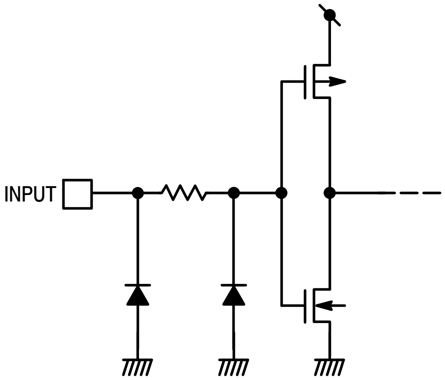
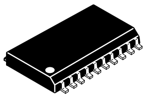


Figure 7. Input Equivalent Circuit

ORDERING INFORMATION

Device	Marking	Package	Shipping†
MC74LVX541DWG	LVX541	SOIC−20 (Pb−Free)	38 Units / Rail
MC74LVX541DTR2G	LVX 541	TSSOP−20 (Pb−Free)	2500 Tape & Reel

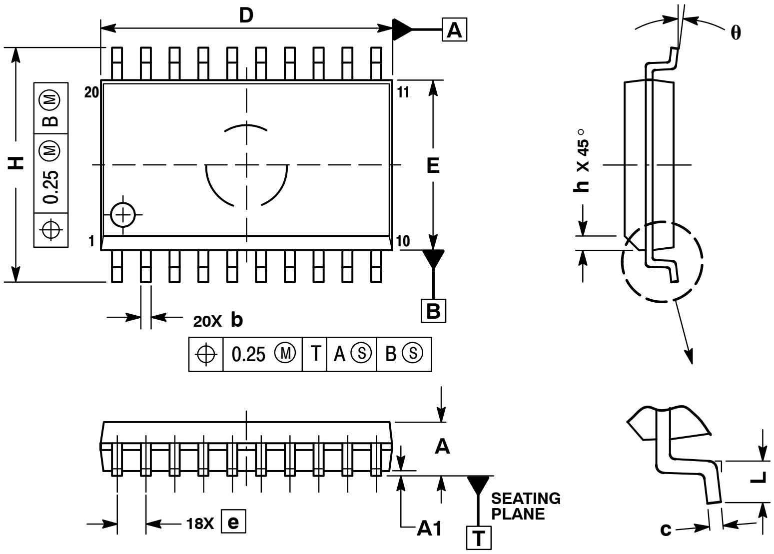
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



SCALE 1:1

SOIC−20 WB
CASE 751D−05
ISSUE H

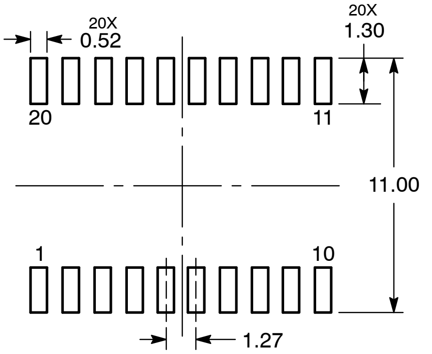
DATE 22 APR 2015



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

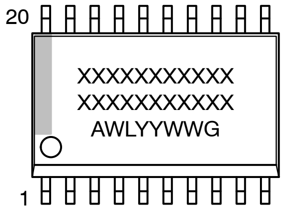
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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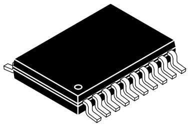
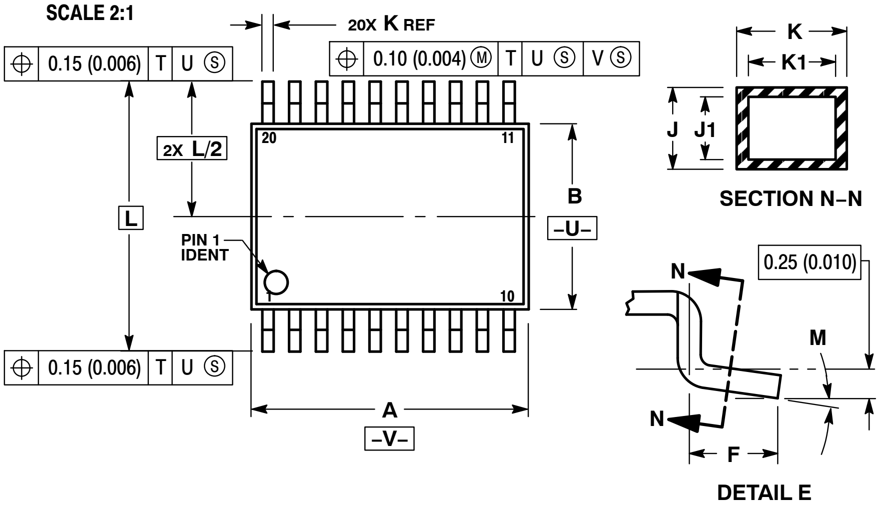
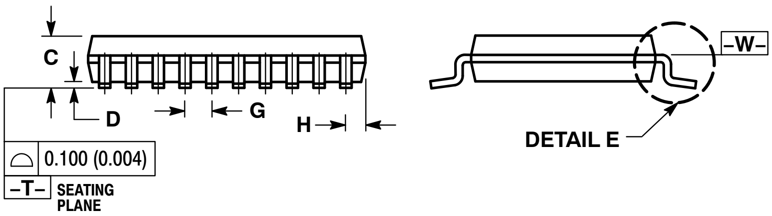
TSSOP−20 WB
CASE 948E
ISSUE D



SCALE 2:1

DATE 17 FEB 2016

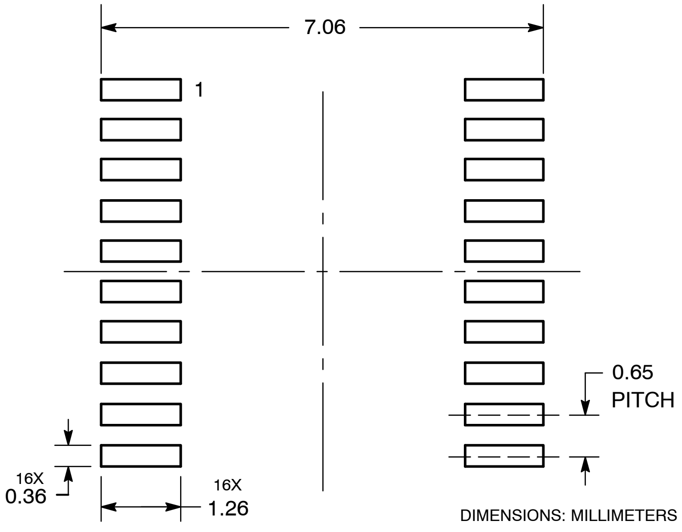




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

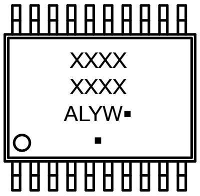
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**TSSOP−20 WB**	**PAGE 1 OF 1**

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