CD74AC540, CDx4ACT54x, CDx4AC541 Octal Buffer/Line Drivers, 3-State

1 Features

- SCR-latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST®/AS/S with significantly reduced power consumption
- Balanced propagation delays
- AC types feature 1.5V to 5.5V operation and balanced noise immunity at 30% of the supply.
- ±24mA output drive current
  - Fanout to 15 FAST®ICs
  - Drives 50Ohm transmission lines

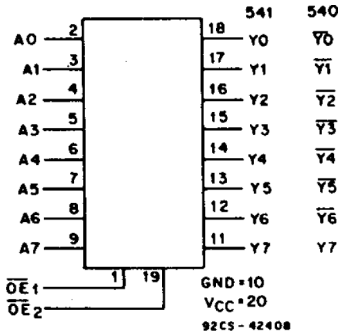
2 Description

The CD54/74AC540, -541, and CD54/74ACT540, -541 octal buffer/line drivers use the RCA ADVANCED CMOS technology. The CD54/74AC/ACT540 are inverting 3-state buffers having two active-LOW output enables. The CD54/74AC/ACT541 are non-inverting 3-state buffers having two active-LOW output enables.

Device Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE(3)
CD74AC540, CDx4ACT54x, CDx4AC541	DW (SOIC, 20)	12.8mm x 10.3mm	12.8mm x 7.5mm
	DB (SSOP, 20)	7.2mm x 7.8mm	7.2mm x 5.3mm
	N (PDIP, 20)	24.33mm x 9.4mm	24.33mm x 6.35mm

(1) For all available packages, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.



Functional Block Diagram

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3 Pin Configuration and Functions

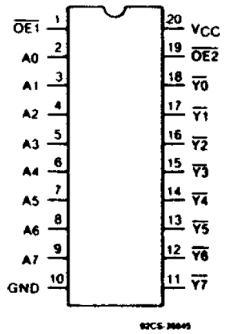


Figure 3-1. CDx4AC540, CDx4ACT540

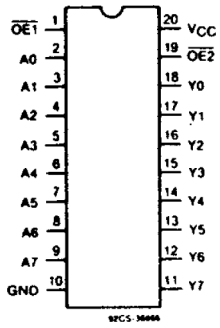


Figure 3-2. CDx4AC541, CDx4ACT541

Table 3-1. Pin Functions

PIN			
NO.	**NAME**	**I/O**[1]	**DESCRIPTION**
!MR	1	I	Master reset, active low
Q0	2	O	Output Q0
D0	3	I	Input D0
D1	4	I	Input D1
Q1	5	O	Output Q1
Q2	6	O	Output Q2
D2	7	I	Input D2
D3	8	I	Input D3
Q3	9	O	Output Q3
GND	10	-	Ground
CP	11	I	Clock, rising edge triggered
Q4	12	O	Output Q4
D4	13	I	Input D4
D5	14	I	Input D5
Q5	15	O	Output Q5
Q6	16	O	Output Q6
D6	17	I	Input D6
D7	18	I	Input D7
Q7	19	O	Output Q7
V_{CC}	20	-	Supply

1. I = input, O = output, P = power, FB = feedback, GND = ground, N/A = not applicable

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		−0.5	6	V
I_{IK}	Input diode current	(V_I < −0.5 or V_I > V_{CC} + 0.5 V)		±20	mA
I_{OK}	Output diode current	(V_O < −0.5 or V_O > V_{CC} + 0.5 V)		±50	mA
I_O	Output source or sink current per output PIN	(V_O > −0.5 or V_O < V_{CC} + 0.5 V)		±50	mA
	V_{cc} or ground current, I_{CC} or I_{GND} (1)			±100	mA
T_{stg}	Storage temperature		−65	+150	°C

(1) For up to 4 outputs per device: add ±25 mA for each additional output.

4.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

4.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage			
	(For T_A = full package-temperature range)			
	AC types	1.5	5.5	V
	ACT types	4.5	5.5	V
V_I, V_O	Input or output voltage	0	V_{CC}	V
T_A	Operating temperature	-55	+125	°C
dt/dv	Input rise and fall slew rate			
	at 1.5V to 3V (AC types)	0	50	ns/V
	at 3.6V to 5.5V (AC types)	0	20	ns/V
	at 4.5V to 5.5V (ACT types)	0	10	ns/V

(1) Unless otherwise specified, all voltages are referenced to ground.

4.4 Thermal Information

THERMAL METRIC(1)		CD74AC540, CDx4ACT54x, CDx4AC541		UNIT
		N (PDIP)	DW (SOIC)	
		20 PINS	20 PINS	
$R_{\theta JA}$	Thermal Resistance	69	101.2	°C/W

(1) The package thermal impedance is calculated in accordance with JESD 51.

4.5 Electrical Characteristics, AC Series

PARAMETER		TEST CONDITIONS		V_{CC} (V)	(T_A) - °C						UNIT
					+25		-40 to +85		-55 to +125		
		V_I (V)	I_O (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
V_{IH}	High-level input voltage			1.5	1.2	—	1.2	—	1.2	—	V
				3	2.1	—	2.1	—	2.1	—	
				5.5	3.85	—	3.85	—	3.85	—	
V_{IL}	Low-level input voltage			1.5	—	0.3	—	0.3	—	0.3	V
				3	—	0.9	—	0.9	—	0.9	
				5.5	—	1.65	—	1.65	—	1.65	
V_{OH}	High-level output voltage	V_{IH} or V_{IL} (1), (2)	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
			-0.05	3	2.9	—	2.9	—	2.9	—	
			-0.05	4.5	4.4	—	4.4	—	4.4	—	
			-4	3	2.58	—	2.48	—	2.4	—	
			-24	4.5	3.94	—	3.8	—	3.7	—	
			-75	5.5	—	—	3.85	—	—	—	
			-50	5.5	—	—	—	—	3.85	—	
V_{OL}	Low-level output voltage	V_{IH} or V_{IL} (1), (2)	0.05	1.5	—	0.1	—	0.1	—	0.1	V
			0.05	3	—	0.1	—	0.1	—	0.1	
			0.05	4.5	—	0.1	—	0.1	—	0.1	
			12	3	—	0.36	—	0.44	—	0.5	
			24	4.5	—	0.36	—	0.44	—	0.5	
			75	5.5	—	—	—	1.65	—	—	
			50	5.5	—	—	—	—	—	1.65	
I_I	Input leakage current	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
I_{OZ}	3-state leakage current	V_{IH} or V_{IL} V_O = V_{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
I_{CC}	Quiescent supply current, MSI	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA

(1) Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
(2) Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

4.6 Electrical Characteristics, ACT Series

PARAMETER		TEST CONDITIONS		V_{CC} (V)	(T_A) - °C					UNIT
					+25		-40 to +85		-55 to +125	
		V_I (V)	I_O (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
V_{IH}	High-level input voltage			4.5 to 5.5	2	—	2	—	2	—	V
V_{IL}	Low-level input voltage			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
V_{OH}	High-level output voltage	V_{IH} or V_{IL} (1), (2)	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
			-24	4.5	3.94	—	3.8	—	3.7	—	
			-75	5.5	—	—	3.85	—	—	—	
			-50	5.5	—	—	—	—	3.85	—	
V_{OL}	Low-level output voltage	V_{IH} or V_{IL} (1), (2)	0.05	4.5	—	0.1	—	0.1	—	0.1	V
			24	4.5	—	0.36	—	0.44	—	0.5	
			75	5.5	—	—	—	1.65	—	—	
			50	5.5	—	—	—	—	—	1.65	
I_I	Input leakage current	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
I_{OZ}	3-state leakage current	V_{IH} or V_{IL} V_O = V_{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
I_{CC}	Quiescent supply current, MSI	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA
	Additional quiescent supply current per input pin	V_{CC}-2.1		4.5 to 5.5	—	2.4	—	28	—	3	mA
ΔI_{CC}	TTL inputs high										
	1 unit load										

(1) Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
(2) Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

Table 4-1. Act Input Loading Table

INPUT	UNIT LOAD(2)	
	540	541
DATA	1.42	0.5
$\overline{OE1}$, $\overline{OE2}$	1.3	1.3

4.7 Switching Characteristics, AC Series

t_r, t_f = 3ns, C_L = 50pF (See Section 5)

PARAMETER			V_{CC} (V)	(T_A) - °C				UNIT
				-40 to +85		-55 to +125		
				MIN	MAX	MIN	MAX	
Propagation Delays:								
	Data to Output	AC540						
t_{PLH}			1.5	–	77	—	85	
t_{PHL}			3.3*	2.4	8.6	2.4	9.5	ns
			5†	1.8	6.2	1.7	6.8	
		AC541						
t_{PLH}			1.5	—	89	—	98	
t_{PHL}			3.3	2.8	9.9	2.7	10.9	ns
			5	2.1	7.1	2	7.8	
	Enable, to Output to Output		1.5	—	136	—	150	
t_{PZL}			3.3	4.6	16.4	4.5	18	ns
t_{PZH}			5	3.1	10.9	3	12	
	Disable to Output to Output		1.5	—	136	—	150	
t_{PLZ}			3.3	3.9	13.6	3.8	15	ns
t_{PHZ}			5	3.1	10.9	3	12	
C_{PD} ‡	Power Dissipation Capacitance	AC540	—	60 Typ.		60 Typ.		pF
		AC541	—	60 Typ.		60 Typ.		
V_{OHV}	Min. (Valley) V_{OH}	During Switching of Other Outputs (Output Under Test Not Switching)	5	4 Typ. @ 25°C				V
V_{OLP}	Max. (Peak) V_{OL}	During Switching of Other Outputs (Output Under Test Not Switching)	5	1 Typ. @ 25°C				V
C_I	Input Capacitance		—	—	10	—	10	pF
C_O	3-State Output Capacitance		—	—	15	—	15	pF

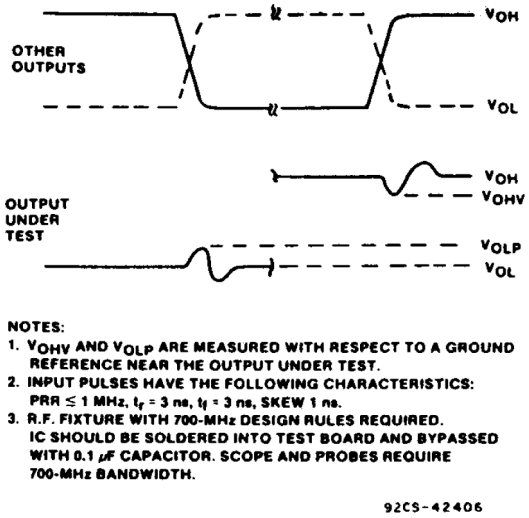
4.8 Switching Characteristics, ACT Series

t_r, t_f = 3ns, C_L = 50pF (See Section 5)

PARAMETER			V_{CC} (V)	(T_A) - °C				UNIT
				-40 to +85		-55 to =125		
				MIN	MAX	MIN	MAX	
	Propagation Delays:							
t_{PLH}	Data to Output:	ACT540	5[1]	1.9	6.5	1.8	7.2	ns
t_{PHL}		ACT541	5[1]	2.1	7.5	2.1	8.2	ns
t_{PZL}	Enable to Output		5	5	3.5	12.2	3.4	ns
t_{PZH}								
t_{PLZ}	Disable to Output		5	3.5	12.2	3.4	13.4	ns
t_{PHZ}								
C_{PD} CPD is used to determine the dynamic power consumption, per channel.	Power Dissipation Capacitance ACT540/ ACT541		—	60 Typ.		60 Typ.		pF
V_{OHV}	Min. (Valley) V_{OH} During Switching of Other Outputs (Output Under Test Not Switching)		5	4 Typ. @ 25°C				V
V_{OLP}	Max. (Peak) V_{OL} During Switching of Other Outputs (Output Under Test Not Switching)		5	1 Typ. @ 25°C				V
C_I	Input Capacitance		—	—	10	—	10	pF
C_O	3-State Output Capacitance		—	—	15	—	15	pF

(1) 5V: min. is @5.5 V
(2) C_{PD} is used to determine the dynamic power consumption, per channel.

5 Parameter Measurement Information



A. V_{OHV} AND V_{OLP} ARE MEASURED WITH RESPECT TO A GROUND REFERENCE NEAR THE OUTPUT UNDER TEST,
B. INPUT PULSES HAVE THE FOLLOWING CHARACTERISTICS: PRR ≤ 1 MHz, t_r = 3 ns, $t_($ = 3 ns, SKEW 1 ns.
C. R.F. FIXTURE WITH 700-MHz DESIGN RULES REQUIRED. IC SHOULD BE SOLDERED INTO TEST BOARD AND BYPASSED WITH 0.1 *μF* CAPACITOR. SCOPE AND PROBES REQUIRE 700-MHz BANDWIDTH.
D. 92CS-42406

Figure 5-1. Simultaneous Switching Transient Waveforms.

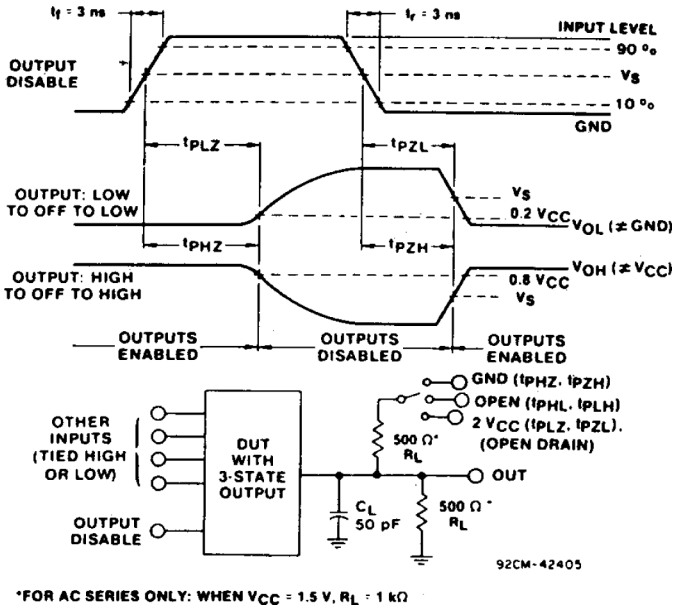


Figure 5-2. Three-state Propagation Delay Waveforms and Test Circuit.

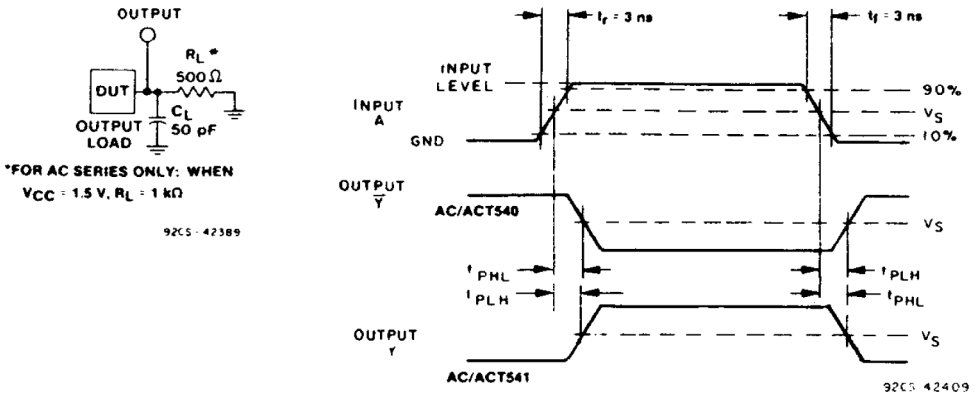


Figure 5-3. Propagation Delay Times and Test Circuit.

	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
input Switching Voltage, V_S	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

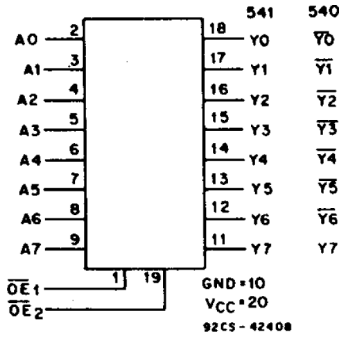
6 Detailed Description

6.1 Overview

The CD74AC540, -541, and CD74ACT540, -541 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Industrial (−40 to +85°C) and Extended Industrial/Military (−55 to +125°C).

The CD54AC540, -541, and CD54ACT540, -541, available in chip form (H suffix), are operable over the −55 to +125°C temperature range.

6.2 Functional Block Diagram



6.3 Device Functional Modes

Table 6-1. Truth Table

CD54/74AC/ACT540		
INPUTS		**OUTPUTS**
$\overline{OE1}$,$\overline{OE1}$	A	Y
L	L	H
L	H	L
H	X	Z

Table 6-2. Truth Table

CD54/74AC/ACT541		
INPUTS		**OUTPUTS**
$\overline{OE1}$,$\overline{OE2}$	A	Y
L	L	L
L	H	H
H	X	Z

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in *Section 4.3*.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends 0.1 µF and if there are multiple V_{CC} terminals, then TI recommends .01 µF or .022 µF for each power terminal. It is okay to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

7.2 Layout

7.2.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only three of the four buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient. Floating outputs is generally acceptable, unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This will not disable the input section of the I.O's so they also cannot float when disabled.

8 Device and Documentation Support

8.1 Documentation Support (Analog)

8.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 8-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
CD74AC540	Click here	Click here	Click here	Click here	Click here
CD54AC541	Click here	Click here	Click here	Click here	Click here
CD74AC541	Click here	Click here	Click here	Click here	Click here
CD54ACT540	Click here	Click here	Click here	Click here	Click here
CD74ACT540	Click here	Click here	Click here	Click here	Click here
CD54ACT541	Click here	Click here	Click here	Click here	Click here
CD74ACT541	Click here	Click here	Click here	Click here	Click here

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

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All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (December 1998) to Revision B (May 2024)	Page
• Added *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Device Functional Modes, Application and Implementation* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Updated θJA value: DW = 58 to 101.2, all values in °C/W	4

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD54AC541F3A	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD54AC541F3A	Samples
CD54ACT540F3A	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD54ACT540F3A	Samples
CD54ACT541F3A	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD54ACT541F3A	Samples
CD74AC540M	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	-55 to 125	AC540M	
CD74AC540M96	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		AC540M	Samples
CD74AC541E	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74AC541E	Samples
CD74AC541EE4	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74AC541E	Samples
CD74AC541M96	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	(AC541, AC541M)	Samples
CD74AC541M96E4	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	(AC541, AC541M)	Samples
CD74AC541SM96	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC541SM	Samples
CD74ACT540E	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74ACT540E	Samples
CD74ACT540M	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	-55 to 125	ACT540M	
CD74ACT540M96	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT540M	Samples
CD74ACT541E	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74ACT541E	Samples
CD74ACT541EE4	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74ACT541E	Samples
CD74ACT541M96	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT541M	Samples
CD74ACT541M96E4	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT541M	Samples
CD74ACT541M96G4	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT541M	Samples
CD74ACT541SM96	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT541SM	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF CD54AC541, CD54ACT540, CD54ACT541, CD74AC541, CD74ACT540, CD74ACT541 :

- Catalog : CD74AC541, CD74ACT540, CD74ACT541
- Military : CD54AC541, CD54ACT540, CD54ACT541

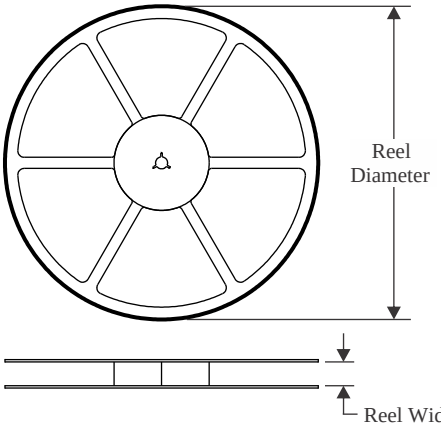
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

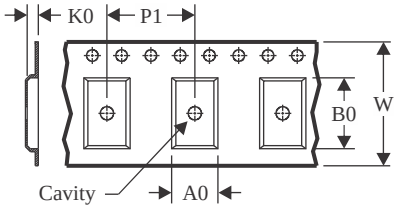
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

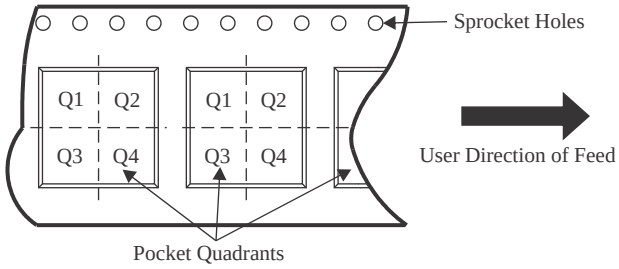


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

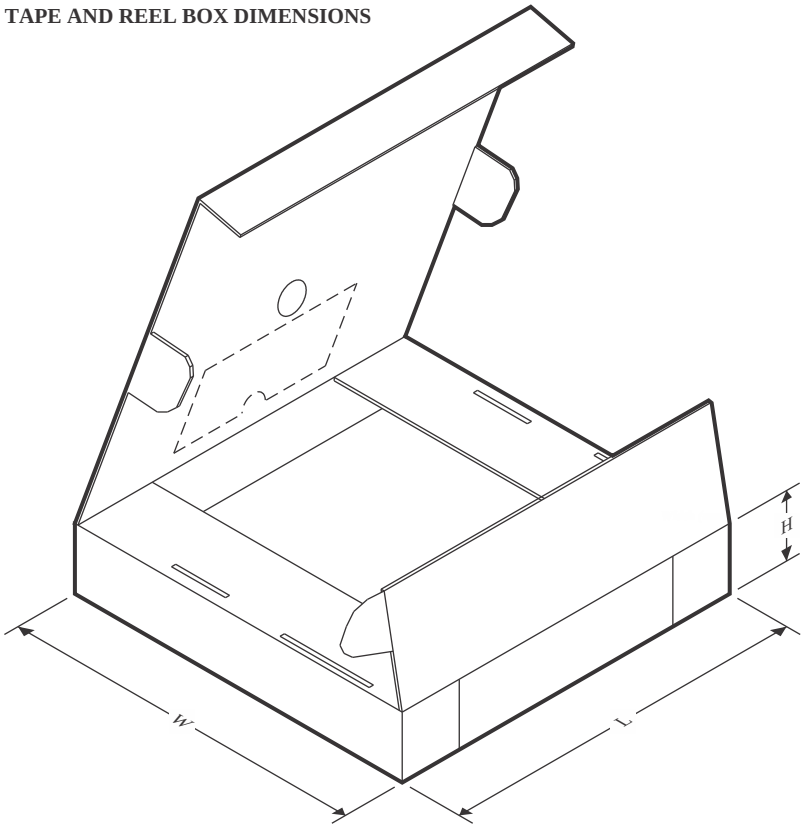
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74AC540M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CD74AC541M96	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
CD74AC541M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CD74AC541SM96	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
CD74ACT540M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CD74ACT540M96	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
CD74ACT541M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CD74ACT541M96	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
CD74ACT541SM96	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
CD74ACT541SM96	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1

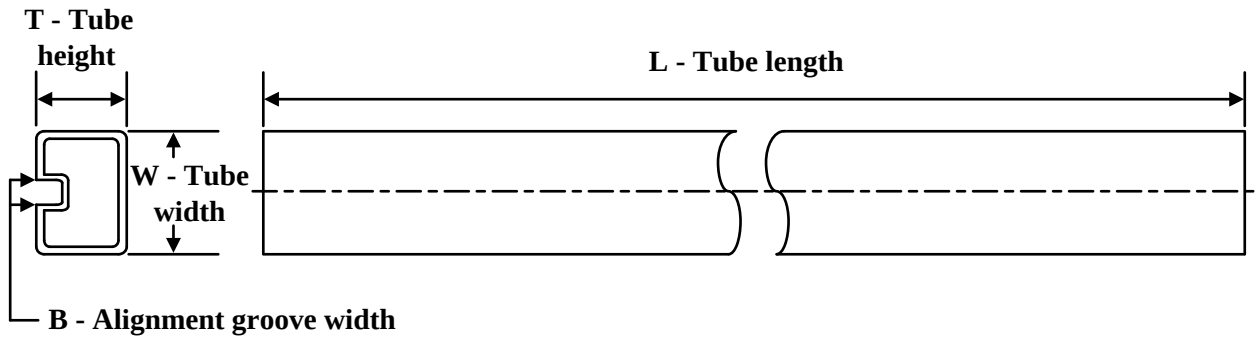
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74AC540M96	SOIC	DW	20	2000	367.0	367.0	45.0
CD74AC541M96	SOIC	DW	20	2000	356.0	356.0	45.0
CD74AC541M96	SOIC	DW	20	2000	367.0	367.0	45.0
CD74AC541SM96	SSOP	DB	20	2000	356.0	356.0	35.0
CD74ACT540M96	SOIC	DW	20	2000	367.0	367.0	45.0
CD74ACT540M96	SOIC	DW	20	2000	356.0	356.0	45.0
CD74ACT541M96	SOIC	DW	20	2000	367.0	367.0	45.0
CD74ACT541M96	SOIC	DW	20	2000	356.0	356.0	45.0
CD74ACT541SM96	SSOP	DB	20	2000	353.0	353.0	32.0
CD74ACT541SM96	SSOP	DB	20	2000	356.0	356.0	35.0

TUBE



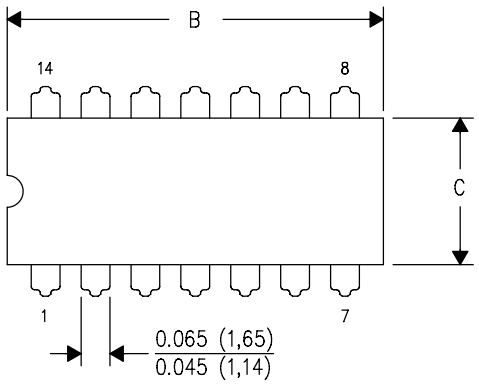
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74AC541E	N	PDIP	20	20	506	13.97	11230	4.32
CD74AC541EE4	N	PDIP	20	20	506	13.97	11230	4.32
CD74ACT540E	N	PDIP	20	20	506	13.97	11230	4.32
CD74ACT541E	N	PDIP	20	20	506	13.97	11230	4.32
CD74ACT541EE4	N	PDIP	20	20	506	13.97	11230	4.32

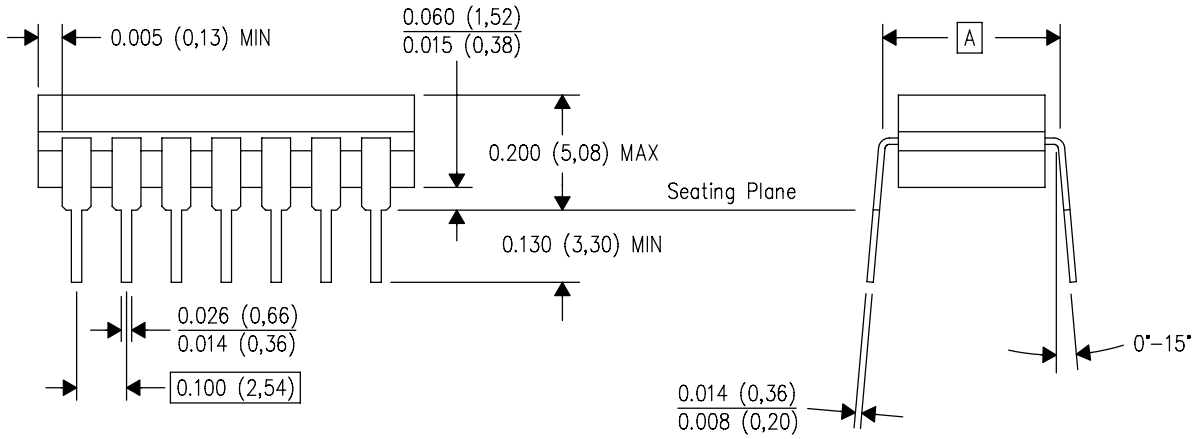
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



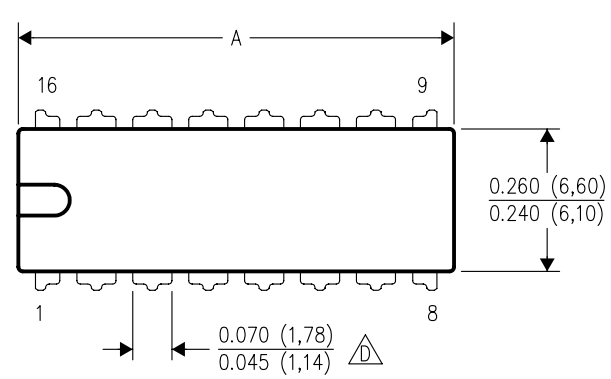
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

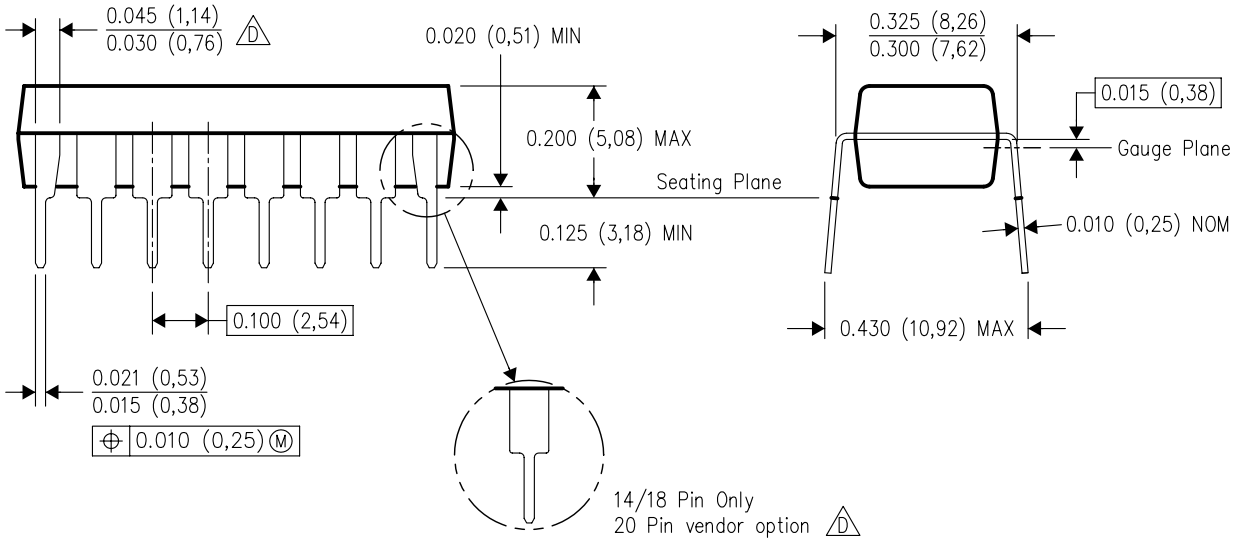
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

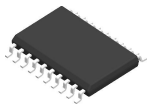


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

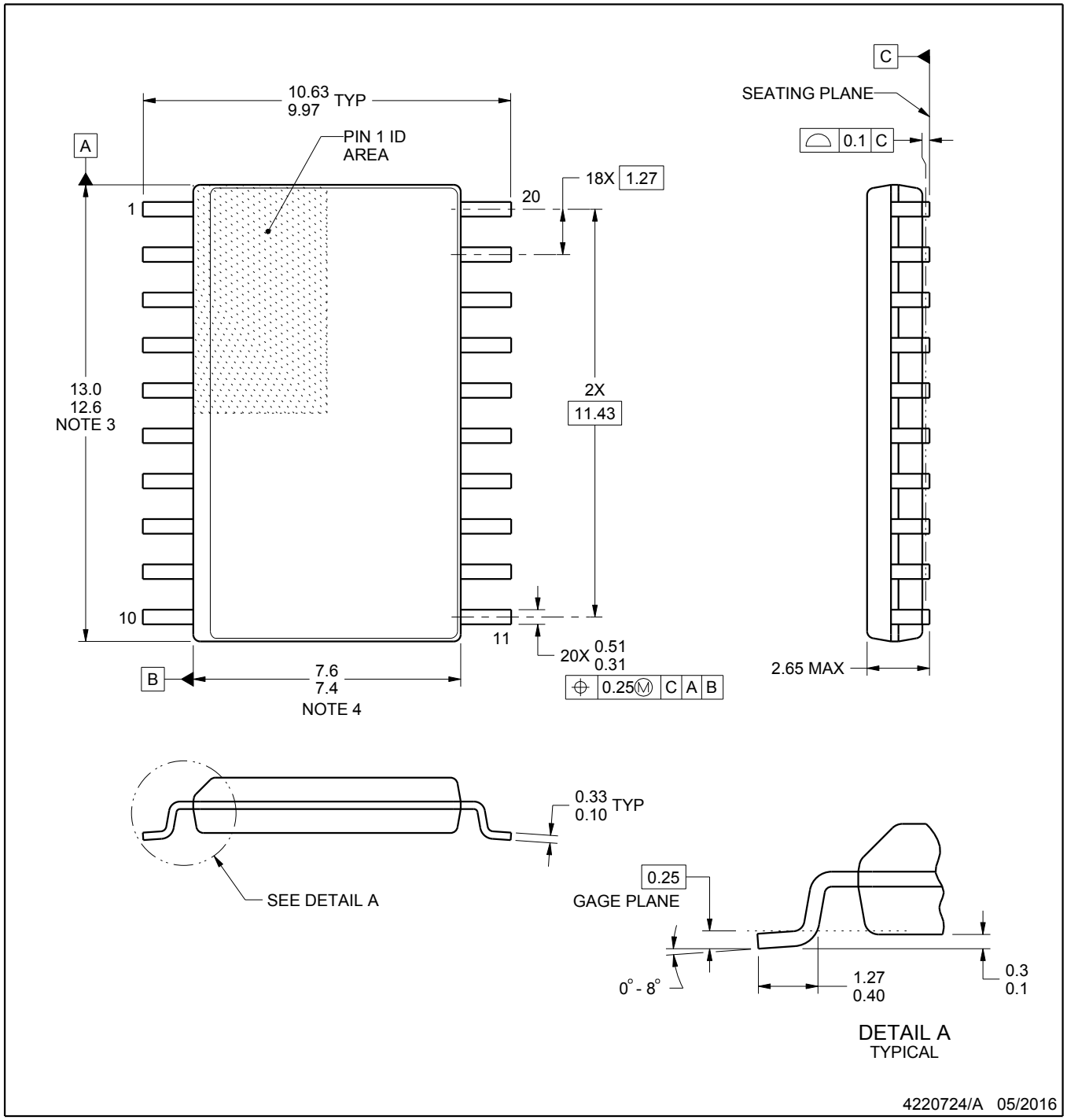


PACKAGE OUTLINE

DW0020A

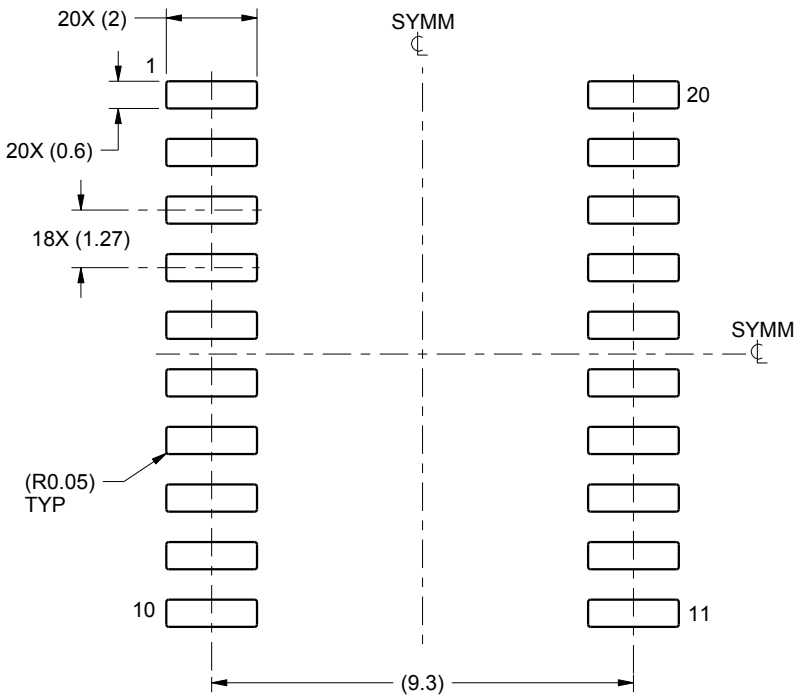
SOIC - 2.65 mm max height

SOIC

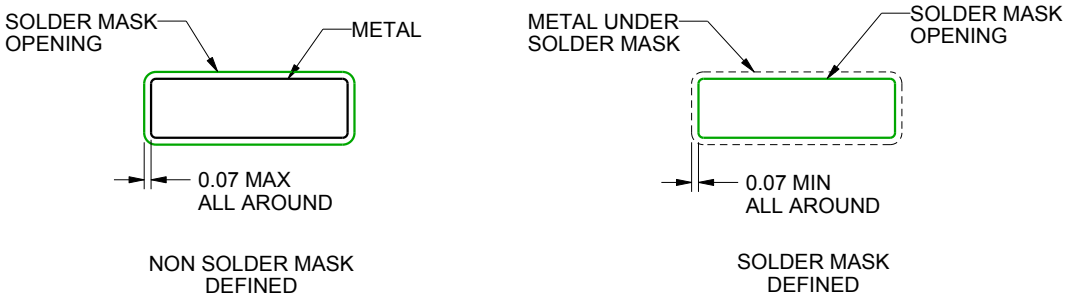


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

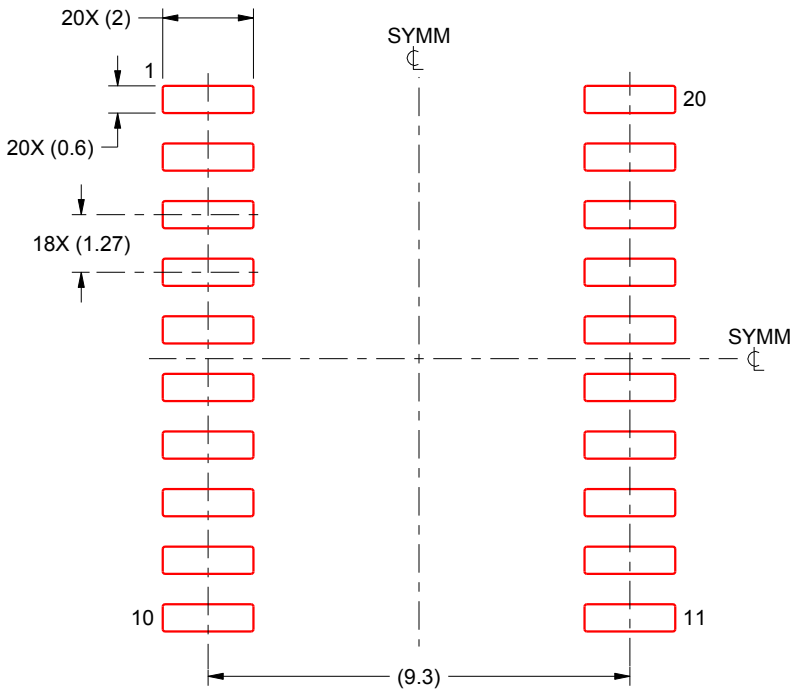


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

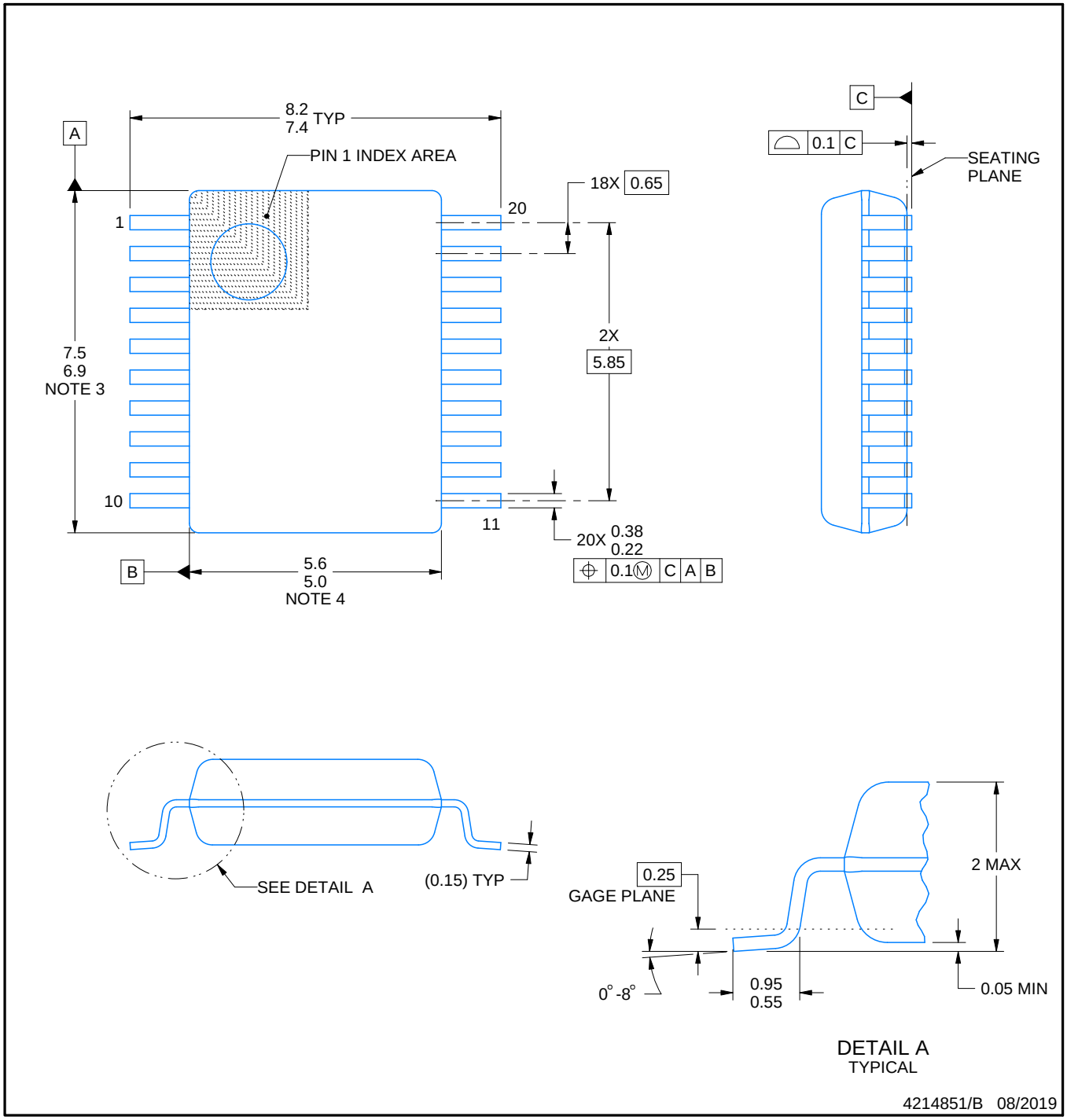
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DB0020A

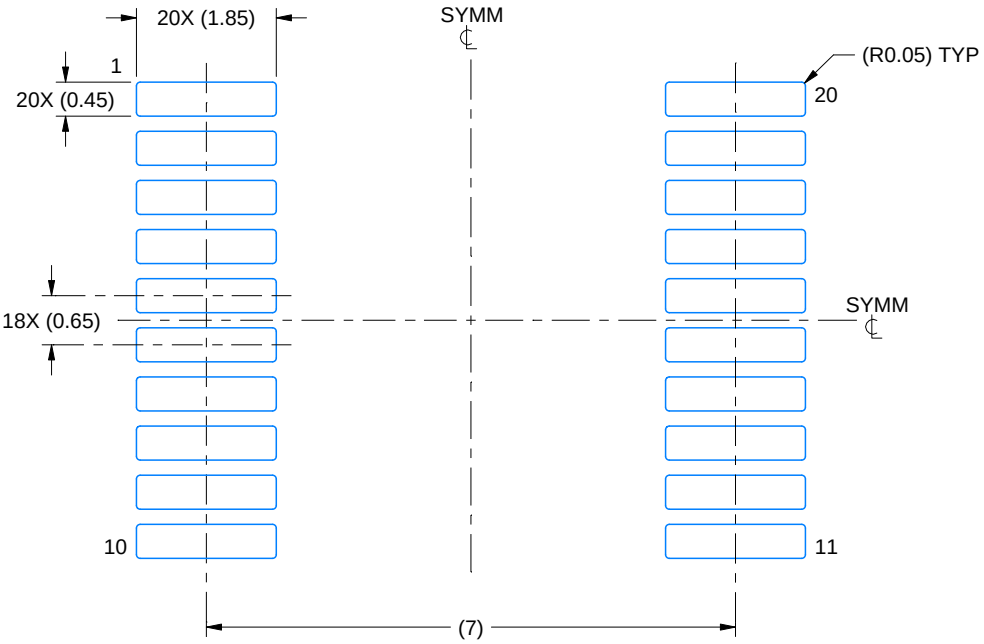
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

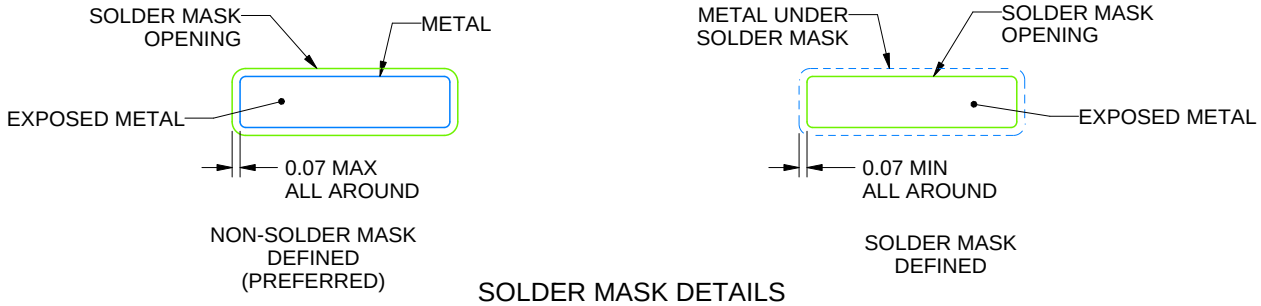


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

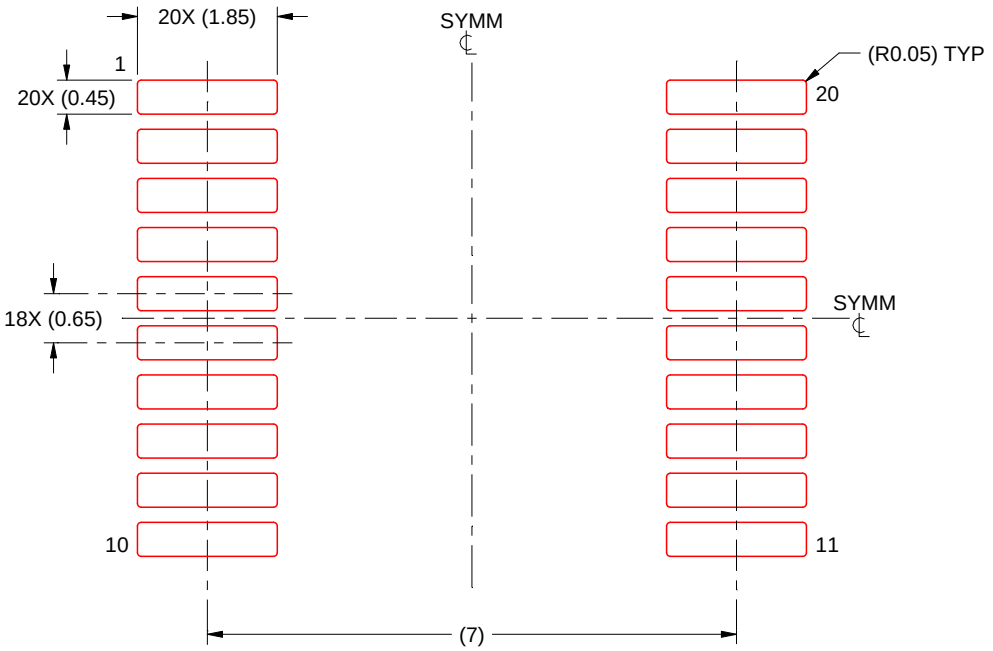
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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