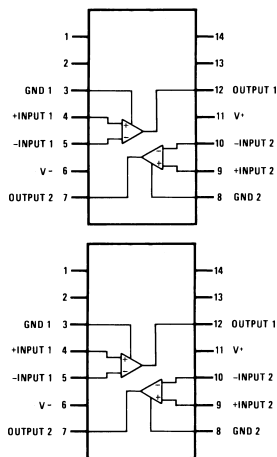


LMx19 High Speed Dual Comparator

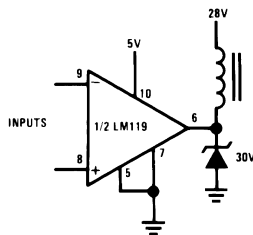
1 Features

- Two Independent Comparators
- Operates from a Single 5-V Supply
- Typically 80-ns Response Time at ± 15 V
- Minimum Fan-out of 2 Each Side
- Maximum Input Current of 1 μ A Over Temperature
- Inputs and Outputs can be Isolated from System Ground
- High Common-Mode Slew Rate

Connection Diagram



Typical Application - Relay Driver



2 Description

The LM119 series are precision high-speed dual comparators fabricated on a single monolithic chip. They are designed to operate over a wide range of supply voltages down to a single 5-V logic supply and ground. They have higher gain and lower input currents than devices such as the LM710. The uncommitted collector of the output stage makes the LM119 compatible with RTL, DTL, and TTL, as well as capable of driving lamps and relays at currents of up to 25 mA.

The LM319A offers improved precision over the standard LM319, with tighter tolerances on offset voltage, offset current, and voltage gain.

Although designed primarily for applications requiring operation from digital logic supplies, the LM119 series are fully specified for power supplies up to ± 15 V. The series features faster response than the LM111, at the expense of higher power dissipation. However, the high-speed, wide operating voltage range and low package count make the LM119 more versatile than older devices such as the LM711.

The LM119 is specified from -55°C to $+125^{\circ}\text{C}$, the LM219 is specified from -25°C to $+85^{\circ}\text{C}$, and the LM319A and LM319 are specified from 0°C to $+70^{\circ}\text{C}$.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|------------------------|-------------|--------------------|
| LM119, LM219, LM319 | TO-100 (10) | 8.96 mm x 8.96 mm |
| | CDIP (14) | 6.67 mm x 19.56 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Table of Contents

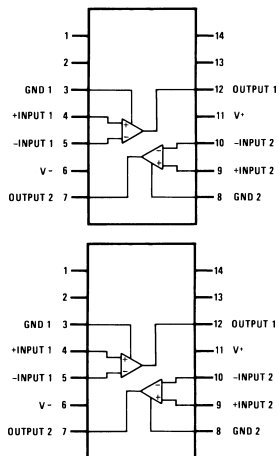
| | | | |
|--|----------|---|-----------|
| 1 Features | 1 | 6 Detailed Description | 10 |
| 2 Description | 1 | 6.1 Functional Block Diagram | 10 |
| 3 Revision History | 2 | 7 Application and Implementation | 11 |
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| 5.6 Typical Characteristics | 7 | 9 Mechanical, Packaging, and Orderable Information | 12 |

3 Revision History

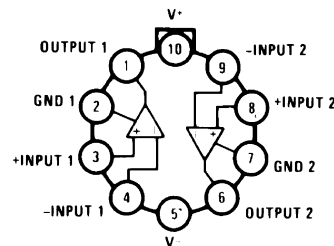
| Changes from Revision A (May 2004) to Revision B | Page |
|--|-------------|
| • Changed datasheet to new TI format from National. | 1 |
| • Added <i>Pin Functions</i> and <i>Thermal Information</i> tables, the <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section | 1 |

4 Pin Configuration and Functions

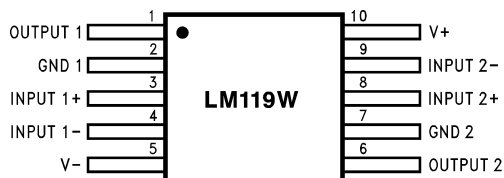
**D, J, or NFF Package
14-Pins CDIP and PDIP
Top View**



**LME Package
10-Pins TO-100 (Metal Can Package)
Top View**



**NAD Package
10-Pins CFP
Top View**



Pin Functions

| NAME | PIN | | | I/O | DESCRIPTION |
|----------|-----------------------|-----------------|-----------------|-----|---------------------------------------|
| | NO. (D, J, NFF 14) | NO. (LME 10) | NO. (NAD 10) | | |
| OUTPUT 1 | 1 | 12 | 1 | O | Comparator 1 output |
| GND 1 | 2 | 3 | 2 | G | Comparator 1 ground connection |
| INPUT 1+ | 3 | 4 | 3 | I | Comparator 1 input |
| INPUT 1- | 4 | 5 | 4 | I | Comparator 1 input |
| V- | 5 | 6 | 5 | P | Negative supply voltage |
| OUTPUT 2 | 6 | 7 | 6 | O | Comparator 2 output |
| GND 2 | 7 | 8 | 7 | G | Comparator 2 ground connection |
| INPUT 2+ | 8 | 9 | 8 | I | Comparator 2 input |
| INPUT 2- | 9 | 10 | 9 | I | Comparator 2 input |
| V+ | 10 | 11 | 10 | P | Positive supply voltage |
| NC | 1,2,13,14 | | | | No connect. Do not connect to ground. |

5 Specifications

5.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾⁽²⁾⁽³⁾

| | | MIN | MAX | UNIT |
|---------------------------------------|--|-----|-----|------|
| Total supply voltage | | | 36 | V |
| Output to negative supply voltage | | | 36 | V |
| Ground to negative supply voltage | | | 25 | V |
| Ground to positive supply voltage | | | 18 | V |
| Differential input voltage | | –5 | +5 | V |
| Input voltage ⁽⁴⁾ | | –15 | +15 | V |
| Power dissipation ⁽⁵⁾ | | | 500 | mW |
| Output short circuit duration | | | 10 | sec |
| Lead temperature (soldering, 10 sec.) | | | 260 | °C |
| Soldering information ⁽⁶⁾ | Dual-In-Line Package Soldering (10 seconds) | | 260 | °C |
| | Small Outline Package Vapor Phase (60 seconds) | | 215 | |
| | Small Outline Package Infrared (15 seconds) | | 220 | |
| Operating temperature | LM119 | –55 | 125 | °C |
| | LM219 | –25 | 85 | |
| | LM319A, LM319 | 0 | 70 | |
| Storage temperature, T _{stg} | | –65 | 150 | °C |

- Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- Refer to RETS119X for LM119H/883 and LM119J/883 specifications.
- For supply voltages less than ± 15 V the absolute maximum input voltage is equal to the supply voltage.
- The maximum junction temperature of the LM119 is 150°C, while that of the LM219 is 110°C. For operating at elevated temperatures, devices in the H10 package must be derated based on a thermal resistance of 160°C/W, junction to ambient, or 19°C/W, junction to case. The thermal resistance of the J14 and N14 packages is 100°C/W, junction to ambient.
- See AN-450 “Surface Mounting Methods and Their Effect on Product Reliability” for other methods of soldering surface mount devices.

5.2 ESD Ratings

| | | | VALUE | UNIT |
|--------------------|-------------------------|---|-------|------|
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±800 | V |

- JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

5.3 Thermal Information

| THERMAL METRIC ⁽¹⁾ | LM119, LM219, LM319 | | | UNIT |
|---|---------------------|------------|----------|------|
| | TO-100 (LME) | PDIP (NFF) | CDIP (J) | |
| | 10 PINS | 14 PINS | 14 PINS | |
| R _{θJA} Junction-to-ambient thermal resistance | 160 | 100 | 100 | °C/W |
| R _{θJC(top)} Junction-to-case (top) thermal resistance | 19 | NA | NA | °C/W |

- For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

5.4 Electrical Characteristics LM119, LM219

These specifications apply for $V_S = \pm 15\text{ V}$, and the Ground pin at ground, and $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, unless otherwise stated. With the LM219, all temperature specifications are limited to $-25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5-V supply up to $\pm 15\text{-V}$ supplies. Do not operate the device with more than 16 V from ground to V_S .

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------------|---|-----|----------|---------|---------------|
| Input Offset Voltage ⁽¹⁾ | $T_A = 25^\circ\text{C}$, $R_S \leq 5\text{k}$ | | 0.7 | 4 | mV |
| Input Offset Current ⁽¹⁾ | $T_A = 25^\circ\text{C}$ | | 30 | 75 | nA |
| Input Bias Current | $T_A = 25^\circ\text{C}$ | | 150 | 500 | nA |
| Voltage Gain | $T_A = 25^\circ\text{C}$ ⁽²⁾ | 10 | 40 | | V/mV |
| Response Time ⁽³⁾ | $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$ | | 80 | | ns |
| Saturation Voltage | $V_{IN} \leq -5\text{ mV}$, $I_{OUT} = 25\text{ mA}$ $T_A = 25^\circ\text{C}$ | | 0.75 | 1.5 | V |
| Output Leakage Current | $V_{IN} \geq 5\text{ mV}$, $V_{OUT} = 35\text{ V}$ $T_A = 25^\circ\text{C}$ | | 0.2 | 2 | μA |
| Input Offset Voltage ⁽¹⁾ | $R_S \leq 5\text{k}$ | | | 7 | mV |
| Input Offset Current ⁽¹⁾ | | | | 100 | nA |
| Input Bias Current | | | | 1000 | nA |
| Input Voltage Range | $V_S = \pm 15\text{ V}$ | -12 | ± 13 | +12 | V |
| | $V^+ = 5\text{ V}$, $V^- = 0$ | 1 | | 3 | |
| Saturation Voltage | $V^+ \geq 4.5\text{ V}$, $V^- = 0$ $V_{IN} \leq -6\text{ mV}$, $I_{SINK} \leq 3.2\text{ mA}$ $T_A \geq 0^\circ\text{C}$ | | 0.23 | 0.4 | V |
| | $T_A \leq 0^\circ\text{C}$ | | | 0.6 | |
| Output Leakage Current | $V_{IN} \geq 5\text{ mV}$, $V_{OUT} = 35\text{ V}$, $V^- = V_{GND} = 0\text{ V}$ | | 1 | 10 | μA |
| Differential Input Voltage | | | | ± 5 | V |
| Positive Supply Current | $T_A = 25^\circ\text{C}$, $V^+ = 5\text{ V}$, $V^- = 0$ | | 4.3 | | mA |
| Positive Supply Current | $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$ | | 8 | 11.5 | mA |
| Negative Supply Current | $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$ | | 3 | 4.5 | mA |

- (1) The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1-mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.
- (2) Output is pulled up to 15 V through a 1.4-kW resistor.
- (3) The response time specified is for a 100-mV input step with 5-mV overdrive.

5.5 Electrical Characteristics LM319, LM319A

These specifications apply for $V_S = \pm 15\text{ V}$, and $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$, unless otherwise stated. The offset voltage, offset current, and bias current specifications apply for any supply voltage from a single 5-V supply up to $\pm 15\text{-V}$ supplies. Do not operate the device with more than 16 V from ground to V_S .

| PARAMETER | TEST CONDITIONS | LM319A | | | LM319 | | | UNIT |
|-------------------------------------|---|--------|----------|---------|-------|----------|---------|---------------|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| Input Offset Voltage ⁽¹⁾ | $T_A = 25^\circ\text{C}$, $R_S \leq 5\text{k}$ | | 0.5 | 1 | | 2 | 8 | mV |
| Input Offset Current ⁽¹⁾ | $T_A = 25^\circ\text{C}$ | | 20 | 40 | | 80 | 200 | nA |
| Input Bias Current | $T_A = 25^\circ\text{C}$ | | 150 | 500 | | 250 | 1000 | nA |
| Voltage Gain | $T_A = 25^\circ\text{C}$ ⁽²⁾ | 20 | 40 | | 8 | 40 | | V/mV |
| Response Time ⁽³⁾ | $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$ | | 80 | | | 80 | | ns |
| Saturation Voltage | $V_{IN} \leq -10\text{ mV}$, $I_{OUT} = 25\text{ mA}$ $T_A = 25^\circ\text{C}$ | | 0.75 | 1.5 | | 0.75 | 1.5 | V |
| Output Leakage Current | $V_{IN} \geq 10\text{ mV}$, $V_{OUT} = 35\text{ V}$ $V^- = V_{GND} = 0\text{ V}$, $T_A = 25^\circ\text{C}$ | | 0.2 | 10 | | 0.2 | 10 | μA |
| Input Offset Voltage ⁽¹⁾ | $R_S \leq 5\text{k}$ | | | 10 | | | 10 | mV |
| Input Offset Current ⁽¹⁾ | | | | 300 | | | 300 | nA |
| Input Bias Current | | | | 1000 | | | 1200 | nA |
| Input Voltage Range | $V_S = \pm 15\text{ V}$ | | ± 13 | | | ± 13 | | V |
| | $V^+ = 5\text{ V}$, $V^- = 0$ | 1 | | 3 | 1 | | 3 | |
| Saturation Voltage | $V^+ \geq 4.5\text{ V}$, $V^- = 0$ $V_{IN} \leq -10\text{ mV}$, $I_{SINK} \leq 3.2\text{ mA}$ | | 0.3 | 0.4 | | 0.3 | 0.4 | V |
| Differential Input Voltage | | | | ± 5 | | | ± 5 | V |
| Positive Supply Current | $T_A = 25^\circ\text{C}$, $V^+ = 5\text{ V}$, $V^- = 0$ | | 4.3 | | | 4.3 | | mA |
| Positive Supply Current | $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$ | | 8 | 12.5 | | 8 | 12.5 | mA |
| Negative Supply Current | $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$ | | 3 | 5 | | 3 | 5 | mA |

- (1) The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1-mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.
- (2) Output is pulled up to 15 V through a 1.4-kW resistor.
- (3) The response time specified is for a 100-mV input step with 5-mV overdrive.

5.6 Typical Characteristics

5.6.1 Typical Characteristics – LM119, LM119A, LM219

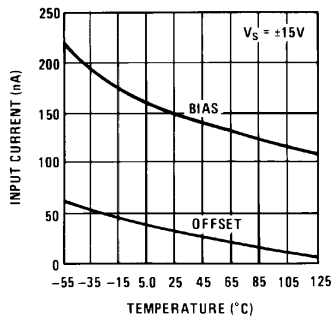


Figure 1. Input Currents

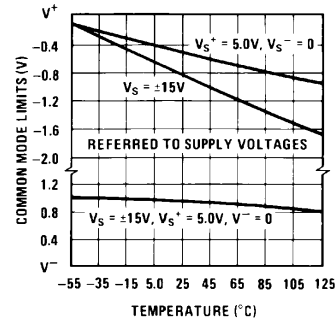


Figure 2. Common-Mode Limits

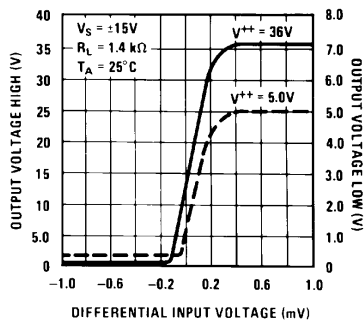


Figure 3. Transfer Function

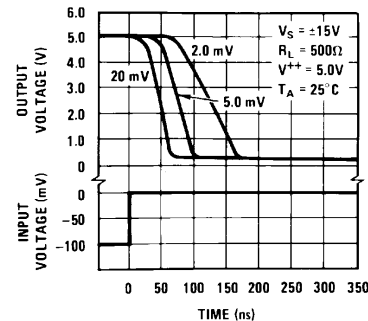


Figure 4. Response Time for Various Input Overdrives

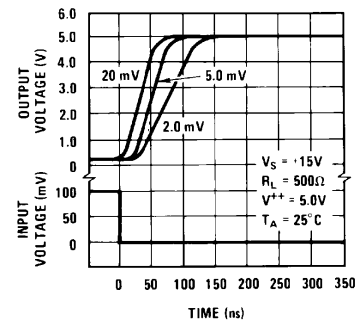


Figure 5. Response Time for Various Input Overdrives

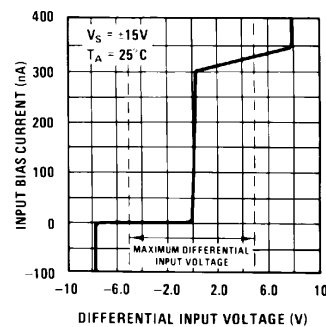


Figure 6. Input Characteristics

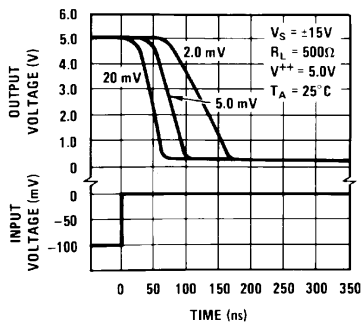


Figure 7. Response Time for Various Input Overdrives

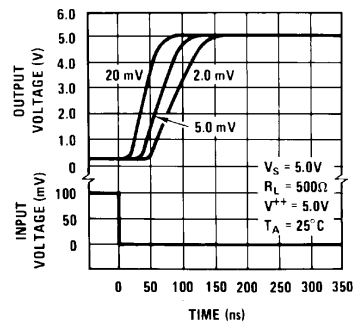


Figure 8. Response Time for Various Input Overdrives

Typical Characteristics – LM119, LM119A, LM219 (continued)

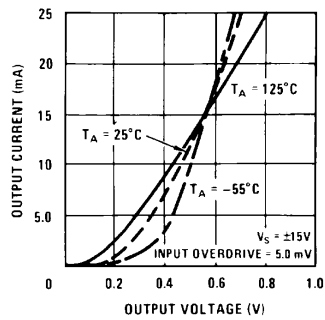


Figure 9. Output Saturation Voltage

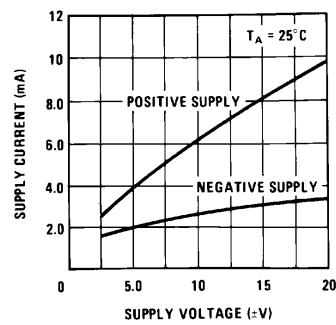


Figure 10. Supply Current

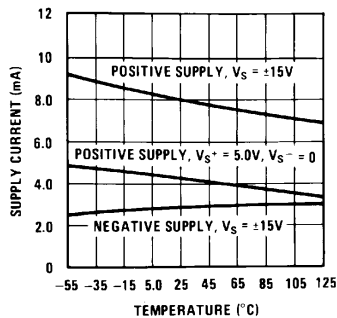


Figure 11. Supply Current

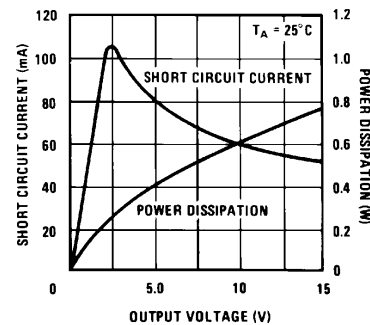


Figure 12. Output Limiting Characteristics

5.6.2 Typical Characteristics – LM319, LM319A

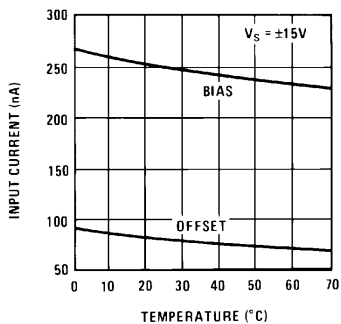


Figure 13. Input Currents

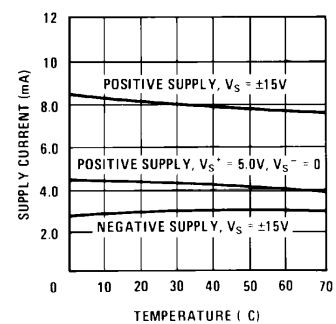


Figure 14. Supply Currents

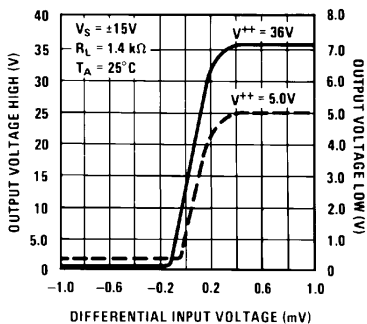


Figure 15. Transfer Function

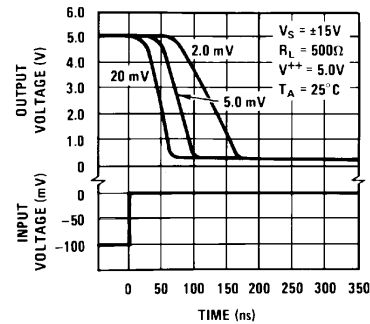


Figure 16. Response Time for Various Input Overdrives

Typical Characteristics – LM319, LM319A (continued)

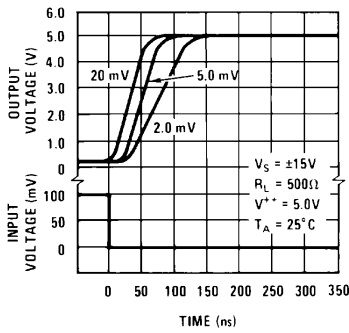


Figure 17. Response Time for Various Input Overdrives

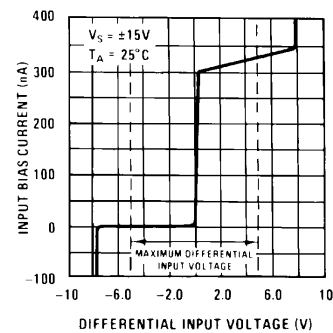


Figure 18. Input Characteristics

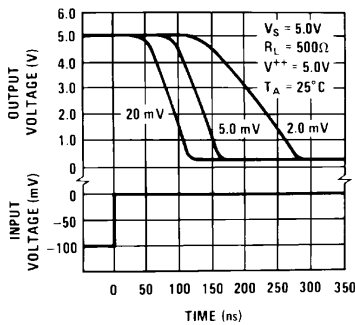


Figure 19. Response Time for Various Input Overdrives

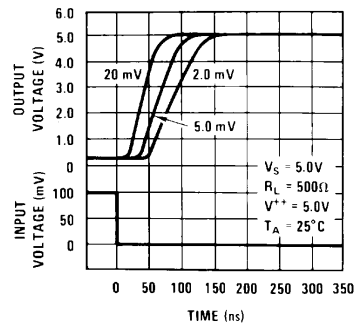


Figure 20. Response Time for Various Input Overdrives

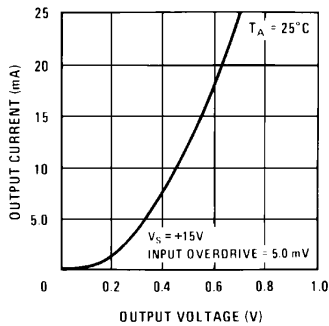


Figure 21. Output Saturation Voltage

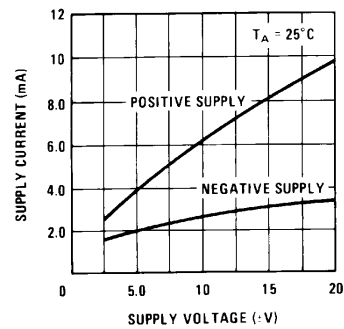


Figure 22. Supply Current

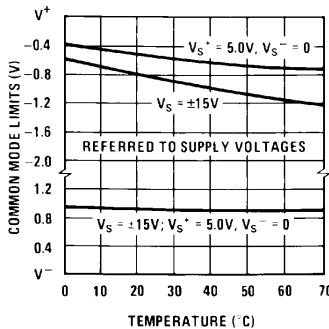


Figure 23. Common-Mode Limits

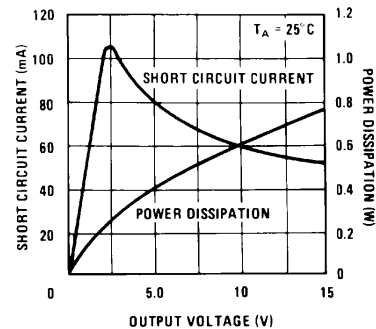
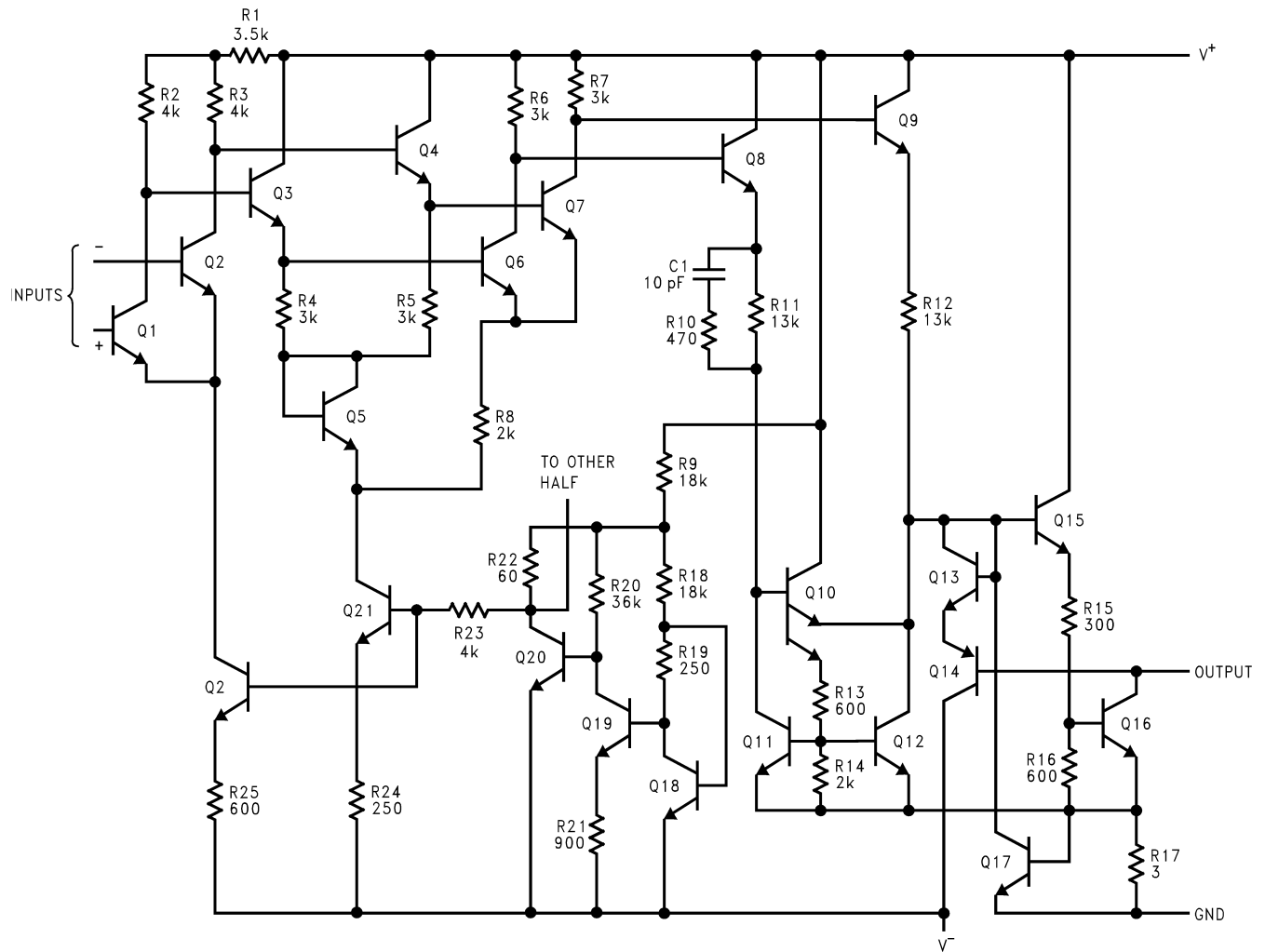


Figure 24. Output Limiting Characteristics

6 Detailed Description

6.1 Functional Block Diagram



DS005705-1

*Do not operate the LM119 with more than 16V between GND and V⁺

7 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Typical Applications

7.1.1 Relay Driver

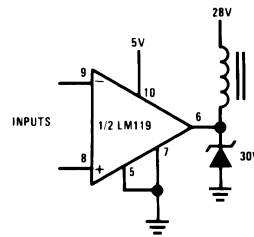


Figure 25. Relay Driver

7.1.2 Window Detector

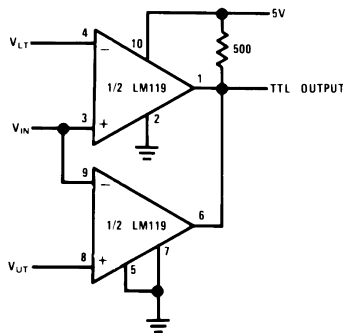


Figure 26. Window Detector

8 Device and Documentation Support

8.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|-------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| LM119 | Click here | Click here | Click here | Click here | Click here |
| LM219 | Click here | Click here | Click here | Click here | Click here |
| LM319 | Click here | Click here | Click here | Click here | Click here |

8.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

8.3 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

8.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

8.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|------------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| LM119H | ACTIVE | TO-100 | LME | 10 | 500 | Non-RoHS & Green | Call TI | Level-1-NA-UNLIM | -55 to 125 | (LM119H, LM119H) | Samples |
| LM119H/NOPB | ACTIVE | TO-100 | LME | 10 | 500 | RoHS & Green | Call TI | Level-1-NA-UNLIM | -55 to 125 | (LM119H, LM119H) | Samples |
| LM119J | ACTIVE | CDIP | J | 14 | 25 | Non-RoHS & Green | Call TI | Level-1-NA-UNLIM | -55 to 125 | LM119J | Samples |
| LM319AM/NOPB | ACTIVE | SOIC | D | 14 | 55 | RoHS & Green | SN | Level-1-260C-UNLIM | 0 to 70 | LM319AM | Samples |
| LM319AMX/NOPB | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | SN | Level-1-260C-UNLIM | 0 to 70 | LM319AM | Samples |
| LM319M/NOPB | ACTIVE | SOIC | D | 14 | 55 | RoHS & Green | SN | Level-1-260C-UNLIM | 0 to 70 | LM319M | Samples |
| LM319MX/NOPB | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | SN | Level-1-260C-UNLIM | 0 to 70 | LM319M | Samples |
| LM319N/NOPB | ACTIVE | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | Level-1-NA-UNLIM | 0 to 70 | LM319N | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LM319AMX/NOPB | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.35 | 2.3 | 8.0 | 16.0 | Q1 |
| LM319MX/NOPB | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.35 | 2.3 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LM319AMX/NOPB | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 35.0 |
| LM319MX/NOPB | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 35.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|--------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| LM119J | J | CDIP | 14 | 25 | 502 | 14 | 11938 | 4.32 |
| LM319AM/NOPB | D | SOIC | 14 | 55 | 495 | 8 | 4064 | 3.05 |
| LM319M/NOPB | D | SOIC | 14 | 55 | 495 | 8 | 4064 | 3.05 |
| LM319N/NOPB | N | PDIP | 14 | 25 | 502 | 14 | 11938 | 4.32 |

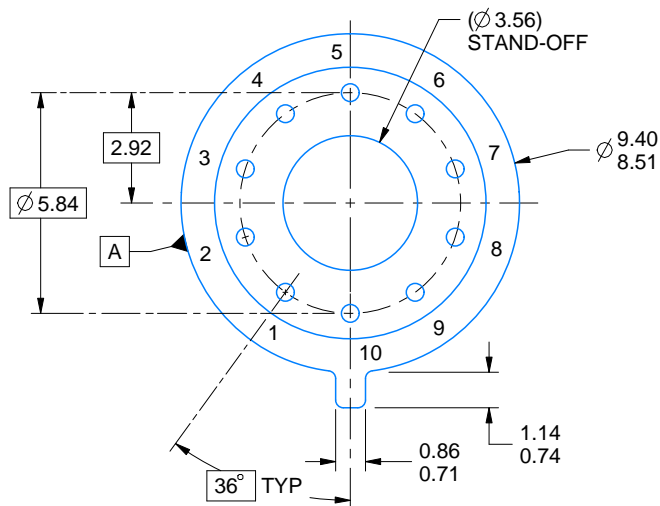
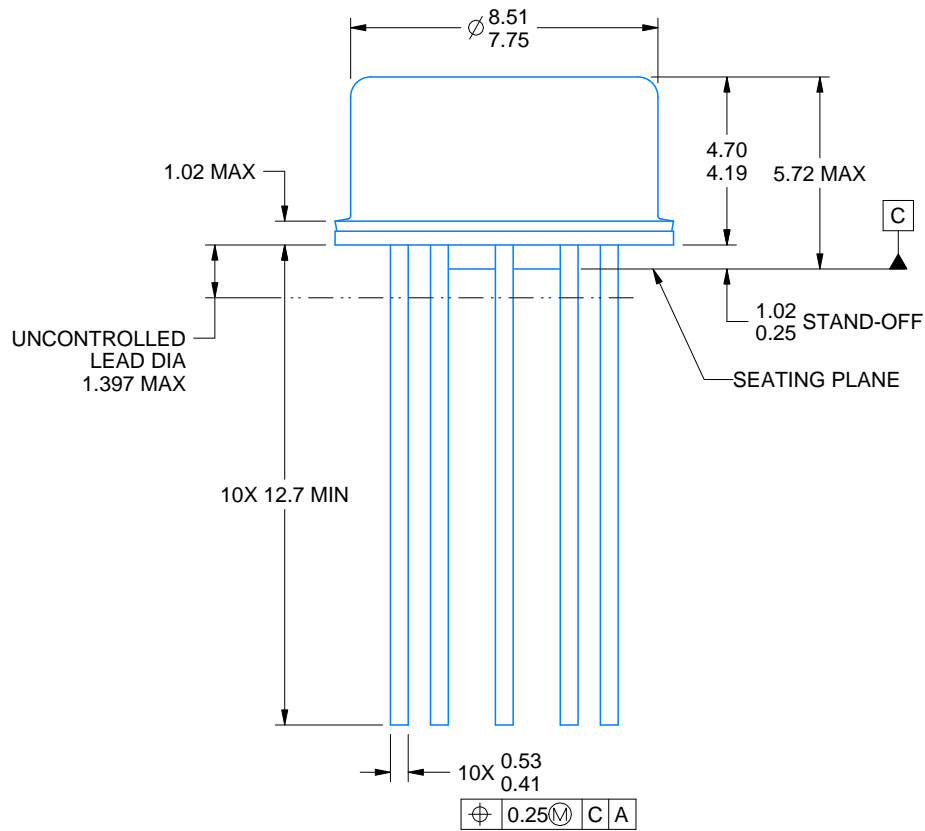


LME0010A

PACKAGE OUTLINE

TO-CAN - 5.72 mm max height

TRANSISTOR OUTLINE



4220604/B 09/2024

NOTES:

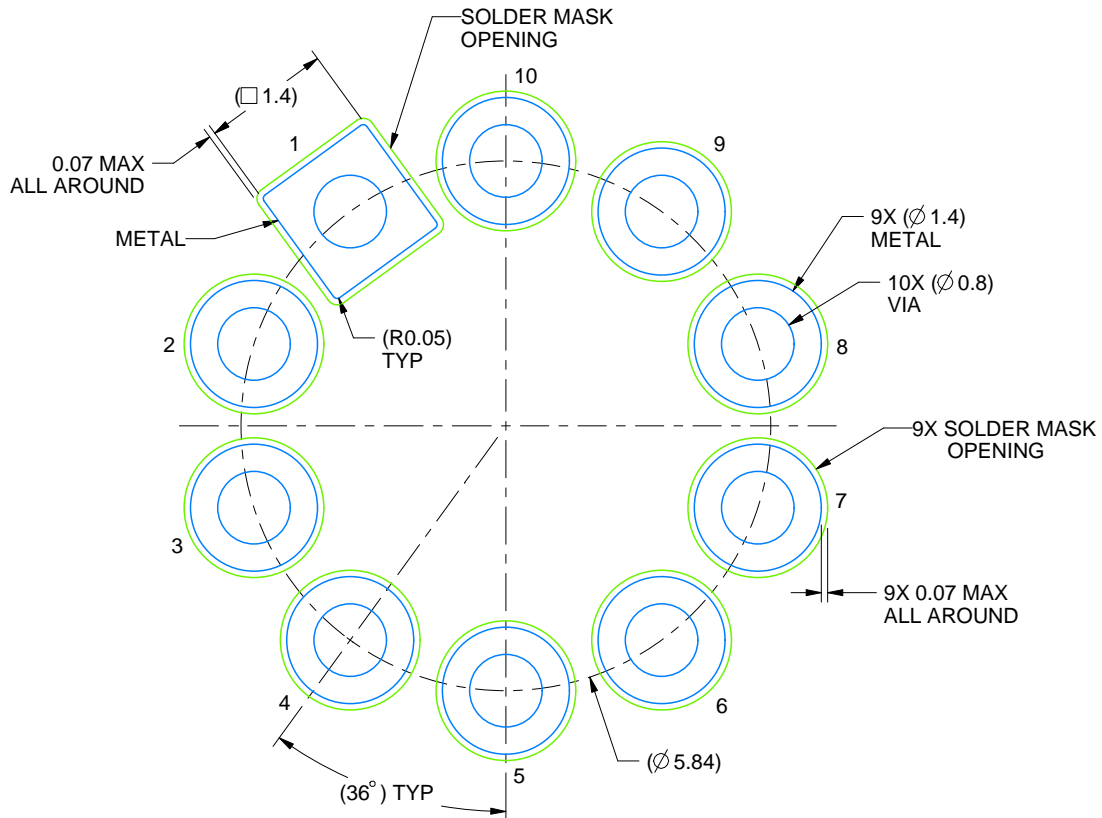
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-006/TO-100.

EXAMPLE BOARD LAYOUT

LME0010A

TO-CAN - 5.72 mm max height

TRANSISTOR OUTLINE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 12X

4220604/B 09/2024



D0014A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

J 14

GENERIC PACKAGE VIEW
CDIP - 5.08 mm max height
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

J0014A



PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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