Programmable GAMMA-VOLTAGE GENERATOR with Two High Slew Rate V_{COM}s

Check for Samples: BUF18830

FEATURES

- **10-BIT RESOLUTION**
- **18-CHANNEL P-GAMMA:**
  - **300-mV Min Swing-to-Rail (10 mA)**
- **TWO-CHANNEL P-V_{COM}:**
  - **400-mA Typical I_{OUT}**
- **HIGH SLEW RATE V_{COM}: 45 V/µs**
- **RAIL-TO-RAIL OUTPUT**
- **LOW SUPPLY CURRENT**
- **SUPPLY VOLTAGE: 6.5 V to 20 V**
- **DIGITAL SUPPLY: 2.0 V to 5.5 V**
- **TWO-WIRE INTERFACE: Supports 400 kHz and 3.4 MHz**

APPLICATIONS

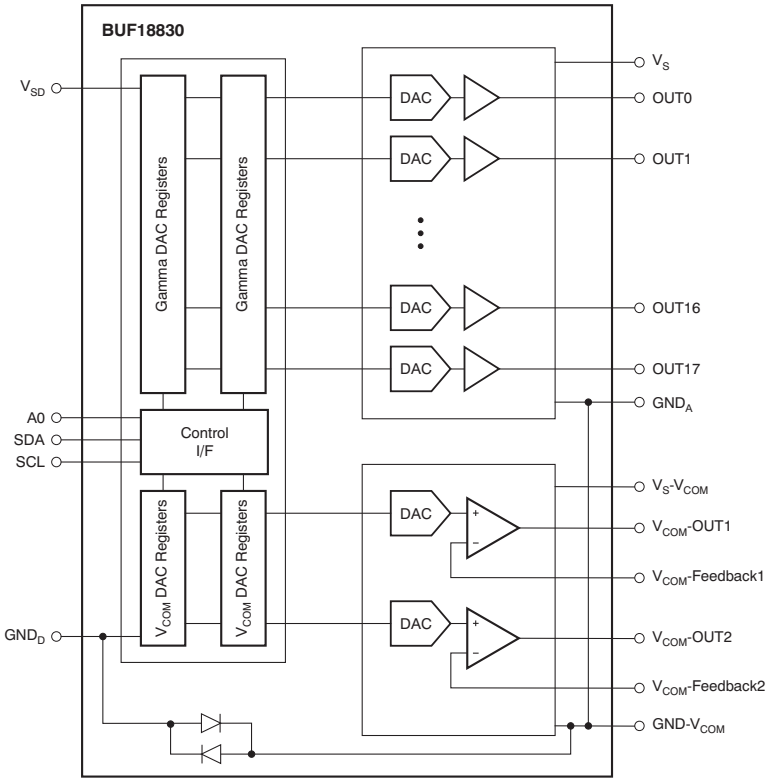
- **TFT-LCD AND OLED REFERENCE DRIVERS**

DESCRIPTION

The BUF18830 offers 18 programmable gamma channels and two programmable V_{COM} channels.

All gamma and V_{COM} channels offer a rail-to-rail output that typically swings to within 300 mV of either supply rail with a 10-mA load. All channels are programmed using a two-wire interface that supports standard operations up to 400 kHz and high-speed data transfers up to 3.4 MHz.

The BUF18830 is manufactured using Texas Instruments' proprietary, state-of-the-art, high-voltage CMOS process. This process offers very dense logic and high supply voltage operation of up to 20 V. The BUF18830 is offered in a QFN-38 package and is specified from –40°C to +85°C.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE	PACKAGE DESIGNATOR	PACKAGE MARKING	ORDERING NUMBER
BUF18830	QFN-38	RGF	BUF18830	BUF18830AIRGFTR

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

			BUF18830	UNIT
Supply Voltage		V_S	+22	V
Supply Voltage		V_{SD}	+6	V
Digital Input Pins, SCL, SDA, AO: Voltage			–0.5 to +6	V
Digital Input Pins, SCL, SDA, AO: Current			±10	mA
Output Pins, OUT0 through OUT17, and VCOM1 and VCOM2(2)			(V–) – 0.5 to (V+) + 0.5	V
Output Short-Circuit(3)			Continuous	
Ambient Operating Temperature			–40 to +85	°C
Ambient Storage Temperature			–65 to +150	°C
Junction Temperature		T_J	+150	°C
ESD Ratings:	Human Body Model	HBM	3000	V
	Charged Device Model	CDM	1000	V
	Machine Model	MM	200	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
(2) See the *Output Protection* section.
(3) Short-circuit to ground, one amplifier per package. Exposed thermal die is soldered to the PCB using thermal vias. Refer to Texas Instruments application report *QFN/SON PCB Attachment* (SLUA271).

THERMAL INFORMATION

THERMAL METRIC(1)(2)		BUF18830 RGF 38 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	35.4	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	20.6	
θ_{JB}	Junction-to-board thermal resistance	9.0	
ψ_{JT}	Junction-to-top characterization parameter	0.3	
ψ_{JB}	Junction-to-board characterization parameter	8.9	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	1.2	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.
(2) Refer to SLUA271 for printed circuit board (PCB) requirements for meeting thermal performance. Thermal pad attached to PCB, 0-lfm airflow, and 76-mm × 76-mm copper area.

ELECTRICAL CHARACTERISTICS

Boldface limits apply over the specified temperature range, **T_A = –40°C to +85°C.**
At T_A = +25°C, V_S = V_S-V_{COM} = +13.5 V, V_{SD} = +3.3 V, and C_L = 200 pF, unless otherwise noted.

PARAMETER		CONDITIONS	BUF18830 MIN	BUF18830 TYP	BUF18830 MAX	UNIT
ANALOG GAMMA BUFFER CHANNELS						
OUT 0, 5, 6, 11, 12, 17 Output Swing: High		Code = 1023, sourcing 10 mA	13.2	13.35		V
OUT 0, 5, 6, 11, 12, 17 Output Swing: Low		Code = 0, sinking 10 mA		0.07	0.3	V
OUT 1-4, 7-10, 13-16 Output Swing: High		Code = 1023, sourcing 10 mA	13.0	13.35		V
OUT 1-4, 7-10, 13-16 Output Swing: Low		Code = 0, sinking 10 mA		0.07	0.5	V
Continuous Output Current		See (1), (2)		100		mA
Output Accuracy		Code 512		4.3	±35	mV
vs Temperature		**Code 512**		**0.8**		**µV/°C**
Integral Nonlinearity	INL			0.3	1	LSB
Differential Nonlinearity	DNL			0.3	1	LSB
Load Regulation, 10 mA	REG	Code 512 or V_{CC}/2, I_{OUT} = +5-mA to –5-mA Step		0.18	0.5	mV/mA
V_{COM} OUTPUT						
Output Swing: High		Sourcing/sinking 400 mA, G = 2	9.5	10.8		V
Output Swing: Low		Sourcing/sinking 400 mA, G = 2		3.8	5	V
Slew Rate		R_{LOAD} = 10 kΩ, C_{LOAD} = 50 pF		45		V/µs
Continuous Output Current		See (1), (2)		400		mA
Output Accuracy		Code 512		–3.5	±50	mV
vs Temperature		**Code 512**		**–2.0**		**µV/°C**
Integral Nonlinearity	INL			0.5	1	LSB
Differential Nonlinearity	DNL			0.5	1	LSB
Load Regulation, 10 mA	REG	Code 512 or V_{CC}/2, I_{OUT} = +5-mA to –5-mA Step		–0.07	1.5	mV/mA
ANALOG POWER SUPPLY						
Operating Range			6.5		20	V
Total Analog Supply Current	I_S	Outputs at reset values, no load		14	20.5	mA
Over Temperature					**22.0**	**mA**
DIGITAL						
Logic 1 Input Voltage	V_{IH}		0.7 × V_{SD}			V
Logic 0 Input Voltage	V_{IL}				0.3 × V_{SD}	V
Logic 0 Output Voltage	V_{OL}	I_{SINK} = 3 mA		0.15	0.4	V
Input Leakage				±0.01	±10	µA
Clock Frequency	**f_{CLK}**	**Standard/Fast Mode**			**400**	**kHz**
		High-Speed Mode			**3.4**	**MHz**
Reset Codes						
OUT0, OUT6, OUT12				887		
OUT1, OUT7, OUT13				827		
OUT2, OUT8, OUT14				667		
OUT3, OUT9, OUT15				607		
OUT4, OUT10, OUT16				554		
OUT5, OUT11, OUT17				448		
V_{COM}1				834		
V_{COM}2				228		

(1) Observe maximum power dissipation. Refer to *SOA* curves and *Output Voltage vs Output Current* curves.
(2) Thermal pad attached to PCB, 0-lfm airflow and 76-mm x 76-mm copper area. Refer to SLUA271 for PCB design.

ELECTRICAL CHARACTERISTICS (continued)

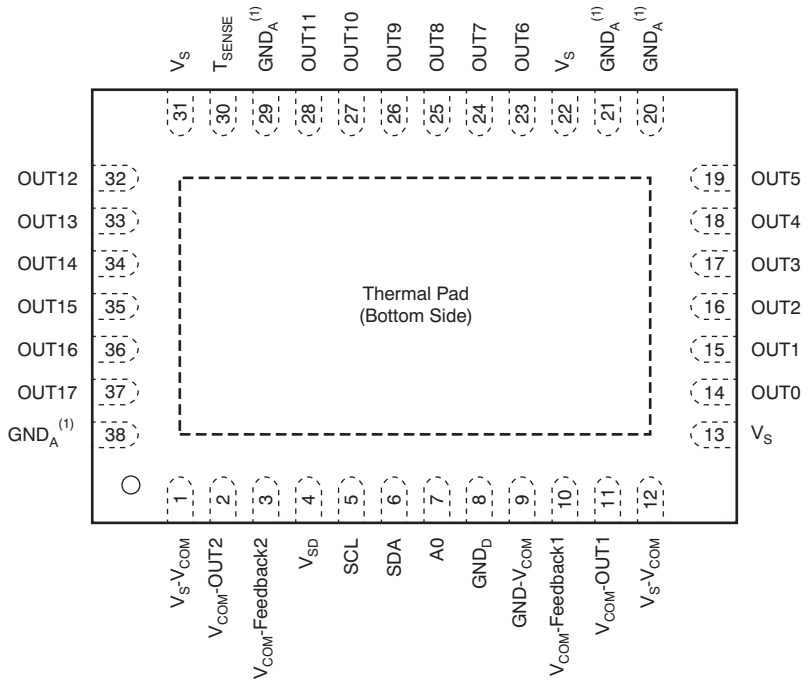
Boldface limits apply over the specified temperature range, **T_A = –40°C to +85°C.**
At T_A = +25°C, V_S = V_S-V_{COM} = +13.5 V, V_{SD} = +3.3 V, and C_L = 200 pF, unless otherwise noted.

PARAMETER		CONDITIONS	BUF18830 MIN	BUF18830 TYP	BUF18830 MAX	UNIT
DIGITAL POWER SUPPLY						
Operating Range	V_{SD}		2.0		5.5	V
Digital Supply Current(3)	I_{SD}	Outputs at reset values, no load, two-wire bus inactive		115	180	µA
Over Temperature				**115**		µ**A**
TEMPERATURE RANGE						
Specified Range			–40		+85	°C
Operating Range		Junction temperature < +125°C	–40		+95	°C
Storage Range			–65		+150	°C

(3) Observe maximum power dissipation. Refer to *SOA* curves and *Output Voltage vs Output Current* curves.

PIN CONFIGURATION

RGF PACKAGE
5mm × 7mm VQFN-38
(TOP VIEW)



(1) All GND_A pins must be tied to ground.

PIN DESCRIPTIONS

PIN NO.	NAME	DESCRIPTION
1	V_S-V_{COM}	AVDD for the V_{COM}s
2	V_{COM}-OUT2	V_{COM} output #2
3	V_{COM}-Feedback2	V_{COM} feedback #2
4	V_{SD}	Digital supply; connect to logic supply
5	SCL	Serial clock
6	SDA	Serial data
7	A0	Slave address
8	GND_D	Digital ground
9	GND-V_{COM}	V_{COM} ground
10	V_{COM}-Feedback1	V_{COM} feedback #1
11	V_{COM}-OUT1	V_{COM} output #1
12	V_S-V_{COM}	AVDD for the V_{COM}s
13	V_S	AVDD; connected to analog supply
14	OUT0	Gamma output #1
15	OUT1	Gamma output #2
16	OUT2	Gamma output #3
17	OUT3	Gamma output #4
18	OUT4	Gamma output #5
19	OUT5	Gamma output #6
20	GND_A	Analog ground; must be connected to digital ground (GND_D)
21	GND_A	Analog ground; must be connected to digital ground (GND_D)
22	V_S	AVDD; connected to analog supply

PIN DESCRIPTIONS (continued)

PIN NO.	NAME	DESCRIPTION
23	OUT6	Gamma output #7
24	OUT7	Gamma output #8
25	OUT8	Gamma output #9
26	OUT9	Gamma output #10
27	OUT10	Gamma output #11
28	OUT11	Gamma output #12
29	GND_A	Analog ground; must be connected to digital ground (GND_D)
30	T_{SENSE}	Thermal sense pin; see *Application Section*.
31	V_S	AVDD; connected to analog supply
32	OUT12	Gamma output #13
33	OUT13	Gamma output #14
34	OUT14	Gamma output #15
35	OUT15	Gamma output #16
36	OUT16	Gamma output #17
37	OUT17	Gamma output #18
38	GND_A	Analog ground; must be connected to digital ground (GND_D)

TYPICAL CHARACTERISTICS

At T_A = +25°C, V_S = V_S-V_{COM} = +13.5 V, V_{SD} = +3.3 V, and C_L = 200 pF, unless otherwise noted.

OUTPUT VOLTAGE vs OUTPUT CURRENT (V_{COM})

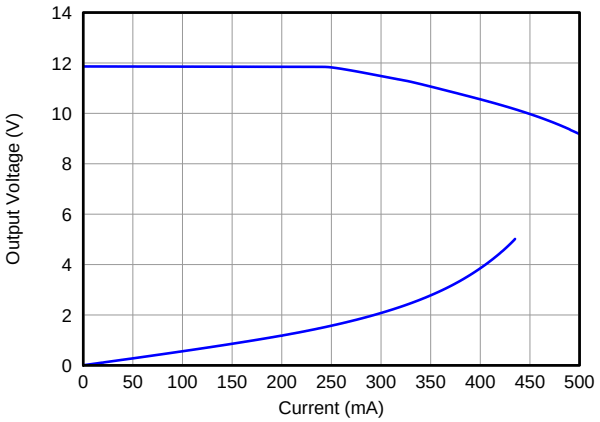


Figure 1.

OUTPUT VOLTAGE vs OUTPUT CURRENT (Channels 1–18)

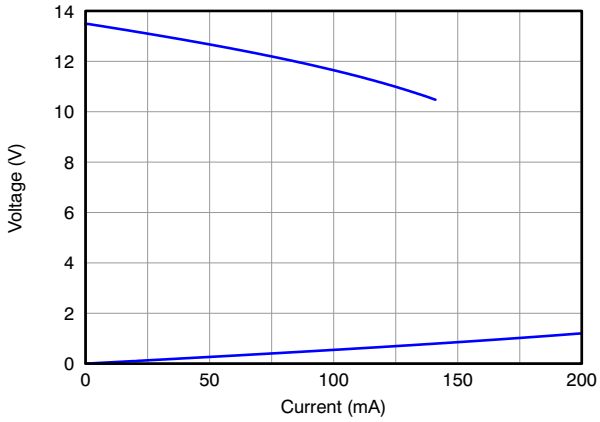


Figure 2.

V_{COM} OUTPUT VOLTAGE vs CODE

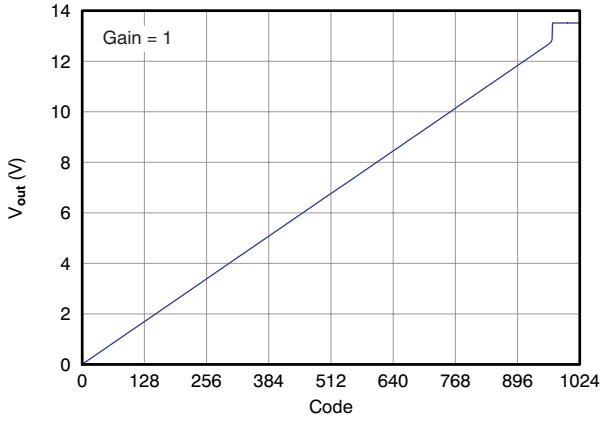


Figure 3.

ANALOG SUPPLY CURRENT HISTOGRAM

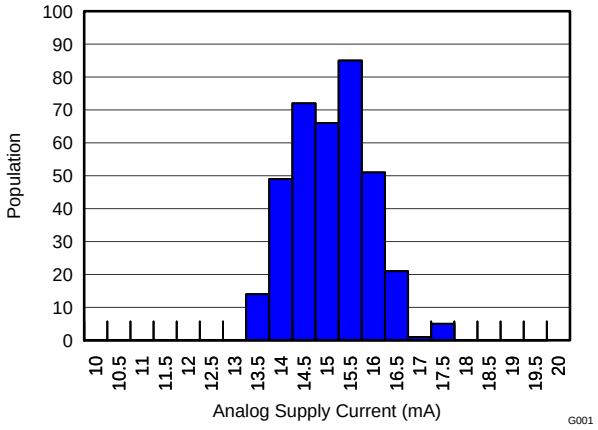


Figure 4.

ANALOG SUPPLY CURRENT vs TEMPERATURE

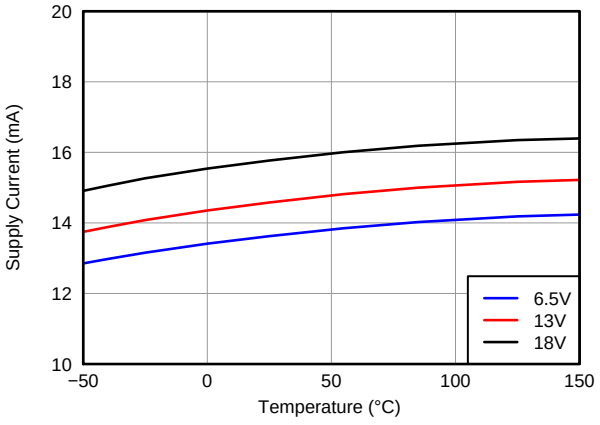


Figure 5.

OUTPUT VOLTAGE vs TEMPERATURE

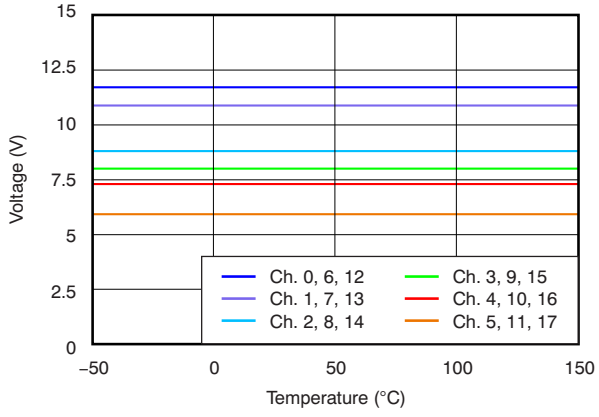


Figure 6.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = V_S-V_{COM} = +13.5 V, V_{SD} = +3.3 V, and C_L = 200 pF, unless otherwise noted.

DIGITAL SUPPLY CURRENT vs TEMPERATURE

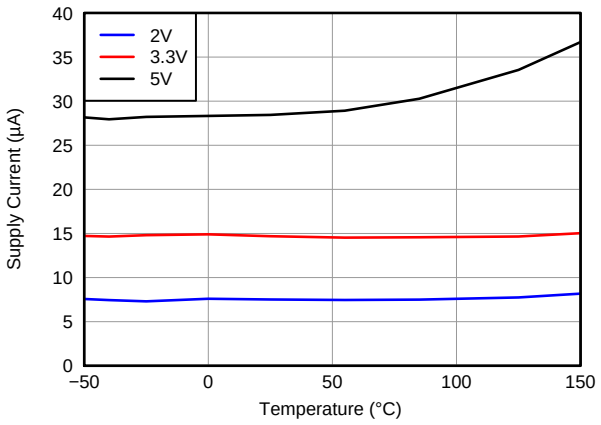


Figure 7.

DIFFERENTIAL LINEARITY ERROR

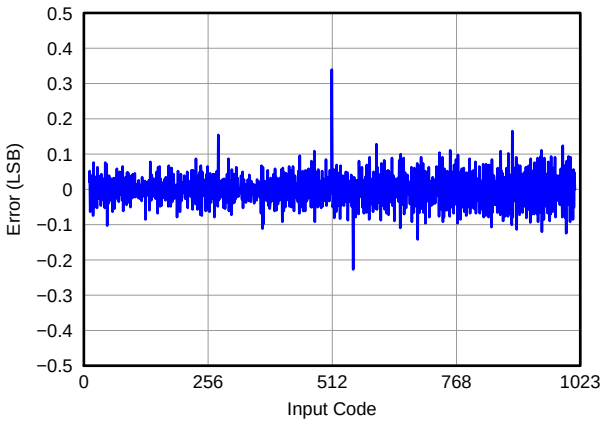


Figure 8.

INTEGRAL LINEARITY ERROR

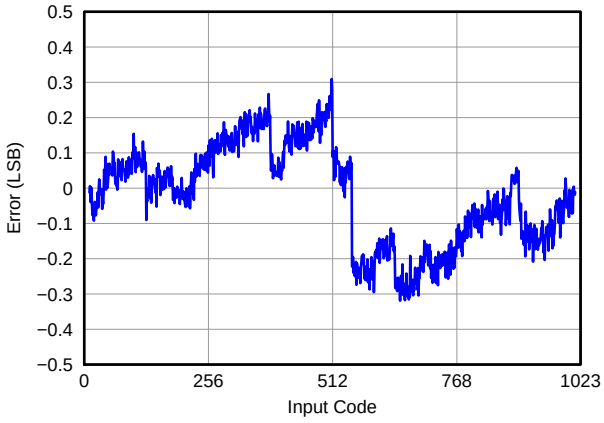


Figure 9.

LARGE-SIGNAL STEP RESPONSE, RISING

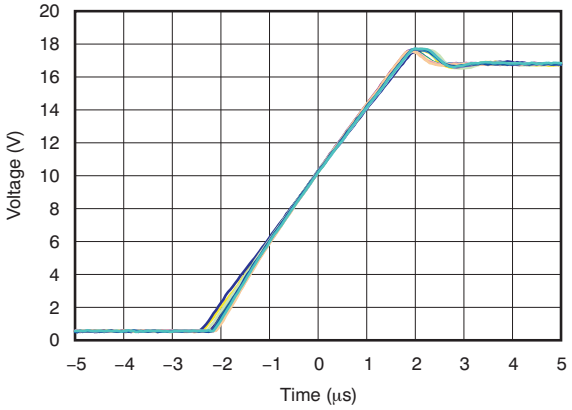


Figure 10.

LARGE-SIGNAL STEP RESPONSE, RISING, V_{COM}

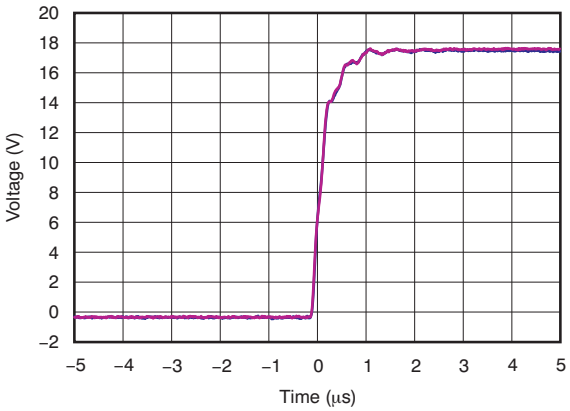


Figure 11.

LARGE-SIGNAL STEP RESPONSE, FALLING

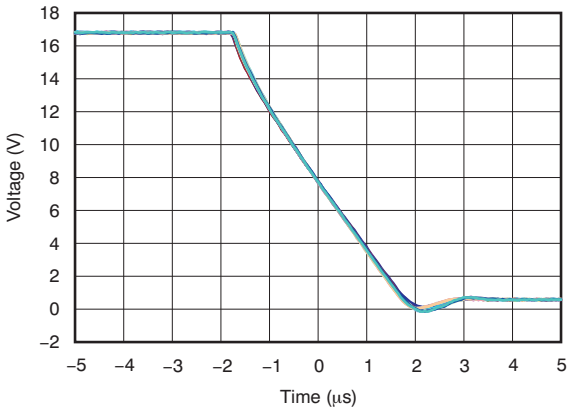


Figure 12.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = V_S-V_{COM} = +13.5 V, V_{SD} = +3.3 V, and C_L = 200 pF, unless otherwise noted.

LARGE-SIGNAL STEP RESPONSE, FALLING, V_{COM}

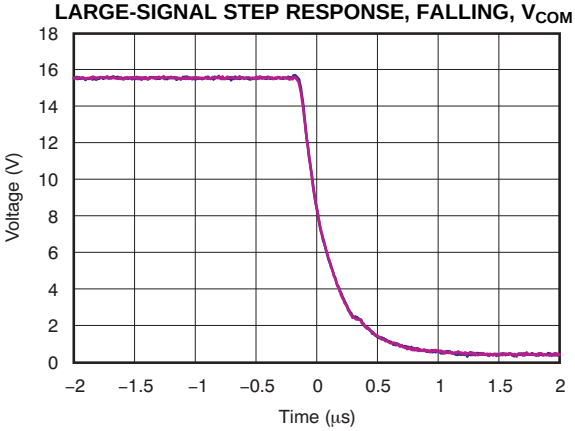


Figure 13.

APPLICATION INFORMATION

GENERAL

The BUF18830 programmable voltage reference allows fast and easy adjustment of 18 programmable gamma reference outputs, each with 10-bit resolution. The BUF18830 is programmed through a high-speed, two-wire interface.

The BUF18830 can be powered using an analog supply voltage from 6.5 V to 20 V, and a digital supply from 2.2 V to 5.5 V. The digital supply must be applied before the analog supply to avoid excessive current and power consumption, or possibly even damage to the device if left connected only to the analog supply for extended periods of time. See Figure 18 for a typical configuration of the BUF18830.

TWO-WIRE BUS OVERVIEW

The BUF18830 communicates over an industry-standard, two-wire interface to receive data in slave mode. This model uses a two-wire, open-drain interface that supports multiple devices on a single bus. Bus lines are driven to a logic low level only. The device that initiates the communication is called a *master*, and the devices controlled by the master are *slaves*. The master generates the serial clock on the clock signal line (SCL), controls the bus access, and generates the START and STOP conditions.

To address a specific device, the master initiates a START condition by pulling the data signal line (SDA) from a high to a low logic level while SCL is high. All slaves on the bus shift in the slave address byte on the rising edge of SCL, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an Acknowledge and pulling SDA low.

Data transfer is then initiated and eight bits of data are sent, followed by an Acknowledge bit. During data transfer, SDA must remain stable while SCL is high. Any change in SDA while SCL is high is interpreted as a START or STOP condition.

Once all data have been transferred, the master generates a STOP condition, indicated by pulling SDA from low to high while SCL is high. The BUF18830 can act only as a slave device; therefore, it never drives SCL. SCL is an input only for the BUF18830.

ADDRESSING THE BUF18830

The address of the BUF18830 is 111010x, where *x* is the state of the A0 pin. When the A0 pin is low, the device acknowledges on address 74h (1110100). If the A0 pin is high, the device acknowledges on address 75h (1110101). Table 1 shows the A0 pin settings and the BUF18830 address options.

Other valid addresses are possible through a simple mask change. Contact your TI representative for information.

Table 1. Quick Reference of BUF18830 Addresses

DEVICE/COMPONENT	
BUF18830 ADDRESS	**ADDRESS**
A0 pin is low (device acknowledges on address 74h)	1110100
A0 pin is high (device acknowledges on address 75h)	1110101

Table 2. Quick Reference of Command Codes

COMMAND	CODE
General-Call Reset	Address byte of 00h followed by a data byte of 06h.
High-Speed Mode	00001xxx, with SCL ≤ 400kHz; where *xxx* are bits unique to the Hs-capable master. This byte is called the Hs master code.

DATA RATES

The two-wire bus operates in one of three speed modes:

- Standard: allows a clock frequency of up to 100 kHz;
- Fast: allows a clock frequency of up to 400 kHz; and
- High-speed mode (also called Hs mode): allows a clock frequency of up to 3.4 MHz.

The BUF18830 is fully compatible with all three modes. No special action is required to use the device in Standard or Fast modes, but High-speed mode must be activated. To activate High-speed mode, send a special address byte of 00001 xxx, with SCL ≤ 400kHz, following the START condition; where *xxx* are bits unique to the Hs-capable master, which can be any value. This byte is called the Hs master code. Refer to Table 2 for a reference for the High-speed mode command code. (Note that this configuration is different from normal address bytes—the low bit does not indicate read/write status.) The BUF18830 responds to the High-speed command regardless of the value of these last three bits. The BUF18830 does not acknowledge this byte; the communication protocol prohibits acknowledgment of the Hs master code. Upon receiving a master code, the BUF18830 switches on its Hs mode filters, and communicates at up to 3.4 MHz. Additional high-speed transfers may be initiated without resending the Hs mode byte by generating a repeat START without a STOP. The BUF18830 switches out of Hs mode with the next STOP condition.

OUTPUT VOLTAGE

Buffer output values are determined by the analog supply voltage (V_S) and the decimal value of the binary input code used to program that buffer. The value is calculated using Equation 1 (for the gamma buffers) and Equation 2 (for the V_{COM} channels):

$$OUT_X = V_S \times \left(\frac{CODE}{1024} \right) \quad (1)$$

$$V_{COM} - OUT_X = V_S - V_{COM} \times \left(\frac{CODE}{1024} \right) \quad (2)$$

The BUF18830 outputs are capable of a full-scale voltage output change in typically 5µs; no intermediate steps are required.

UPDATING THE DAC OUTPUT VOLTAGES

Because the BUF18830 features a double-buffered register structure, updating the digital-to-analog converter (DAC) **register** is not the same as updating the DAC **output voltage**. There are two methods for updating the DAC output voltages.

Method 1: Method 1 is used when it is desirable to have the DAC output voltage change immediately after writing to a DAC register. For each write transaction, the master sets data bit 15 to a '1'. The DAC output voltage update occurs after receiving the 16th data bit for the currently-written register.

Method 2: Method 2 is used when it is desirable to have all DAC output voltages change at the same time. First, the master writes to the desired DAC channels with data bit 15 a '0'. Then, when writing the last desired DAC channel, the master sets data bit 15 to a '1'. All DAC channels are updated at the same time after receiving the 16th data bit.

READ/WRITE OPERATIONS

Read and write operations can be performed for a single DAC/V_{COM} or for multiple DACs/V_{COM}s. Bit D15 of the most significant byte of data determines whether data are loaded to the DACs or not. See Figure 14 and Figure 15 for register timing information.

Read/Write: DAC/V_{COM} Register (volatile memory)

The BUF18830 is able to read from a single DAC/V_{COM}, or multiple DACs/V_{COM}s, or write to the register of a single DAC/V_{COM}, or multiple DACs/V_{COM}s in a single communication transaction. DAC pointer addresses begin with *000000* (which corresponds to OUT0) through *010011* (which corresponds to V_{COM}2).

Write commands are performed by setting the read/write bit LOW. Setting the read/write bit HIGH performs a read transaction.

Writing: DAC/V_{COM} Register (volatile memory)

To write to a single DAC/V_{COM} register:

1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF18830 acknowledges this byte.
3. Send a DAC/V_{COM} pointer address byte. Set bit D7 = 0 and D6 = 0. Bits D5 to D0 are the DAC/V_{COM} address. Only addresses *000000* to *010011* are valid and are acknowledged; see Table 3 for valid addresses.
4. Send two bytes of data for the specified register. Begin by sending the most significant byte first (bits D15 to D8, of which only bits D9 and D8 are used), followed by the least significant byte (bits D7 to D0). The register is updated after receiving the second byte.
5. Send a STOP or START condition on the bus.

The BUF18830 acknowledges each data byte. If the master terminates communication early by sending a STOP or START condition on the bus, the specified register is not updated. Updating the DAC/V_{COM} register is not the same as updating the DAC/V_{COM} output voltage.

The process of updating multiple DAC/V_{COM} registers begins the same as when updating a single register. However, instead of sending a STOP condition after writing the addressed register, the master continues to send data for the next register. The BUF18830 automatically and sequentially steps through subsequent registers as additional data are sent. The process continues until all desired registers have been updated or a STOP or START condition is sent.

To write to multiple DAC/V_{COM} registers:

1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF18830 acknowledges this byte.
3. Send either the OUT0 pointer address byte to start at the first DAC, or send the pointer address byte for whichever DAC/V_{COM} is the first in the sequence of DACs/V_{COM}s to be updated. The BUF18830 begins with this DAC/V_{COM} and steps through subsequent DACs/V_{COM}s in sequential order.
4. Send the bytes of data; begin by sending the most significant byte (bits D15 to D8, of which only bits D9 and D8 have meaning, and bits D15 to D14 must not be 01), followed by the least significant byte (bits D7 to D0). The first two bytes are for the DAC/V_{COM} addressed in the previous step. The DAC/V_{COM} register is automatically updated after receiving the second byte. The next two bytes are for the following DAC/V_{COM}. That DAC/V_{COM} register is updated after receiving the fourth byte. This process continues until the registers of all following DACs/V_{COM}s have been updated.
5. Send a STOP or START condition on the bus.

The BUF18830 acknowledges each byte. To terminate communication, send a STOP or START condition on the bus. Only DAC registers that have received both bytes of data are updated.

Table 3. DAC Register Pointer Addresses

REGISTER	POINTER ADDRESS
000000	OUT0
000001	OUT1
000010	OUT2
000011	OUT3
000100	OUT4
000101	OUT5
000110	OUT6
000111	OUT7
001000	OUT8
001001	OUT9
001010	OUT10
001011	OUT11
001100	OUT12
001101	OUT13
001110	OUT14
001111	OUT15
010000	OUT16
010001	OUT17
010010	VCOM1
010011	VCOM2

Reading: DAC/V_{COM}/OTHER Register

Reading a register returns the data stored in that DAC/V_{COM}/OTHER register. OTHER register addresses are shown in Table 4.

To read a single DAC/V_{COM}/OTHER register:

1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF18830 acknowledges this byte.
3. Send the DAC/V_{COM}/OTHER pointer address byte. Set bit D7 = 0 and D6 = 0; bits D5 to D0 are the DAC/V_{COM}/OTHER address. Only addresses 000000 to 010011, 111100, and 111101 are valid and are acknowledged.
4. Send a START or STOP/START condition.
5. Send the correct device address and read/write bit = HIGH. The BUF18830 acknowledges this byte.
6. Receive two bytes of data. They are for the specified register. The most significant byte (bits D15 to D8) is received first; next is the least significant byte (bits D7 to D0). In the case of DAC/V_{COM} channels, bits D15 to D10 have no meaning.
7. Acknowledge after receiving the first byte.
8. Send a STOP or START condition on the bus or do not acknowledge the second byte to end the read transaction.

Communication may be terminated by sending a premature STOP or START condition on the bus, or by not acknowledging.

To read multiple registers:

1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF18830 acknowledges this byte.
3. Send either the OUT0 pointer address byte to start at the first DAC, or send the pointer address byte for whichever register is the first in the sequence of DACs/V_{COM}s to be read. The BUF18830 begins with this DAC/V_{COM} and steps through subsequent DACs/V_{COM}s in sequential order.
4. Send a START or STOP/START condition on the bus.
5. Send the correct device address and read/write bit = HIGH. The BUF18830 acknowledges this byte.
6. Receive two bytes of data. They are for the specified DAC/V_{COM}. The first received byte is the most significant byte (bits D15 to D8, only bits D9 and D8 have meaning), next is the least significant byte (bits D7 to D0).
7. Acknowledge after receiving each byte of data.
8. When all desired DACs have been read, send a STOP or START condition on the bus.

Communication may be terminated by sending a premature STOP or START condition on the bus, or by not sending the acknowledge bit. The reading of registers Die_ID and Die_Rev is not supported in this mode of operation (they must be read using the single register read method).

Table 4. OTHER Register Pointer Addresses

REGISTER	POINTER ADDRESS
Die_Rev	111100
Die_ID	111101

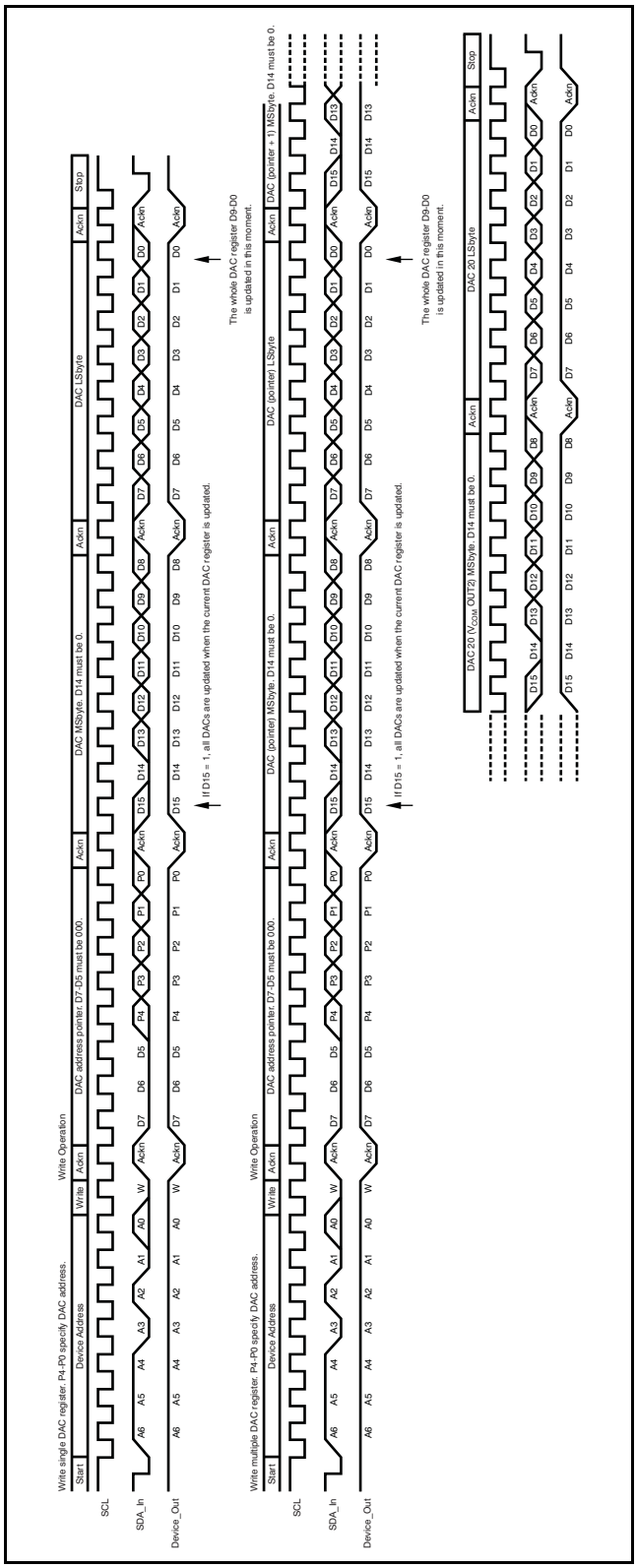


Figure 14. Write DAC Register Timing

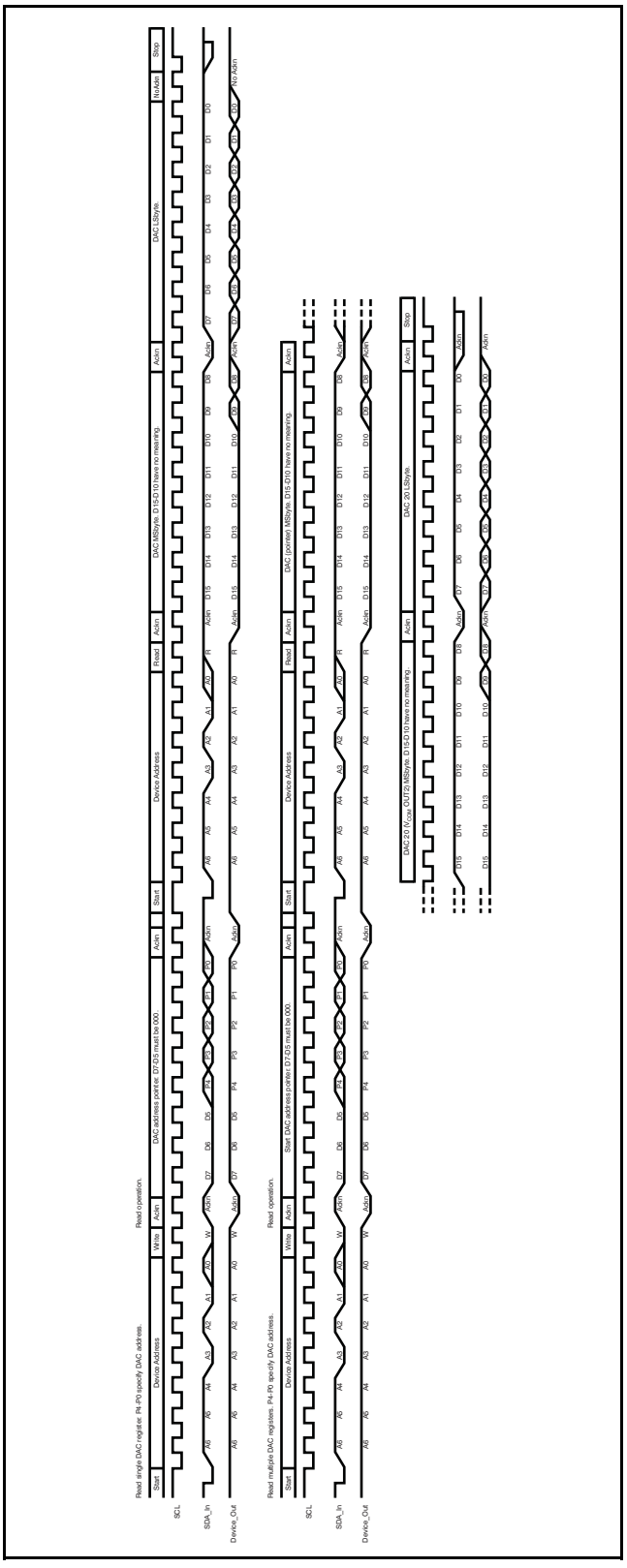


Figure 15. Read Register Timing

TIMING DIAGRAMS

Figure 16 describes the timing operations on the BUF18830. Parameters for Figure 16 are defined in Table 5. Bus definitions are:

Bus Idle: Both SDA and SCL lines remain high.

Start Data Transfer: A change in the state of the SDA line, from high to low, while the SCL line is high, defines a START condition. Each data transfer is initiated with a START condition, denoted as *S* in Figure 16.

Stop Data Transfer: A change in the state of the SDA line from low to high while the SCL line is high defines a STOP condition. Each data transfer terminates with a repeated START or STOP condition, denoted as *P* in Figure 16.

Data Transfer: The number of data bytes transferred between a START and a STOP condition is not limited and is determined by the master device. The receiver acknowledges data transfer.

Acknowledge: Each receiving device, when addressed, is obliged to generate an Acknowledge bit. A device that acknowledges must pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the Acknowledge clock pulse. Setup and hold times must be taken into account. On a master receive, data transfer termination can be signaled by the master generating a Not-Acknowledge on the last byte that has been transmitted by the slave.

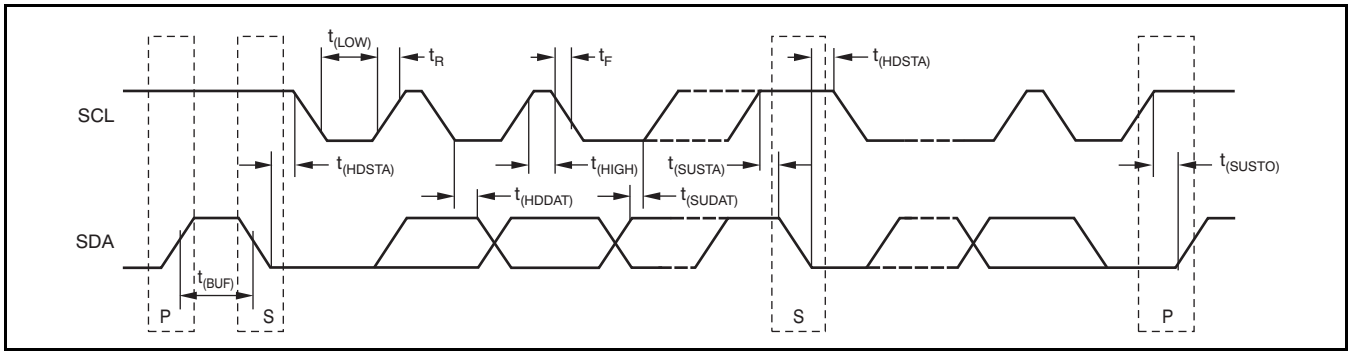


Figure 16. Two-Wire Timing Diagram

Table 5. Timing Characteristics for Figure 16

PARAMETER		FAST MODE		HIGH-SPEED MODE		UNITS
		MIN	MAX	MIN	MAX	
SCL operating frequency	$f_{(SCL)}$	0	0.4	0	3.4	MHz
Bus free time between STOP and START condition	$t_{(BUF)}$	600		160		ns
Hold time after repeated START condition. After this period, the first clock is generated.	$t_{(HDSTA)}$	100		100		ns
Repeated START condition setup time	$t_{(SUSTA)}$	100		100		ns
STOP condition setup time	$t_{(SUSTO)}$	100		100		ns
Data hold time	$t_{(HDDAT)}$	0(1)		0(2)		ns
Data setup time	$t_{(SUDAT)}$	100		10		ns
SCL clock low period	$t_{(low)}$	1300		160		ns
SCL clock high period	$t_{(high)}$	600		60		ns
Clock/data fall time	t_F		300		160	ns
Clock/data rise time	t_R		300		160	ns
for SCLK ≤ 100 kHz			1000			ns

(1) For cases with a fall time of SCL less than 20 ns and/or the rise time or fall time of SDA less than 20 ns, the hold time should be greater than 20 ns.
(2) For cases with a fall time of SCL less than 10 ns and/or the rise or fall time of SDA less than 10 ns, the hold time should be greater than 10 ns.

OUTPUT PROTECTION

The BUF18830 output stages can safely source and sink the current levels indicated in Figure 1 and Figure 2. However, there are other modes where precautions must be taken to prevent to the output stages from being damaged by excessive current flow. The outputs (OUT0 through OUT17) include electrostatic discharge (ESD) protection diodes, as shown in Figure 17. Normally, these diodes do not conduct and are passive during typical device operation. Unusual operating conditions can occur where the diodes may conduct, potentially subjecting them to high, even damaging current levels. These conditions are most likely to occur when a voltage applied to an output exceeds (V_S) + 0.5 V, or drops below GND – 0.5 V.

One common scenario where this condition can occur is when the output pin is connected to a sufficiently large capacitor, and the BUF18830 power-supply source (V_S) is suddenly removed. Removing the power-supply source allows the capacitor to discharge through the current-steering diodes. The energy released during the high current flow period causes the power dissipation limits of the diode to be exceeded. Protection against the high current flow may be provided by placing current-limiting resistors in series with the output, as shown in Figure 17. Select a resistor value that restricts the current level to the maximum rating for the particular pin.

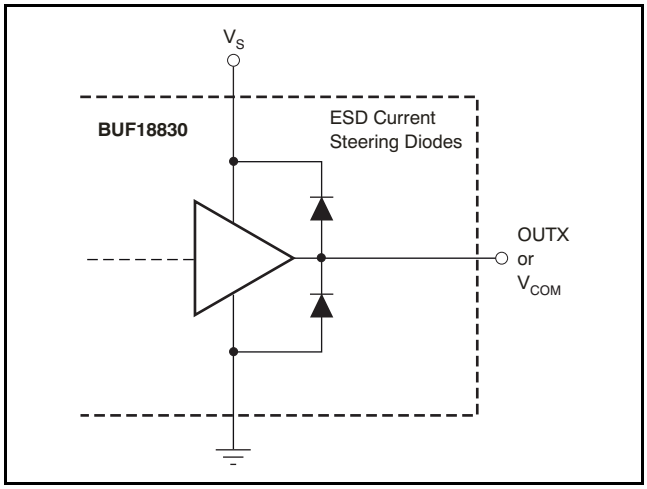
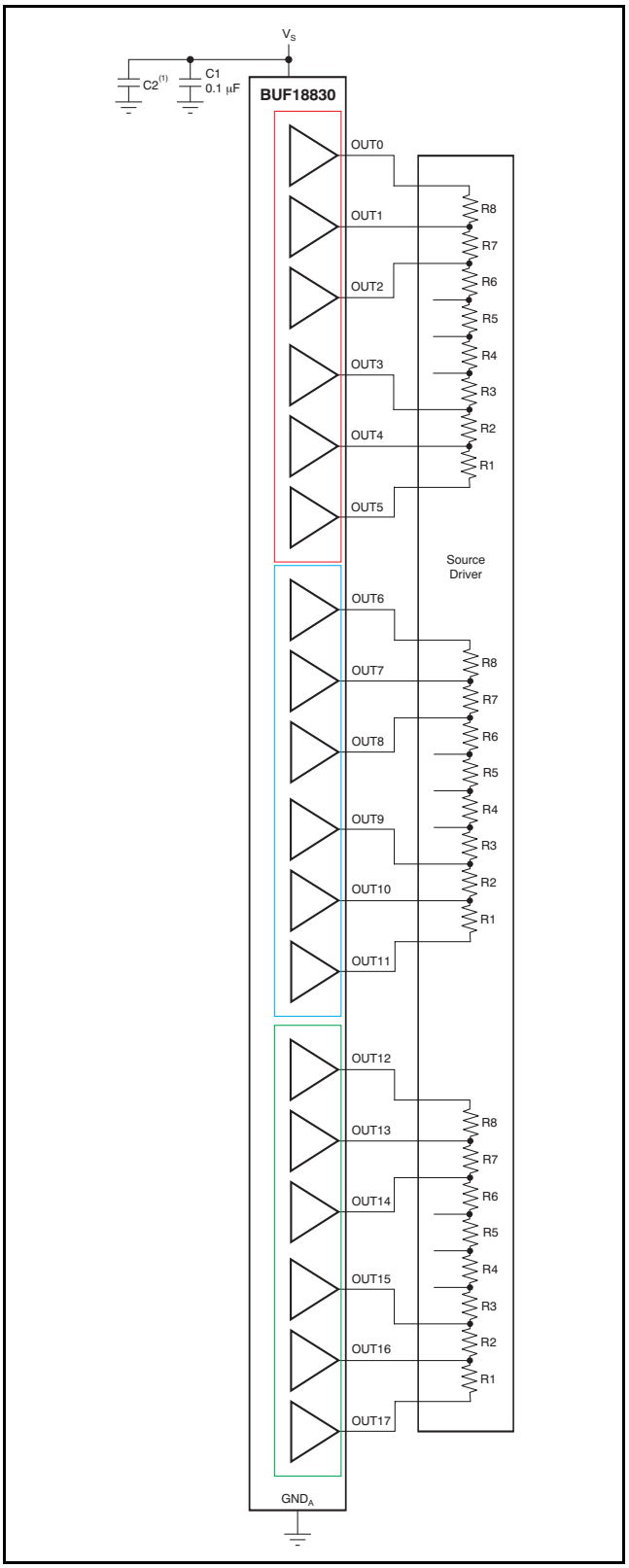


Figure 17. Output Pins ESD Protection Current-Steering Diodes

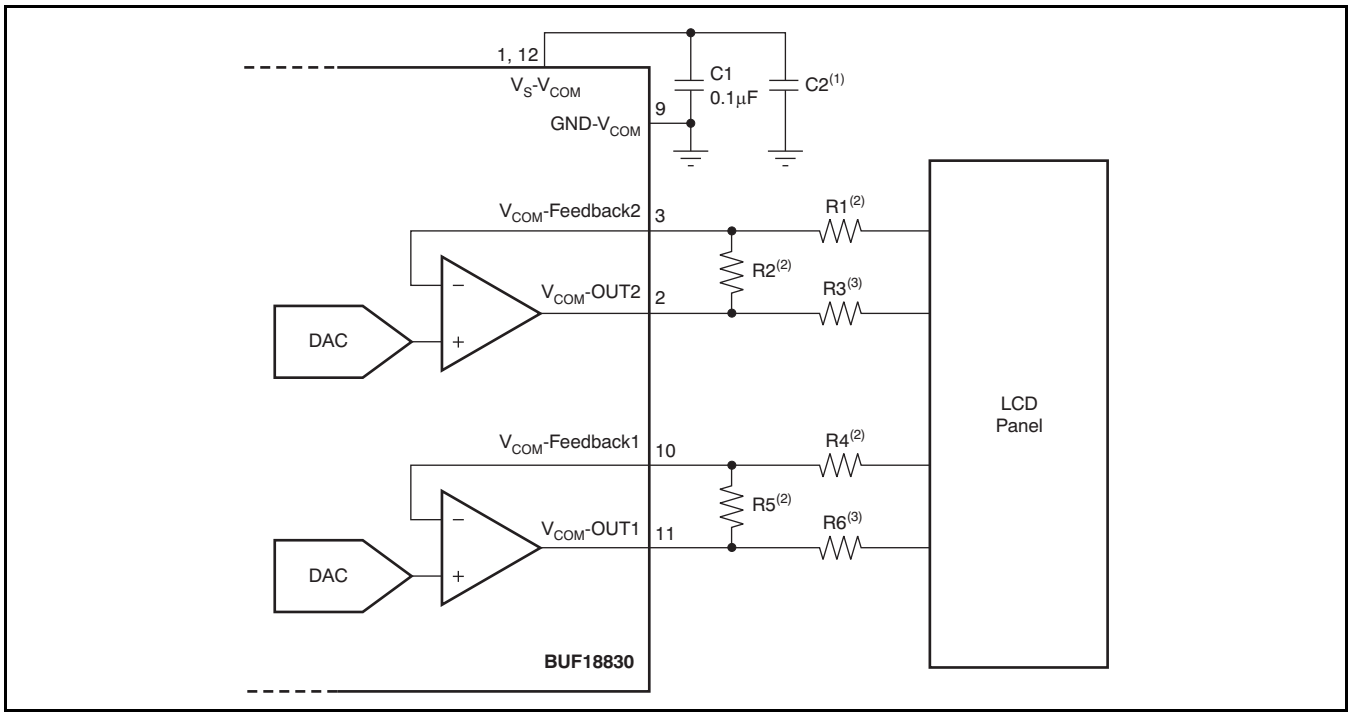
TYPICAL APPLICATIONS

Figure 18 and Figure 19 illustrate typical applications for the BUF18830. Figure 20 shows how to connect a TMP411 to monitor the die temperature of the device.



(1) Tantalum bypass capacitor should be chosen based on peak output current of gamma buffers. Use at least 1 µF for every 1 A of peak current.

Figure 18. Typical OLED Application



(1) Tantalum bypass capacitor should be chosen based on peak output current of V_{COM} buffers. Use at least 1 µF for every 1 A of peak current.

(2) Select gain to provide best picture performance.

(3) Values must be selected for good phase margin when driving large capacitive loads.

Figure 19. Typical V_{COM} Application

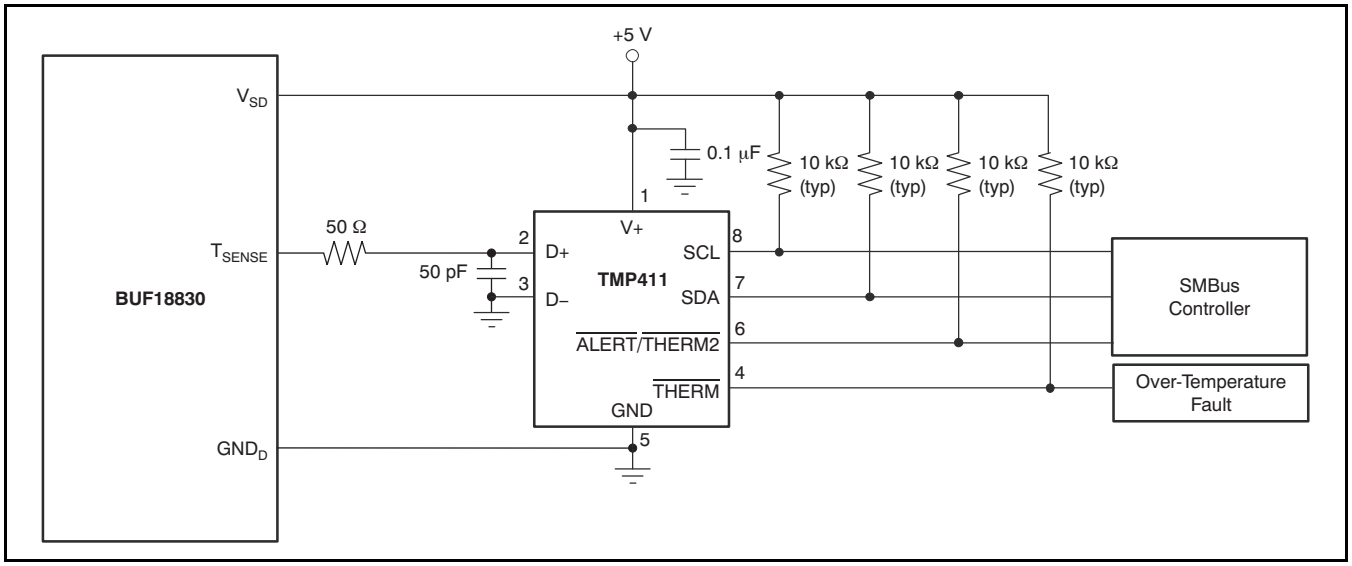
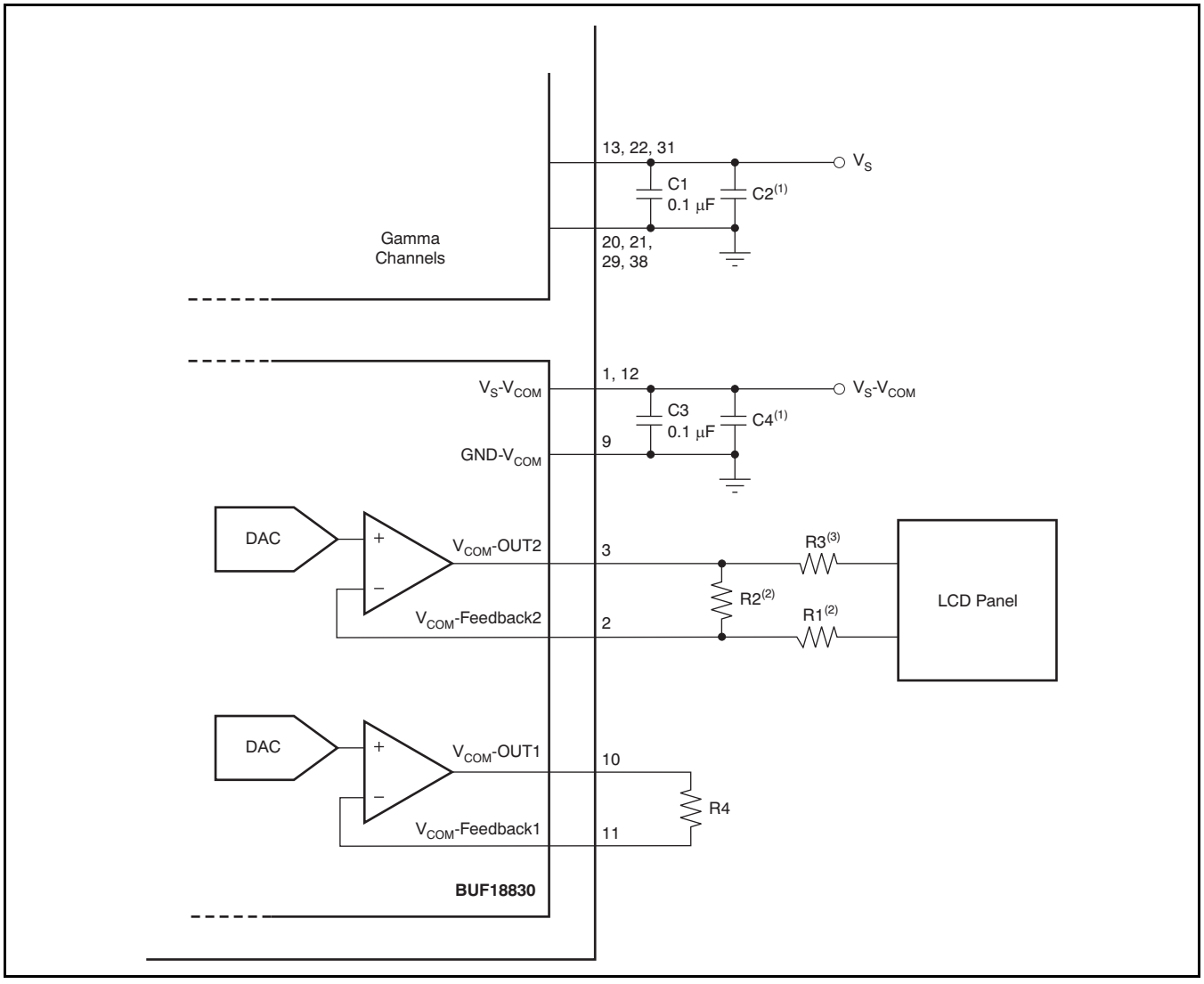


Figure 20. Temperature Measurement Using T_{SENSE} and TMP411

Figure 19 shows a preferred, typical V_{COM} application circuit. It is possible to connect V_S-V_{COM} to a different potential than V_S. However, the operating range for V_S and V_S-V_{COM} must meet the product data sheet specification of 6.5 V to 20 V. There are two sets of gain resistors: R1 and R2, and R4 and R5. These gain resistors should be selected to provide the best V_{COM} performance for the chosen LCD panel. As a result of the large capacitance of the LCD panel, resistors R3 and R6 are selected to improve the phase margin of the amplifier and prevent oscillation that might otherwise occur.

Figure 21 shows how to connect the V_{COM} buffers when only one buffer will be used. It does not matter which V_{COM} buffer is used. V_{COM}-OUT1 is used for this example, but V_{COM}-OUT2 could be used as well. Resistor R3 can be 0 Ω, or the two connections can simply be shorted together with a trace on the PCB. The inputs to the V_{COM} buffers should never be left floating.



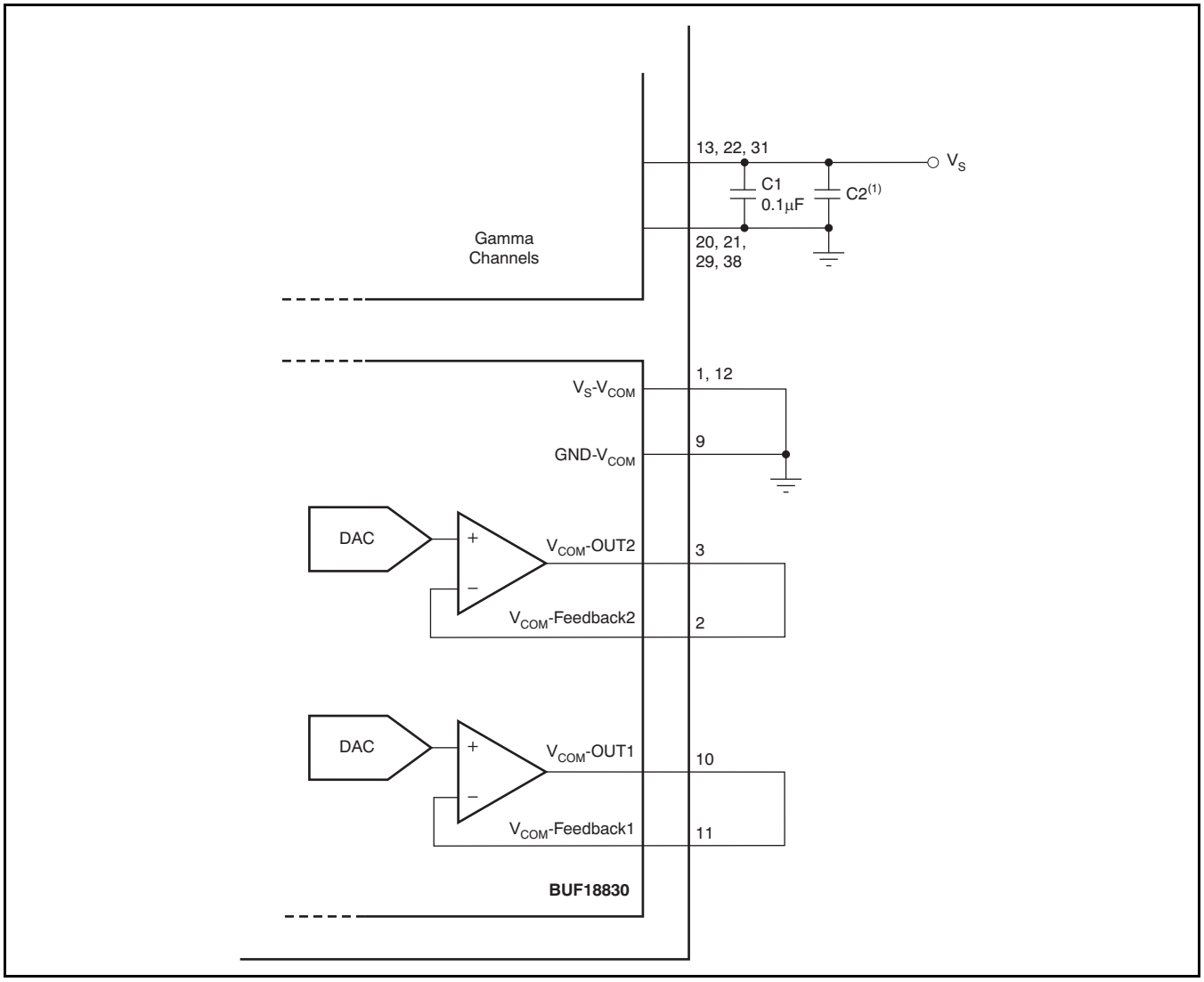
(1) Tantalum bypass capacitor should be chosen based on peak output current of V_{COM} buffers. Use at least 1 µF for every 1 A of peak current.

(2) Select gain to provide best picture performance.

(3) Values must be selected for good phase margin when driving large capacitive loads.

Figure 21. Typical V_{COM} Application Using Only One V_{COM} Amplifier

It is possible to use only the gamma channels of the BUF18830. Figure 22 shows the correct wiring of the BUF18830 when only the gamma channels are used and the V_{COM} amplifiers are not used. Do not leave any pins disconnected; they must be connected as shown.



(1) Tantalum bypass capacitor should be chosen based on peak output current of V_{COM} buffers. Use at least 1 µF for every 1 A of peak current.

Figure 22. Typical Application with No V_{COM} Amplifiers

POWER DISSIPATION AND SAFE OPERATING AREA

Power dissipation depends on power supply, signal, and load conditions. For dc signals, power dissipation is equal to the product of output current (I_{OUT}) and the voltage across the conducting output transistor [(V_S-V_{COM}) – V_{OUT} when sourcing; V_{OUT} – GND when sinking]. Dissipation with ac signals is lower. Application Bulletin AB-039, *Power Amplifier Stress and Power Handling Limitations* (SBOA022, available for download from www.ti.com) explains how to calculate or measure power dissipation with unusual signals and loads.

Figure 23 shows the safe operating area at room temperature with various heatsinking efforts for one V_{COM}. If both V_{COM}s are used, then the maximum power dissipated by all V_{COM}s plus all gamma buffers must be less than 4W when properly heatsinked. Under no circumstances should the design allow the junction temperature to exceed +150°C. Note that the safe output current decreases as (V_S-V_{COM}) – V_{OUT} or V_{OUT} – GND increases.

The power that can be safely dissipated in the package is related to the ambient temperature and the heatsink design. The PowerPAD package was specifically designed to provide excellent power dissipation, but board layout greatly influences the heat dissipation of the package. Refer to the *Thermally-Enhanced PowerPAD Package* section for further details.

The relationship between thermal resistance and power dissipation can be expressed as:

$T_J = T_A + T_{JA}$

$T_{JA} = P_D \times \theta_{JA}$

Combining these equations produces:

$T_J = T_A + P_D \times \theta_{JA}$

where:

T_J = Junction temperature (°C)

T_A = Ambient temperature (°C)

θ_{JA} = Junction-to-ambient thermal resistance (°C/W)

P_D = Power dissipation (W)

To determine the required heatsink area, required power dissipation should be calculated and the relationship between power dissipation and thermal resistance should be considered to minimize shutdown conditions and allow for proper long-term operation (junction temperature of +85°C or less).

Once the heatsink area has been selected, worst-case load conditions should be tested to ensure proper thermal protection.

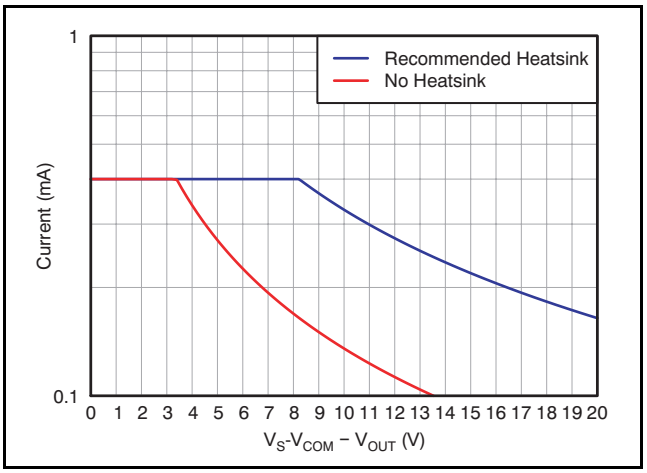


Figure 23. Safe Operating Area at Room Temperature for One V_{COM} Operating

To achieve the thermal performance shown in the Electrical Characteristics, a 2-oz copper plane size of 9 in^2 was used. The PowerPAD package is well-suited for continuous power levels from 2 W to 4 W, depending on ambient temperature and heatsink area. The addition of airflow also influences maximum power dissipation.

THERMALLY-ENHANCED PowerPAD PACKAGE

The BUF18830 uses a thermally-enhanced, standard size IC package. This package enhances power dissipation capability significantly and can be easily mounted using standard printed circuit board (PCB) assembly techniques, and can also be removed and replaced using standard repair procedures.

The RGF PowerPAD package is designed so that the leadframe die pad (or thermal pad) is exposed on the bottom of the IC. The thermal pad provides an extremely low thermal resistance (θ_{JC}) path between the die and the exterior of the package.

PowerPAD packages with exposed pad down are designed to be soldered directly to the PCB, using the PCB as a heatsink. Texas Instruments does not recommend the use of the of a PowerPAD package without soldering it to the PCB because of the risk of lower thermal performance and mechanical integrity. In addition, through the use of thermal vias, the bottom-side thermal pad can be directly connected to a power plane or special heatsink structure designed into the PCB. The PowerPAD should be at the same voltage potential as GND. Soldering the PowerPAD to the PCB is always required, even with applications that have low power dissipation. It provides the necessary thermal and mechanical connection between the leadframe die and the PCB.

PowerPAD PCB Design Procedures

1. The PowerPAD must be connected to GND.
2. Prepare the PCB with a top side etch pattern, as shown in the attached thermal land pattern mechanical drawing. There should be etch for the leads as well as etch for the thermal land.
3. Place the recommended number of holes (or thermal vias) in the area of the thermal pad, as seen in the attached thermal land pattern mechanical drawing. These holes should be 13 mils (.013 in, or 330.2 µm) in diameter. They are kept small so that solder wicking through the holes is not a problem during reflow.
4. Connect all holes, including those within the thermal pad area and outside the pad area, to the internal plane that is connected to GND.
5. When connecting the thermal vias to the internal plane, do not use the typical web or spoke via connection methodology (as Figure 24 shows). Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This configuration makes the soldering of vias that have plane connections easier. However, in this application, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the PowerPAD package should be connected to the internal plane with a complete connection around the entire circumference of the plated through-hole.

For solder mask requirements and complete assembly procedures, as well as detailed information on the PowerPAD package including thermal modeling considerations and repair procedures, see Technical Brief SLUA271, *QFN/SON PCB Attachment*, available at www.ti.com.

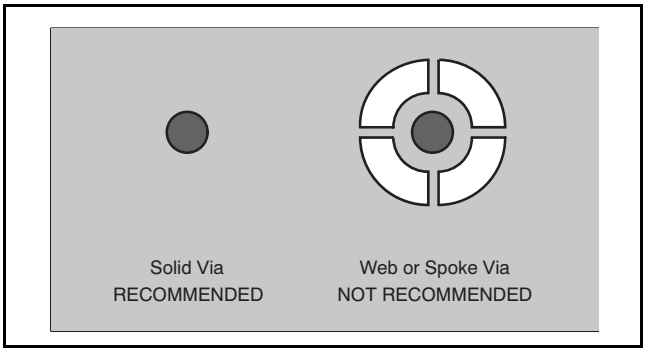


Figure 24. Via Connection Methods

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BUF18830AIRGFR	ACTIVE	VQFN	RGF	38	3000	RoHS & Green	Call TI | NIPDAU	Level-3-260C-168 HR	-40 to 85	BUF18830	Samples
BUF18830AIRGFT	ACTIVE	VQFN	RGF	38	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	BUF18830	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

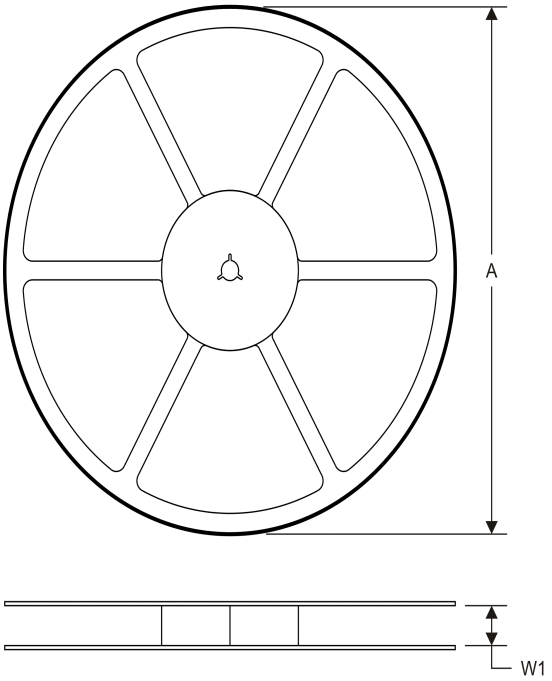
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

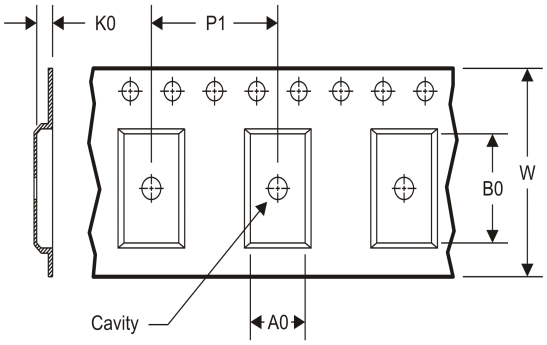
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



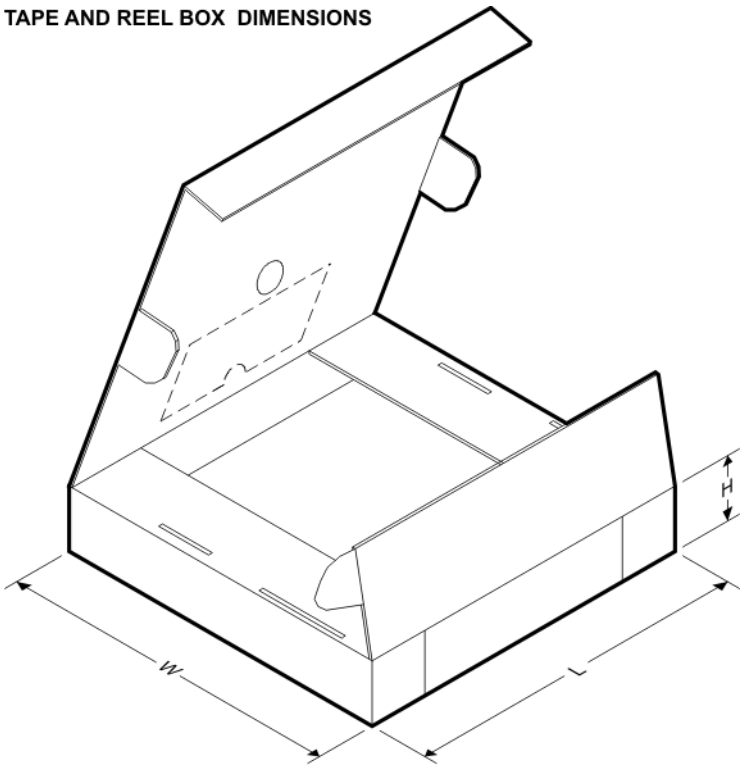
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BUF18830AIRGFR	VQFN	RGF	38	3000	330.0	16.4	5.25	7.25	1.45	8.0	16.0	Q1
BUF18830AIRGFT	VQFN	RGF	38	250	180.0	16.4	5.25	7.25	1.45	8.0	16.0	Q1

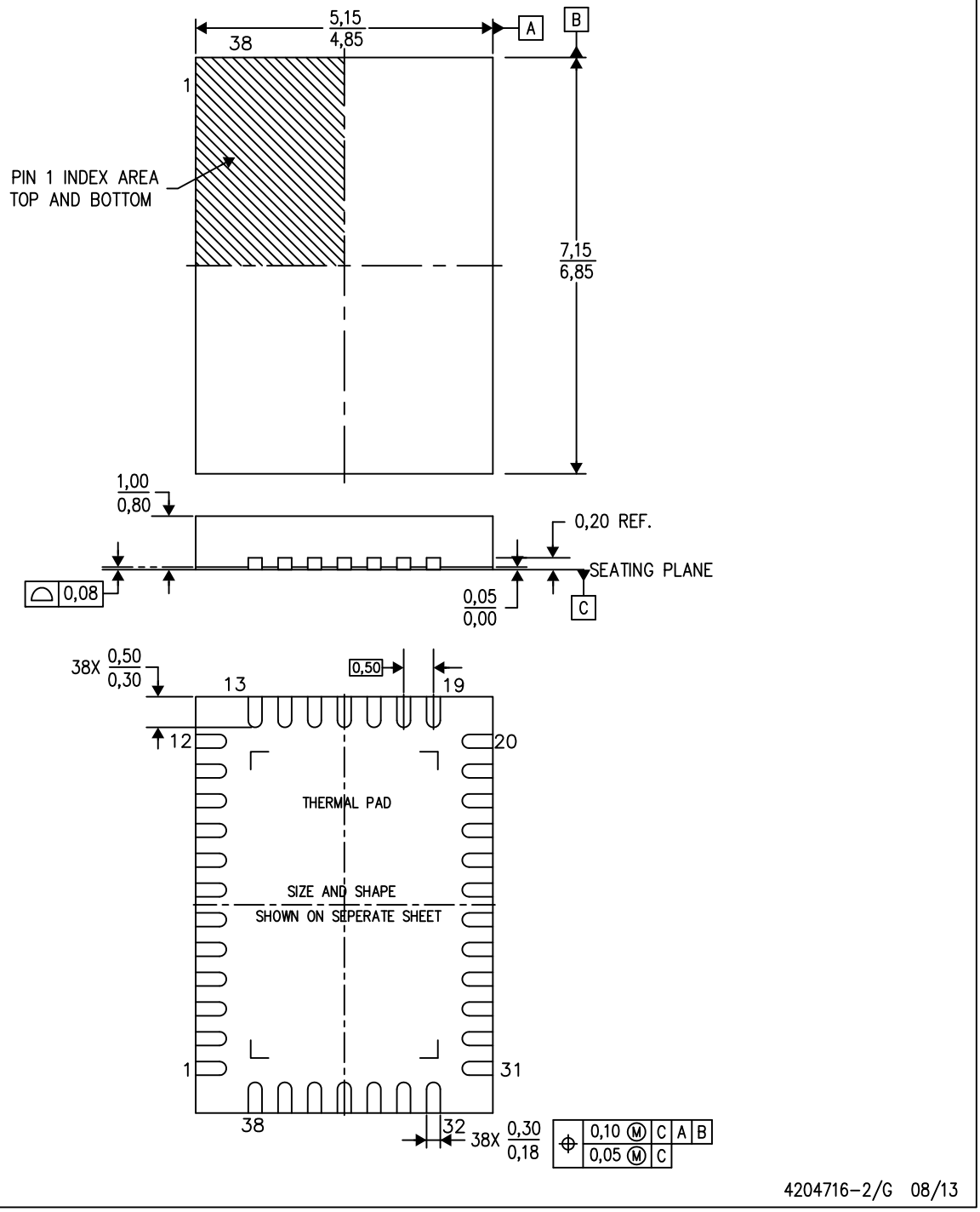
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BUF18830AIRGFR	VQFN	RGF	38	3000	367.0	367.0	38.0
BUF18830AIRGFT	VQFN	RGF	38	250	210.0	185.0	35.0

RGF (R–PVQFN–N38) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

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