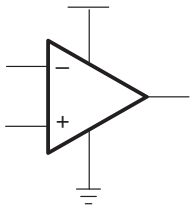
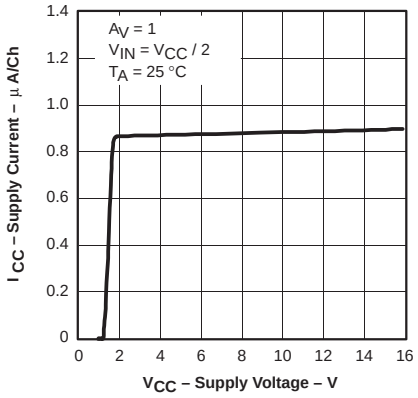
- **Micro-Power Operation . . . < 1 μA/Channel**
- **Input Common-Mode Range Exceeds the Rails . . . –0.1 V to V_{CC} + 5 V**
- **Reverse Battery Protection Up To 18 V**
- **Rail-to-Rail Input/Output**
- **Gain Bandwidth Product . . . 5.5 kHz**
- **Supply Voltage Range . . . 2.5 V to 16 V**
- **Specified Temperature Range**
  - **– T_A = 0°C to 70°C . . . Commercial Grade**
  - **– T_A = –40°C to 125°C . . . Industrial Grade**
- **Ultrasmall Packaging**
  - **– 5-Pin SOT-23 (TLV2401)**
  - **– 8-Pin MSOP (TLV2402)**
- **Universal OpAmp EVM (Refer to the EVM Selection Guide SLOU060)**

Operational Amplifier



SUPPLY CURRENT vs SUPPLY VOLTAGE



description

The TLV240x family of single-supply operational amplifiers has the lowest supply current available today at only 880 nA per channel. Reverse battery protection guards the amplifier from an over-current condition due to improper battery installation. For harsh environments, the inputs can be taken 5 V above the positive supply rail without damage to the device.

The low supply current is coupled with extremely low input bias currents enabling them to be used with mega-Ω resistors making them ideal for portable, long active life, applications. DC accuracy is ensured with a low typical offset voltage as low as 390 μV, CMRR of 120 dB and minimum open loop gain of 130 V/mV at 2.7 V.

The maximum recommended supply voltage is as high as 16 V and ensured operation down to 2.5 V, with electrical characteristics specified at 2.7 V, 5 V and 15 V. The 2.5-V operation makes it compatible with Li-Ion battery-powered systems and many micro-power microcontrollers available today including TI's MSP430.

All members are available in PDIP and SOIC with the singles in the small SOT-23 package, duals in the MSOP, and quads in TSSOP.

SELECTION OF SINGLE SUPPLY OPERATIONAL AMPLIFIER PRODUCTS†

DEVICE	V_{CC} (V)	V_{IO} (mV)	BW (MHz)	SLEW RATE (V/μs)	I_{CC}/ch (μA)	RAIL-TO-RAIL
TLV240x‡	2.5–16	0.390	0.005	0.002	0.880	I/O
TLV224x	2.5–12	0.600	0.005	0.002	1	I/O
TLV2211	2.7–10	0.450	0.065	0.025	13	O
TLV245x	2.7–6	0.020	0.22	0.110	23	I/O
TLV225x	2.7–8	0.200	0.2	0.12	35	O

† All specifications are typical values measured at 5 V.
‡ This device also offers 18-V reverse battery protection and 5-V over-the-rail operation on the inputs.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TLV2401 AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES			
		SMALL OUTLINE† (D)	SOT-23† (DBV)	SYMBOLS	PLASTIC DIP (P)
0°C to 70°C	1500 μV	TLV2401CD	TLV2401CDBV	VAWC	—
-40°C to 125°C		TLV2401ID	TLV2401IDBV	VAWI	TLV2401IP

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2401CDR).

TLV2402 AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES			
		SMALL OUTLINE† (D)	MSOP† (DGK)	SYMBOLS	PLASTIC DIP (P)
0°C to 70°C	1500 μV	TLV2402CD	TLV2402CDGK	xxTIAIX	—
–40°C to 125°C		TLV2402ID	TLV2402IDGK	xxTIAIY	TLV2402IP

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2402CDR).

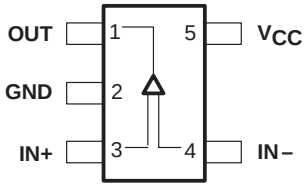
TLV2404 AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES		
		SMALL OUTLINE† (D)	PLASTIC DIP (N)	TSSOP (PW)
0°C to 70°C	1500 μV	TLV2404CD	TLV2404CN	TLV2404CPW
–40°C to 125°C		TLV2404ID	TLV2404IN	TLV2404IPW

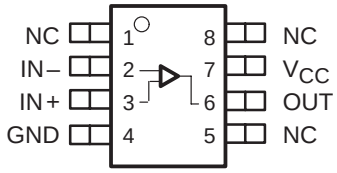
† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2404CDR).

TLV240x PACKAGE PINOUTS

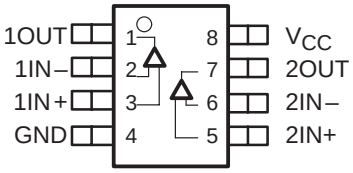
TLV2401
DBV PACKAGE
(TOP VIEW)



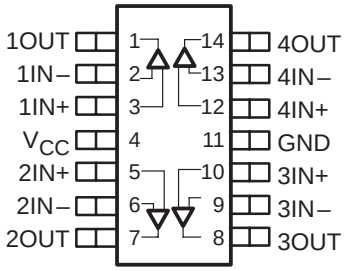
TLV2401
D OR P PACKAGE
(TOP VIEW)



TLV2402
D, DGK, OR P PACKAGE
(TOP VIEW)



TLV2404
D, N, OR PW PACKAGE
(TOP VIEW)



NC – No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 17 V
Differential input voltage range, V_{ID} . . . . . ±20 V
Input current range, I_I (any input) . . . . . ±10 mA
Output current range, I_O . . . . . ±10 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix . . . . . 0°C to 70°C
I suffix . . . . . –40°C to 125°C
Maximum junction temperature, T_J . . . . . 150°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential voltages, are with respect to GND

DISSIPATION RATING TABLE

PACKAGE	Θ_{JC} (°C/W)	Θ_{JA} (°C/W)	$T_A \le 25°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D (8)	38.3	176	710 mW	142 mW
D (14)	26.9	122.6	1022 mW	204.4 mW
DBV (5)	55	324.1	385 mW	77.1 mW
DGK (8)	54.2	259.9	481 mW	96.2 mW
N (14)	32	78	1600 mW	320.5 mW
P (8)	41	104	1200 mW	240.4 mW
PW (14)	29.3	173.6	720 mW	144 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}	Single supply	2.5	16	V
	Split supply	±1.25	±8	
Common-mode input voltage range, V_{ICR}		–0.1	V_{CC}+5	V
Operating free-air temperature, T_A	C-suffix	0	70	°C
	I-suffix	–40	125	

electrical characteristics at recommended operating conditions, V_{CC} = 2.7, 5 V, and 15 V (unless otherwise noted)

dc performance

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_O = V_{CC}/2$ V, $V_{IC} = V_{CC}/2$ V, $R_S = 50\ \Omega$		25°C		390	1200	μV
				Full range			1500	
α_{VIO}	Offset voltage draft			25°C		3		μV/°C
CMRR	Common-mode rejection ratio	V_{IC} = 0 to V_{CC}, $R_S = 50\ \Omega$	V_{CC} = 2.7 V	25°C	63	120		dB
				Full range	60			
			V_{CC} = 5 V	25°C	70	120		
				Full range	63			
			V_{CC} = 15 V	25°C	80	120		
				Full range	75			
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 2.7 V, $V_{O(pp)}$ = 1 V, R_L = 500 kΩ		25°C	130	400		V/mV
				Full range	30			
		V_{CC} = 5 V, $V_{O(pp)}$ = 3 V, R_L = 500 kΩ		25°C	300	1000		
				Full range	100			
		V_{CC} = 15 V, $V_{O(pp)}$ = 6 V, R_L = 500 kΩ		25°C	1000	1800		
				Full range	120			

† Full range is 0°C to 70°C for the C suffix and –40°C to 125°C for the I suffix. If not specified, full range is –40°C to 125°C.

input characteristics

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
I_{IO}	Input offset current	$V_O = V_{CC}/2$ V, $V_{IC} = V_{CC}/2$ V, $R_S = 50\ \Omega$		25°C		25	250	pA
			TLV240xC	Full range			300	
			TLV240xI				400	
I_{IB}	Input bias current			25°C		100	300	pA
			TLV240xC	Full range			350	
			TLV240xI				900	
$r_{i(d)}$	Differential input resistance			25°C		300		MΩ
$C_{i(c)}$	Common-mode input capacitance	f = 100 kHz		25°C		3		pF

† Full range is 0°C to 70°C for the C suffix and –40°C to 125°C for the I suffix. If not specified, full range is –40°C to 125°C.

electrical characteristics at recommended operating conditions, V_{CC} = 2.7, 5 V, and 15 V (unless otherwise noted) (continued)

output characteristics

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$V_{IC} = V_{CC}/2$, $I_{OH} = -2\ \mu A$	V_{CC} = 2.7 V	25°C	2.65	2.68		V
				Full range	2.63			
			V_{CC} = 5 V	25°C	4.95	4.98		
				Full range	4.93			
			V_{CC} = 15 V	25°C	14.95	14.98		
				Full range	14.93			
		$V_{IC} = V_{CC}/2$, $I_{OH} = -50\ \mu A$	V_{CC} = 2.7 V	25°C	2.62	2.65		
				Full range	2.6			
			V_{CC} = 5 V	25°C	4.92	4.95		
				Full range	4.9			
			V_{CC} = 15 V	25°C	14.92	14.95		
				Full range	14.9			
V_{OL}	Low-level output voltage	$V_{IC} = V_{CC}/2$, I_{OL} = 2 µA		25°C		90	150	mV
				Full range			180	
		$V_{IC} = V_{CC}/2$, I_{OL} = 50 µA		25°C		180	230	
				Full range			260	
I_O	Output current	V_O = 0.5 V from rail		25°C		±200		µA

† Full range is 0°C to 70°C for the C suffix and –40°C to 125°C for the I suffix. If not specified, full range is –40°C to 125°C.

power supply

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
I_{CC}	Supply current (per channel)	$V_O = V_{CC}/2$	V_{CC} = 2.7 V or 5 V	25°C		880	950	nA
				Full range			1290	
			V_{CC} = 15 V	25°C		900	990	
				Full range			1350	
	Reverse supply current	V_{CC} = –18 V, V_{IN} = 0 V, V_O = Open circuit		25°C		50		nA
PSRR	Power supply rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	V_{CC} = 2.7 to 5 V, $V_{IC} = V_{CC}/2$ V, No load,		25°C	100	120		dB
			TLV240xC	Full range	96			
			TLV240xI		85			dB
		V_{CC} = 5 to 15 V, $V_{IC} = V_{CC}/2$ V, No load		25°C	100	120		dB
				Full range	100			

† Full range is 0°C to 70°C for the C suffix and –40°C to 125°C for the I suffix. If not specified, full range is –40°C to 125°C.

electrical characteristics at recommended operating conditions, V_{CC} = 2.7, 5 V, and 15 V (unless otherwise noted) (continued)

dynamic performance

PARAMETER		TEST CONDITIONS			T_A	MIN	TYP	MAX	UNIT
UGBW	Unity gain bandwidth	R_L = 500 kΩ,		C_L = 100 pF	25°C		5.5		kHz
SR	Slew rate at unity gain	$V_{O(pp)}$ = 0.8 V,	R_L = 500 kΩ,	C_L = 100 pF	25°C		2.5		V/ms
ϕM	Phase margin	R_L = 500 kΩ,	C_L = 100 pF		25°C		60°		
	Gain margin						15		dB
t_S	Settling time	V_{CC} = 2.7 or 5 V, $V_{(STEP)PP}$ = 1 V, A_V = –1,	C_L = 100 pF, R_L = 100 kΩ	0.1%	25°C		1.84		ms
		V_{CC} = 15 V, $V_{(STEP)PP}$ = 1 V, A_V = –1,	C_L = 100 pF, R_L = 100 kΩ	0.1%			6.1		
				0.01%			32		

noise/distortion performance

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		800		nV/√Hz
		f = 100 Hz			500		
I_n	Equivalent input noise current	f = 100 Hz			8		fA/√Hz

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input Offset Voltage	vs Common-mode input voltage	1, 2, 3
I_{IB}	Input Bias Current	vs Free-air temperature	4, 6, 8
		vs Common-mode input voltage	5, 7, 9
I_{IO}	Input Offset Current	vs Free-air temperature	4, 6, 8
		vs Common-mode input voltage	5, 7, 9
CMRR	Common-mode rejection ratio	vs Frequency	10
V_{OH}	High-level output voltage	vs High-level output current	11, 13, 15
V_{OL}	Low-level output voltage	vs Low-level output current	12, 14, 16
$V_{O(PP)}$	Output voltage peak-to-peak	vs Frequency	17
Z_o	Output impedance	vs Frequency	18
I_{CC}	Supply current	vs Supply voltage	19
PSRR	Power supply rejection ratio	vs Frequency	20
A_{VD}	Differential voltage gain	vs Frequency	21
	Phase	vs Frequency	21
	Gain-bandwidth product	vs Supply voltage	22
SR	Slew rate	vs Free-air temperature	23
ϕ_m	Phase margin	vs Capacitive load	24
	Gain margin	vs Capacitive load	25
	Supply current	vs Reverse voltage	26
	Voltage noise over a 10 Second Period		27
	Large signal follower pulse response		28, 29, 30
	Small signal follower pulse response		31
	Large signal inverting pulse response		32, 33, 34
	Small signal inverting pulse response		35
	Crosstalk	vs Frequency	36

TYPICAL CHARACTERISTICS

INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

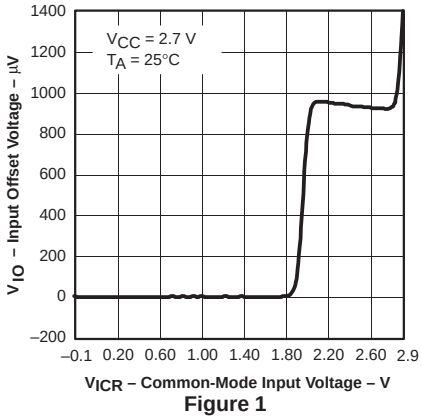


Figure 1

INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

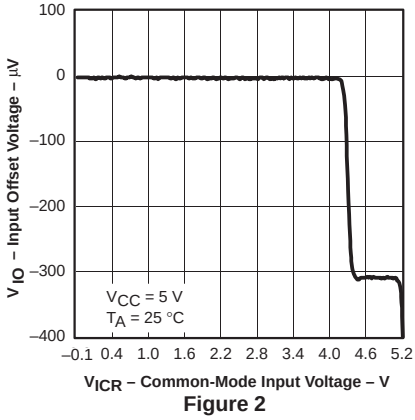


Figure 2

INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

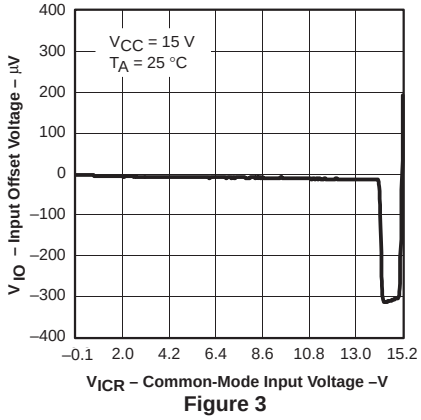


Figure 3

INPUT BIAS / OFFSET CURRENT vs FREE-AIR TEMPERATURE

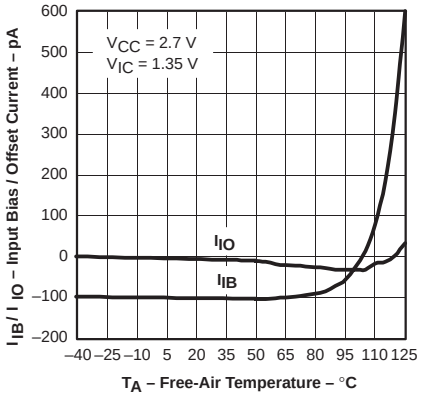


Figure 4

INPUT BIAS / OFFSET CURRENT vs COMMON MODE INPUT VOLTAGE

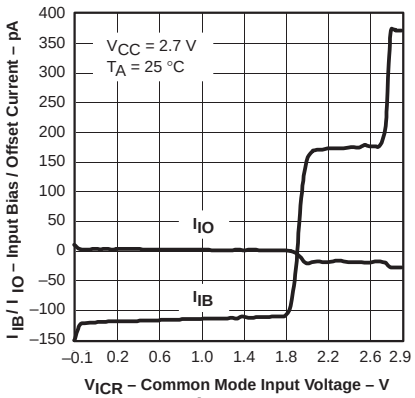


Figure 5

INPUT BIAS / OFFSET CURRENT vs FREE-AIR TEMPERATURE

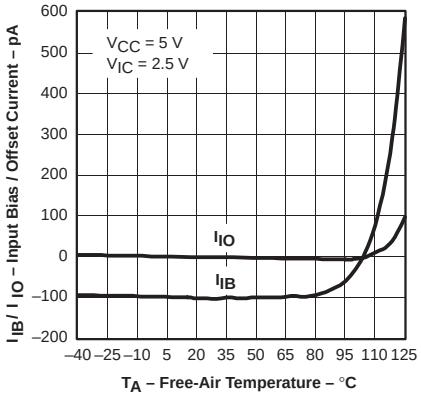


Figure 6

INPUT BIAS / OFFSET CURRENT vs COMMON-MODE INPUT VOLTAGE

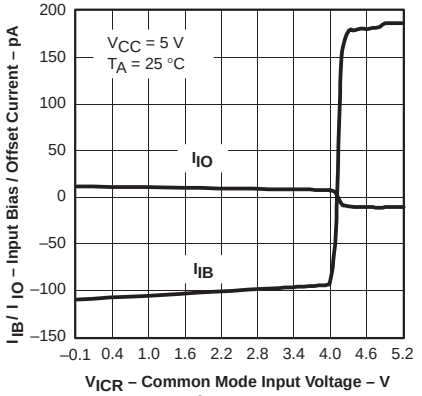


Figure 7

INPUT BIAS / OFFSET CURRENT vs FREE-AIR TEMPERATURE

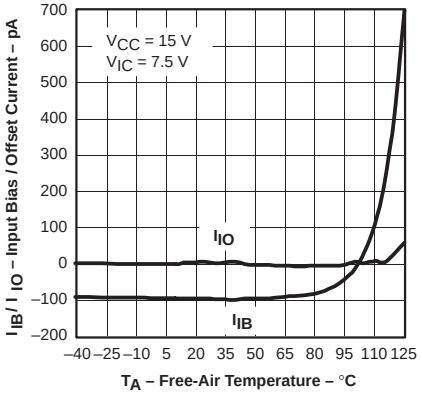


Figure 8

INPUT BIAS / OFFSET CURRENT vs COMMON-MODE INPUT VOLTAGE

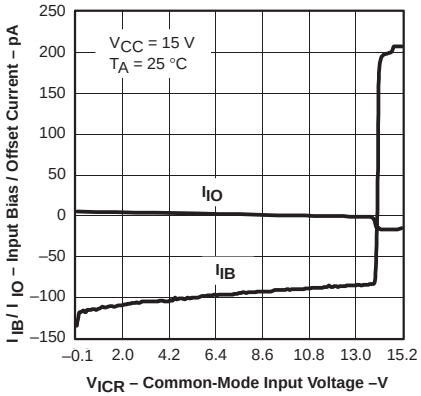


Figure 9

TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO vs FREQUENCY

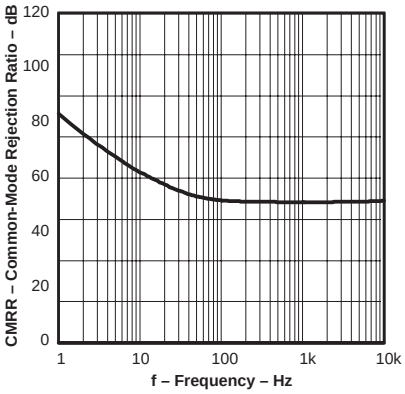


Figure 10

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

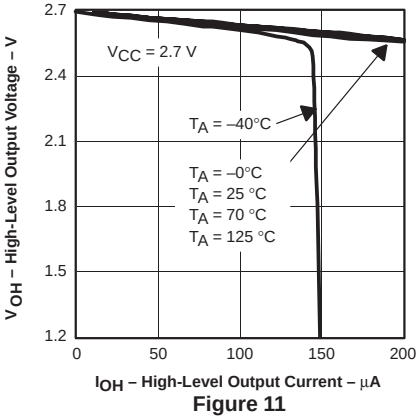


Figure 11

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

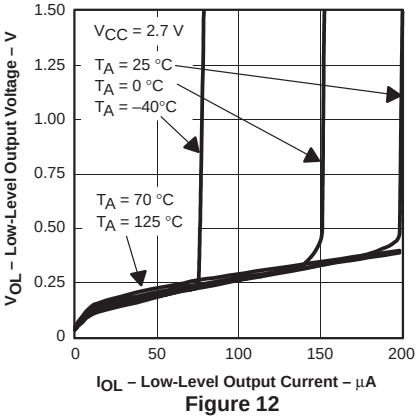


Figure 12

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

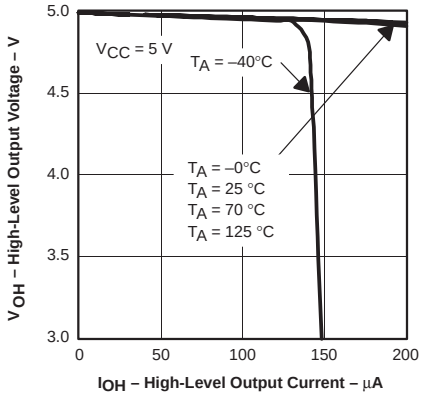


Figure 13

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

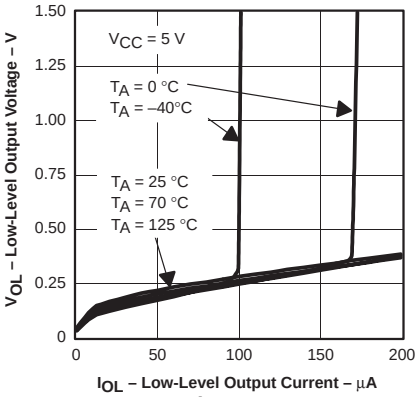


Figure 14

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

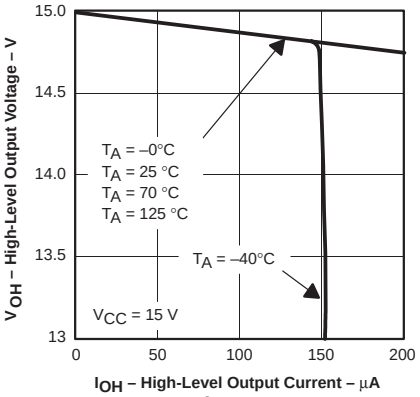


Figure 15

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

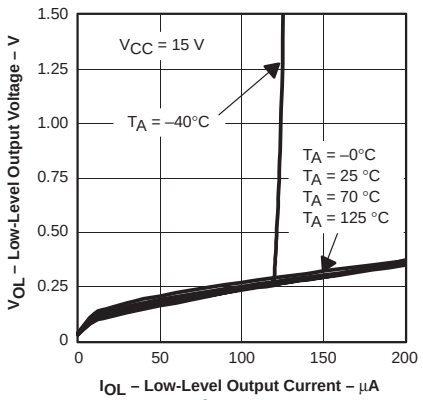


Figure 16

OUTPUT VOLTAGE PEAK-TO-PEAK vs FREQUENCY

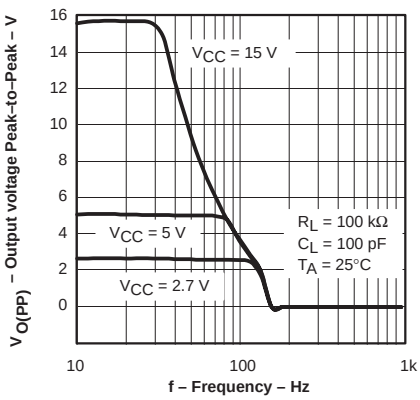


Figure 17

OUTPUT IMPEDANCE vs FREQUENCY

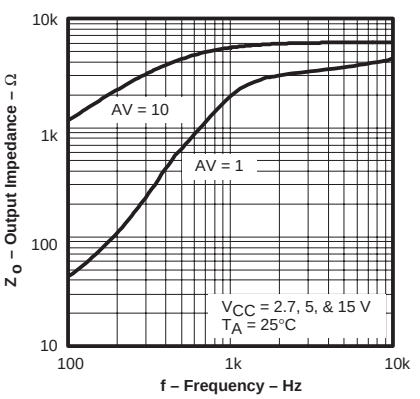


Figure 18

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs SUPPLY VOLTAGE

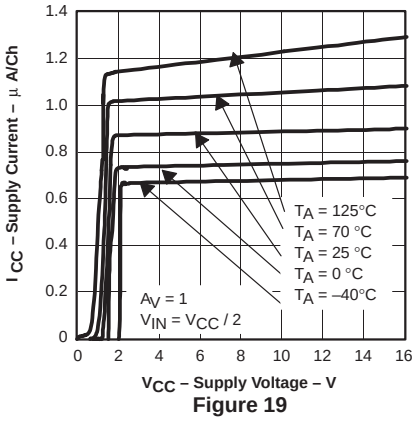


Figure 19

POWER SUPPLY REJECTION RATIO vs FREQUENCY

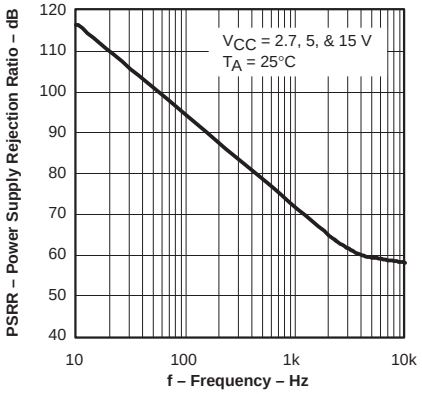


Figure 20

DIFFERENTIAL VOLTAGE GAIN AND PHASE vs FREQUENCY

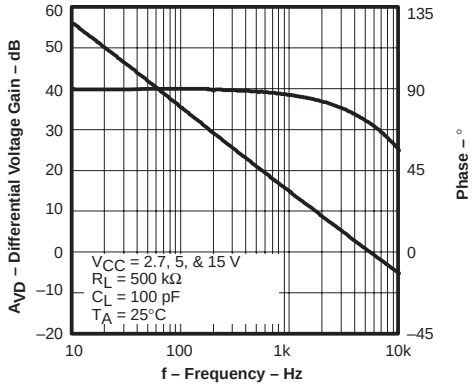


Figure 21

GAIN BANDWIDTH PRODUCT vs SUPPLY VOLTAGE

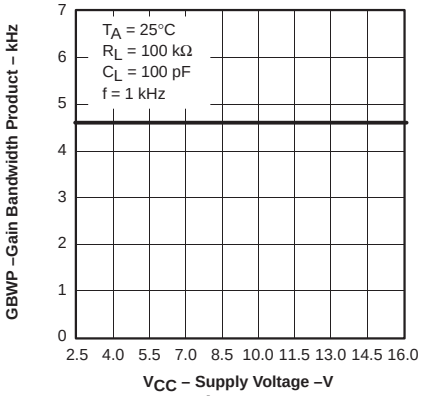


Figure 22

SLEW RATE vs FREE-AIR TEMPERATURE

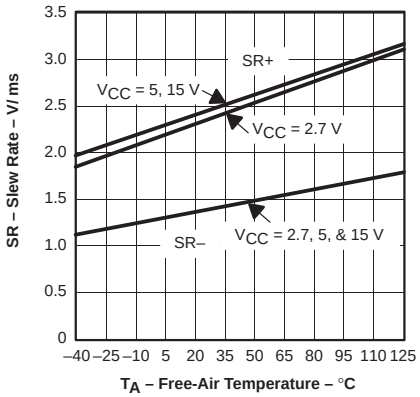


Figure 23

PHASE MARGIN vs CAPACITIVE LOAD

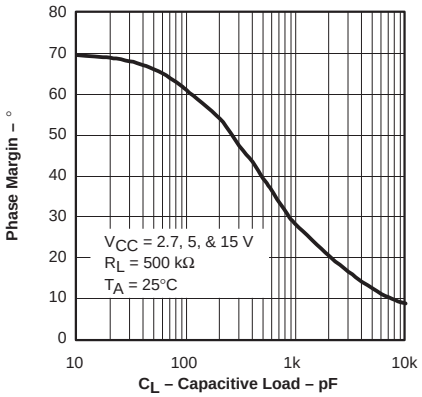


Figure 24

TYPICAL CHARACTERISTICS

GAIN MARGIN vs CAPACITIVE LOAD

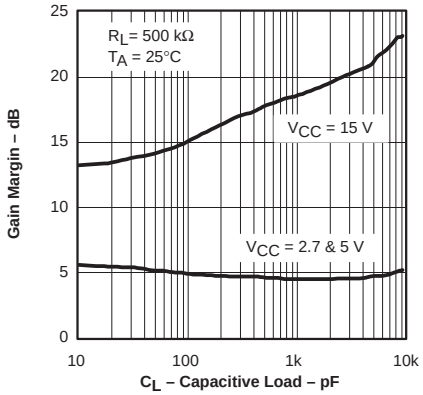


Figure 25

SUPPLY CURRENT vs REVERSE VOLTAGE

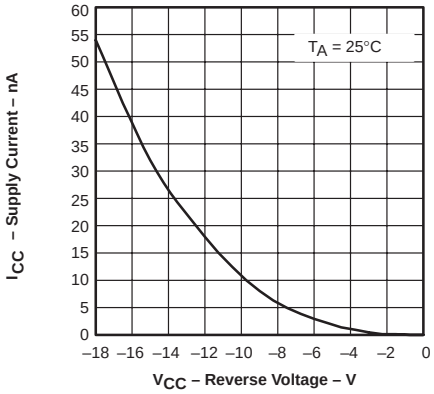


Figure 26

VOLTAGE NOISE OVER A 10 SECOND PERIOD

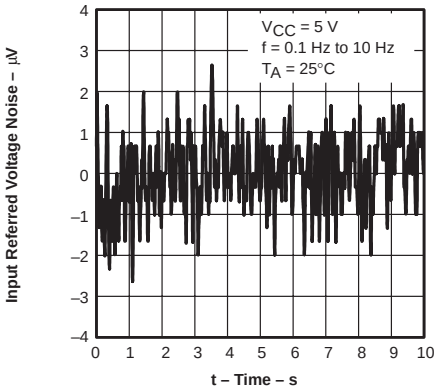


Figure 27

LARGE SIGNAL FOLLOWER PULSE RESPONSE

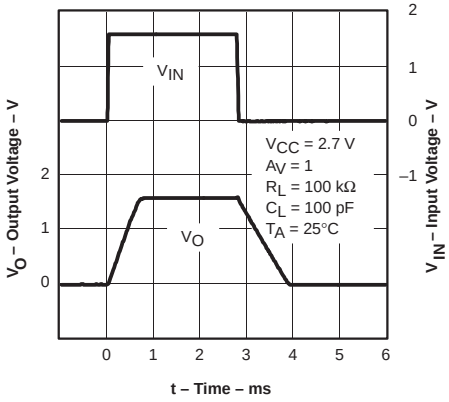


Figure 28

LARGE SIGNAL FOLLOWER PULSE RESPONSE

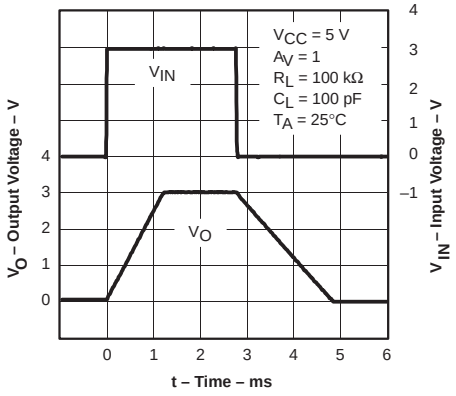


Figure 29

LARGE SIGNAL FOLLOWER PULSE RESPONSE

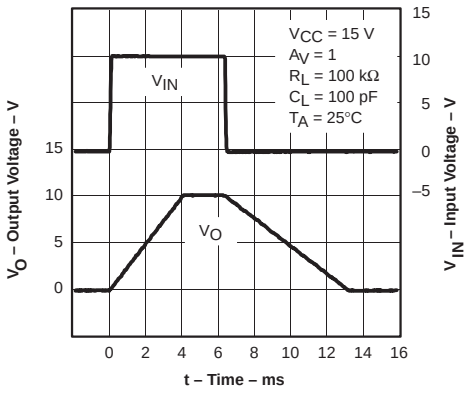


Figure 30

TYPICAL CHARACTERISTICS

SMALL SIGNAL FOLLOWER PULSE RESPONSE

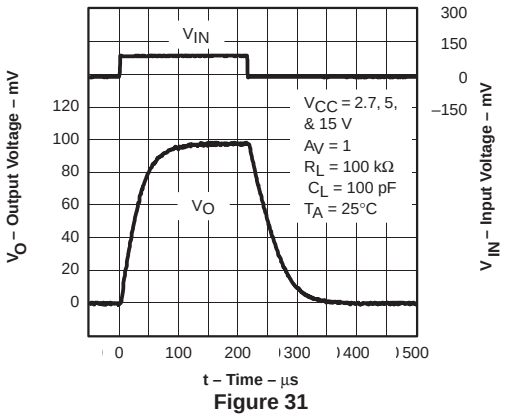


Figure 31

LARGE SIGNAL INVERTING PULSE RESPONSE

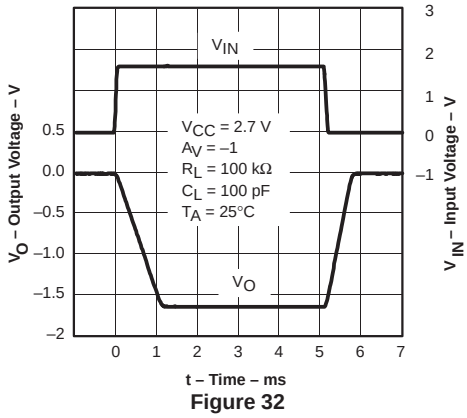


Figure 32

LARGE SIGNAL INVERTING PULSE RESPONSE

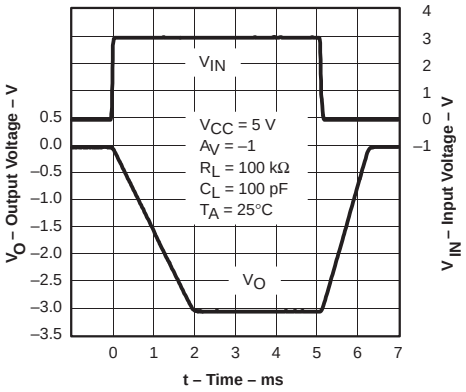


Figure 33

LARGE SIGNAL INVERTING PULSE RESPONSE

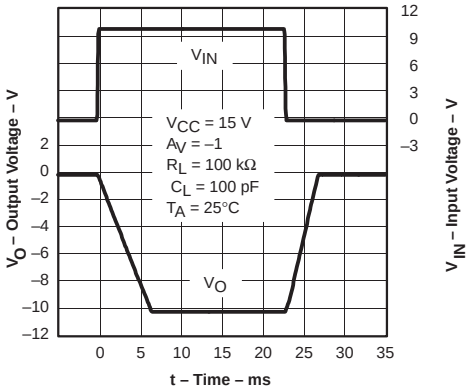


Figure 34

SMALL SIGNAL INVERTING PULSE RESPONSE

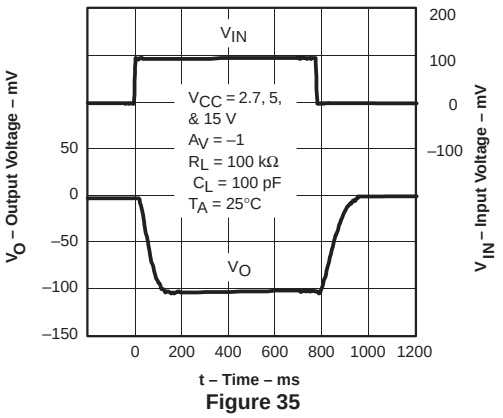


Figure 35

CROSSTALK vs FREQUENCY

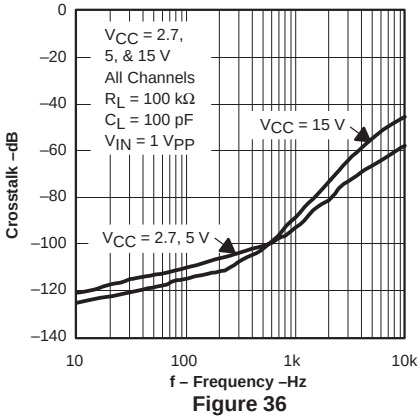


Figure 36

APPLICATION INFORMATION

reverse battery protection

The TLV2401/2/4 are protected against reverse battery voltage up to 18 V. When subjected to reverse battery condition the supply current is typically less than 100 nA at 25°C (inputs grounded and outputs open). This current is determined by the leakage of 6 Schottky diodes and will therefore increase as the ambient temperature increases.

When subjected to reverse battery conditions and negative voltages applied to the inputs or outputs, the input ESD structure will turn on—this current should be limited to less than 10 mA. If the inputs or outputs are referred to ground, rather than midrail, no extra precautions need be taken.

common-mode input range

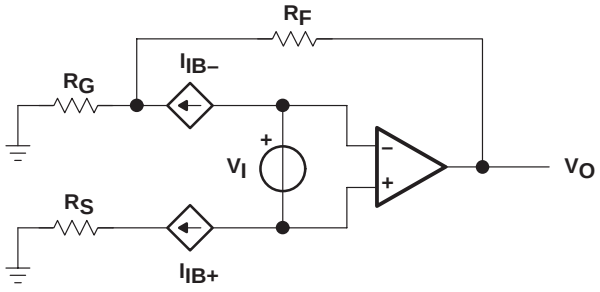
The TLV2401/2/4 has rail-to-rail input and outputs. For common-mode inputs from –0.1 V to V_{CC} – 0.8 V a PNP differential pair will provide the gain.

For inputs between V_{CC} – 0.8 V and V_{CC}, two NPN emitter followers buffering a second PNP differential pair provide the gain. This special combination of NPN/PNP differential pair enables the inputs to be taken 5 V above the rails, because as the inputs go above V_{CC}, the NPNs switch from functioning as transistors to functioning as diodes. This will lead to an increase in input bias current. The second PNP differential pair continues to function normally as the inputs exceed V_{CC}.

The TLV2401/2/4 has a negative common-input range that exceeds ground by 100 mV. If the inputs are taken much below this, reduced open loop gain will be observed with the ultimate possibility of phase inversion.

offset voltage

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:



$$V_{OO} = V_{IO}\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB+}\ R_S\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB-}\ R_F$$

Figure 37. Output Offset Voltage Model

APPLICATION INFORMATION

general configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifier (see Figure 38).

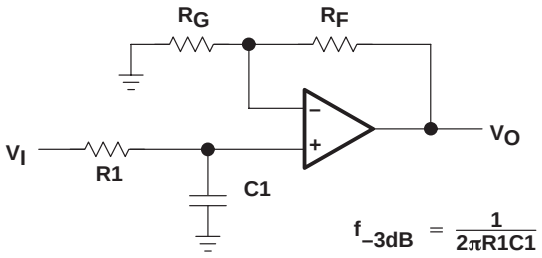


Figure 38. Single-Pole Low-Pass Filter

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task. For best results, the amplifier should have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.

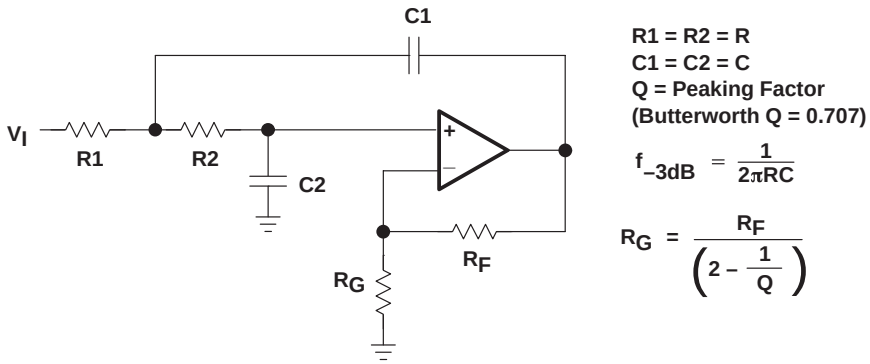


Figure 39. 2-Pole Low-Pass Sallen-Key Filter

APPLICATION INFORMATION

circuit layout considerations

To achieve the levels of high performance of the TLV240x, follow proper printed-circuit board design techniques. A general set of guidelines is given in the following.

- Ground planes – It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling – Use a 6.8-μF tantalum capacitor in parallel with a 0.1-μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-μF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-μF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets – Sockets can be used but are not recommended. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- Short trace runs/compact part placements – Optimum high performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This will help to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components – Using surface-mount passive components is recommended for high performance amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

APPLICATION INFORMATION

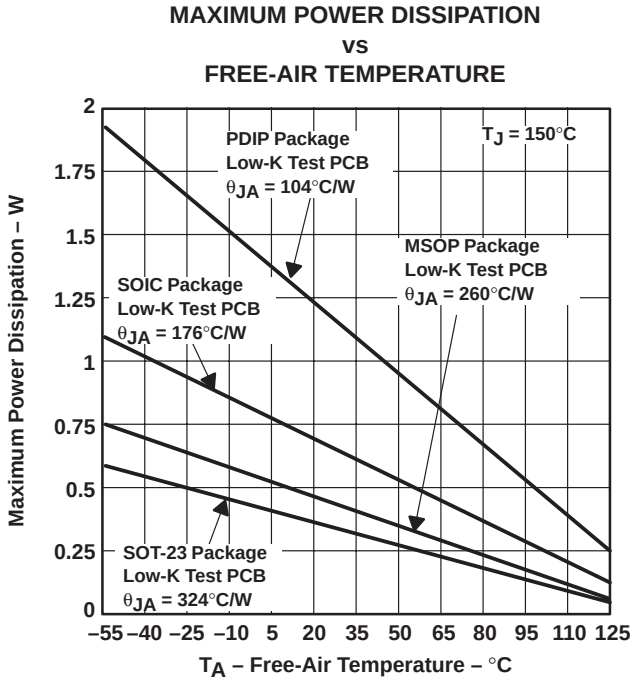
general power dissipation considerations

For a given θ_{JA}, the maximum power dissipation is shown in Figure 40 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

P_D = Maximum power dissipation of THS240x IC (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Free-ambient air temperature (°C)
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} = Thermal coefficient from junction to case
θ_{CA} = Thermal coefficient from case to ambient air (°C/W)



NOTE A: Results are with no air flow and using JEDEC Standard Low-K test PCB.

Figure 40. Maximum Power Dissipation vs Free-Air Temperature

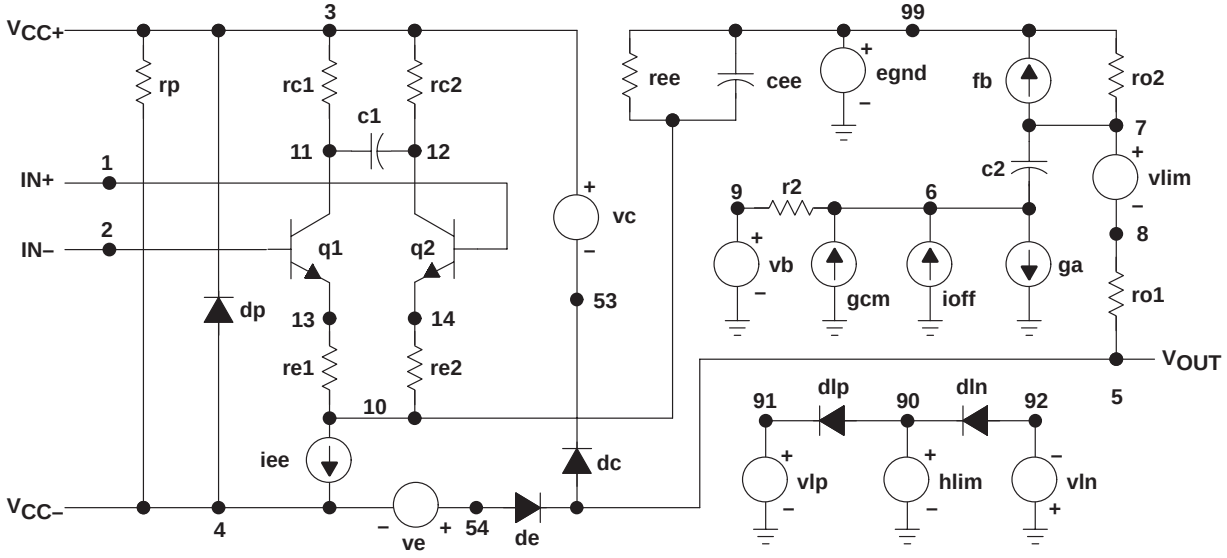
APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*™ Release 8, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 2) and subcircuit in Figure 41 are generated using the TLV240x typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 2: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits,* SC-9, 353 (1974).




```
.subckt 240X_5V–X  1 2 3 4 5
*
c1     11   12   9.8944E–12
c2     6    7    30.000E–12
cee    10   99   8.8738E–12
dc     5    53   dy
de     54   5    dy
dlp    90   91   dx
dln    92   90   dx
dp     4    3    dx
egnd   99   0    poly(2) (3,0) (4,0) 0 .5 .5
fb     7    99   poly(5) vb vc ve vlp vln 0 61.404E6 –1E3 1E3 61E6 –61E6
ga     6    0    11 12 1.0216E–6
gcm    0    6    10 99 10.216E–12
iee    10   4    dc 54.540E–9
ioff   0    6    dc 5e–12
hlim   90   0    vlim 1K
q1     11   2    13 qx1
q2     12   1    14 qx2
r2     6    9    100.00E3
rc1    3    11   978.81E3
rc2    3    12   978.81E3
re1    13   10   30.364E3
re2    14   10   30.364E3
ree    10   99   3.6670E9
ro1    8    5    10
ro2    7    99   10
rp     3    4    1.4183E6
vb     9    0    dc  0
vc     3    53   dc  .88315
ve     54   4    dc  .88315
vlim   7    8    dc  0
vlp    91   0    dc  540
vln    0    92   dc  540
.model dx   D(Is=800.00E–18)
.model dy   D(Is=800.00E–18 Rs=1m Cjo=10p)
.model qx1  NPN(Is=800.00E–18 Bf=27.270E21)
.model qx2  NPN(Is=800.0000E–18 Bf=27.270E21)
.ends
```

Figure 41. Boyle Macromodels and Subcircuit

PSpice and *Parts* are trademarks of MicroSim Corporation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2401CD	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	0 to 70	2401C	
TLV2401CDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	VAWC	Samples
TLV2401CDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	VAWC	Samples
TLV2401CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	2401C	Samples
TLV2401ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2401I	Samples
TLV2401IDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	VAWI	Samples
TLV2401IDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VAWI	Samples
TLV2401IDBVTG4	ACTIVE	SOT-23	DBV	5	250	TBD	Call TI	Call TI	-40 to 125		Samples
TLV2401IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2401I	Samples
TLV2401IP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	TLV2401I	Samples
TLV2402CD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	2402C	Samples
TLV2402CDGK	ACTIVE	VSSOP	DGK	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	AIX	Samples
TLV2402CDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	AIX	Samples
TLV2402CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	2402C	Samples
TLV2402ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2402I	Samples
TLV2402IDGK	ACTIVE	VSSOP	DGK	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AIY	Samples
TLV2402IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AIY	Samples
TLV2402IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2402I	Samples
TLV2402IP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	TLV2402I	Samples
TLV2404CD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLV2404C	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2404CPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	2404C	Samples
TLV2404CPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	2404C	Samples
TLV2404ID	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2404I	Samples
TLV2404IDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2404I	Samples
TLV2404IN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	TLV2404IN	Samples
TLV2404IPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2404I	Samples
TLV2404IPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2404I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TLV2401, TLV2402 :

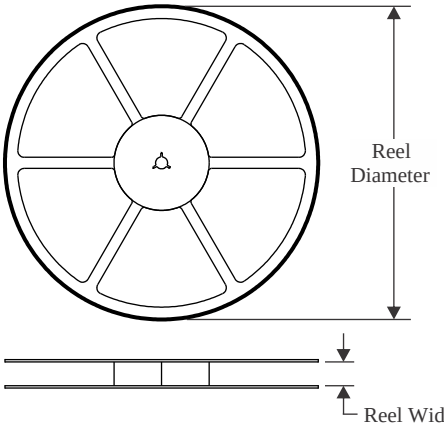
- Automotive : TLV2401-Q1, TLV2402-Q1

NOTE: Qualified Version Definitions:

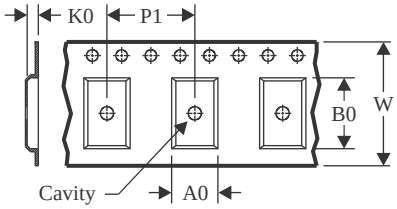
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

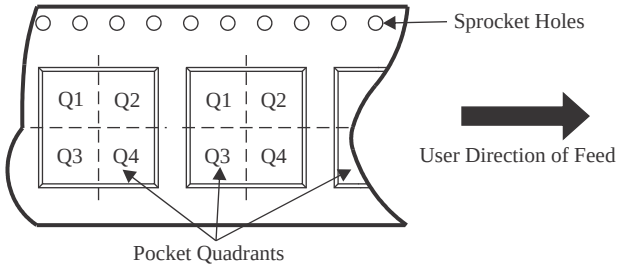


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

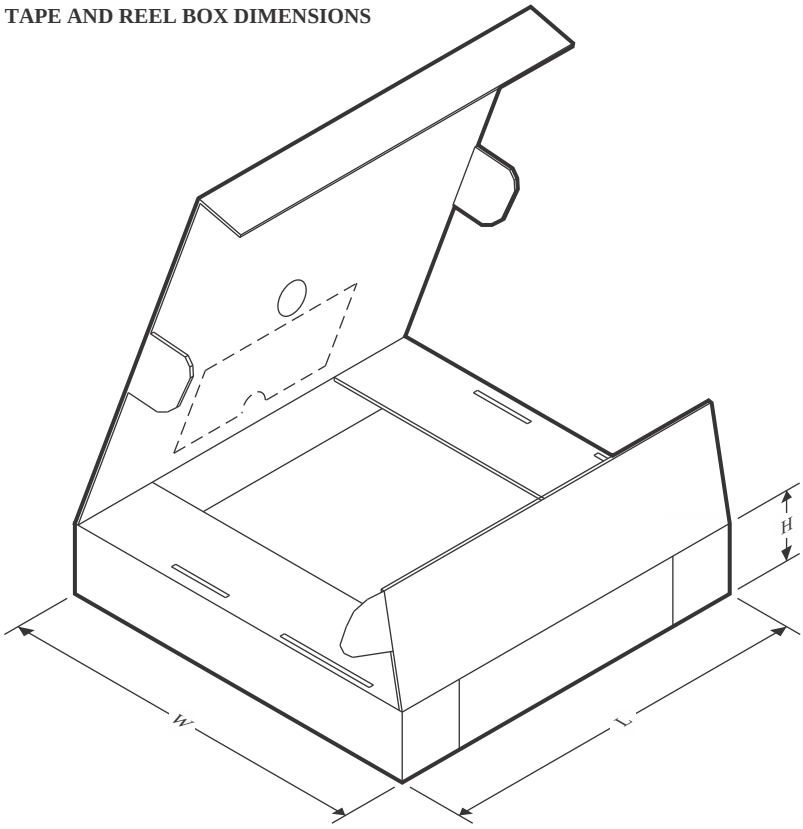
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2401CDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV2401CDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV2401CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2401IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV2401IDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV2401IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2402CDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2402CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2402IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2402IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2404CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV2404IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV2404IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

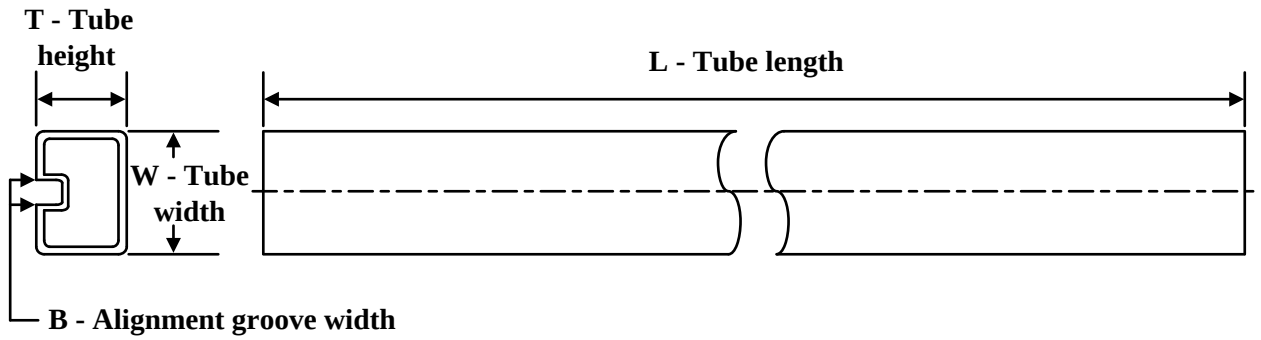
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

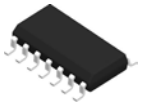
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2401CDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV2401CDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TLV2401CDR	SOIC	D	8	2500	353.0	353.0	32.0
TLV2401IDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV2401IDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TLV2401IDR	SOIC	D	8	2500	353.0	353.0	32.0
TLV2402CDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
TLV2402CDR	SOIC	D	8	2500	353.0	353.0	32.0
TLV2402IDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
TLV2402IDR	SOIC	D	8	2500	353.0	353.0	32.0
TLV2404CPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TLV2404IDR	SOIC	D	14	2500	350.0	350.0	43.0
TLV2404IPWR	TSSOP	PW	14	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLV2401ID	D	SOIC	8	75	505.46	6.76	3810	4
TLV2401ID	D	SOIC	8	75	507	8	3940	4.32
TLV2401IP	P	PDIP	8	50	506	13.97	11230	4.32
TLV2402CD	D	SOIC	8	75	507	8	3940	4.32
TLV2402CD	D	SOIC	8	75	505.46	6.76	3810	4
TLV2402ID	D	SOIC	8	75	507	8	3940	4.32
TLV2402ID	D	SOIC	8	75	505.46	6.76	3810	4
TLV2402IP	P	PDIP	8	50	506	13.97	11230	4.32
TLV2404CD	D	SOIC	14	50	505.46	6.76	3810	4
TLV2404CPW	PW	TSSOP	14	90	530	10.2	3600	3.5
TLV2404ID	D	SOIC	14	50	505.46	6.76	3810	4
TLV2404IN	N	PDIP	14	25	506	13.97	11230	4.32
TLV2404IPW	PW	TSSOP	14	90	530	10.2	3600	3.5

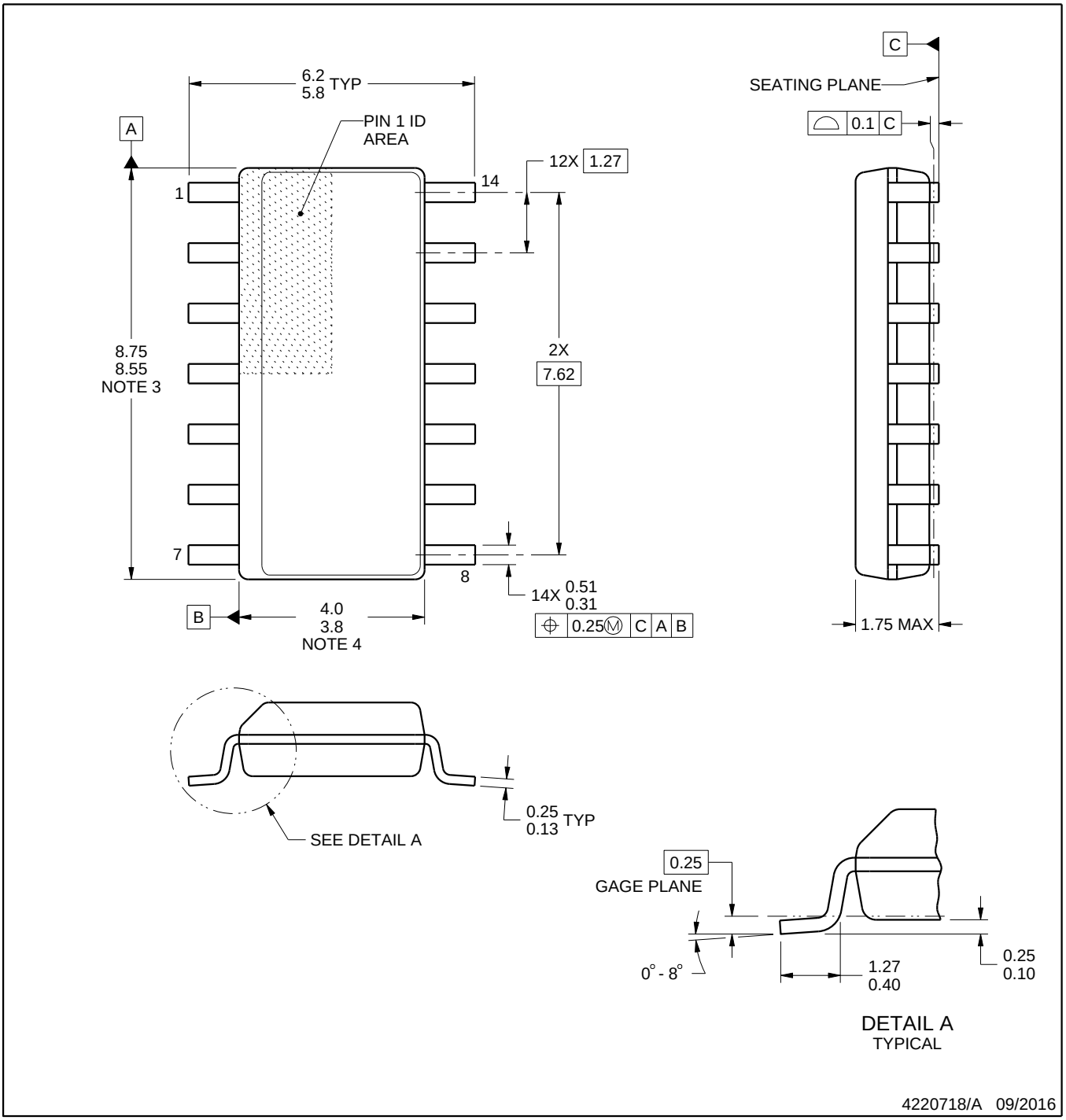


PACKAGE OUTLINE

D0014A

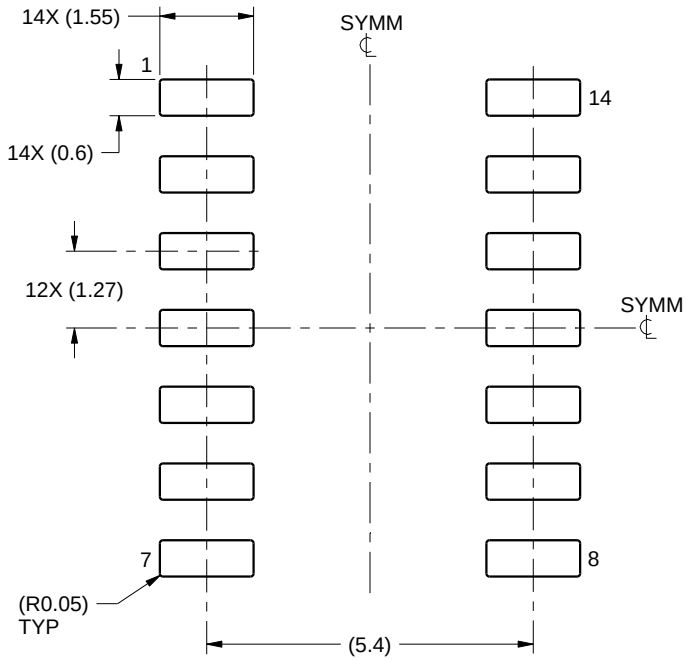
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

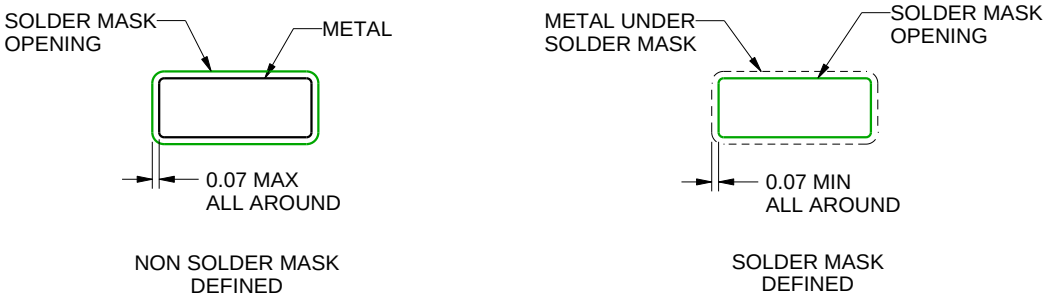


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

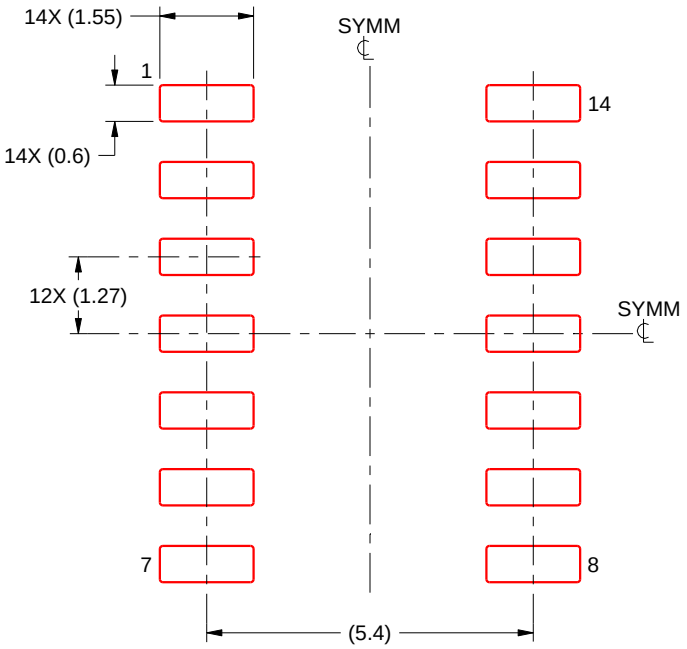
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

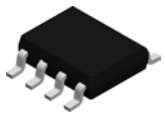


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

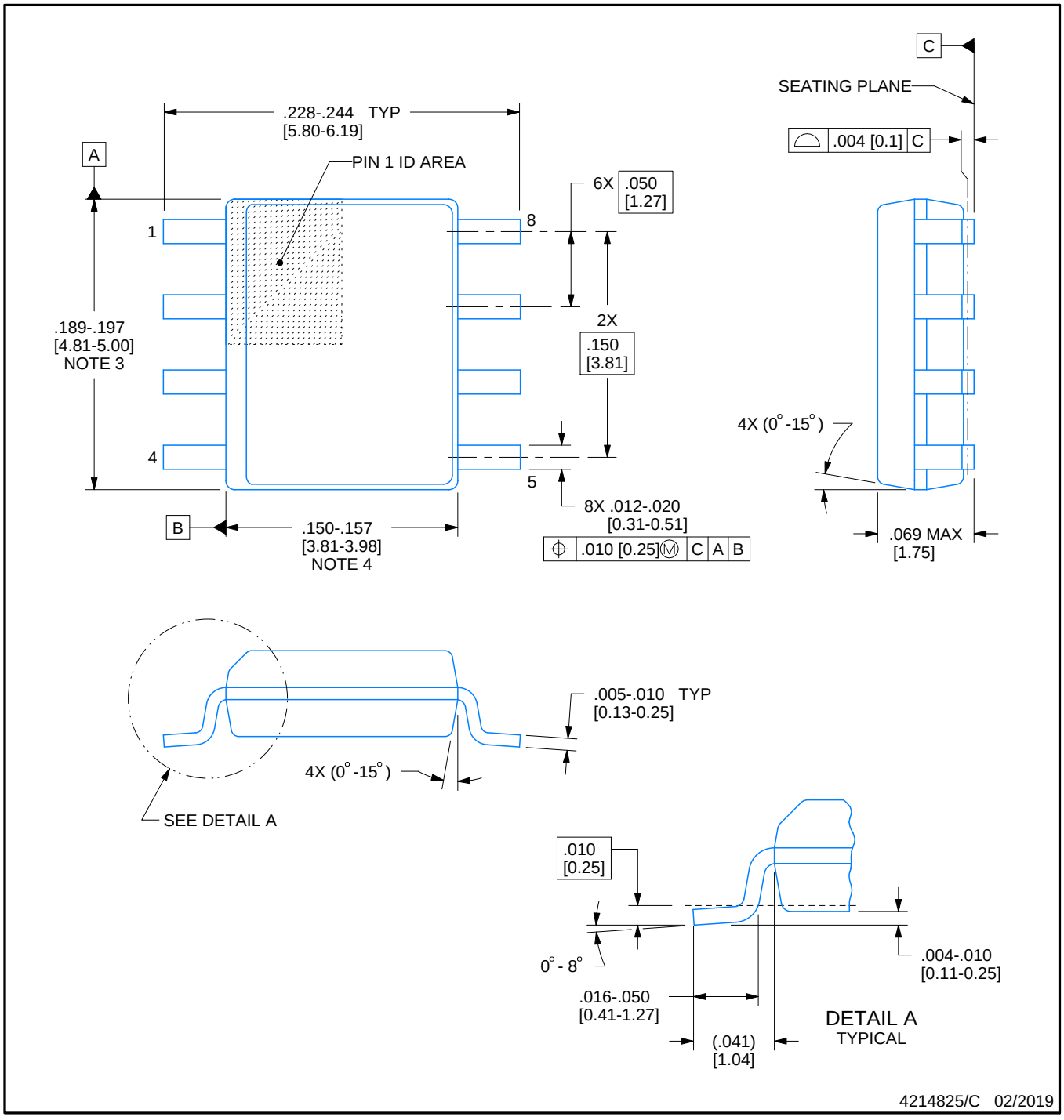


PACKAGE OUTLINE

D0008A

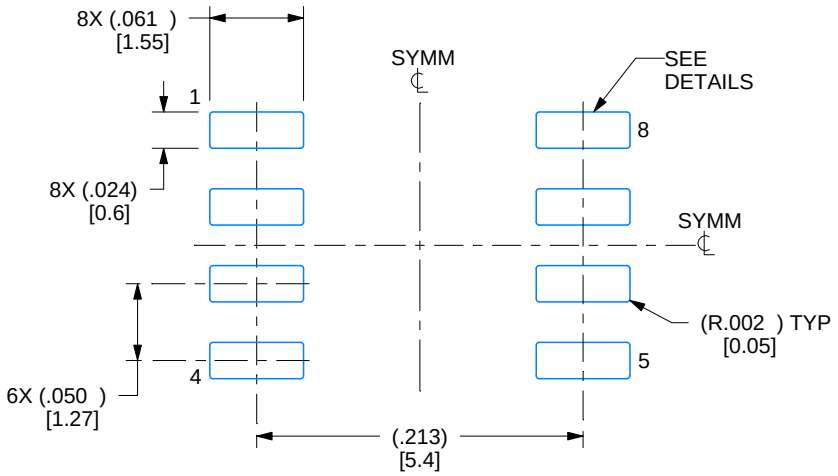
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

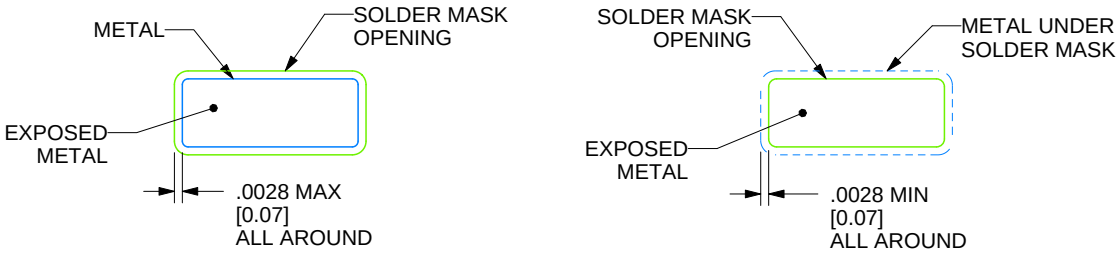


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

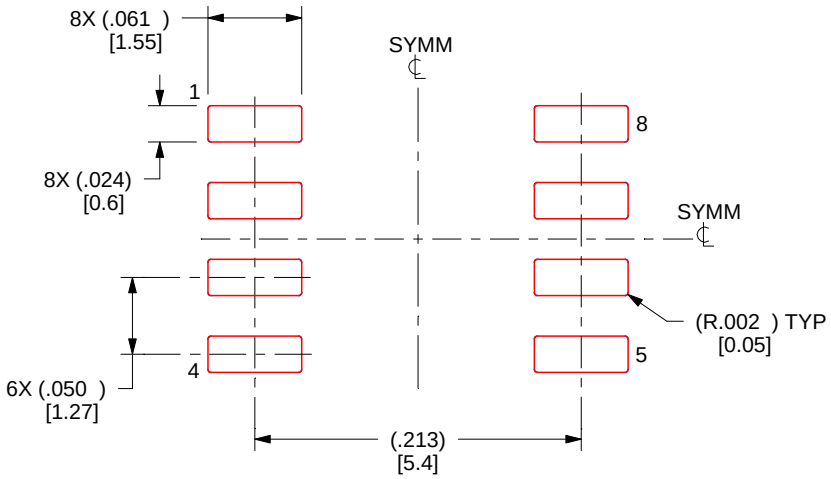
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



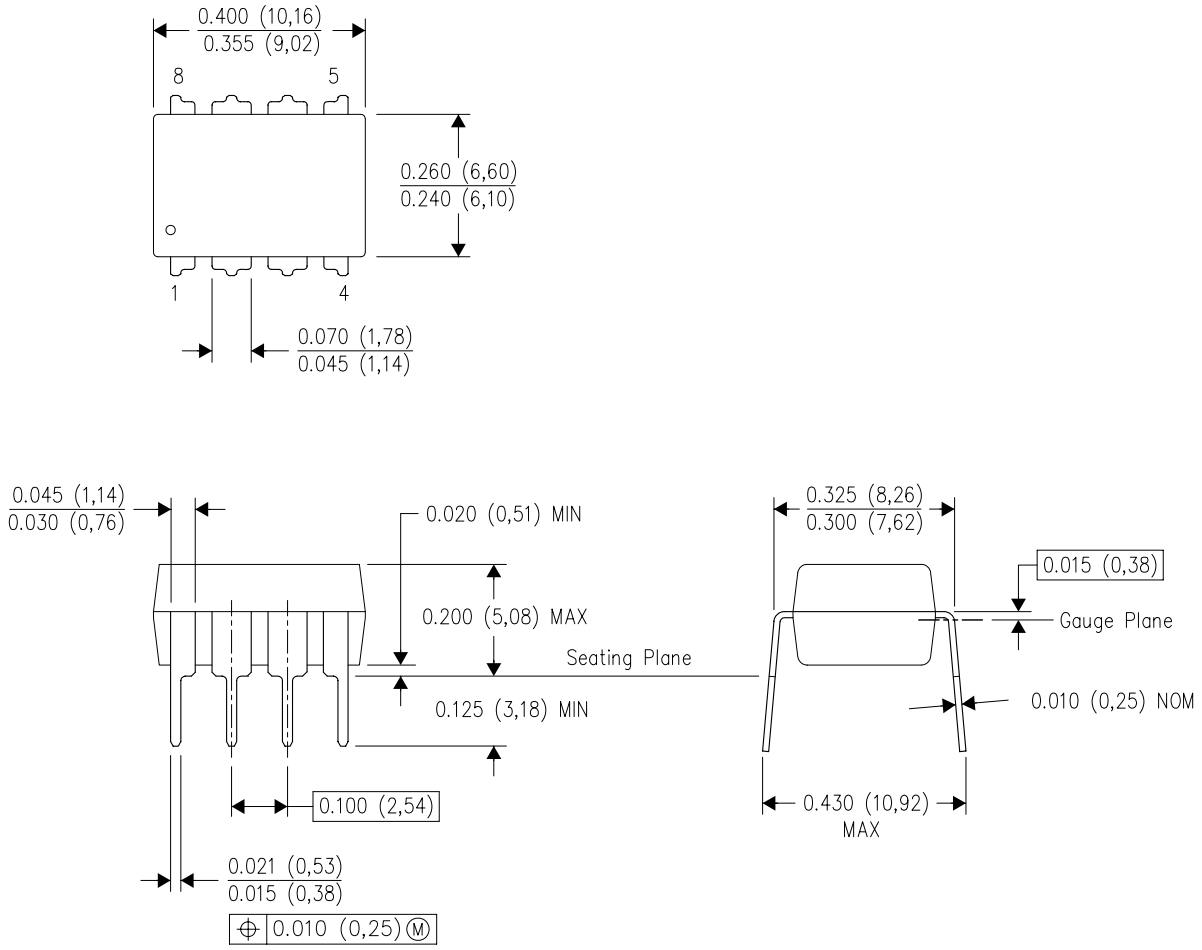
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE

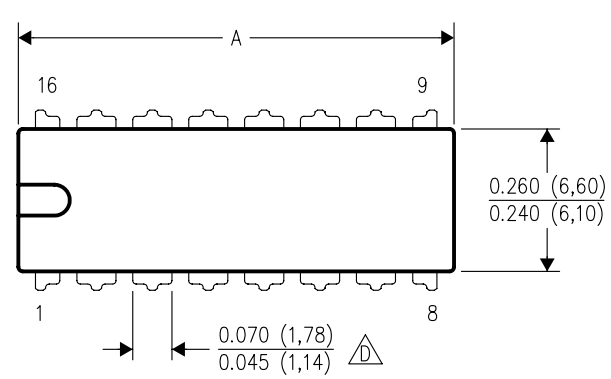


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

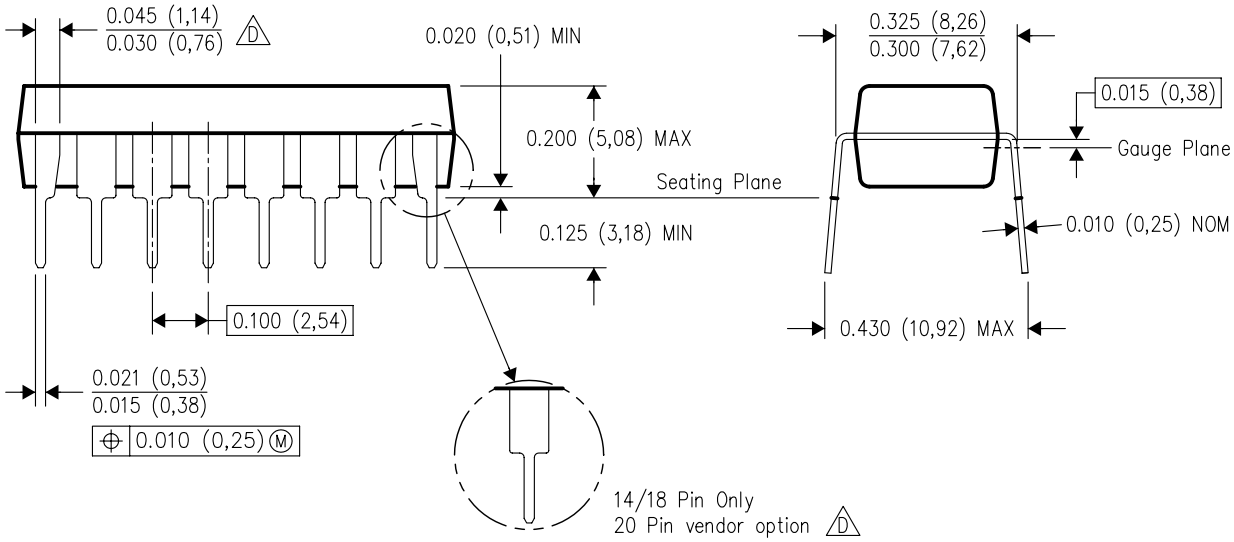
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

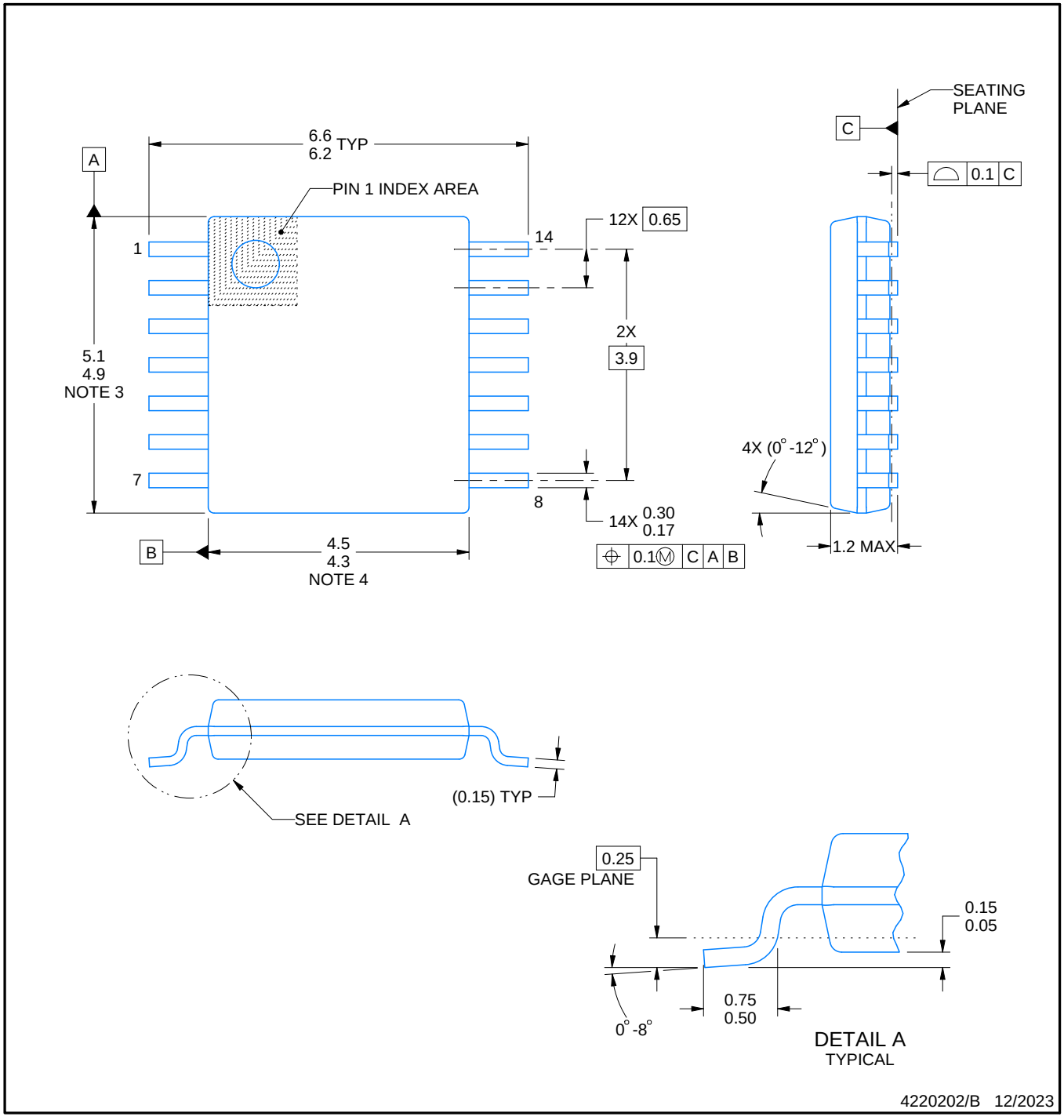
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

PACKAGE OUTLINE

PW0014A

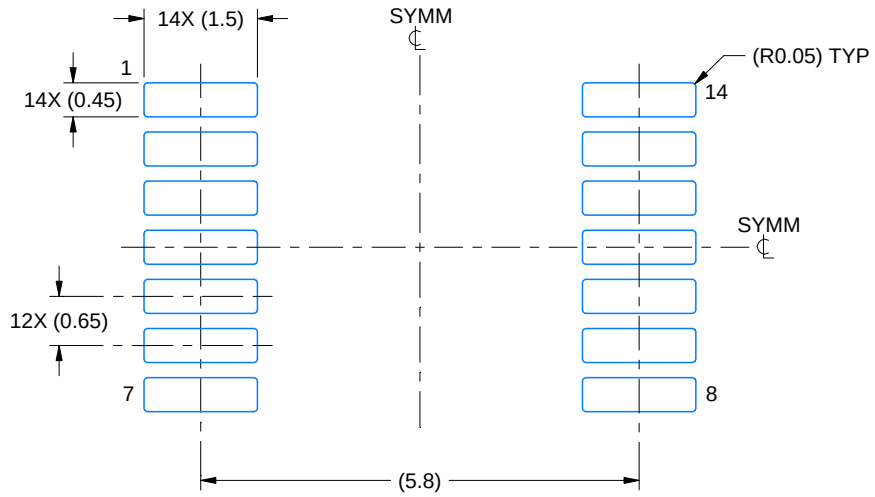
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

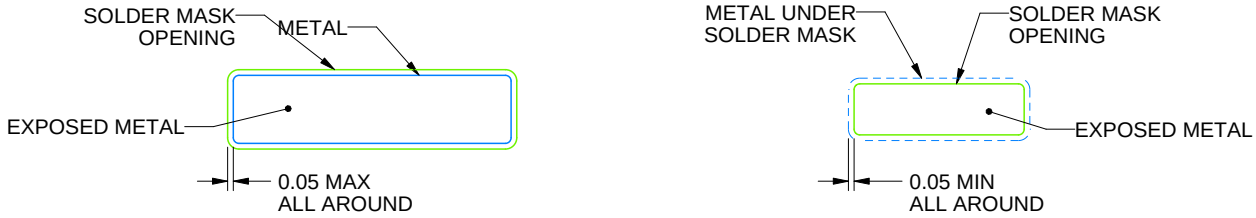


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

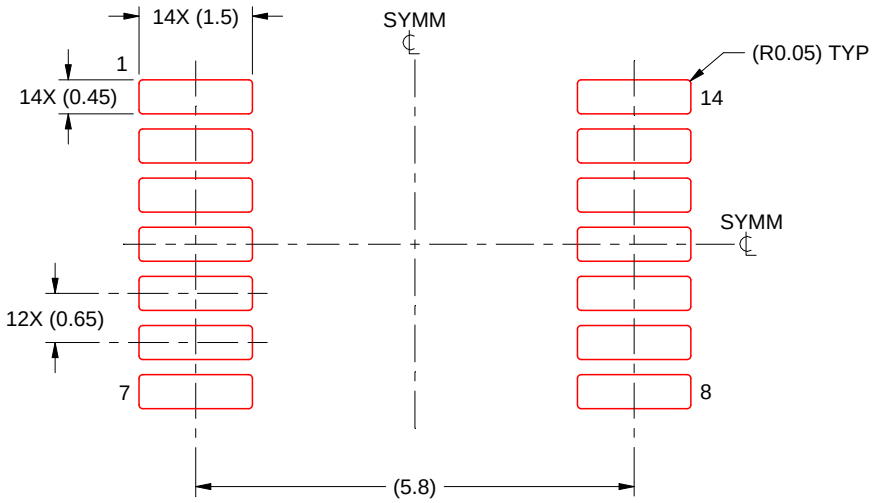


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

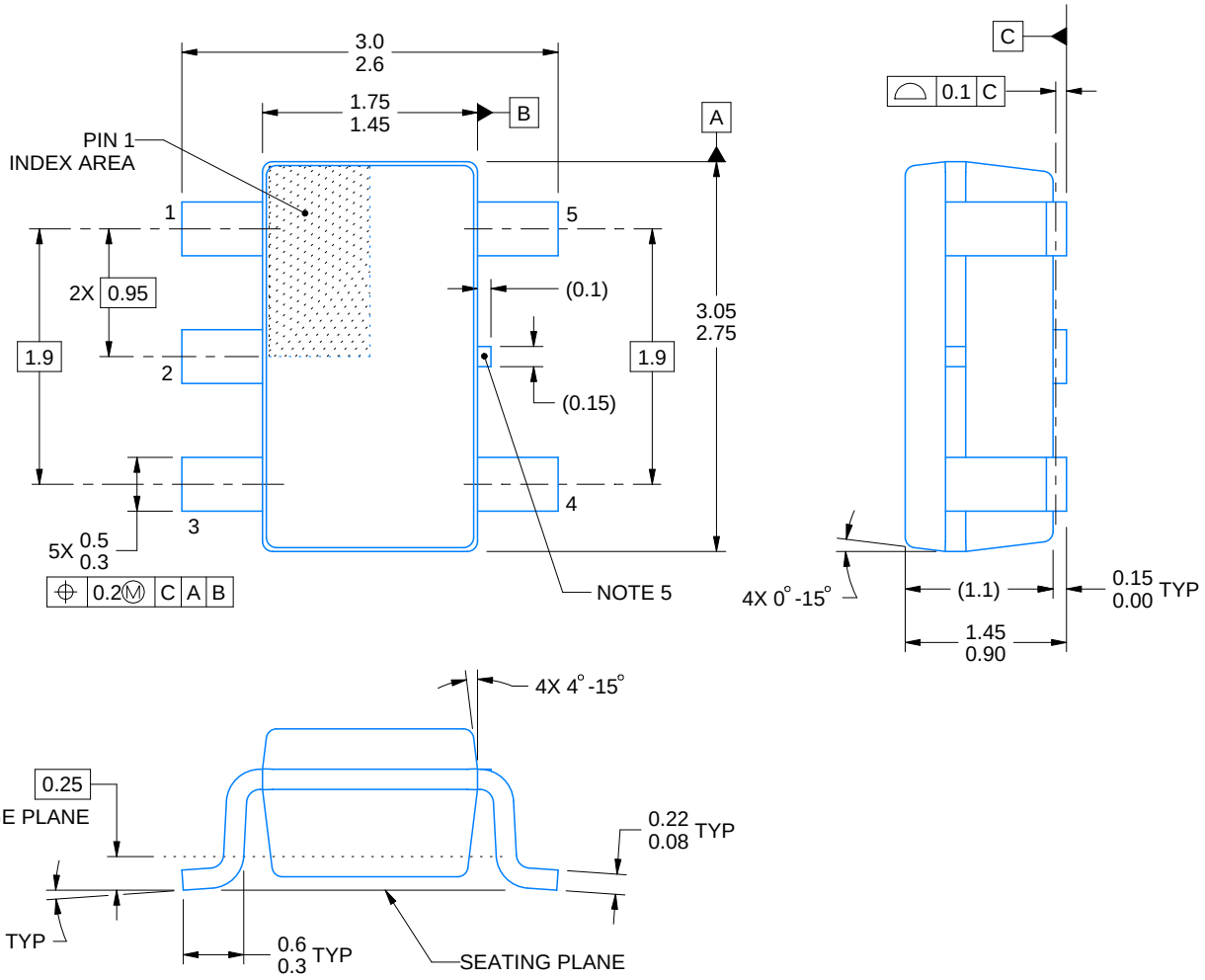
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

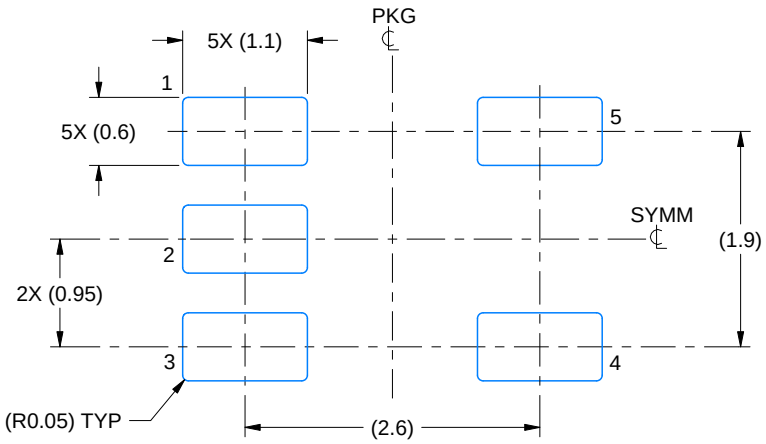
SMALL OUTLINE TRANSISTOR



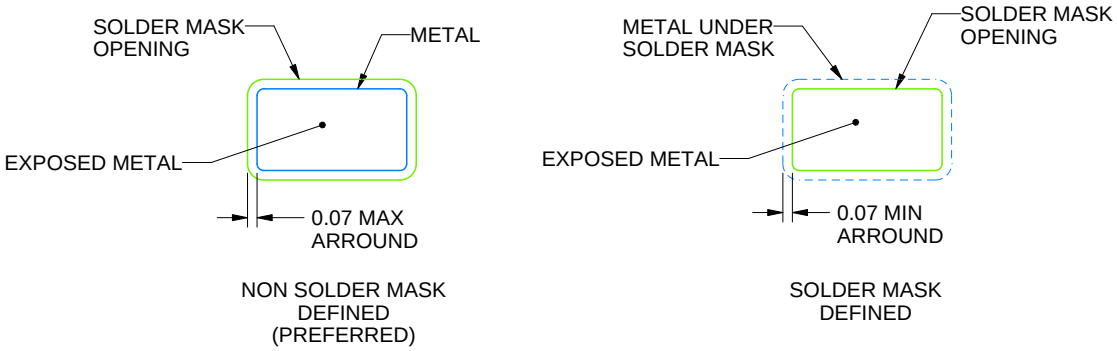
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

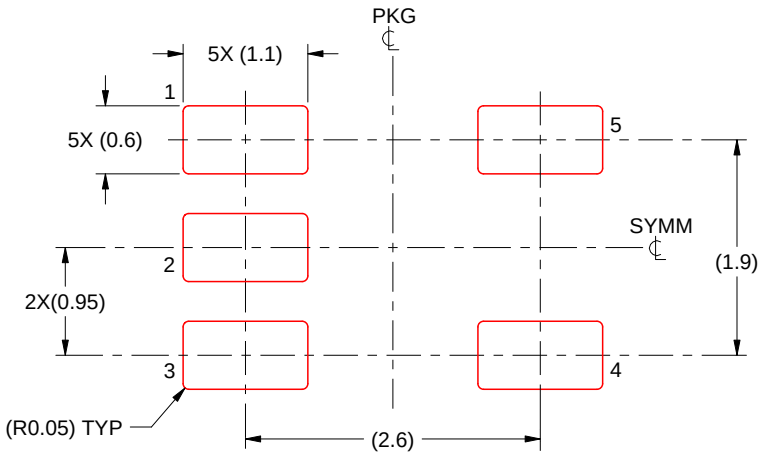


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

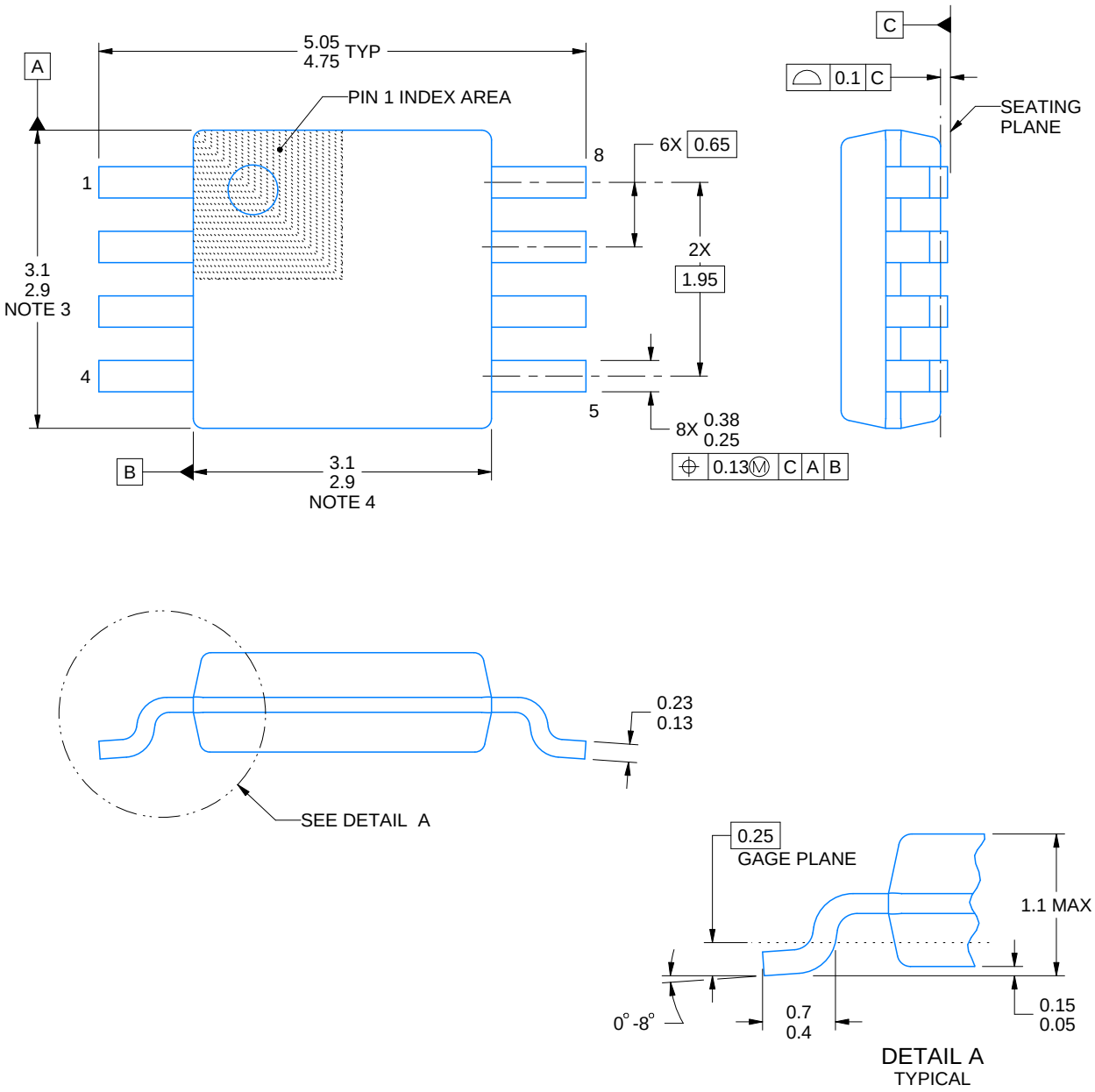
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

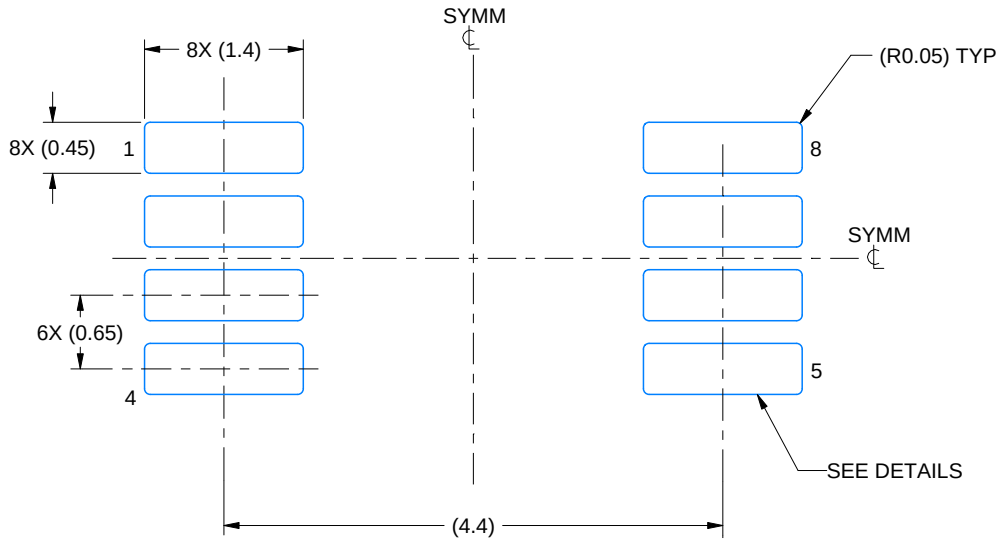
SMALL OUTLINE PACKAGE



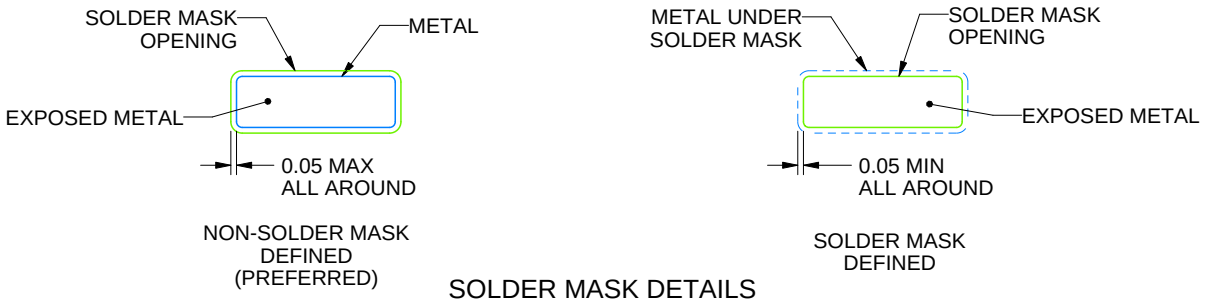
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

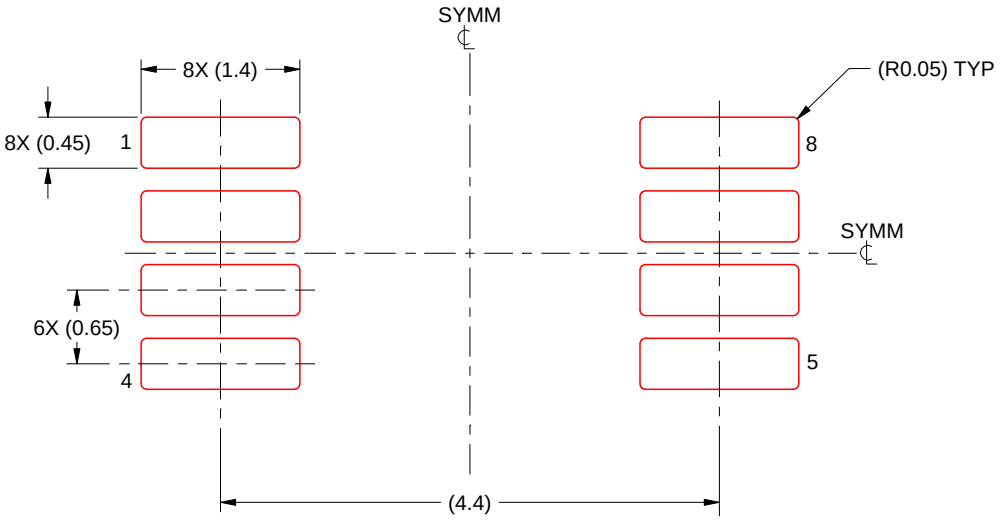


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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