Triple Differential Driver With Sync-On-Common-Mode

Data Sheet

AD8134

FEATURES

- Triple high speed differential driver
  - 225 MHz, −3 dB large signal bandwidth
  - 450 MHz, −3 dB small signal bandwidth
  - Easily drives 1.4 V p-p video signal into doubly terminated 100 Ω UTP cable
  - 1600 V/µs slew rate
  - Fixed internal gain of 2
- Internal common-mode feedback network
  - Output balance error −60 dB @ 50 MHz
- On-chip sync-on-common-mode circuitry
- Output pull-down feature for line isolation
- Differential input and output
- Differential-to-differential or single-ended-to-differential operation
- High isolation between amplifiers: 80 dB @ 10 MHz
- Low distortion: 64 dB SFDR @ 10 MHz on 5 V supply, $R_{L, dm}$ = 200 Ω
- Low offset: 3 mV typical output-referred on 5 V supply
- Low power: 26.5 mA @ 5 V for three drivers and sync circuitry
- Wide supply voltage range: +5 V to ±5 V
- Available in space-saving packaging: 4 mm × 4 mm LFCSP

APPLICATIONS

- Keyboard-video-mouse (KVM) networking

GENERAL DESCRIPTION

The AD8134 is a major advancement beyond using discrete op amps for driving differential RGB signals over twisted pair cable. The AD8134 is a triple, low cost differential or single-ended input to differential output driver, and each amplifier has a fixed gain of 2 to compensate for the attenuation of the line termination resistors. The AD8134 is specifically designed for RGB signals but can be used for any type of analog signals or high speed data transmission. The AD8134 is capable of driving either Category 5 (Cat-5) unshielded twisted pair (UTP) cable or differential printed circuit board transmission lines with minimal signal degradation.

A unique feature that allows the user to transmit balanced horizontal and vertical video sync signals over the three common-mode channels with minimal electromagnetic interference (EMI) radiation is included on-chip.

The outputs of the AD8134 can be set to a low voltage state that allows easy differential multiplexing of multiple drivers on the same twisted pair cable, when used with external series diodes.

FUNCTIONAL BLOCK DIAGRAM

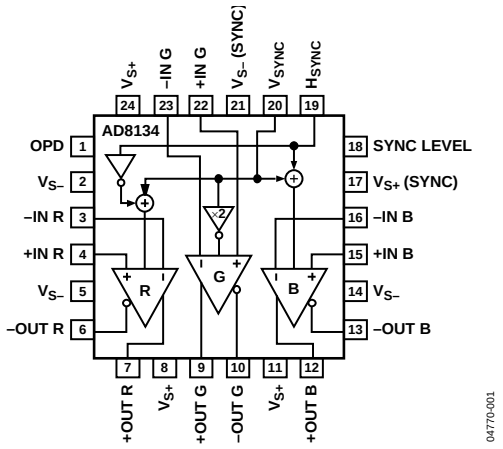


Figure 1.

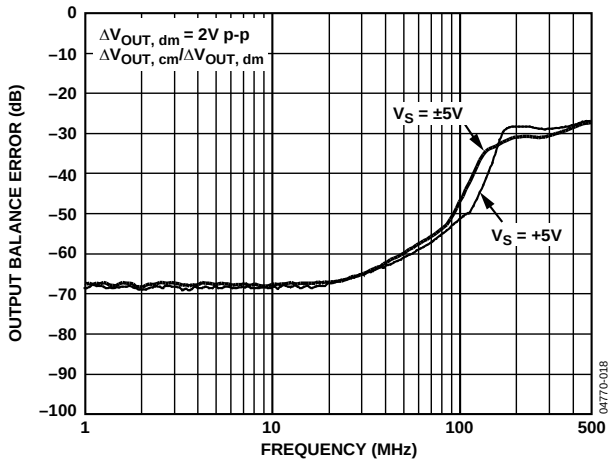


Figure 2. Output Balance vs. Frequency

The AD8134 driver is a natural complement to the AD8143, AD8129, and AD8130 differential receivers.

Manufactured on the Analog Devices next generation XFCB bipolar process, the AD8134 has a large signal bandwidth of 225 MHz and a slew rate of 1600 V/µs. The AD8134 has an internal common-mode feedback feature that provides output gain and phase matching that is balanced to −60 dB at 50 MHz, suppressing harmonics and reducing radiated EMI.

The AD8134 is available in a 24-lead LFCSP and can operate over the −40°C to +85°C extended industrial temperature range.

Rev. B
Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support
www.analog.com

TABLE OF CONTENTS

REVISION HISTORY

3/16—Rev. A to Rev. B

Changed CP-24 to CP-24-10 ... Universal
Changes to Figure 4 and Table 5 ... 6
Updated Outline Dimensions ... 19
Changes to Ordering Guide ... 19

10/05—Rev. Sp0 to Rev. A

Changes to Features and General Description ... 1
Changes to Figure 32 ... 14
Changes to Figure 33 ... 15
Changes to Figure 34 ... 17
Added Level-Shifting Sync Pulses on ±5 V Supplies Section ... 17
Changes to Ordering Guide ... 19

7/04—Revision Sp0: Initial Version

SPECIFICATIONS

V_S = ±5 V, H_{SYNC} and V_{SYNC} = V_{S-}, $R_{L, dm}$ = 200 Ω @ 25°C, unless otherwise noted. T_{MIN} to T_{MAX} = −40°C to +85°C.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DIFFERENTIAL INPUT PERFORMANCE					
DYNAMIC PERFORMANCE					
−3 dB Small Signal Bandwidth	V_O = 0.2 V p-p		450		MHz
−3 dB Large Signal Bandwidth	V_O = 2 V p-p		225		MHz
Bandwidth for 0.1 dB Flatness	V_O = 0.2 V p-p		60		MHz
	V_O = 2 V p-p		55		MHz
Slew Rate	V_O = 2 V p-p, 25% to 75%		1600		V/µs
Settling Time to 0.1%	V_O = 2 V step		15		ns
Isolation Between Amplifiers	f = 10 MHz, between Amplifier R and Amplifier G		80		dB
DIFFERENTIAL INPUT CHARACTERISTICS					
Input Common-Mode Voltage Range			−5 to +5		V
Input Resistance	Differential		1.5		kΩ
	Single-ended input		1.13		kΩ
Input Capacitance	Differential		1		pF
DC CMRR	$\Delta V_{OUT, dm}/\Delta V_{IN, cm}$, $\Delta V_{IN, cm}$ = ±1 V		−48		dB
DIFFERENTIAL OUTPUT CHARACTERISTICS					
Differential Signal Gain	$\Delta V_{OUT, dm}/\Delta V_{IN, dm}$, $\Delta V_{IN, dm}$ = ±1 V	1.920	1.955	2.000	V/V
Output Voltage Swing	Each single-ended output	V_{S-} + 1.9		V_{S+} − 1.6	V
Output Offset Voltage		−24	+4	+24	mV
Output Offset Drift	T_{MIN} to T_{MAX}		±30		µV/°C
Output Balance Error	f = 50 MHz		−60		dB
	DC		−70	−54	dB
Output Voltage Noise (RTO)	f = 1 MHz		25		nV/√Hz
Output Short-Circuit Current			90		mA
COMMON-MODE SYNC PERFORMANCE					
SYNC DYNAMIC PERFORMANCE					
Slew Rate	$V_{OUT, cm}$ = −1 V to +1 V; 25% to 75%		1000		V/µs
H_{SYNC} AND V_{SYNC} INPUTS					
Input Low Voltage			V_{S-} to −2.75		V
Input High Voltage			−2.25 to V_{S+}		V
SYNC LEVEL INPUT					
Input Voltage Range	For linear operation				V
Setting to Achieve 0.5 V Pulse Levels			V_{S-} + 0.5		V
Gain to Red Common-Mode Output	$\Delta V_{O, cm}/\Delta V_{SYNC\ LEVEL}$	0.95	1.02	1.07	V/V
Gain to Green Common-Mode Output	$\Delta V_{O, cm}/\Delta V_{SYNC\ LEVEL}$	1.91	2.04	2.14	V/V
Gain to Blue Common-Mode Output	$\Delta V_{O, cm}/\Delta V_{SYNC\ LEVEL}$	0.95	1.02	1.07	V/V
POWER SUPPLY					
Operating Range		+4.5		±6	V
Quiescent Current			31	33	mA
PSRR	$\Delta V_{OUT, dm}/\Delta V_S$; ΔV_S = ±1V		−54	−48	dB
OUTPUT PULL-DOWN PERFORMANCE					
OPD Input Low Voltage			V_{S-} to V_{S+} − 4.15		V
OPD Input High Voltage			V_{S+} − 3.15 to V_{S+}		V
OPD Input Bias Current			67	90	µA
OPD Assert Time			100		ns
OPD De-Assert Time			100		ns
Output Voltage When OPD Asserted	Each output, OPD input @ V_S+		V_{S-} + 0.86	V_{S-} + 0.90	V

V_{S+} = 5 V, V_{S-} = 0 V, H_{SYNC} and V_{SYNC} = V_{S-}, $R_{L, dm}$ = 200 Ω @ 25°C, unless otherwise noted. T_{MIN} to T_{MAX} = −40°C to +85°C.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
DIFFERENTIAL INPUT PERFORMANCE					
DYNAMIC PERFORMANCE					
−3 dB Small Signal Bandwidth	V_O = 0.2 V p-p		400		MHz
−3 dB Large Signal Bandwidth	V_O = 2 V p-p		200		MHz
Bandwidth for 0.1 dB Flatness	V_O = 0.2 V p-p		50		MHz
Slew Rate	V_O = 2 V p-p, 25% to 75%		1400		V/µs
Settling Time to 0.1%	V_O = 2 V step		14		ns
Isolation Between Amplifiers	f = 10 MHz, between Amplifier R and Amplifier G		75		dB
DIFFERENTIAL INPUT CHARACTERISTICS					
Input Common-Mode Voltage Range			0 to 5		V
Input Resistance	Differential		1.5		kΩ
	Single-ended input		1.13		kΩ
Input Capacitance	Differential		1		pF
DC CMRR	$\Delta V_{OUT, dm}/\Delta V_{IN, cm}$, $\Delta V_{IN, cm}$ = ±1 V		−48		dB
DIFFERENTIAL OUTPUT CHARACTERISTICS					
Differential Signal Gain	$\Delta V_{OUT, dm}/\Delta V_{IN, dm}$, $\Delta V_{IN, dm}$ = ±1 V	1.920	1.955	2.000	V/V
Output Voltage Swing	Each single-ended output	V_{S-} + 1.25		V_{S+} − 1.15	V
Output Offset Voltage		−24	3	+24	mV
Output Offset Drift	T_{MIN} to T_{MAX}		±30		µV/°C
Output Balance Error	f = 50 MHz		−60		dB
	DC		−70	−54	dB
Output Voltage Noise	f = 1 MHz		25		nV/√Hz
Output Short-Circuit Current			90		mA
COMMON-MODE SYNC PERFORMANCE					
SYNC DYNAMIC PERFORMANCE					
Slew Rate	$V_{OUT, cm}$ = −1 V to +1 V; 25% to 75%		700		V/µs
H_{SYNC} AND V_{SYNC} INPUTS					
Input Low Voltage			V_{S-} to 1.10		V
Input High Voltage			1.40 to V_{S+}		V
SYNC LEVEL INPUT					
Input Voltage Range	For linear operation				V
Setting to Achieve 0.5 V Pulse Levels			V_{S-} + 0.5		V
Gain to Red Common-Mode Output	$\Delta V_{O, cm}/\Delta V_{SYNC\ LEVEL}$	0.97	1.02	1.06	V/V
Gain to Green Common-Mode Output	$\Delta V_{O, cm}/\Delta V_{SYNC\ LEVEL}$	1.94	2.03	2.10	V/V
Gain to Blue Common-Mode Output	$\Delta V_{O, cm}/\Delta V_{SYNC\ LEVEL}$	0.96	1.02	1.05	V/V
POWER SUPPLY					
Operating Range		+4.5		±6	V
Quiescent Current			26.5	27.5	mA
PSRR			−54	−48	dB
OUTPUT PULL-DOWN PERFORMANCE					
OPD Input Low Voltage			V_{S-} to V_{S+} − 3.85		V
OPD Input High Voltage			V_{S+} − 2.85 to V_{S+}		V
OPD Input Bias Current			63	80	µA
OPD Assert Time			100		ns
OPD De-Assert Time			100		ns
Output Voltage When OPD Asserted	Each output, OPD input @ V_S+		V_{S-} + 0.79	V_{S-} + 0.82	V

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	12 V
H_{SYNC}, V_{SYNC}, Sync Level	$\pm V_S$
Power Dissipation	See Figure 3
Input Common-Mode Voltage	$\pm V_S$
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering 10 sec)	300°C
Junction Temperature	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, θ_{JA} is specified for the device soldered in a circuit board in still air.

Table 4. Thermal Resistance with the Underside Pad Thermally Connected to a Copper Plane

Package Type/PCB Type	θ_{JA}	Unit
24-Lead LFCSP/4-Layer	70	°C/W

Maximum Power Dissipation

The maximum safe power dissipation in the AD8134 package is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the AD8134. Exceeding a junction temperature of 175°C for an extended period can result in changes in the silicon devices potentially causing failure.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). The load current consists of differential and common-mode currents flowing to the loads, as well as currents flowing through the internal differential and common-mode feedback loops. The internal resistor tap used in the common-mode feedback loop places a 4 kΩ differential load on the output. RMS output voltages should be considered when dealing with ac signals.

Airflow reduces θ_{JA}. In addition, more metal directly in contact with the package leads from metal traces, through holes, ground, and power planes reduce the θ_{JA}. The exposed pad on the underside of the package must be soldered to a pad on the PCB surface that is thermally connected to a PCB plane to achieve the specified θ_{JA}.

Figure 3 shows the maximum safe power dissipation in the package vs. the ambient temperature for the 24-lead LFCSP (70°C/W) on a JEDEC standard 4-layer board with the underside paddle soldered to a pad that is thermally connected to a PCB plane. θ_{JA} values are approximations.

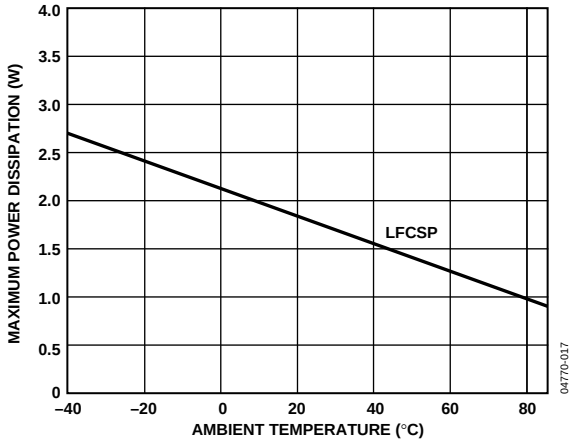
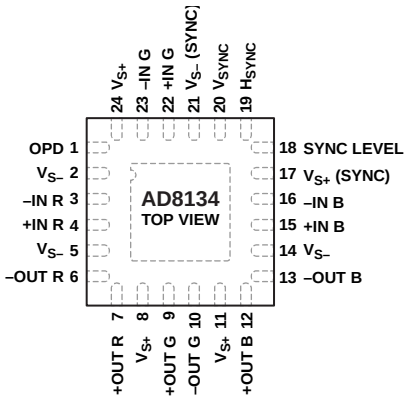


Figure 3. Maximum Power Dissipation vs. Temperature for a 4-Layer Board

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. EXPOSED PAD. THE EXPOSED PADDLE MUST BE SOLDERED TO A PAD ON TOP OF THE BOARD THAT IS CONNECTED TO AN INNER PLANE WITH SEVERAL THERMAL VIAS.

04770-0-101

Figure 4. 24-Lead LFCSP

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	OPD	Output Pull Down.
2, 5, 14, 21	V_{S-}	Negative Power Supply Voltage.
3	−IN R	Inverting Input, Red Amplifier.
4	+IN R	Noninverting Input, Red Amplifier.
6	−OUT R	Negative Output, Red Amplifier.
7	+OUT R	Positive Output, Red Amplifier.
8, 11, 17, 24	V_{S+}	Positive Power Supply Voltage.
9	+OUT G	Positive Output, Green Amplifier.
10	−OUT G	Negative Output, Green Amplifier.
12	+OUT B	Positive Output, Blue Amplifier.
13	−OUT B	Negative Output, Blue Amplifier.
15	+IN B	Noninverting Input, Blue Amplifier.
16	−IN B	Inverting Input, Blue Amplifier.
18	SYNC LEVEL	The voltage applied to this pin controls the amplitude of the sync pulses that are applied to the common-mode voltages.
19	H_{SYNC}	Horizontal Sync Pulse Input.
20	V_{SYNC}	Vertical Sync Pulse Input.
22	+IN G	Noninverting Input, Green Amplifier.
23	−IN G	Inverting Input, Green Amplifier.
	EPAD	Exposed Pad. The exposed paddle must be soldered to a pad on top of the board that is connected to an inner plane with several thermal vias.

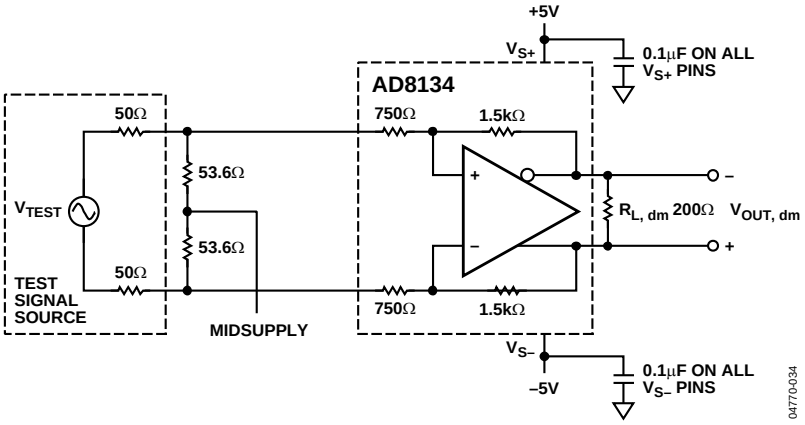


Figure 5. Basic Test Circuit

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = ±5 V, $R_{L, dm}$ = 200, T_A = 25°C, H_{SYNC} and V_{SYNC} = V_{S-}, unless otherwise noted.

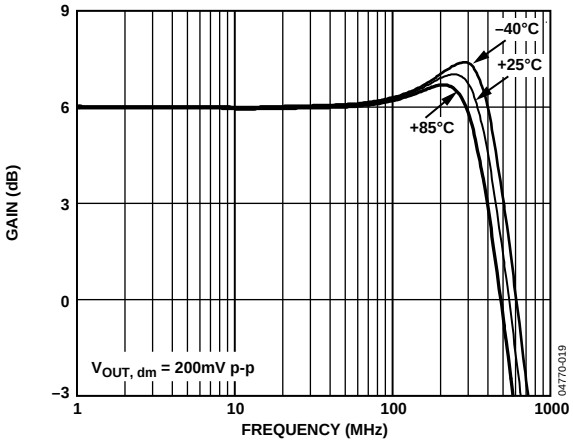


Figure 6. Small Signal Frequency Response at Various Temperatures

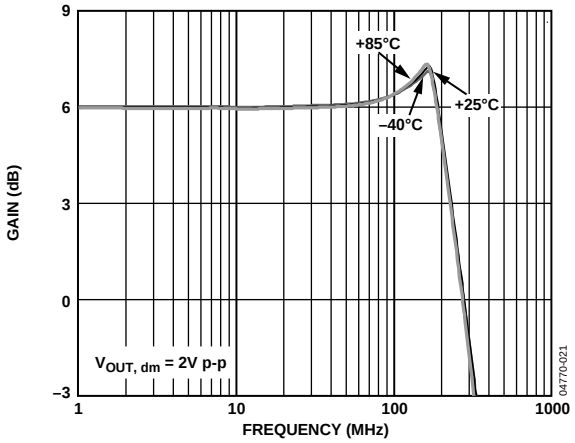


Figure 9. Large Signal Frequency Response at Various Temperatures

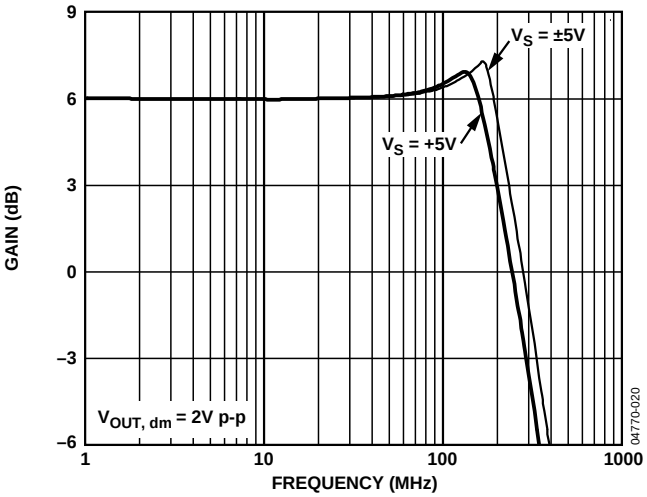


Figure 7. Large Signal Frequency Response for Various Power Supplies

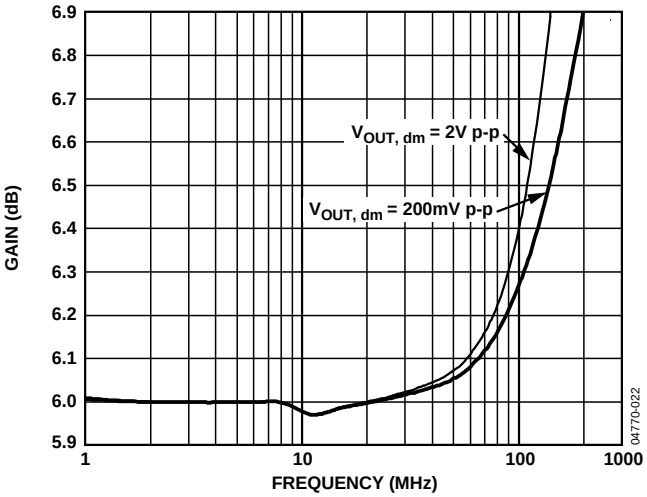


Figure 10. 0.1 dB Flatness

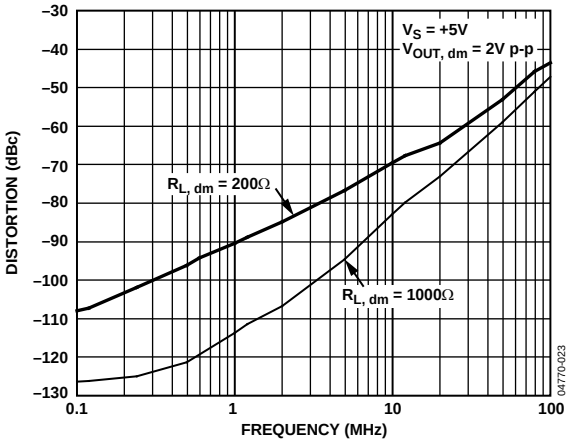


Figure 8. Second Harmonic Distortion at V_S = 5 V at Various Loads

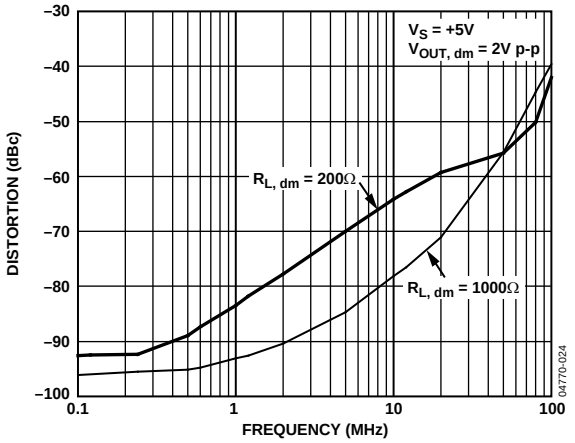


Figure 11. Third Harmonic Distortion at V_S = 5 V at Various Loads

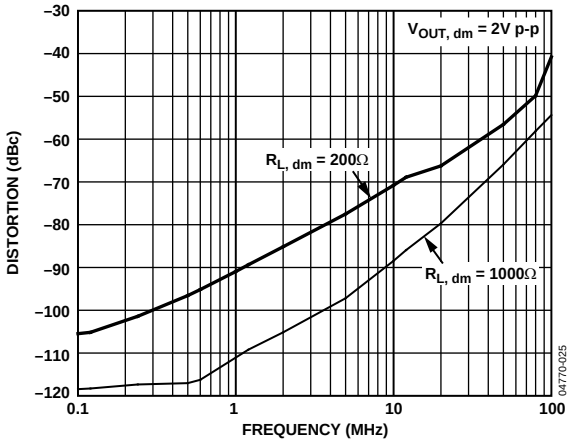


Figure 12. Second Harmonic Distortion at V_S = ±5 V at Various Loads

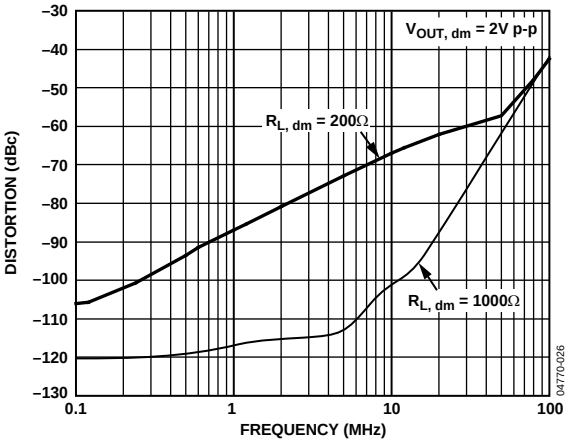


Figure 15. Third Harmonic Distortion at V_S = ±5 V at Various Loads

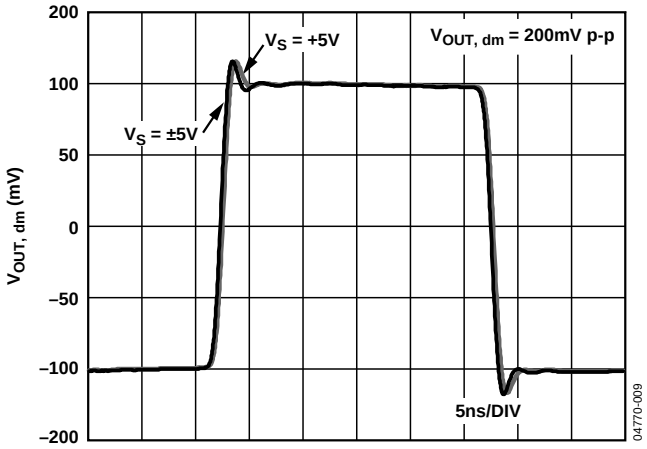


Figure 13. Small Signal Transient Response for Various Power Supply Voltages

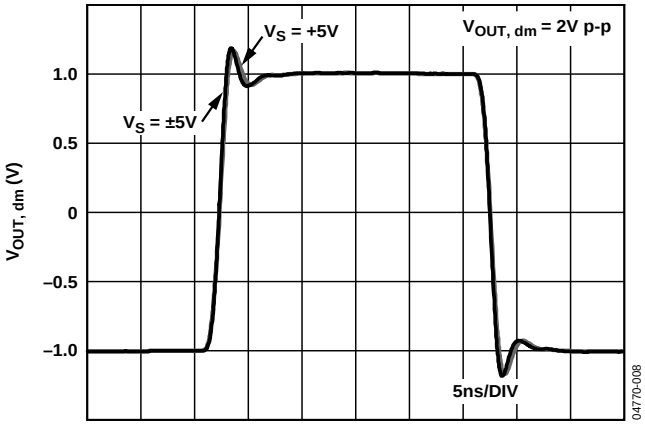


Figure 16. Large Signal Transient Response for Various Power Supply Voltages

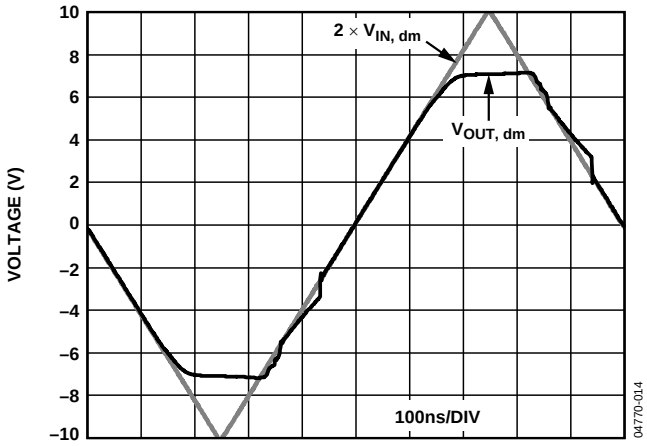


Figure 14. Overdrive Recovery

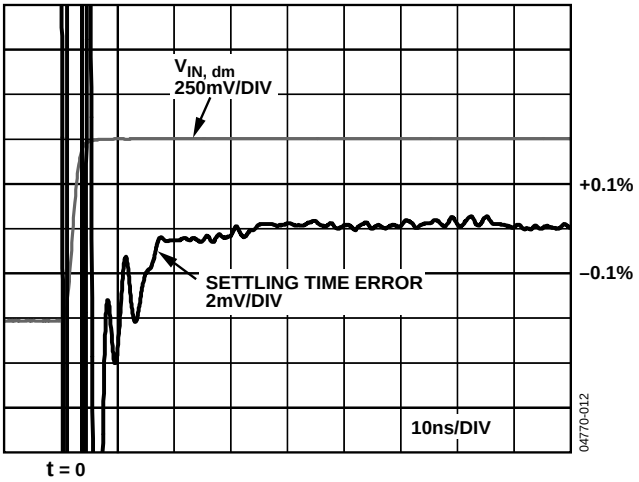


Figure 17. Settling Time (0.1%)

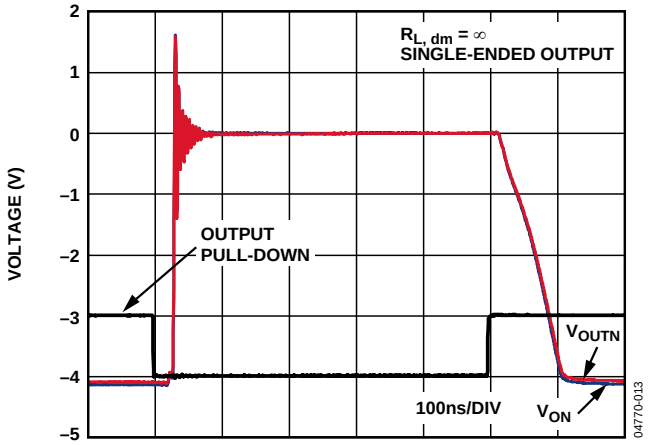


Figure 18. Output Pull-Down Response

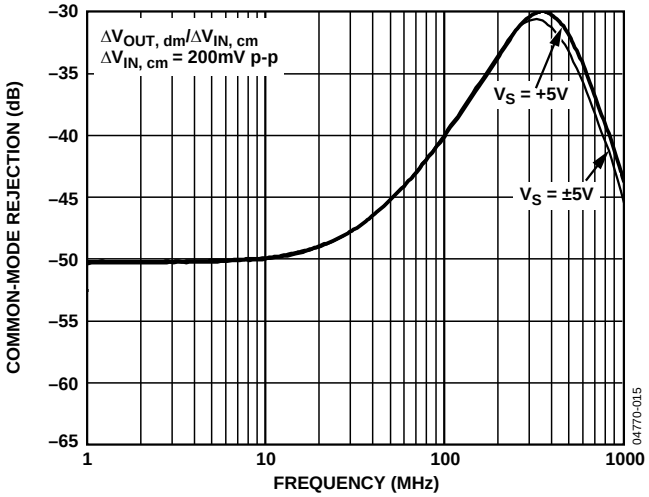


Figure 21. Common-Mode Rejection Ratio vs. Frequency

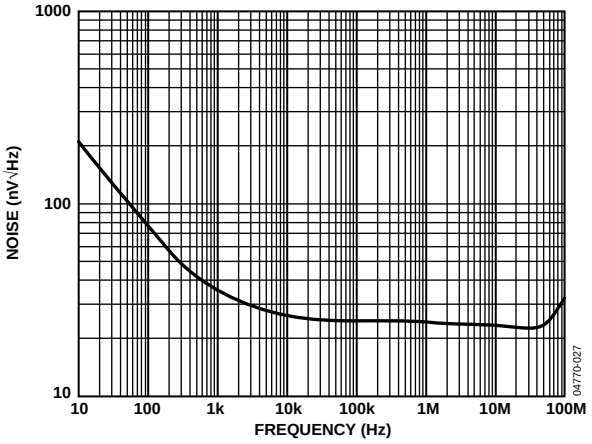


Figure 19. Output-Referred Voltage Noise vs. Frequency

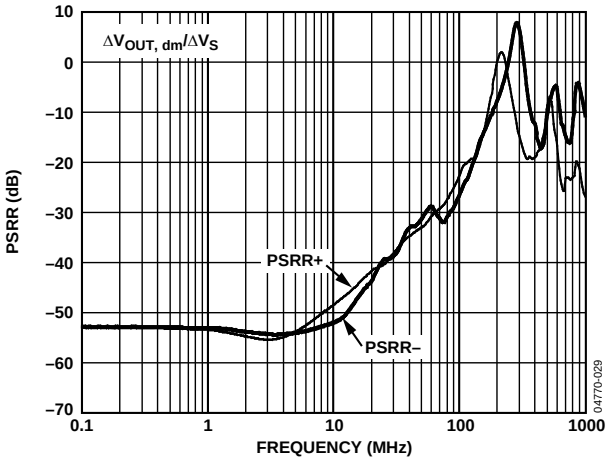


Figure 22. Power Supply Rejection Ratio vs. Frequency

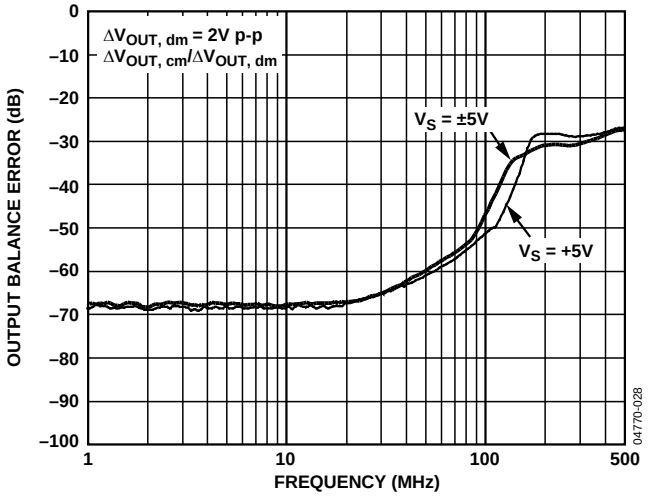


Figure 20. Output Balance vs. Frequency

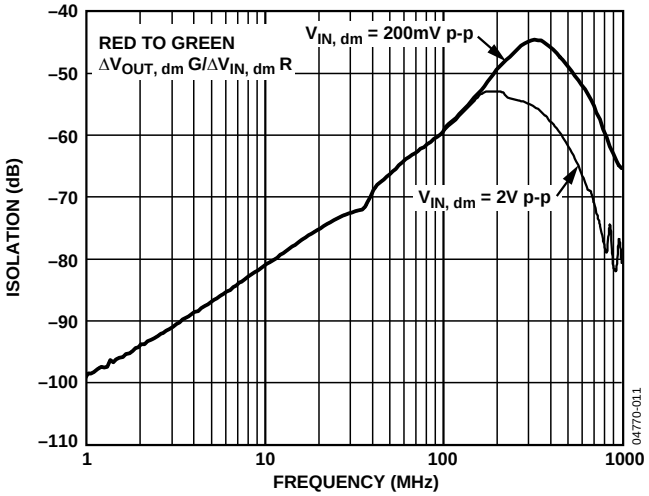


Figure 23. Amplifier-to-Amplifier Isolation vs. Frequency

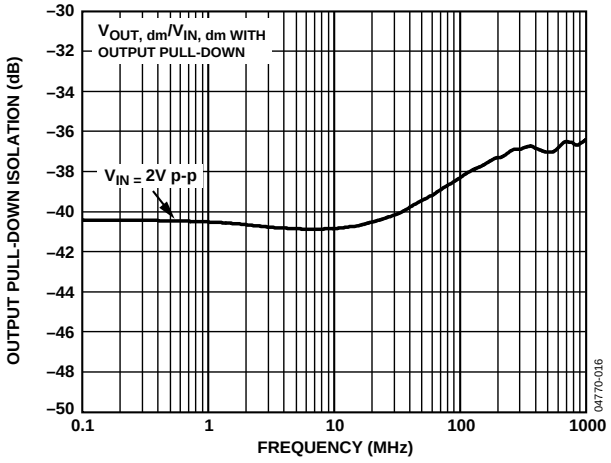


Figure 24. Output Pull-Down Isolation vs. Frequency

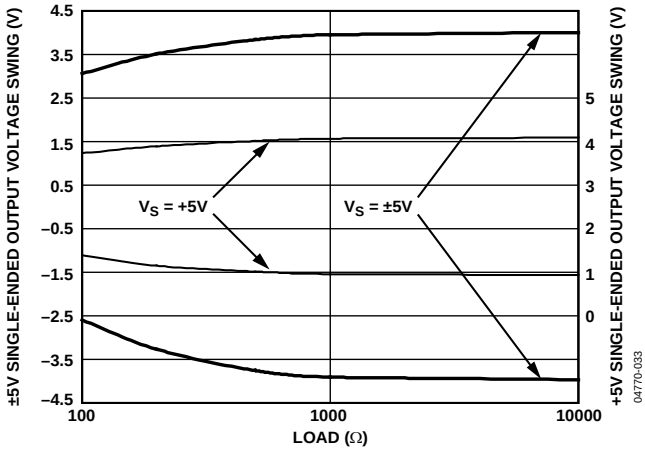


Figure 27. Output Saturation Voltage vs. Output Load

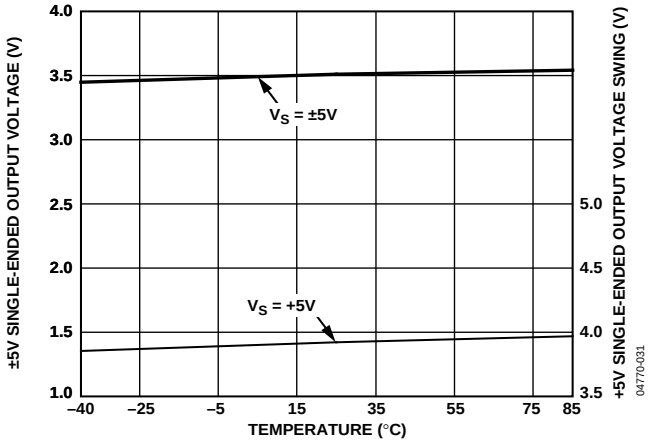


Figure 25. Positive Output Saturation Voltage vs. Temperature

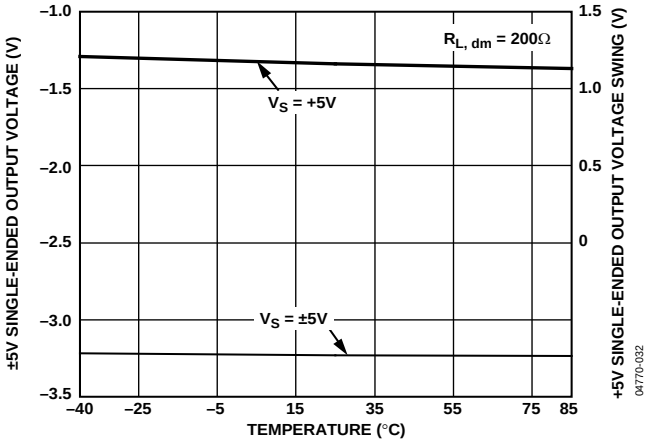


Figure 28. Negative Output Saturation Voltage vs. Temperature

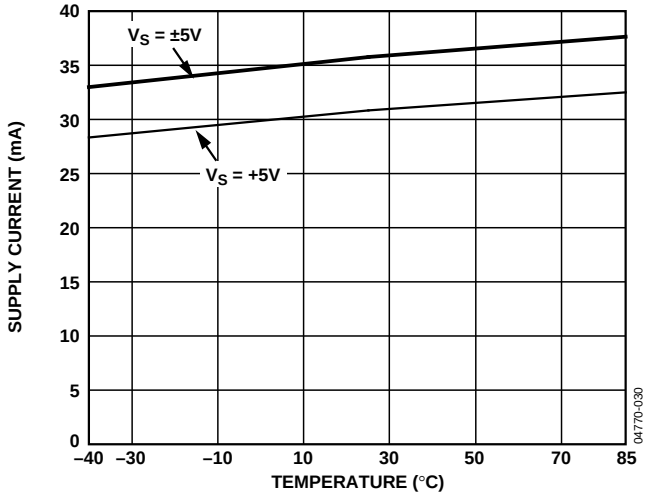


Figure 26. Power Supply Current vs. Temperature

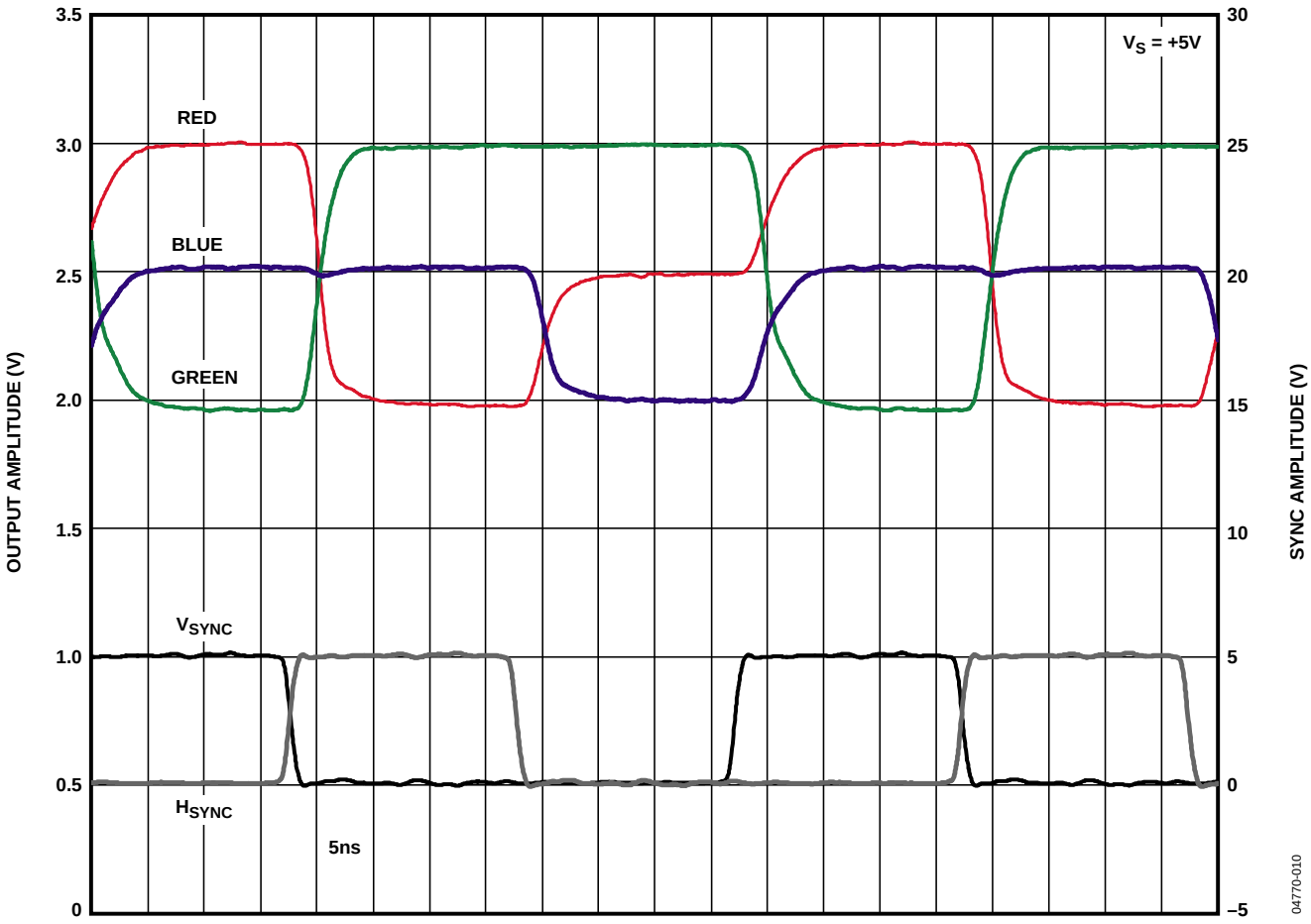


Figure 29. Output Common-Mode Signals for Various Sync Pulse Inputs

THEORY OF OPERATION

Each differential driver in the AD8134 differs from a conventional op amp in that it has two outputs whose voltages move in opposite directions. Like an op amp, it relies on high open-loop gain and negative feedback to force these outputs to the desired voltages. The AD8134 drivers make it easy to perform single-ended-to-differential conversion, common-mode level-shifting, and amplification of differential signals.

Previous differential drivers, both discrete and integrated designs, are based on using two independent amplifiers and two independent feedback loops, one to control each of the outputs. When these circuits are driven from a single-ended source, the resulting outputs are typically not well balanced. Achieving a balanced output has typically required exceptional matching of the amplifiers and feedback networks.

DC common-mode level-shifting has also been difficult with previous differential drivers. Level-shifting has required the use of a third amplifier and feedback loop to control the output common-mode level. Sometimes, the third amplifier has also been used to attempt to correct an inherently unbalanced circuit. Excellent performance over a wide frequency range has proven difficult with this approach.

Each of the AD8134 drivers uses two feedback loops to separately control the differential and common-mode output voltages. The differential feedback, set by the internal resistors, controls the differential output voltage only. The internal common-mode feedback loop controls the common-mode output voltage only. This architecture makes it easy to arbitrarily set the output common-mode level by simply applying a voltage to the V_{OCM} input. The output common-mode voltage is forced, by internal common-mode feedback, to equal the voltage applied to the V_{OCM} input, without affecting the differential output voltage. The V_{OCM} inputs are not available to the user but are internally connected to the sync-on-common-mode circuitry.

The AD8134 architecture results in outputs that are highly balanced over a wide frequency range without requiring external components or adjustments. The common-mode feedback loop forces the signal component of the output common-mode voltage to be zeroed. The result is nearly perfectly balanced differential outputs of identical amplitude that are exactly 180° apart in phase.

DEFINITION OF TERMS

Differential Voltage

Differential voltage refers to the difference between two node voltages that are balanced with respect to each other. For example, in Figure 30, the output differential voltage (or equivalently output differential mode voltage) is defined as

$$V_{OUT,\,dm} = (V_{OP} - V_{ON})$$

Common-mode voltage refers to the average of two node voltages with respect to a common reference. The output common-mode voltage is defined as

$$V_{OUT,\,cm} = \frac{(V_{OP} + V_{ON})}{2}$$

Output Balance

Output balance is a measure of how well the differential output signals are matched in amplitude and how close they are to exactly 180° apart in phase. Balance is easily determined by placing a well-matched resistor divider between the differential output voltage nodes and comparing the magnitude of the signal at the divider's midpoint with the magnitude of the differential signal. By this definition, output balance error is the magnitude of the change in output common-mode voltage divided by the magnitude of the change in output differential-mode voltage in response to a differential input signal

$$Output\ \ Balance\ \ Error = \left|\frac{\Delta V_{OUT,cm}}{\Delta V_{OUT,dm}}\right|$$

ANALYZING AN APPLICATION CIRCUIT

The AD8134 uses high open-loop gain and negative feedback to force its differential and common-mode output voltages to minimize the differential and common-mode input error voltages. The differential input error voltage is defined as the voltage between the differential inputs labeled V_{AP} and V_{AN} in Figure 30. For most purposes, this voltage can be assumed to be zero. Similarly, the difference between the actual output common-mode voltage and the voltage applied to V_{OCM} can also be assumed to be zero. Starting from these two assumptions, any application circuit can be analyzed.

CLOSED-LOOP GAIN

The differential mode gain of the circuit in Figure 30 can be described by

$$\left|\frac{V_{OUT,dm}}{V_{IN,dm}}\right| = \frac{R_F}{R_G} = 2$$

where R_F = 1.5 kΩ and R_G = 750 Ω nominally.

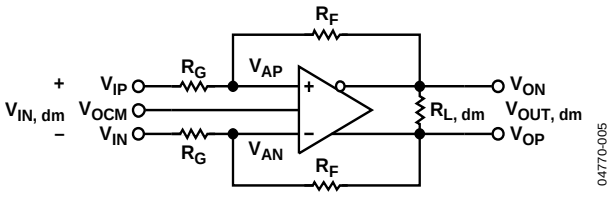


Figure 30. Circuit Definitions

CALCULATING AN APPLICATION CIRCUIT'S INPUT IMPEDANCE

The effective input impedance of a circuit such as that in Figure 30 at V_{IP} and V_{IN} depends on whether the amplifier is being driven by a single-ended or differential signal source. For balanced differential input signals, the differential input impedance, $R_{IN, dm}$, between the inputs V_{IP} and V_{IN} is simply

$$R_{IN,dm} = 2 \times R_G = 1.5\ \text{k}\Omega$$

In the case of a single-ended input signal (for example, if V_{IN} is grounded and the input signal is applied to V_{IP}), the input impedance becomes

$$R_{IN} = \left(\frac{R_G}{1 - \frac{R_F}{2 \times (R_G + R_F)}} \right) = 1.125\ \text{k}\Omega$$

The circuit's input impedance is effectively higher than it would be for a conventional op amp connected as an inverter because a fraction of the differential output voltage appears at the inputs as a common-mode signal, partially bootstrapping the voltage across the input resistor R_G.

INPUT COMMON-MODE VOLTAGE RANGE IN SINGLE-SUPPLY APPLICATIONS

The inputs of the AD8134 are designed to facilitate level-shifting of ground referenced input signals on a single power supply. For a single-ended input, this would imply, for example, that the voltage at V_{IN} in Figure 30 would be 0 V when the amplifier's negative power supply voltage was also set to 0 V.

It is important to ensure that the common-mode voltage at the amplifier inputs, V_{AP} and V_{AN}, stays within its specified range. Since voltages V_{AP} and V_{AN} are driven to be essentially equal by negative feedback, the amplifier's input common-mode voltage can be expressed as a single term, V_{ACM}. V_{ACM} can be calculated as

$$V_{ACM} = \frac{V_{OCM} + 2V_{ICM}}{3}$$

where V_{ICM} is the common-mode voltage of the input signal, that is, $V_{ICM} = \frac{V_{IP} + V_{IN}}{2}$.

DRIVING A CAPACITIVE LOAD

A purely capacitive load can react with the output impedance of the AD8134 to reduce phase margin, resulting in high frequency ringing in the pulse response. The best way to minimize this effect is to place a small resistor in series with each of the amplifier's outputs to buffer the load capacitance.

OUTPUT PULL-DOWN (OPD)

The AD8134 has an OPD pin that when pulled high significantly reduces the power consumed while simultaneously pulling the outputs to within less than 1 V of V_{S-} when used with series diodes (see the Applications section). The equivalent schematic of the output in the output pull-down state is shown in Figure 31. (The ESD diodes shown in Figure 31 are for ESD protection and are distinct from the series diodes used with the output pull-down feature.) See Figure 18 and Figure 24 for the output pull-down transient and isolation performance. The threshold levels for the OPD input pin are referenced to the positive power supply and are listed in the Specifications tables. When the OPD pin is pulled high, the AD8134 enters the output pull-down state.

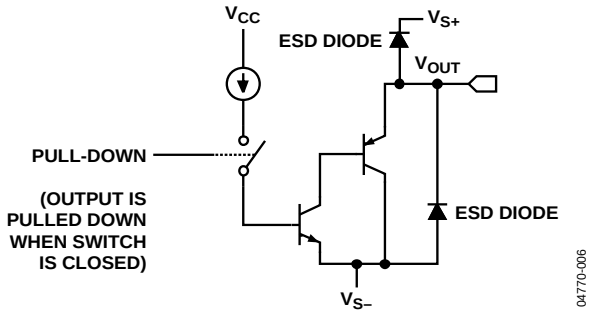


Figure 31. Output Pull-Down Equivalent Circuit

SYNC-ON-COMMON-MODE

The AD8134 drives RGB video signals over UTP cable. The balance of the differential outputs is trimmed to ensure low radiated energy from each of the twisted pairs. The common-mode outputs of each of the R, G, and B differential outputs are set using the circuit in Figure 32. This circuit embeds the horizontal and vertical sync pulses on the three common-mode outputs in a way that also results in low radiated energy. For a more detailed description of the sync scheme, see the Applications section.

The sync-on-common-mode circuit generates a current based on the SYNC LEVEL input pin (Pin 18). With SYNC LEVEL input tied to V_{S-}, the common-mode output of all drivers is set at $(V_{S+} + V_{S-})/2$. Using a resistor divider, a voltage can be applied between V_{S-} and SYNC LEVEL that determines the maximum deviation of the common-mode outputs from their midsupply level. If, for instance, SYNC LEVEL − V_{S-} = 0.5 V and the supply voltage is 5 V, then the common-mode outputs fall within an envelope of 2.5 V ± 0.5 V. The state of each $V_{OUT, cm}$ output based on the H_{SYNC} and V_{SYNC} inputs is determined by the equations defined in the Applications section.

On a single 5 V supply, the sync-on-common-mode circuit can be used by directly applying the H_{SYNC} and V_{SYNC} signals to the respective AD8134 inputs. The logic thresholds of the H_{SYNC} and V_{SYNC} inputs are nominally set at $(V_{S+} - V_{S-})/4$, using a resistor divider with an impedance of approximately 200 kΩ. This allows the inputs to be driven beyond the rails without logic inversion and maintains fast switching speeds. The robustness of the H_{SYNC} and V_{SYNC} inputs therefore allows them to be driven directly off the output of a computer video card without concern of overdriving the inputs. The input path from H_{SYNC} and V_{SYNC} inputs to the switches in the current mode level-shifting circuit are well matched to eliminate false switching transients. This maximizes common-mode balance and minimizes radiated energy.

The sync-on-common-mode circuit can be used with ±5 V supplies, but in this case, the H_{SYNC} and V_{SYNC} logic signals require level-shifting. Level-shifting details are provided in the Applications section.

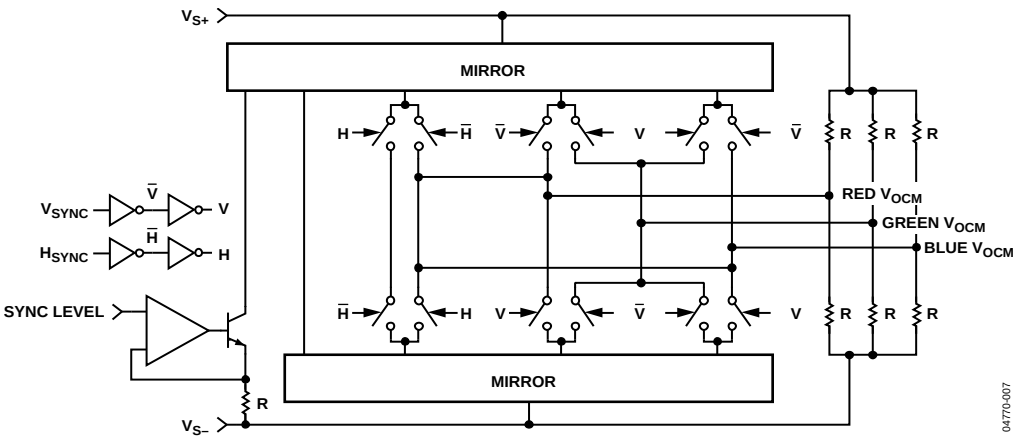


Figure 32. Sync-On-Common-Mode Simplified Circuit

APPLICATIONS

DRIVING RGB VIDEO OVER CAT-5 CABLE

The AD8134 is a device whose foremost application is driving RGB video signals over UTP cable in KVM networks. Single-ended video signals are easily converted to differential signals for transmission over the cable, and the internally fixed gain of 2 automatically compensates for the losses incurred by the source and load terminations. The AD8134 can be used in all of the typical KVM network topologies, including daisy-chained, star, and point-to-point. Figure 33 shows the AD8134 in a triple, single-ended-to-differential application in a daisy-chained network when driven from a 75 Ω video source.

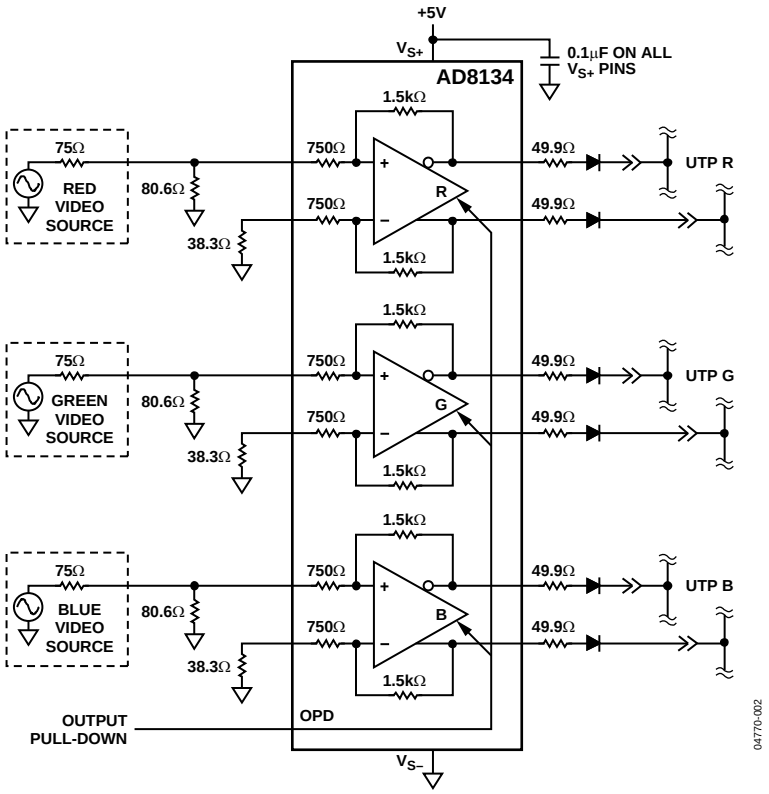


Figure 33. AD8134 in Single-Ended-to-Differential Application on Single 5 V Supply (Sync Pulse Encoding Not Shown)

HOW TO APPLY THE OUTPUT PULL-DOWN FEATURE

The output pull-down feature, when used in conjunction with series Schottky diodes, offers a convenient means to connect a number of transmitters together to form a video network. The OPD pin is a binary input that controls the state of the AD8134 outputs. Its binary input level is referenced to the most positive power supply (see the Specifications section for the logic levels). When the OPD input is driven to its low state, the AD8134 output is enabled and operates in its normal fashion. In this state, the sync-on-common-mode circuitry provides a midsupply voltage and encoded sync pulses on the output common-mode voltage. The midsupply voltage is used to forward bias the series diodes, allowing the AD8134 to transmit signals over the network. When the OPD input is driven to its high state the outputs of the AD8134 are forced to a low voltage irrespective of the levels on the sync inputs. This reverse-biases the series diodes and presents a high impedance to the network. This feature allows a three-state output to be realized that maintains its high impedance state even when the AD8134 is not powered. This condition can occur in KVM networks where the AD8134s do not all reside in the same module, and where some modules in the network are not powered.

It is recommended that the output pull-down feature only be used in conjunction with series diodes in such a way as to ensure that the diodes are reverse-biased when the output pull-down feature is asserted because some loading conditions can prevent the output voltage from being pulled all the way down.

KVM NETWORKS

In daisy-chained KVM networks, the drivers are distributed along one cable and a triple receiver is located at one end. Schottky diodes in series with the driver outputs are biased such that the one driver that is transmitting video signals has its diodes forward-biased and the disabled drivers have their diodes reverse-biased. The output common-mode voltage, set by the sync-on-common-mode circuitry, supplies the forward-biased voltage. When the output pull-down feature is asserted, the differential outputs are pulled to a low voltage, reverse-biasing the diodes.

In star networks, all cables radiate out from a central hub, which contains a triple receiver. The series diodes are all located at the receiver in the star network. Only one ray of the star is transmitting at a given time, and all others are isolated by reverse-biased diodes. Diode biasing is controlled in the same way as in the daisy-chained network.

In the daisy-chained and star networks that use diodes for isolation, return paths are required for the common-mode currents that flow through the series diodes. A common-mode tap can be implemented at each receiver by splitting the 100 Ω termination resistor into two 50 Ω resistors in series. The diode currents are routed from the tap between the 50 Ω resistors back to the respective transmitters over one of the wires of the fourth twisted pair in the UTP cable. Series resistors in the common-mode path are generally required to set the desired diode current.

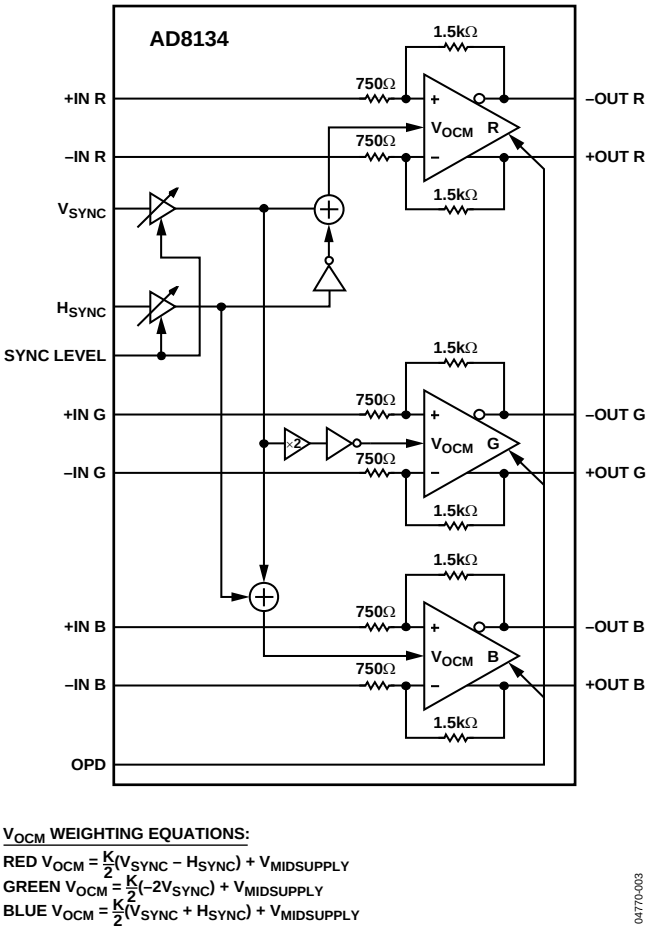
In point-to-point networks, there is one transmitter and one receiver per cable, and the switching is generally implemented with a crosspoint switch. In this case, there is no need to use diodes or the output pull-down feature.

Diode and crosspoint switching are by no means the only type of switching that can be used with the AD8134. Many other types of mechanical, electromechanical, and electronic switches can be used.

VIDEO SYNC-ON-COMMON-MODE

In computer video applications, the horizontal and vertical sync signals are often separate from the video information signals. For example, in typical computer monitor applications, the red, green, and blue (RGB) color signals are transmitted over separate cables, as are the vertical and horizontal sync signals. When transmitting these types of video signals over long distances on UTP cable, it is desirable to reduce the required number of physical channels. One way to do this is to encode the vertical and horizontal sync signals as weighted sums and differences of the output common-mode signals. The RGB color signals are each transmitted differentially over separate physical channels. The fact that the differential and common-mode signals are orthogonal allows the RGB color and sync signals to be separated at the channel's receiver.

Cat-5 cable contains four balanced twisted-pair physical channels that can support both differential and common-mode signals. Transmitting typical computer monitor video over this cable can be accomplished by using three of the twisted pairs for the RGB and sync signals and one wire of the fourth pair as a return path for the Schottky diode bias currents. Each color is transmitted differentially, one on each of the three pairs, and the encoded sync signals are transmitted among the common-mode signals of each of the three pairs. To minimize EMI from the sync signals, the common-mode signals on each of the three pairs produced by the sync encoding scheme induce electric and magnetic fields that for the most part cancel each other. A conceptual block diagram of the sync encoding scheme is presented in Figure 34. Since the AD8134 has the sync encoding scheme implemented internally, the user simply applies the horizontal and vertical sync signals to the appropriate inputs. (See the Specifications tables for the definitions of the high and low levels of the horizontal and vertical sync pulse voltages).



V_{OCM} WEIGHTING EQUATIONS:

RED $V_{OCM} = \frac{K}{2}(V_{SYNC} - H_{SYNC}) + V_{MIDSUPPLY}$

GREEN $V_{OCM} = \frac{K}{2}(-2V_{SYNC}) + V_{MIDSUPPLY}$

BLUE $V_{OCM} = \frac{K}{2}(V_{SYNC} + H_{SYNC}) + V_{MIDSUPPLY}$

Figure 34. AD8134 Sync-On-Common-Mode Encoding Scheme

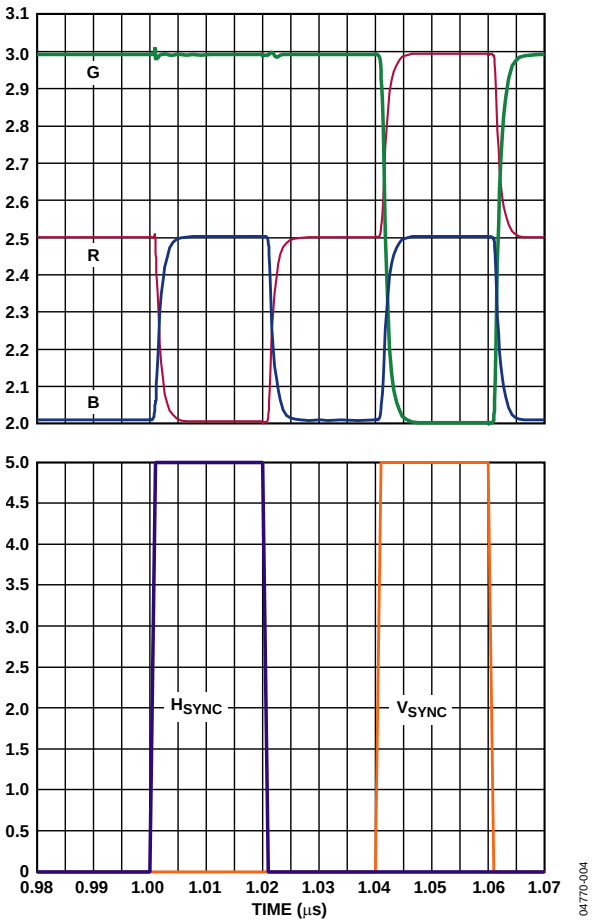


Figure 35. AD8134 Sync-On-Common-Mode Signals in Single 5 V Application

The transmitted common-mode sync signal magnitudes are scaled by applying a dc voltage to the SYNC LEVEL input, referenced to the negative supply. The difference between the voltage applied to the SYNC LEVEL input and the negative supply sets the peak deviation of the encoded sync signals about the midsupply common-mode voltage. For example, with the SYNC LEVEL input set at V_{S-} + 500 mV, the deviation of the encoded sync pulses about the nominal midsupply common-mode voltage is typically ±500 mV. The equations in Figure 34 describe how the V_{SYNC} and H_{SYNC} signals are encoded on each color's midsupply common-mode signal. In these equations, the weights of the V_{SYNC} and H_{SYNC} signals are ±1 (+1 for high, −1 for low), and the constant K is equal to the peak deviation of the encoded sync signals.

Figure 35 shows how the sync signals appear on each common-mode voltage in a single 5 V supply application when the voltage applied to the SYNC LEVEL input is 500 mV. A typical setting for the SYNC LEVEL voltage is 500 mV above the negative supply.

LEVEL-SHIFTING SYNC PULSES ON ±5 V SUPPLIES

The vertical and horizontal sync pulses received from a computer video port are generally referenced to ground. When using ±5 V supplies, these pulses must be level-shifted before being applied to the negative-supply referenced V_{SYNC} and H_{SYNC} inputs because these inputs are referenced to the negative supply. The circuit shown in Figure 36 provides the proper sync pulse level-shifting for a negative supply voltage of −5 V. The vertical and horizontal sync pulses each require a level-shift circuit.

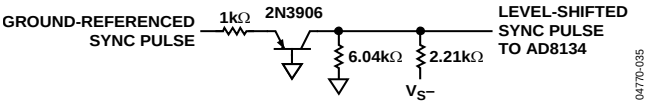


Figure 36. Level-Shifting Sync Pulses on ±5 V Supplies

LAYOUT AND POWER SUPPLY DECOUPLING CONSIDERATIONS

Standard high speed PCB layout practices should be adhered to when designing with the AD8134. A solid ground plane is recommended and good wideband power supply decoupling networks should be placed as close as possible to the supply pins. Small surface-mount ceramic capacitors are recommended for these networks, and tantalum capacitors are recommended for bulk supply decoupling.

AMPLIFIER-TO-AMPLIFIER ISOLATION

The least amount of isolation between the three amplifiers exists between Amplifier R and Amplifier G. This is therefore viewed as the worst-case isolation and is what is reflected in the Specifications tables and Typical Performance Characteristics. Refer to the basic test circuit in Figure 5 for test conditions.

EXPOSED PADDLE (EP)

The 24-lead LFCSP package has an exposed paddle on the underside of its body. To achieve the specified thermal resistance, it must have a good thermal connection to one of the PCB planes. The exposed paddle must be soldered to a pad on top of the board that is connected to an inner plane with several thermal vias.

OUTLINE DIMENSIONS

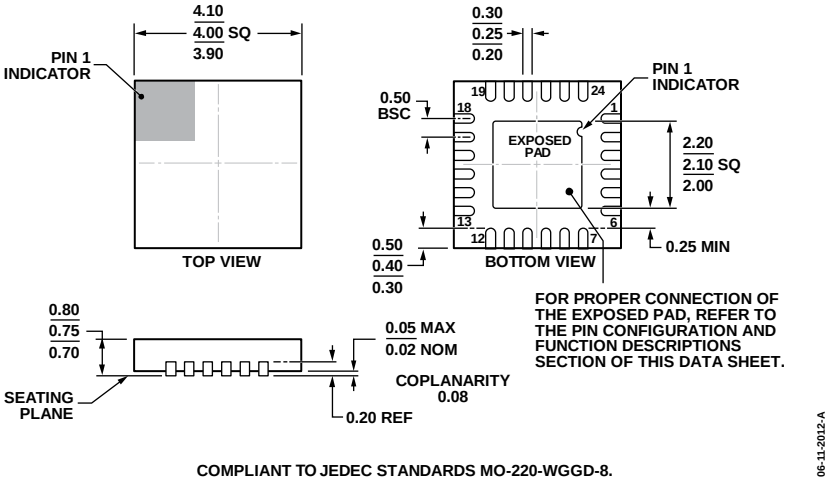


Figure 37. 24-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-24-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Package	Package Description	Package Outline
AD8134ACPZ-R2	−40°C to +85°C	24-Lead LFCSP	CP-24-10
AD8134ACPZ-REEL	−40°C to +85°C	24-Lead LFCSP	CP-24-10
AD8134ACPZ-REEL7	−40°C to +85°C	24-Lead LFCSP	CP-24-10

[1] Z = RoHS Compliant Part.