- **Wide Gain-Bandwidth Product . . . 4 MHz**
- **High Slew Rate . . . 13 V/μs**
- **Fast Settling Time . . . 1.1 μs to 0.1%**
- **Wide-Range Single-Supply Operation . . . 4 V to 36 V**
- **Wide Input Common-Mode Range Includes Ground (V_{CC-})**
- **Low Total Harmonic Distortion . . . 0.02%**
- **Large-Capacitance Drive Capability . . . 10,000 pF**
- **Output Short-Circuit Protection**

D OR P PACKAGE
(TOP VIEW)

1OUT	1	8	V_{CC+}
1IN−	2	7	2OUT
1IN+	3	6	2IN−
V_{CC-}/GND	4	5	2IN+
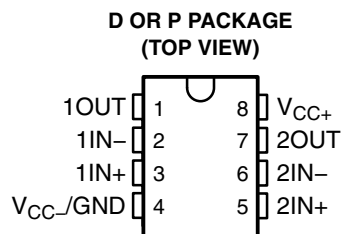
description/ordering information

Quality, low-cost, bipolar fabrication with innovative design concepts is employed for the TL3472 operational amplifier. This device offers 4 MHz of gain-bandwidth product, 13-V/μs slew rate, and fast settling time, without the use of JFET device technology. Although the TL3472 can be operated from split supplies, it is particularly suited for single-supply operation because the common-mode input voltage range includes ground potential (V_{CC-}). With a Darlington transistor input stage, this device exhibits high input resistance, low input offset voltage, and high gain. The all-npn output stage, characterized by no dead-band crossover distortion and large output voltage swing, provides high-capacitance drive capability, excellent phase and gain margins, low open-loop high-frequency output impedance, and symmetrical source/sink ac frequency response. This low-cost amplifier is an alternative to the MC33072 and the MC34072 operational amplifiers.

ORDERING INFORMATION

| T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP (P)	Tube of 25	TL3472CP	TL3472CP
	SOIC (D)	Tube of 50	TL3472CD	3472C
		Reel of 2500	TL3472CDR	
−40°C to 105°C	PDIP (P)	Tube of 25	TL3472IP	TL3472IP
	SOIC (D)	Tube of 50	TL3472ID	Z3472
		Reel of 2500	TL3472IDR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TEXAS INSTRUMENTS

schematic (each amplifier)
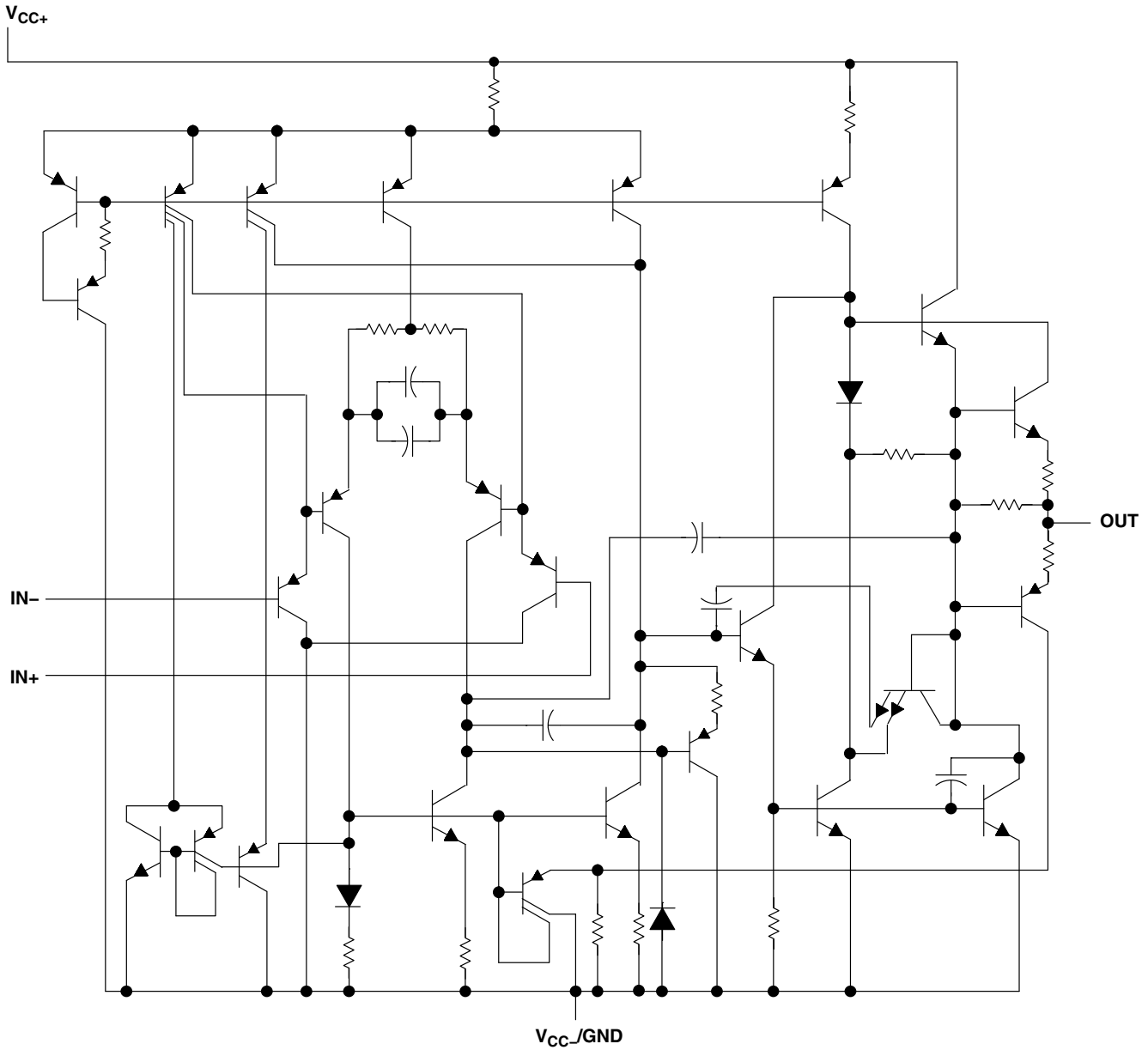
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (see Note 1): V_{CC+} . . . . 18 V

V_{CC-} . . . . –18 V

Differential input voltage, V_{ID} (see Note 2) . . . . ±36 V

Input voltage, V_I (any input) . . . . $V_{CC\pm}$

Input current, I_I (each input) . . . . ±1 mA

Output current, I_O . . . . ±80 mA

Total current into V_{CC+} . . . . 80 mA

Total current out of V_{CC-} . . . . 80 mA

Duration of short-circuit current at (or below) 25°C (see Note 3) . . . . Unlimited

Package thermal impedance, θ_{JA} (see Notes 4 and 5): D package . . . . 97°C/W

P package . . . . 85°C/W

Operating virtual junction temperature, T_J . . . . 150°C

Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

Storage temperature range, T_{stg} . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive input current can flow when the input is less than V_{CC-} – 0.3 V.
3. The output can be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.
4. Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

			MIN	MAX	UNIT
$V_{CC\pm}$	Supply voltage		4	36	V
V_{IC}	Common-mode input voltage	$V_{CC} = 5$ V	0	2.8	V
		$V_{CC\pm} = \pm15$ V	–15	12.8	
T_A	Operating free-air temperature	TL3472C	0	70	°C
		TL3472I	–40	105	

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP†	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$	$V_{CC} = 5$ V	25°C		1.5	10	mV
			$V_{CC} = \pm 15$ V	25°C		1.0	10	
				Full range‡			12	
$\alpha_{V_{IO}}$	Temperature coefficient of input offset voltage		$V_{CC} = \pm 15$ V	Full range‡		10		µV/°C
I_{IO}	Input offset current		$V_{CC} = \pm 15$ V	25°C		6	75	nA
				Full range‡			300	
I_{IB}	Input bias current		$V_{CC} = \pm 15$ V	25°C		100	500	nA
				Full range‡			700	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$		25°C		−15 to 12.8		V
				Full range‡		−15 to 12.8		
V_{OH}	High-level output voltage	$V_{CC+} = 5$ V, $V_{CC-} = 0$, $R_L = 2\ k\Omega$		25°C	3.7	4		V
		$R_L = 10\ k\Omega$		25°C	13.6	14		
		$R_L = 2\ k\Omega$		Full range‡	13.4			
V_{OL}	Low-level output voltage	$V_{CC+} = 5$ V, $V_{CC-} = 0$, $R_L = 2\ k\Omega$		25°C		0.1	0.3	V
		$R_L = 10\ k\Omega$		25°C		−14.7	−14.3	
		$R_L = 2\ k\Omega$		Full range‡			−13.5	
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L = 2\ k\Omega$		25°C	25	100		V/mV
				Full range‡	20			
I_{OS}	Short-circuit output current	Source: $V_{ID} = 1$ V, $V_O = 0$		25°C	−10	−34		mA
		Sink: $V_{ID} = -1$ V, $V_O = 0$			20	27		
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$(min), $R_S = 50\ \Omega$		25°C	65	97		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm} = \pm 13.5$ V to ± 16.5 V, $R_S = 100\ \Omega$		25°C	70	97		dB
I_{CC}	Supply current (per channel)	$V_O = 0$, No load		25°C		3.5	4.5	mA
				Full range‡		4.5	5.5	
		$V_{CC+} = 5$ V, $V_O = 2.5$ V, $V_{CC-} = 0$, No load		25°C		3.5	4.5	

† All typical values are at $T_A = 25$°C.
‡ Full range is 0°C to 70°C for the TL3472C device and −40°C to 105°C for the TL3472I device.

operating characteristics, $V_{CC\pm} = \pm15$ V, $T_A = 25°C$

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR+	Positive slew rate	$V_I = -10$ V to 10 V, $R_L = 2$ kΩ, $C_L = 300$ pF	$A_V = 1$	8	10		V/µs
SR−	Negative slew rate		$A_V = -1$		13		V/µs
t_s	Settling time	$A_{VD} = -1$, 10-V step	To 0.1%		1.1		µs
			To 0.01%		2.2		
V_n	Equivalent input noise voltage	f = 1 kHz,	$R_S = 100$ Ω		49		nV/√Hz
I_n	Equivalent input noise current	f = 1 kHz			0.22		pA/√Hz
THD	Total harmonic distortion	$V_{O(PP)} = 2$ V to 20 V, $R_L = 2$ kΩ, $A_{VD} = 10$, f = 10 kHz			0.02		%
GBW	Gain-bandwidth product	f =100 kHz		3	4		MHz
BW	Power bandwidth	$V_{O(PP)} = 20$ V, $R_L = 2$ kΩ, $A_{VD} = 1$, THD = 5.0%			160		kHz
ϕ_m	Phase margin	$R_L = 2$ kΩ	$C_L = 0$		70		deg
			$C_L = 300$ pF		50		
	Gain margin	$R_L = 2$ kΩ	$C_L = 0$		12		dB
			$C_L = 300$ pF		4		
r_i	Differential input resistance	$V_{IC} = 0$			150		MΩ
C_i	Input capacitance	$V_{IC} = 0$			2.5		pF
	Channel separation	f = 10 kHz			101		dB
z_o	Open-loop output impedance	f = 1 MHz,	$A_V = 1$		20		Ω

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL3472CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	3472C	Samples
TL3472CP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL3472CP	Samples
TL3472IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z3472	Samples
TL3472IP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 105	TL3472IP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TL3472 :

- Automotive : TL3472-Q1

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL3472CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL3472IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL3472CDR	SOIC	D	8	2500	356.0	356.0	35.0
TL3472IDR	SOIC	D	8	2500	356.0	356.0	35.0

TUBE

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TL3472CP	P	PDIP	8	50	506	13.97	11230	4.32
TL3472IP	P	PDIP	8	50	506	13.97	11230	4.32

.228-.244   TYP
[5.80-6.19]

PIN 1 ID AREA

A

1

.189-.197
[4.81-5.00]
NOTE 3

4

B

.150-.157
[3.81-3.98]
NOTE 4

6X .050
[1.27]

8

2X
.150
[3.81]

5

8X .012-.020
[0.31-0.51]

⊕ .010 [0.25]Ⓜ C A B

C

SEATING PLANE

⌒ .004 [0.1] C

4X (0°-15°)

.069 MAX
[1.75]

SEE DETAIL A

4X (0°-15°)

.005-.010   TYP
[0.13-0.25]

.010
[0.25]

0° - 8°

.016-.050
[0.41-1.27]

(.041)
[1.04]

.004-.010
[0.11-0.25]

DETAIL A
TYPICAL

4214825/C   02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches.
   Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
   exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

8X (.061)
[1.55]

1

8X (.024)
[0.6]

6X (.050)
[1.27]

4

SYMM

SEE
DETAILS

8

SYMM

(R.002) TYP
[0.05]

5

(.213)
[5.4]

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

METAL

SOLDER MASK
OPENING

EXPOSED
METAL

.0028 MAX
[0.07]
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
OPENING

METAL UNDER
SOLDER MASK

EXPOSED
METAL

.0028 MIN
[0.07]
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214825/C   02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

8X (.061)
[1.55]

SYMM

1

8X (.024)
[0.6]

SYMM

8

(R.002) TYP
[0.05]

6X (.050)
[1.27]

4

5

(.213)
[5.4]

SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C   02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R−PDIP−T8)   PLASTIC DUAL−IN−LINE PACKAGE

0.400 (10,16)
0.355 (9,02)

8   5

0.260 (6,60)
0.240 (6,10)

1   4

0.070 (1,78)
0.045 (1,14)

0.045 (1,14)
0.030 (0,76)

0.020 (0,51) MIN

0.200 (5,08) MAX

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

Seating Plane

0.125 (3,18) MIN

0.010 (0,25) NOM

0.100 (2,54)

0.430 (10,92)
MAX

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

4040082/E 04/2010

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   Falls within JEDEC MS−001 variation BA.

IMPORTANT NOTICE AND DISCLAIMER