LPV542 Dual Nanopower 1.8 V, 490nA, RRIO CMOS Operational Amplifier

1 Features

- Wide Supply Range: 1.6 V to 5.5 V
- Low Supply Current: 490 nA (typical/channel)
- Good Offset Voltage: 3 mV (maximum/room)
- Good TcVos: 1µV/°C (typical)
- Gain-Bandwidth: 8 kHz (typical)
- Rail-to-Rail Input and Output
- Unity-Gain Stable
- Low Input Bias Current : 1 pA (typ)
- EMI Hardened
- Temperature Range: -40°C to 125°C
- Thin 3 mm x 3 mm x 0.45 mm X1SON package

2 Applications

- Wearables
- Personal Health Monitors
- Battery Packs
- Mobile Phones and Tablets
- Solar-Powered or Energy Harvested Systems
- PIR, Smoke, Gas, and Fire Detection Systems
- Battery Powered Internet of Things (IoT) Devices
- Remote Sensors
- Micropower Reference Buffer

3 Description

The LPV542 is an ultra-low-power, dual operational amplifier that provides 8kHz of bandwidth from 490nA of quiescent current making it well suited for battery-powered applications such as health and fitness wearables, building automation, and remote sensing nodes.

Each amplifier has a CMOS input stage with pico-amp bias currents which reduces errors commonly introduced in megaohm feedback resistance topologies such as photodiode and charge sense applications. In addition, the input common-mode range extends to the power supply rails and the output swings to within 3 mV of the rails, maintaining the widest dynamic range possible. Likewise, EMI protection is designed into the LPV542 in order to reduce system sensitivity to unwanted RF signals from mobile phones, WiFi, radio transmitters, and tag readers.

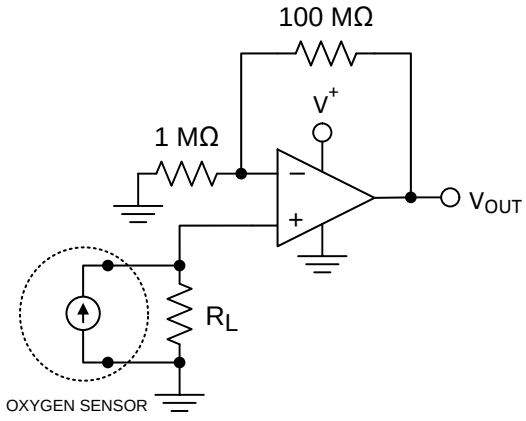
The LPV542 operates on a supply voltage as low as 1.6 V, ensuring continuous superior performance in low battery situations. The device is available in an 8-pad, low-profile, leadless 3 mm x 3 mm x 0.45 mm X1SON package and a standard 8 pin VSSOP.

Device Information(1)

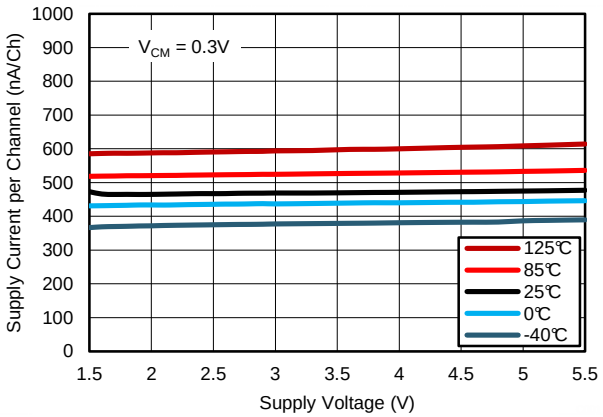
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LPV542	X1SON (8)	3.00 mm x 3.00 mm
	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Nanopower Oxygen Sensor Amplifier



Supply Current vs. Supply Voltage



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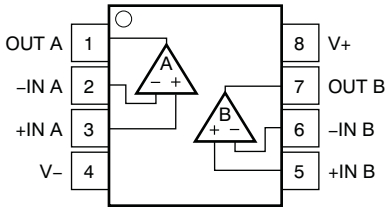
4 Revision History

Changes from Original (March 2015) to Revision A **Page**

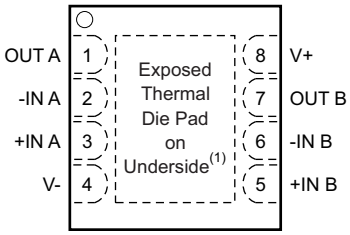
- Changed Front Page Bias Current to Typ ... 1
- Changed PSRR condition to 1.8V in all tables ... 5
- Changed PSRR Minimum in all tables ... 5
- Changed CMVR Condition to 57dB in 1.8V Table ... 5
- Changed CMRR Min in all tables ... 5
- Deleted Removed Maximum Bias Current Spec in all tables ... 5

5 Pin Configuration and Functions

8-Pin VSSOP
DGK Package
Top View



8-Pad X1SON
DNX Package
Top View



(1) Connect thermal die pad to V-.

Pin Functions

PIN			I/O	DESCRIPTION
NAME	DGK	DNX		
OUT A	1	1	O	Channel A Output
-IN A	2	2	I	Channel A Inverting Input
+IN A	3	3	I	Channel A Non-Inverting Input
V-	4	4	P	Negative (lowest) power supply
+IN B	5	5	I	Channel B Non-Inverting Input
-IN B	6	6	I	Channel B Inverting Input
OUT B	7	7	O	Channel B Output
V+	8	8	P	Positive (highest) power supply
Die Pad	--	DAP	P	Die Attach Pad. Connect to V- (DNX package only)

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)(2)(3)

		MIN	MAX	UNIT
Supply voltage, V+ to V–		-0.3	6	V
Signal input pins	Voltage(2)	(V-) - 0.3	(V+) + 0.3	V
	Current(2)	-10	10	mA
Output short current		Continuous(4)		
Junction temperature		-40	150	°C
Storage temperature, T_{stg}		-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails should be current-limited to 10 mA or less.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(4) Short-circuit to V-.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Ratings

	MIN	NOM	MAX	UNIT
Supply Voltage ($V^+ – V^-$)	1.6		5.5	V
Specified Temperature	-40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		DGK (VSSOP) 8 PINS	DNX (X1SON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	182.5	46.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	73.6	33.3	
$R_{\theta JB}$	Junction-to-board thermal resistance	104.1	21	
ψ_{JT}	Junction-to-top characterization parameter	13.7	0.2	
ψ_{JB}	Junction-to-board characterization parameter	102.5	21.2	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	7	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

6.5 Electrical Characteristics 1.8 V

T_A = 25°C, V^+ = 1.8V, V^- = 0V, V_{CM} = V_O = V^+/2, and R_L > 1 MΩ , unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
OFFSET VOLTAGE					
Input offset voltage (V_{OS})	V_{CM} = 0.3 V		±1	±2	mV
	V_{CM} = 1.5 V		±1	±3	
Over temperature	V_{CM} = 0.3 V and 1.5 V			±4	
Drift (dV_{OS}/dT)			1		µV/°C
Power-Supply Rejection Ratio (PSRR)	V_S = 1.8 V to 5.5 V, V_{CM} = 0.3 V	80	109		dB
INPUT VOLTAGE RANGE					
Common-mode voltage range (V_{CM})	CMRR ≥ 57 dB	0		1.8	V
Common-Mode Rejection Ratio (CMRR)	0 V < V_{CM} < 1.8 V	57	92		dB
	0 V < V_{CM} < 0.7 V	87	92		
	1.3 V < V_{CM} < 1.8 V	57	98		
INPUT BIAS CURRENT					
Input bias current (I_B)			±0.1		pA
Input offset current (I_{OS})			±0.1		
INPUT IMPEDANCE					
Differential			10^{13} || 2.5		Ω || pF
Common mode			10^{13} || 2.5		
NOISE					
Input voltage noise density, f = 1 kHz (e_n)			250		nV/√Hz
Current noise density, f = 1 kHz (i_n)			80		fA√Hz
OPEN-LOOP GAIN					
Open-loop voltage gain (A_{OL})	R_L = 100 kΩ to V^+/2, 0.5 V < V_O < 1.3 V	91	101		dB
OUTPUT					
Voltage output swing from positive rail	R_L = 100 kΩ to V^+/2		3	20	mV
Voltage output swing from negative rail	R_L = 100 kΩ to V^+/2		2	20	
Output current sourcing	Sourcing, V_O to V^-, V_{IN}(diff) = 100 mV	1	3		mA
Output current sinking	Sinking, V_O to V^+, V_{IN}(diff) = –100 mV	1	5		
FREQUENCY RESPONSE					
Gain-bandwidth product (GBWP)	C_L = 20 pF		7		kHz
Slew rate (SR)	G = +1, Rising edge, 1V_{p-p}, C_L = 20 pF		3.4		V/ms
	G = +1, Falling edge, 1V_{p-p}, C_L = 20 pF		3.7		
POWER SUPPLY					
Specified voltage range (V_S)		1.6		5.5	V
Quiescent current per channel (I_Q)	V_{CM} = 0.3 V, I_O = 0		490	800	nA
Over temperature				1100	
Quiescent current per channel (I_Q)	V_{CM} = 1.5 V, I_O = 0		680	1100	
Over temperature				1500	

(1) Refer to *Typical Characteristics*.

6.6 Electrical Characteristics 3.3 V

T_A = 25°C, V^+ = 3.3V, V^- = 0V, V_{CM} = V_O = V^+/2, and R_L > 1 MΩ , unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
OFFSET VOLTAGE					
Input offset voltage (V_{OS})	V_{CM} = 0.3		±1	±2	mV
	V_{CM} = 3 V		±1	±3	
Over temperature	V_{CM} = 0.3 V and 3 V			±4	
Drift (dV_{OS}/dT)			1		µV/°C
Power-Supply Rejection Ratio (PSRR)	V_S = 1.8 V to 5.5 V, V_{CM} = 0.3 V	80	109		dB
INPUT VOLTAGE RANGE					
Common-mode voltage range (V_{CM})	CMRR ≥ 60 dB	0		3.3	V
Common-Mode Rejection Ratio (CMRR)	0 V < V_{CM} < 3.3 V	62	98		dB
	0 V < V_{CM} < 2.2V	88	98		
	2.7 V < V_{CM} < 3.3 V	62	105		
INPUT BIAS CURRENT					
Input bias current (I_B)			±0.1		pA
Input offset current (I_{OS})			±0.1		
INPUT IMPEDANCE					
Differential			10^{13} || 2.5		Ω || pF
Common mode			10^{13} || 2.5		
NOISE					
Input voltage noise density, f = 1 kHz (e_n)			250		nV/√Hz
Current noise density, f = 1 kHz (i_n)			60		fA√Hz
OPEN-LOOP GAIN					
Open-loop voltage gain (A_{OL})	R_L = 100 kΩ to V^+/2, 0.5 V < V_O < 2.8 V	91	101		dB
OUTPUT					
Voltage output swing from positive Rail	R_L = 100 kΩ to V^+/2		3	20	mV
Voltage output swing from negative Rail	R_L = 100 kΩ to V^+/2		2	20	
Output current sourcing	Sourcing, V_O to V^-, V_{IN}(diff) = 100 mV	5	14		mA
Output current sinking	Sinking, V_O to V^+, V_{IN}(diff) = –100 mV	5	19		
FREQUENCY RESPONSE					
Gain-bandwidth product (GBWP)	C_L = 20 pF		8		kHz
Slew rate (SR)	G = +1, Rising edge, 1V_{p-p}, C_L = 20 pF		3.6		V/ms
	G = +1, Falling edge, 1V_{p-p}, C_L = 20 pF		3.7		
POWER SUPPLY					
Specified voltage range (V_S)		1.6		5.5	V
Quiescent current per channel (I_Q)	V_{CM} = 0.3 V, I_O = 0		480	800	nA
Over temperature				1200	
Quiescent current per channel (I_Q)	V_{CM} = 3 V, I_O = 0		650	1100	
Over temperature				1500	

(1) Refer to *Typical Characteristics*.

6.7 Electrical Characteristics 5 V

T_A = 25°C, V^+ = 5 V, V^- = 0 V, V_{CM} = V_O = V^+/2, and R_L > 1 MΩ , unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
OFFSET VOLTAGE					
Input offset voltage (V_{OS})	V_{CM} = 0.3 V		±1	±2	mV
	V_{CM} = 4.7V		±1	±3	
Over temperature	V_{CM} = 0.3 V and 4.7V			±4	
Drift (dV_{OS}/dT)			1		µV/°C
Power-Supply Rejection Ratio (PSRR)	V_S = 1.8 V to 5.5 V, V_{CM} = 0.3 V	80	109		dB
INPUT VOLTAGE RANGE					
Common-Mode voltage range (V_{CM})	CMRR ≥ 60 dB	0		5	V
Common-Mode Rejection Ratio (CMRR)	0 V < V_{CM} < 5 V	65	101		dB
	0 V < V_{CM} < 3.9V	88	101		
	4.4 V < V_{CM} < 5 V	65	109		
INPUT BIAS CURRENT					
Input bias current (I_B)			±0.1		pA
Input offset current (I_{OS})			±0.1		
INPUT IMPEDANCE					
Differential			10^{13} || 2.5		Ω || pF
Common mode			10^{13} || 2.5		
NOISE					
Input voltage noise density, f = 1 kHz (e_n)			250		nV/√Hz
Current noise density, f = 1 kHz (i_n)			65		fA√Hz
OPEN-LOOP GAIN					
Open-loop voltage gain (A_{OL})	R_L = 100 kΩ to V^+/2, 0.5 V < V_O < 4.5 V	91	101		dB
OUTPUT					
Voltage output swing from positive rail	R_L = 100 kΩ to V^+/2		3	20	mV
Voltage output swing from negative rail	R_L = 100 kΩ to V^+/2		2	20	
Output current sourcing	Sourcing, V_O to V^-, V_{IN}(diff) = 100 mV	10	30		mA
Output current sinking	Sinking, V_O to V^+, V_{IN}(diff) = –100 mV	10	36		
FREQUENCY RESPONSE					
Gain-bandwidth product (GBWP)	C_L = 20 pF		8		kHz
Slew rate (SR)	G = +1, Rising edge, $1V_{p-p}$, C_L = 20 pF		3.6		V/ms
	G = +1, Falling edge, $1V_{p-p}$, C_L = 20 pF		3.7		
POWER SUPPLY					
Specified voltage range (V_S)		1.6		5.5	V
Quiescent current per channel (I_Q)	V_{CM} = 0.3 V, I_O = 0		480	850	nA
Over temperature				1300	
Quiescent current per channel (I_Q)	V_{CM} = 4.7 V, I_O = 0		680	1100	
Over temperature				1600	

(1) Refer to *Typical Characteristics*.

6.8 Typical Characteristics

T_A = 25 °C, V_S = 5 V, V_{OUT} = V_{CM} = V_S/2, R_{LOAD} = 1 MΩ connected to V_S/2, and C_L = 20 pF, unless otherwise noted.

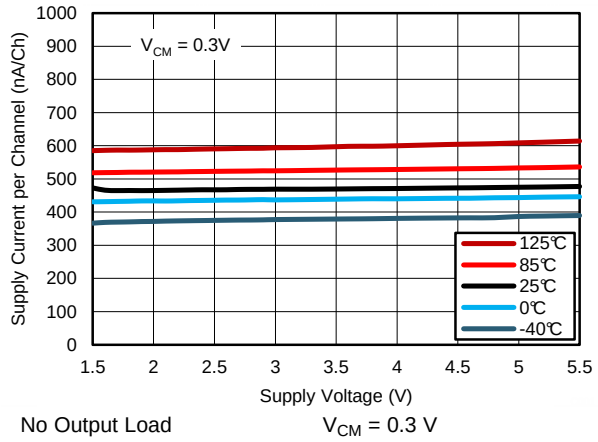


Figure 1. Supply Voltage vs Supply Current per Channel, Low Vcm

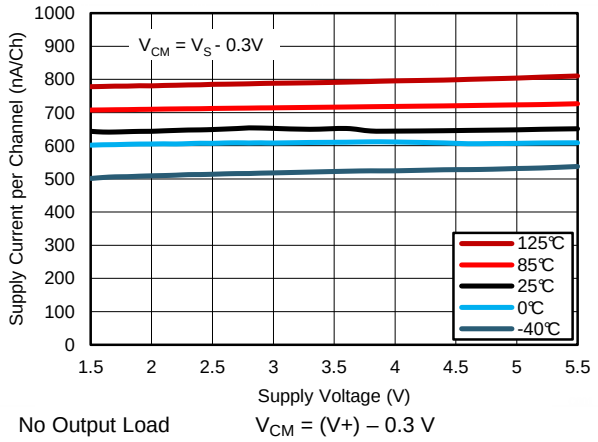


Figure 2. Supply Voltage vs Supply Current per Channel, High Vcm

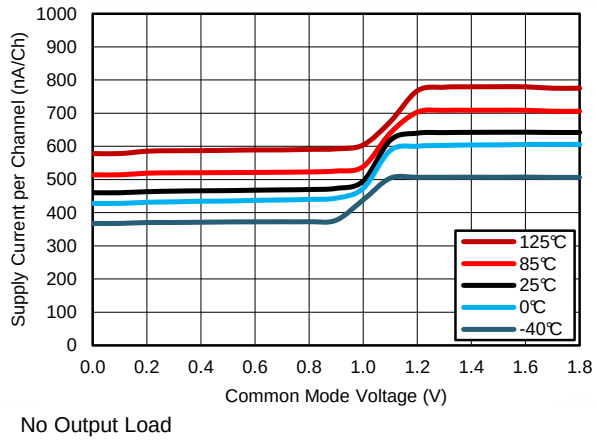


Figure 3. Supply Current vs Common Mode at 1.8 V

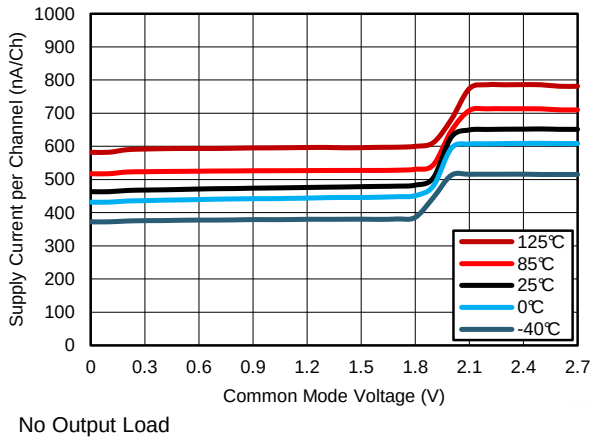


Figure 4. Supply Current vs Common Mode at 2.7 V

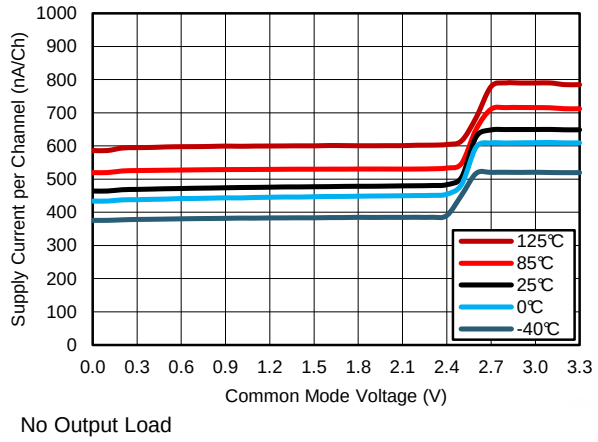


Figure 5. Supply Current vs Common Mode at 3.3 V

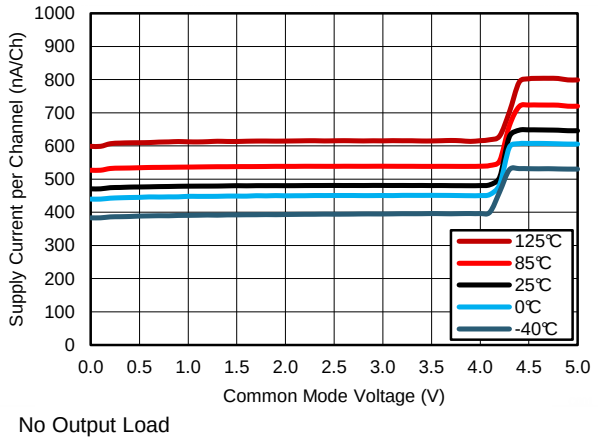
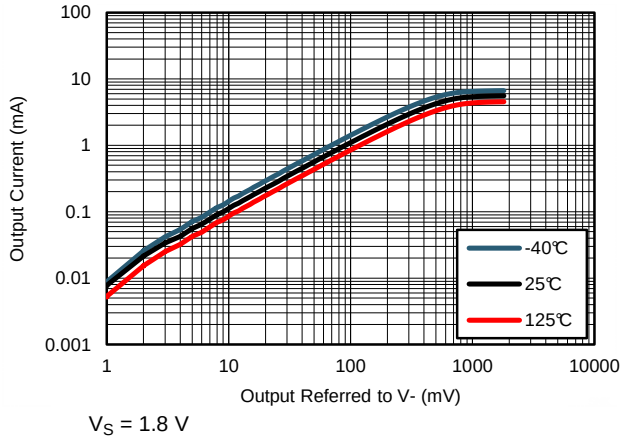


Figure 6. Supply Current vs Common Mode at 5 V

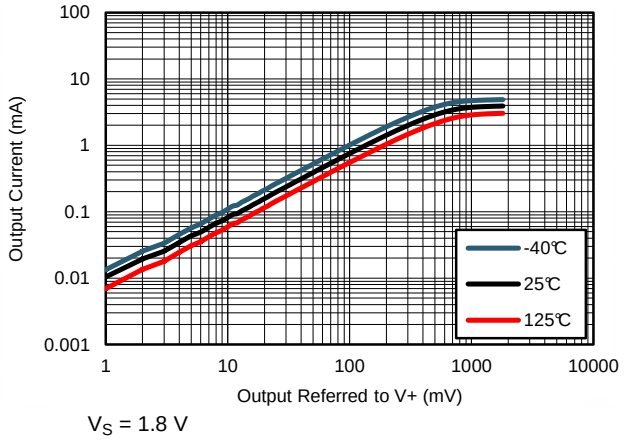
Typical Characteristics (continued)

T_A = 25 °C, V_S = 5 V, V_{OUT} = V_{CM} = V_S/2, R_{LOAD} = 1 MΩ connected to V_S/2, and C_L = 20 pF, unless otherwise noted.



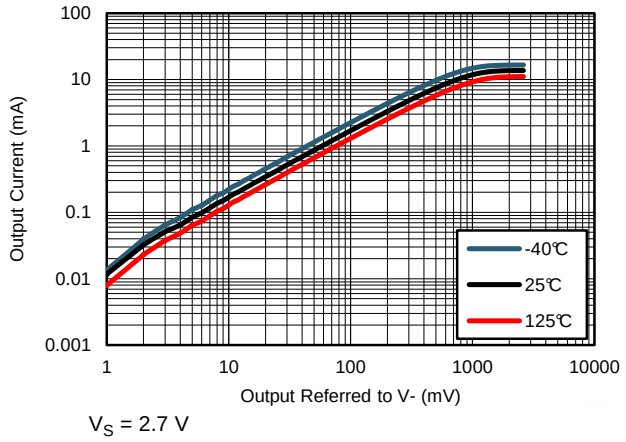
V_S = 1.8 V

Figure 7. Output Sinking Current vs Output Swing at 1.8 V



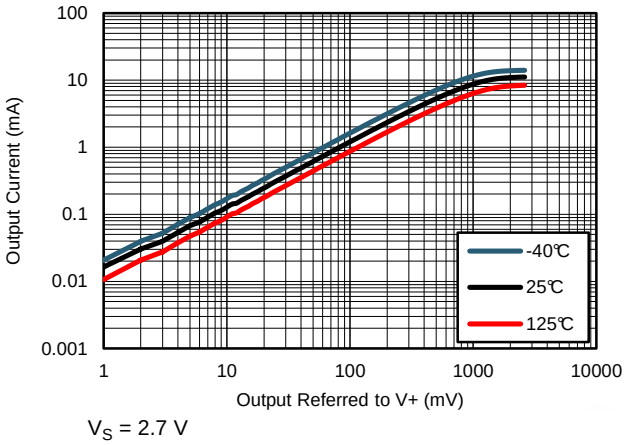
V_S = 1.8 V

Figure 8. Output Sourcing Current vs Output Swing at 1.8 V



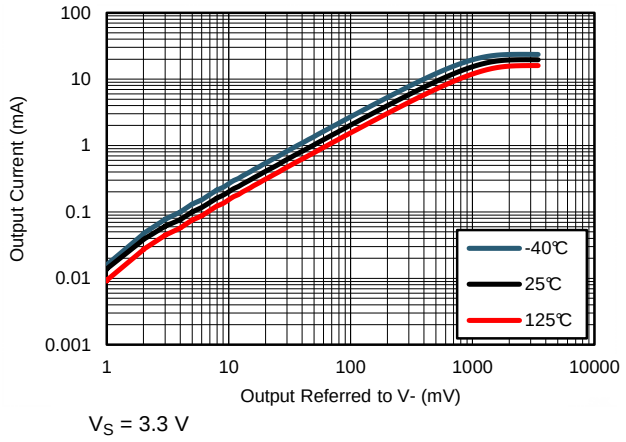
V_S = 2.7 V

Figure 9. Output Sinking Current vs Output Swing at 2.7 V



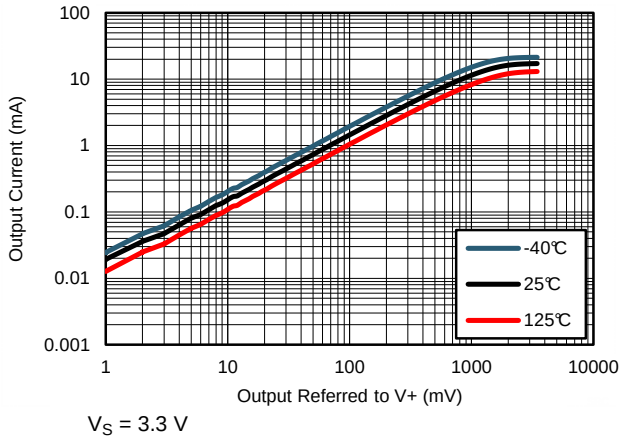
V_S = 2.7 V

Figure 10. Output Sourcing Current vs Output Swing at 2.7 V



V_S = 3.3 V

Figure 11. Output Sinking Current vs Output Swing at 3.3 V

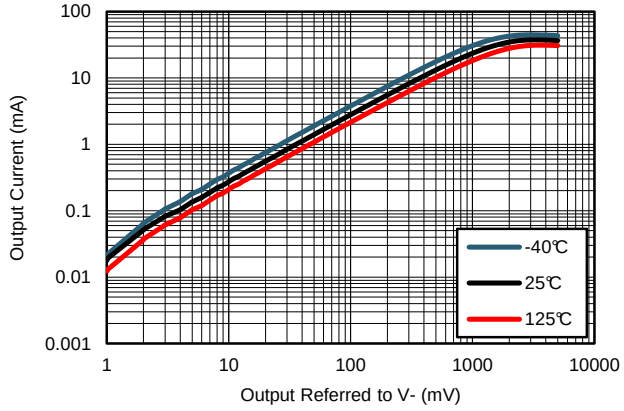


V_S = 3.3 V

Figure 12. Output Sourcing Current vs Output Swing at 3.3 V

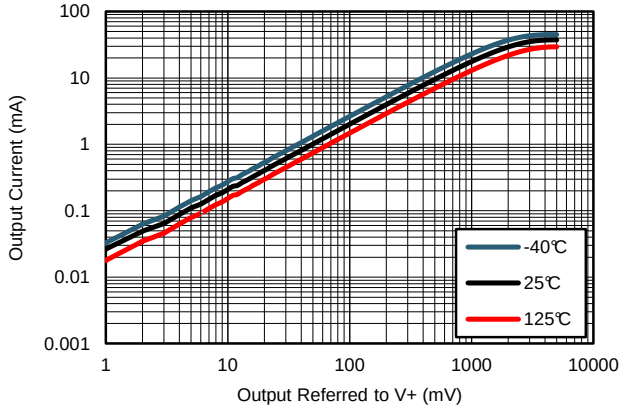
Typical Characteristics (continued)

T_A = 25 °C, V_S = 5 V, V_{OUT} = V_{CM} = V_S/2, R_{LOAD} = 1 MΩ connected to V_S/2, and C_L = 20 pF, unless otherwise noted.



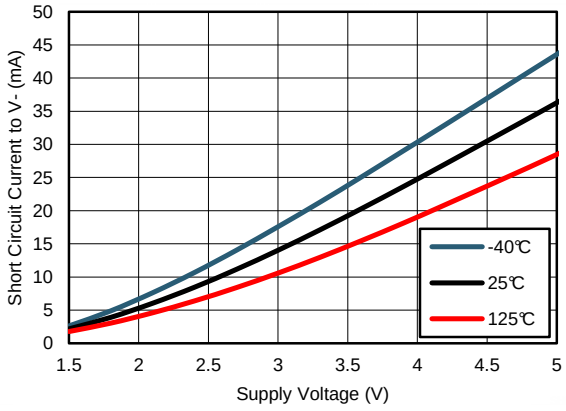
V_S = 5 V

Figure 13. Output Sinking Current vs Output Swing at 5 V



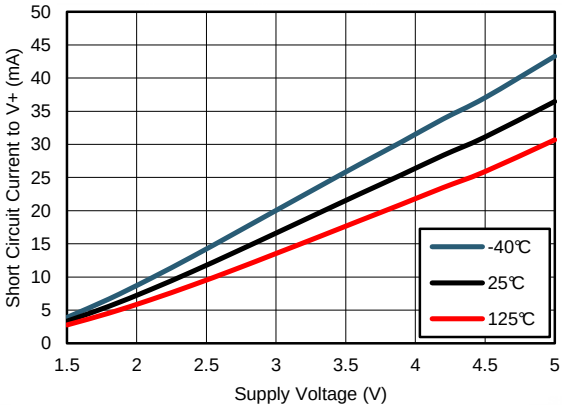
V_S = 5 V

Figure 14. Output Sourcing Current vs Output Swing at 5 V



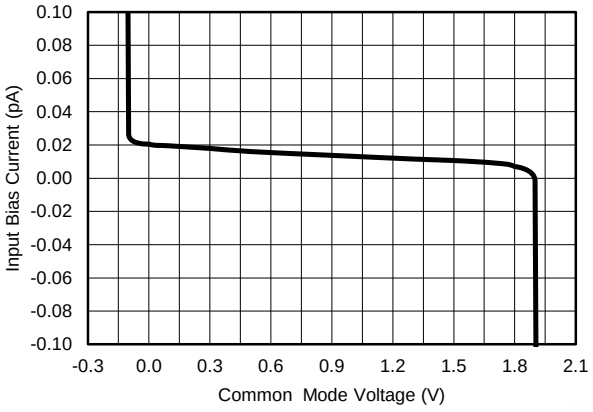
Output set high (sourcing), shorted to V–

Figure 15. Output Short Circut Current to V- vs Supply Voltage



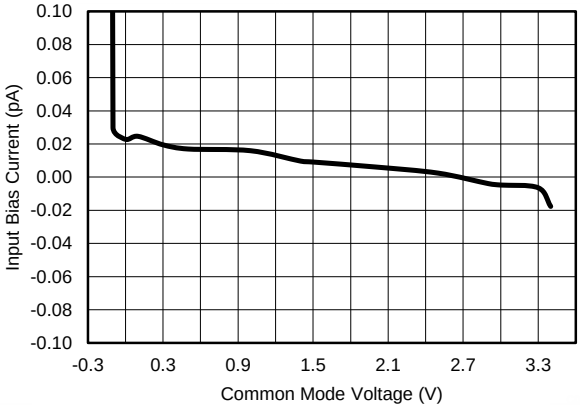
Ouput set low (sinking), shorted to V+

Figure 16. Output Short Circut Current to V+ vs Supply Voltage



V_S = 1.8 V T_A = 25°C

Figure 17. Input Bias Current vs Common Mode Voltage at 1.8 V



V_S = 3.3 V T_A = 25°C

Figure 18. Input Bias Current vs Common Mode Voltage at 3.3V

Typical Characteristics (continued)

T_A = 25 °C, V_S = 5 V, V_{OUT} = V_{CM} = V_S/2, R_{LOAD} = 1 MΩ connected to V_S/2, and C_L = 20 pF, unless otherwise noted.

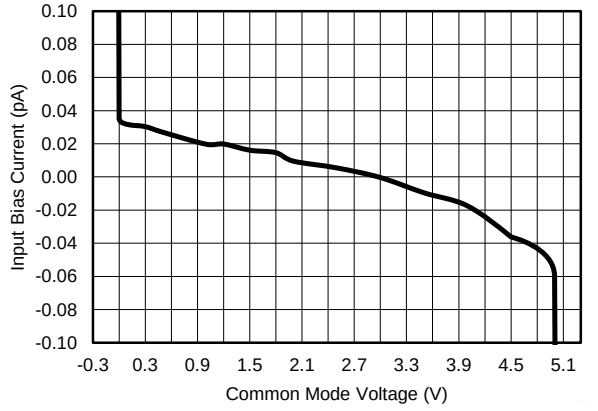


Figure 19. Input Bias Current vs Common Mode Voltage at 5V

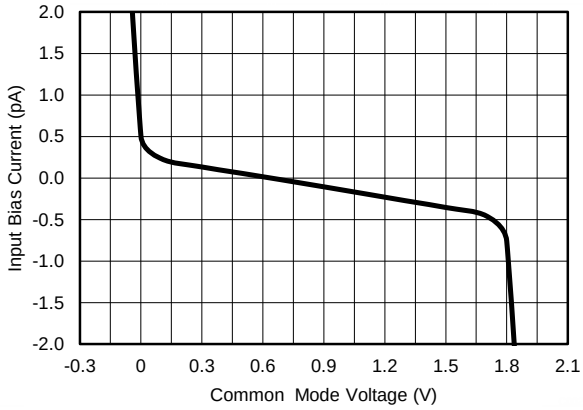


Figure 20. Input Bias Current vs Common Mode Voltage at 1.8V

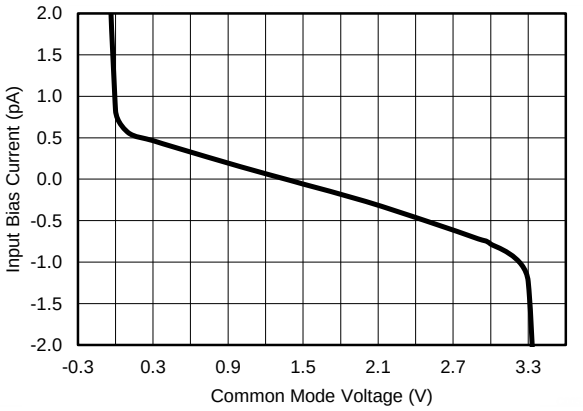


Figure 21. Input Bias Current vs Common Mode Voltage at 3.3 V

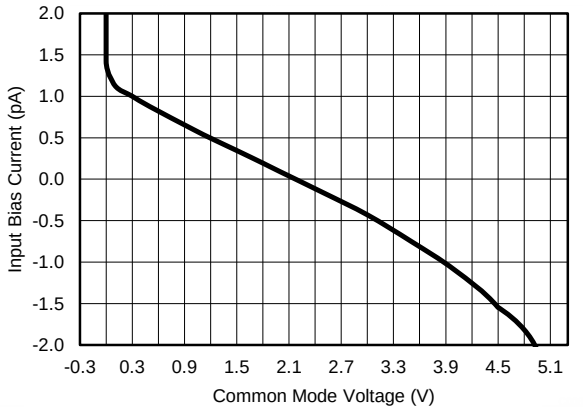


Figure 22. Input Bias Current vs Common Mode Voltage at 5 V

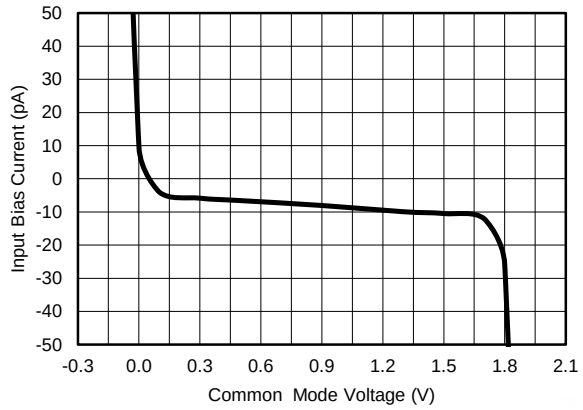


Figure 23. Input Bias Current vs Common Mode Voltage at 1.8 V

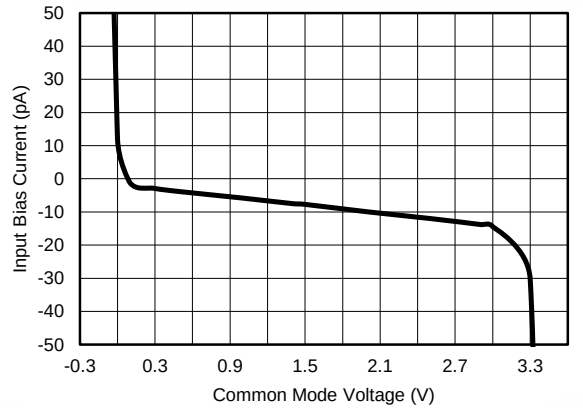
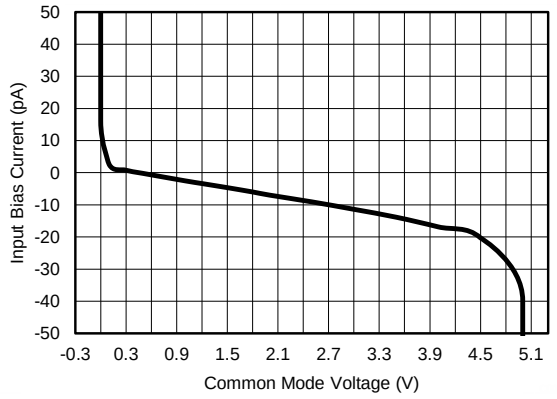


Figure 24. Input Bias Current vs Common Mode Voltage at 3.3 V

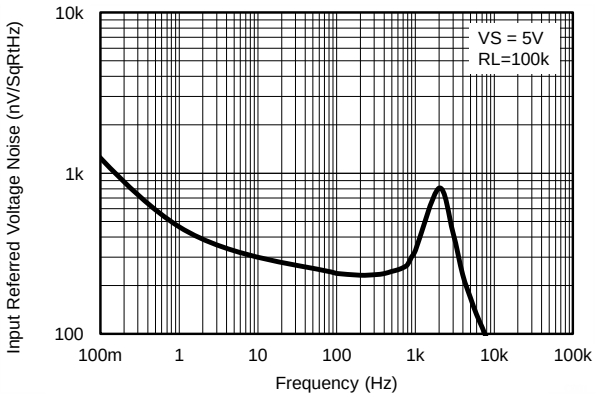
Typical Characteristics (continued)

T_A = 25 °C, V_S = 5 V, V_{OUT} = V_{CM} = V_S/2, R_{LOAD} = 1 MΩ connected to V_S/2, and C_L = 20 pF, unless otherwise noted.



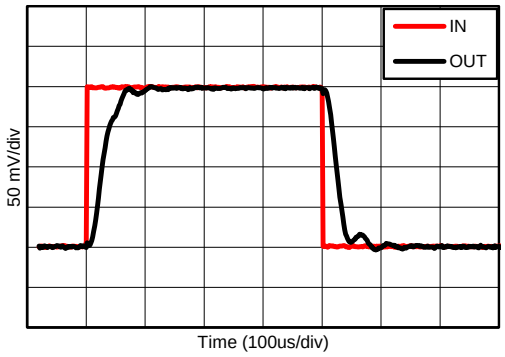
V_S = 5 V T_A = 125°C C_L = 20 pF

Figure 25. Input Bias Current vs Common Mode Voltage at 5 V



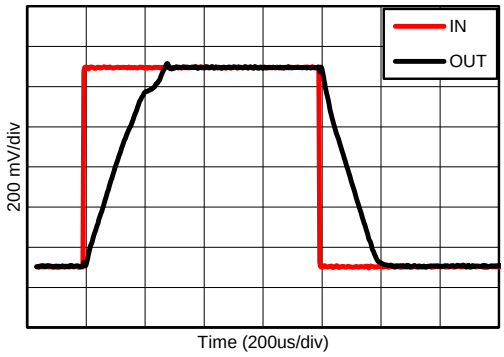
V_S = 5 V R_L = 100 kΩ C_L = 20 pF

Figure 26. Input Referred Voltage Noise



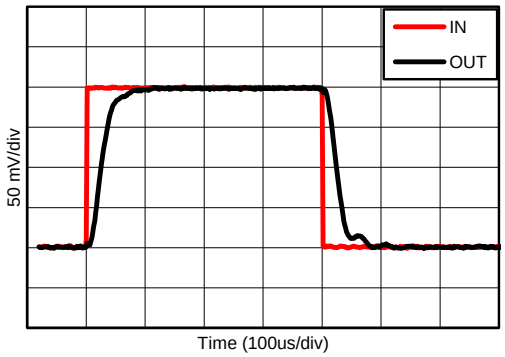
V_S = ±0.9 V R_L = 10 MΩ C_L = 20 pF
G = +1 V_{IN} = ±100 mV

Figure 27. Pulse Response, 200mVpp at 1.8 V



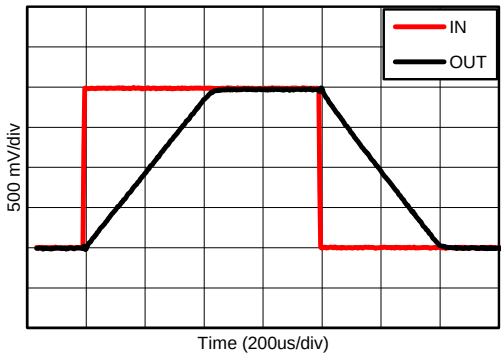
V_S = ±0.9 V R_L = 10 MΩ C_L = 20 pF
G = +1 V_{IN} = ±500mV

Figure 28. Pulse Response, 1Vpp at 1.8V



V_S = ±2.5 V R_L = 10 MΩ C_L = 20 pF
G = +1 V_{IN} = ±100 mV

Figure 29. Pulse Response, 200mVpp at 5V

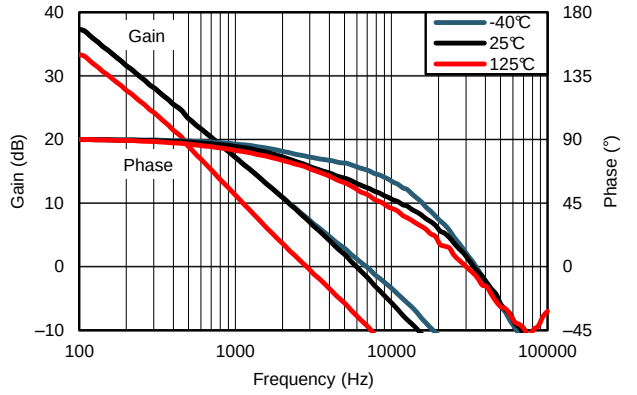


V_S = ±2.5 V R_L = 10 MΩ C_L = 20 pF
G = +1 V_{IN} = ±1V

Figure 30. Pulse Response, 2Vpp at 5V

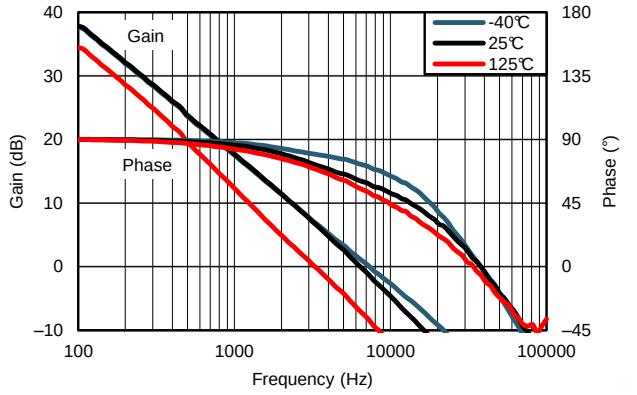
Typical Characteristics (continued)

T_A = 25 °C, V_S = 5 V, V_{OUT} = V_{CM} = V_S/2, R_{LOAD} = 1 MΩ connected to V_S/2, and C_L = 20 pF, unless otherwise noted.



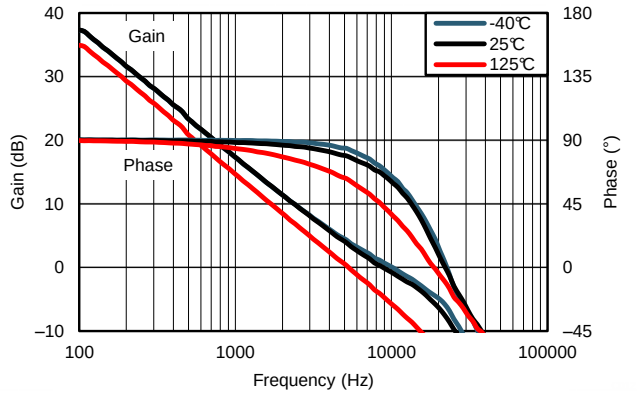
V_S = 1.8 V R_L = 100 kΩ C_L = 20 pF

Figure 31. Gain and Phase vs Temperature at 1.8 V



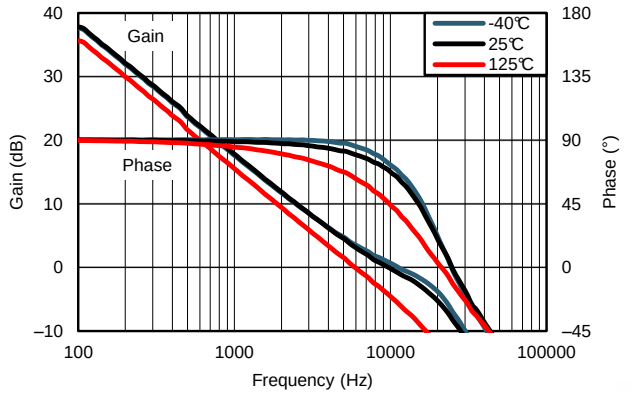
V_S = 5 V R_L = 100 kΩ C_L = 20 pF

Figure 32. Gain and Phase vs Temperature at 5 V



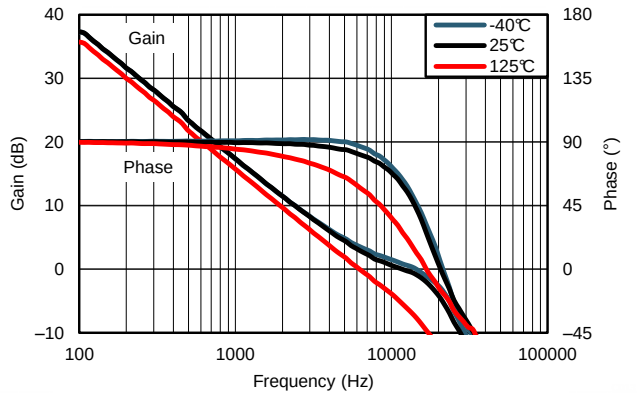
V_S = 1.8 V R_L = 1 MΩ C_L = 20 pF

Figure 33. Gain and Phase vs Temperature at 1.8 V



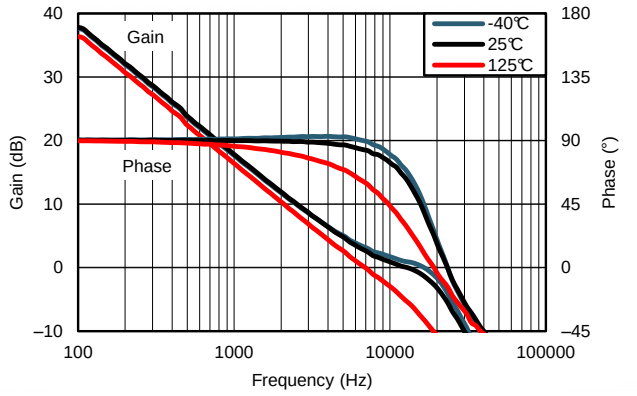
V_S = 5 V R_L = 1 MΩ C_L = 20 pF

Figure 34. Gain and Phase vs Temperature at 5 V



V_S = 1.8 V R_L = 10 MΩ C_L = 20 pF

Figure 35. Gain and Phase vs Temperature at 1.8 V



V_S = 5 V R_L = 10 MΩ C_L = 20 pF

Figure 36. Gain and Phase vs Temperature at 5 V

7 Detailed Description

7.1 Overview

The LPV542 dual op amplifier is unity-gain stable and can operate on a single supply, making it highly versatile and easy to use.

The LPV542 is fully specified and tested from 1.6 V to 5.5 V. Parameters that vary significantly with operating voltages or temperature are shown in the *Typical Characteristics* curves.

7.2 Functional Block Diagram

7.3 Feature Description

The amplifier's differential inputs consist of a non-inverting input (+IN) and an inverting input (–IN). The amplifer amplifies only the difference in voltage between the two inputs, which is called the differential input voltage. The output voltage of the op-amp V_{OUT} is given by Equation 1:

$$V_{OUT} = A_{OL} (IN^+ – IN^–) \quad (1)$$

where

- A_{OL} is the open-loop gain of the amplifier, typically around 100 dB (100,000x, or 100,000 Volts per microvolt).

7.4 Device Functional Modes

7.4.1 Rail-To-Rail Input

The input common-mode voltage range of the LPV542 extends to the supply rails. This is achieved with a complementary input stage — an N-channel input differential pair in parallel with a P-channel differential pair. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 800 mV to 200 mV above the positive supply, while the P-channel pair is on for inputs from 300 mV below the negative supply to approximately (V+) – 800 mV. There is a small transition region, typically (V+) – 1.2 V to (V+) – 0.8 V, in which both pairs are on. This 400 mV transition region can vary 200 mV with process variation. Within the 400 mV transition region PSRR, CMRR, offset voltage, offset drift, and THD may be degraded compared to operation outside this region.

7.4.2 Supply Current Changes over Common Mode

Because of the ultra-low supply current, changes in common mode voltages will cause a noticeable change in the supply current as the input stages transition through the transition region, as shown in Figure 37 below.

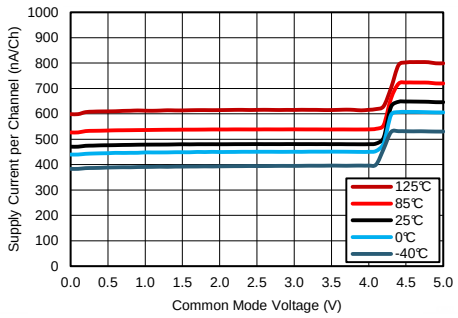


Figure 37. Supply Current Change over Common Mode at 5 V

For the lowest supply current operation, keep the input common mode range between V- and 1 V below V+.

Device Functional Modes (continued)

7.4.3 Design Optimization With Rail-To-Rail Input

In most applications, operation is within the range of only one differential pair. However, some applications can subject the amplifier to a common-mode signal in the transition region. Under this condition, the inherent mismatch between the two differential pairs may lead to degradation of the CMRR and THD. The unity-gain buffer configuration is the most problematic as it will traverse through the transition region if a sufficiently wide input swing is required.

7.4.4 Design Optimization for Nanopower Operation

When designing for ultralow power, choose system components carefully. To minimize current consumption, select large-value resistors. Any resistors will react with stray capacitance in the circuit and the input capacitance of the operational amplifier. These parasitic RC combinations can affect the stability of the overall system. A feedback capacitor may be required to assure stability and limit overshoot or gain peaking.

When possible, use AC coupling and AC feedback to reduce static current draw through the feedback elements. Use film or ceramic capacitors since large electolytics may have static leakage currents in the tens to hundreds of nanoamps.

7.4.5 Common-Mode Rejection

The CMRR for the LPV542 is specified in two ways so the best match for a given application may be used. First, the CMRR of the device in the common-mode range below the transition region (V_{CM} < (V+) – 0.9 V) is given. This specification is the best indicator of the capability of the device when the application requires use of one of the differential input pairs. Second, the CMRR at V_S = 5 V over the entire common-mode range is specified.

7.4.6 Output Stage

The LPV542 output voltage swings 3 mV from rails at 3.3 V supply, which provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

The LPV542 Maximum Output Voltage Swing defines the maximum swing possible under a particular output load.

7.4.7 Driving Capacitive Load

The LPV542 is internally compensated for stable unity gain operation, with a 8 kHz typical gain bandwidth. However, the unity gain follower is the most sensitive configuration to capacitive load. The combination of a capacitive load placed directly on the output of an amplifier along with the amplifier's output impedance creates a phase lag, which reduces the phase margin of the amplifier. If the phase margin is significantly reduced, the response will be under damped which causes peaking in the transfer and, when there is too much peaking, the op amp might start oscillating.

In order to drive heavy (>50pF) capacitive loads, an isolation resistor, R_{ISO}, should be used, as shown in Figure 38. By using this isolation resistor, the capacitive load is isolated from the amplifier's output. The larger the value of R_{ISO}, the more stable the amplifier will be. If the value of R_{ISO} is sufficiently large, the feedback loop will be stable, independent of the value of C_L. However, larger values of R_{ISO} result in reduced output swing and reduced output current drive.

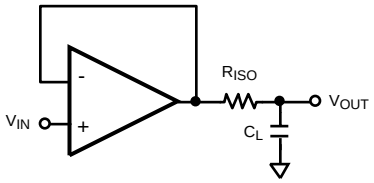


Figure 38. Resistive Isolation Of Capacitive Load

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LPV542 is a ultra-low power operational amplifier that provides 8 kHz bandwidth with only 490nA quiescent current, and near precision offset and drift specifications at a low cost. These rail-to-rail input and output amplifiers are specifically designed for battery-powered applications. The input common-mode voltage range extends to the power-supply rails and the output swings to within millivolts of the rails, maintaining a wide dynamic range.

8.2 Typical Application: 60 Hz Twin "T" Notch Filter

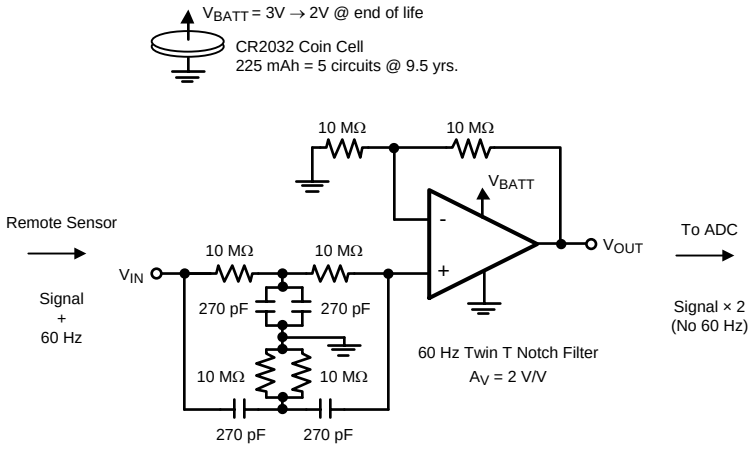


Figure 39. 60 Hz Notch Filter

8.2.1 Design Requirements

Small signals from transducers in remote and distributed sensing applications commonly suffer strong 60 Hz interference from AC power lines. The circuit of Figure 39 notches out the 60 Hz and provides a gain A_V = 2 for the sensor signal represented by a 1 kHz sine wave. Similar stages may be cascaded to remove 2nd and 3rd harmonics of 60 Hz. Thanks to the nA power consumption of the LPV542, even 5 such circuits can run for 9.5 years from a small CR2032 lithium cell. These batteries have a nominal voltage of 3 V and an end of life voltage of 2 V. With an operating voltage from 1.6 V to 5.5 V the LPV542 can function over this voltage range.

8.2.2 Detailed Design Procedure

The notch frequency is set by:

$$F_0 = 1 / 2\pi RC. \quad (2)$$

To achieve a 60 Hz notch use R = 10 MΩ and C = 270 pF. If eliminating 50 Hz noise, which is common in European systems, use R = 11.8 MΩ and C = 270 pF.

The Twin T Notch Filter works by having two separate paths from V_{IN} to the amplifier's input. A low frequency path through the series input resistors and another separate high frequency path through the series input capacitors. However, at frequencies around the notch frequency, the two paths have opposing phase angles and the two signals will tend to cancel at the amplifier's input.

Typical Application: 60 Hz Twin "T" Notch Filter (continued)

To ensure that the target center frequency is achieved and to maximize the notch depth (Q factor) the filter needs to be as balanced as possible. To obtain circuit balance, while overcoming limitations of available standard resistor and capacitor values, use passives in parallel to achieve the 2C and R/2 circuit requirements for the filter components that connect to ground.

To make sure passive component values stay as expected clean board with alcohol, rinse with deionized water, and air dry. Make sure board remains in a relatively low humidity environment to minimize moisture which may increase the conductivity of board components. Also large resistors come with considerable parasitic stray capacitance which effects can be reduced by cutting out the ground plane below components of concern.

Large resistors are used in the feedback network to minimize battery drain. When designing with large resistors, resistor thermal noise, op amp current noise, as well as op amp voltage noise, must be considered in the noise analysis of the circuit. The noise analysis for the circuit in Figure 39 can be done over a bandwidth of 2 kHz, which takes the conservative approach of overestimating the bandwidth (LPV542 typical GBW/A_V is lower). The total noise at the output is approximately 800 µVpp, which is excellent considering the total consumption of the circuit is only 900 nA. The dominant noise terms are op amp voltage noise , current noise through the feedback network (430 µVpp), and current noise through the notch filter network (280 µVpp). Thus the total circuit's noise is below 1/2 LSB of a 10-bit system with a 2 V reference, which is 1 mV.

8.2.3 Application Curve

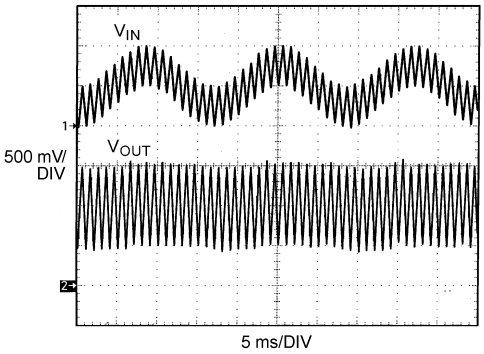


Figure 40. 60 Hz Notch Filter Waveform

8.3 Do's and Don'ts

Do properly bypass the power supplies.

Do add series resistance to the output when driving capacitive loads, particularly cables, Muxes and ADC inputs.

Do add series current limiting resistors and external schottky clamp diodes if input voltage is expected to exceed the supplies. Limit the current to 1 mA or less (1 KΩ per volt).

9 Power Supply Recommendations

The LPV542 is specified for operation from 1.6 V to 5.5 V (±0.8 V to ±2.75 V) over a –40°C to 125°C temperature range. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

CAUTION

Supply voltages larger than 6 V can permanently damage the device.

For proper operation, the power supplies bust be properly decoupled. For decoupling the supply lines it is suggested that 10 nF capacitors be placed as close as possible to the operational amplifier power supply pins. For single supply, place a capacitor between V^+ and $V^–$ supply leads. For dual supplies, place one capacitor between V^+ and ground, and one capacitor between $V^–$ and ground.

Low bandwidth nanopower devices do not have good high frequency (> 1 kHz) AC PSRR rejection against high-frequency switching supplies and other 1 kHz and above noise sources, so extra supply filtering is recommended if kilohertz or above noise is expected on the power supply lines.

10 Layout

10.1 Layout Guidelines

The V+ pin should be bypassed to ground with a low ESR capacitor.

The optimum placement is closest to the V+ and ground pins.

Care should be taken to minimize the loop area formed by the bypass capacitor connection between V+ and ground.

The ground pin should be connected to the PCB ground plane at the pin of the device.

The feedback components should be placed as close to the device as possible to minimize strays.

There is an internal electrical connection between the exposed Die Attach Pad (DAP) and the V- pin. For best performance the DAP should be connected to the exact same potential as the V- pin. Do not use the DAP as the primary V- supply. Floating the DAP pad is not recommended. The DAP and V- pin should be joined directly as shown in the *Layout Example*.

10.2 Layout Example

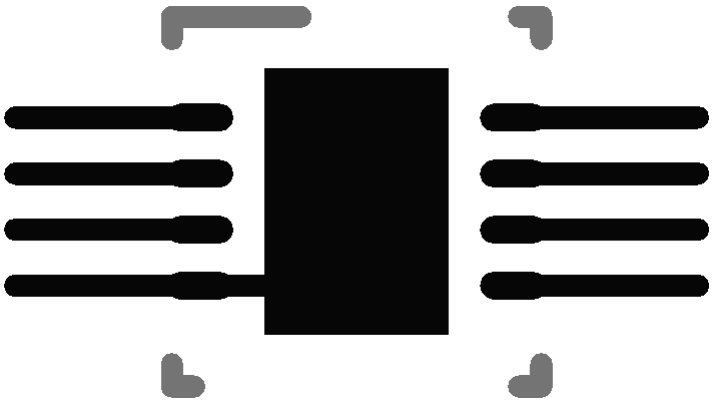


Figure 41. X1SON Layout Example (top view)

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

TINA-TI SPICE-Based Analog Simulation Program, http://www.ti.com/tool/tina-ti

DIP Adapter Evaluation Module, http://www.ti.com/tool/dip-adapter-evm

TI Universal Operational Amplifier Evaluation Module, http://www.ti.com/tool/opampevm

TI FilterPro Filter Design software, http://www.ti.com/tool/filterpro

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

- AN-1798 Designing with Electro-Chemical Sensors, SNOA514
- AN-1803 Design Considerations for a Transimpedance Amplifier, SNOA515
- AN-1852 Designing With pH Electrodes, SNOA529
- Compensate Transimpedance Amplifiers Intuitively, SBOA055
- Transimpedance Considerations for High-Speed Operational Amplifiers, SBOA112
- Noise Analysis of FET Transimpedance Amplifiers, SBOA060
- Circuit Board Layout Techniques, SLOA089
- Handbook of Operational Amplifier Applications, SBOA092

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LPV542DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(LP, V542)	Samples
LPV542DGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(LP, V542)	Samples
LPV542DNXR	ACTIVE	X1SON	DNX	8	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	LPV542	Samples
LPV542DNXT	ACTIVE	X1SON	DNX	8	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	LPV542	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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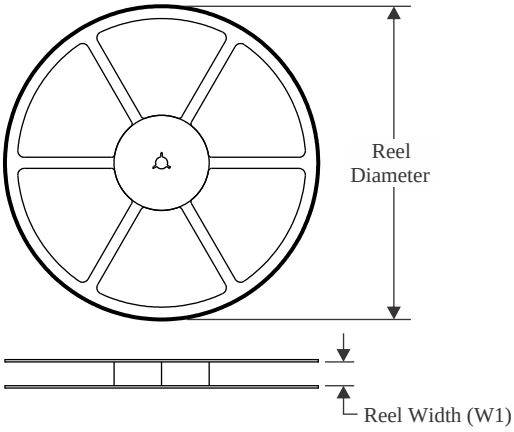
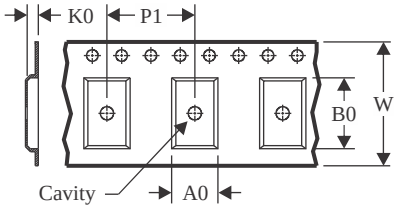
TAPE AND REEL INFORMATION

REEL DIMENSIONS

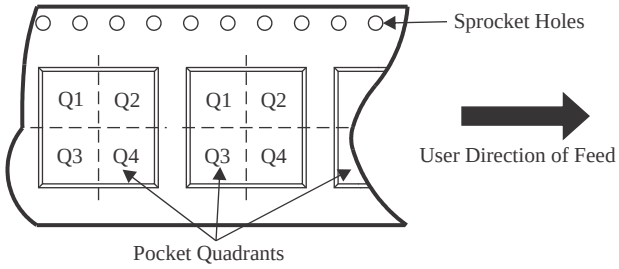


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

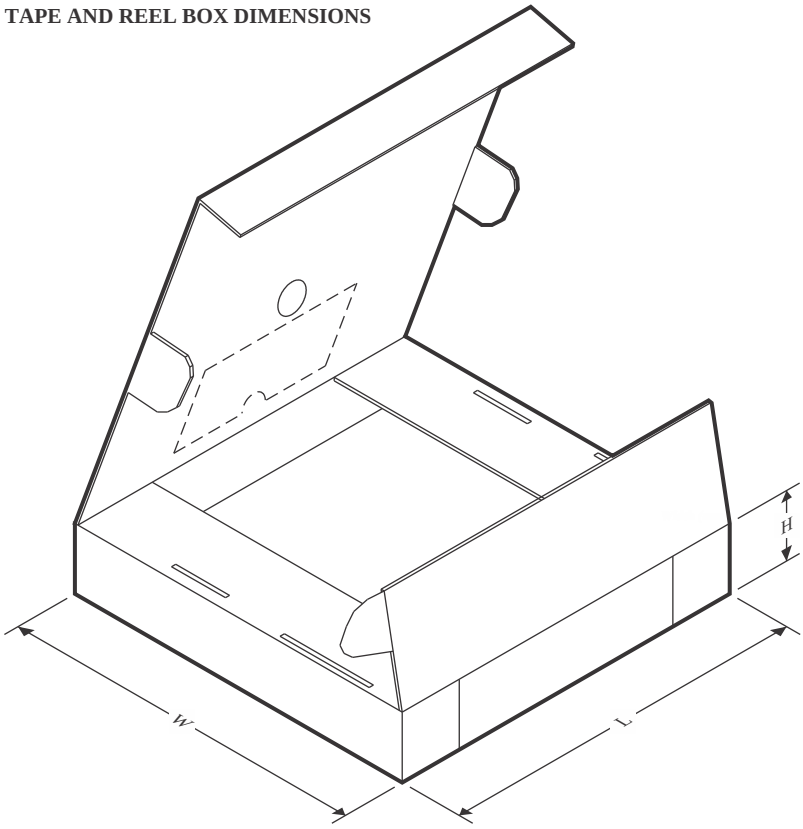
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LPV542DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LPV542DGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LPV542DNXR	X1SON	DNX	8	3000	330.0	12.4	3.3	3.3	0.7	8.0	12.0	Q1
LPV542DNXT	X1SON	DNX	8	250	180.0	12.5	3.3	3.3	0.7	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

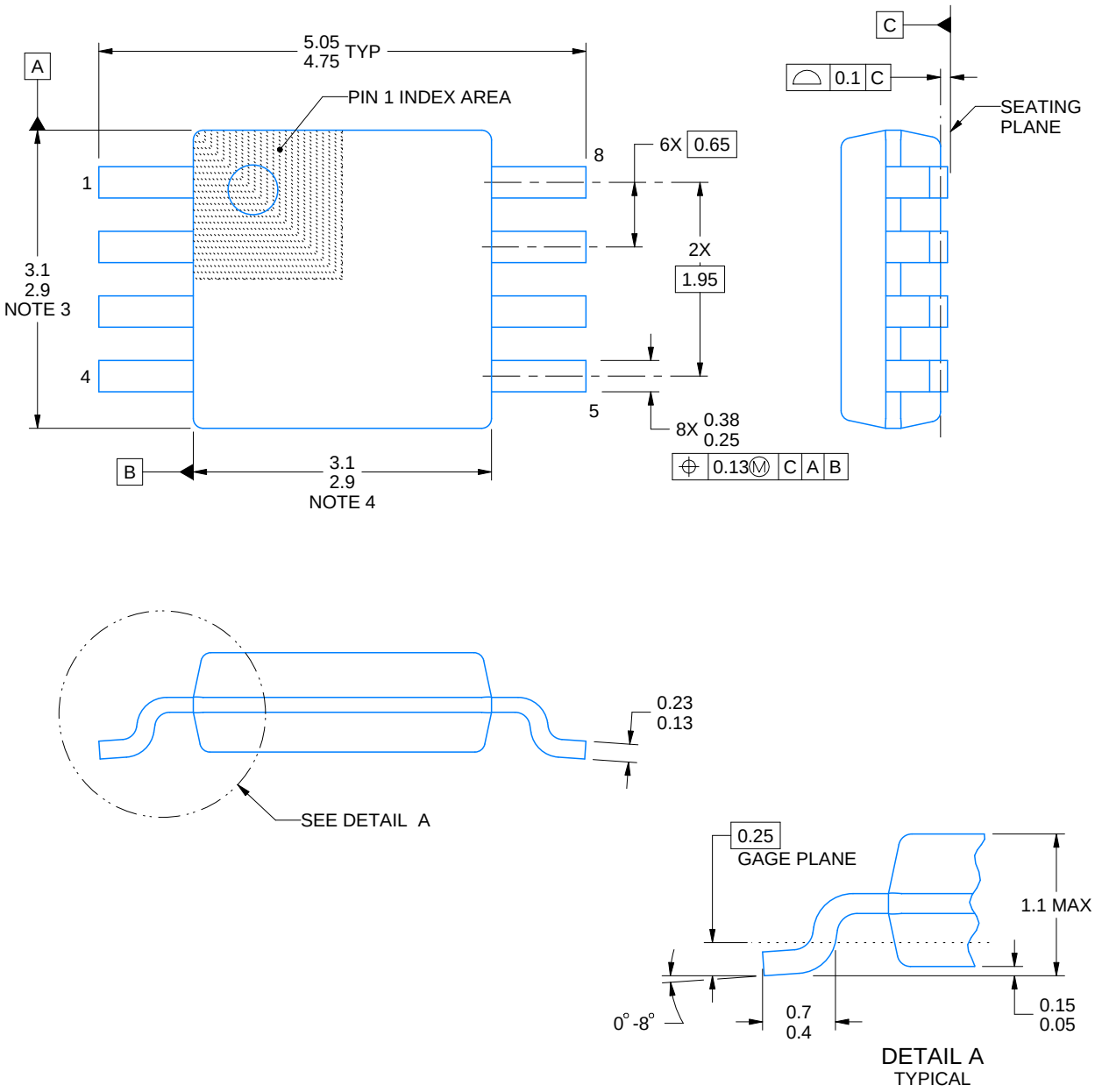
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LPV542DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
LPV542DGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
LPV542DNXR	X1SON	DNX	8	3000	338.0	355.0	50.0
LPV542DNXT	X1SON	DNX	8	250	338.0	355.0	50.0

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

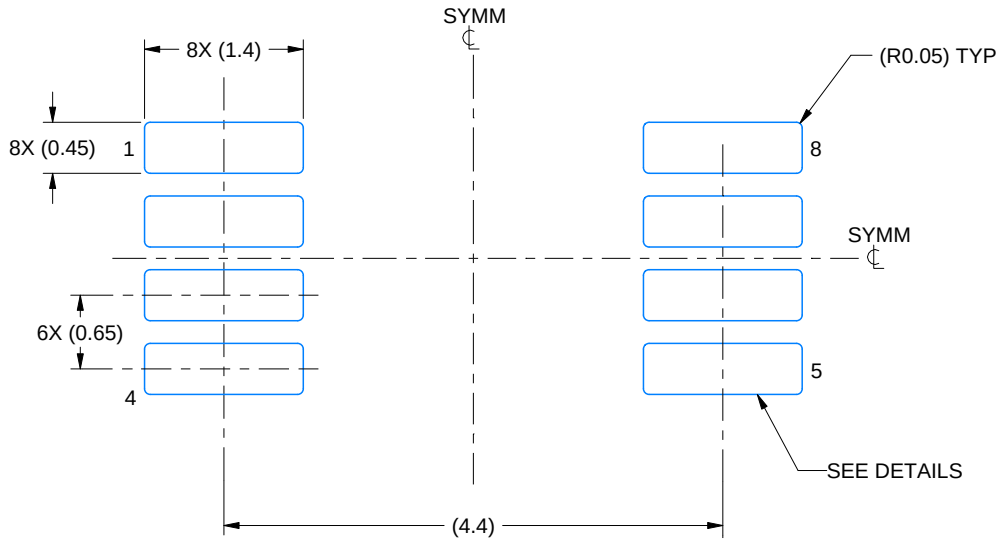
SMALL OUTLINE PACKAGE



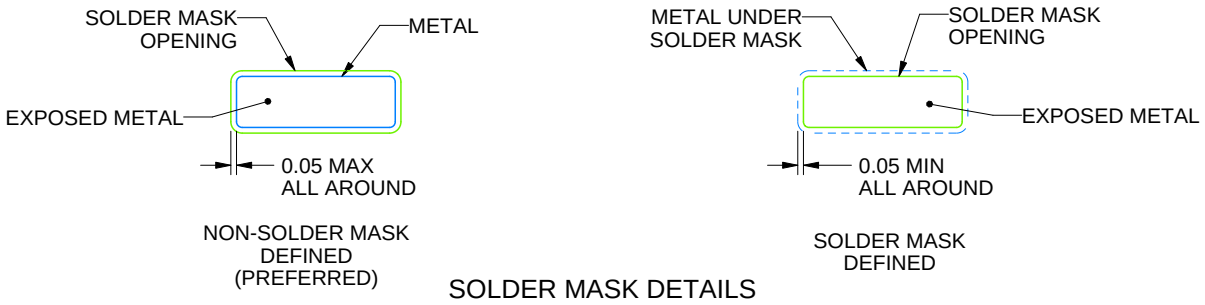
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

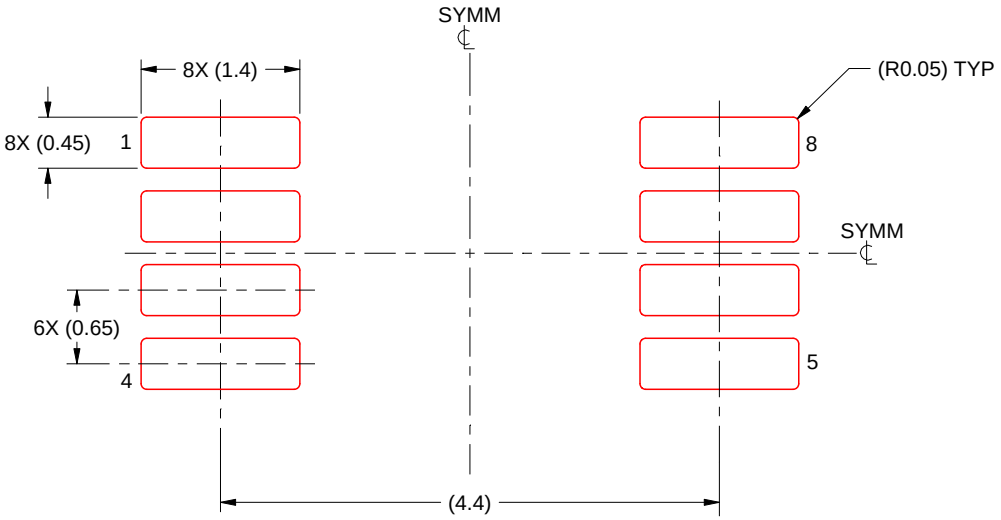


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

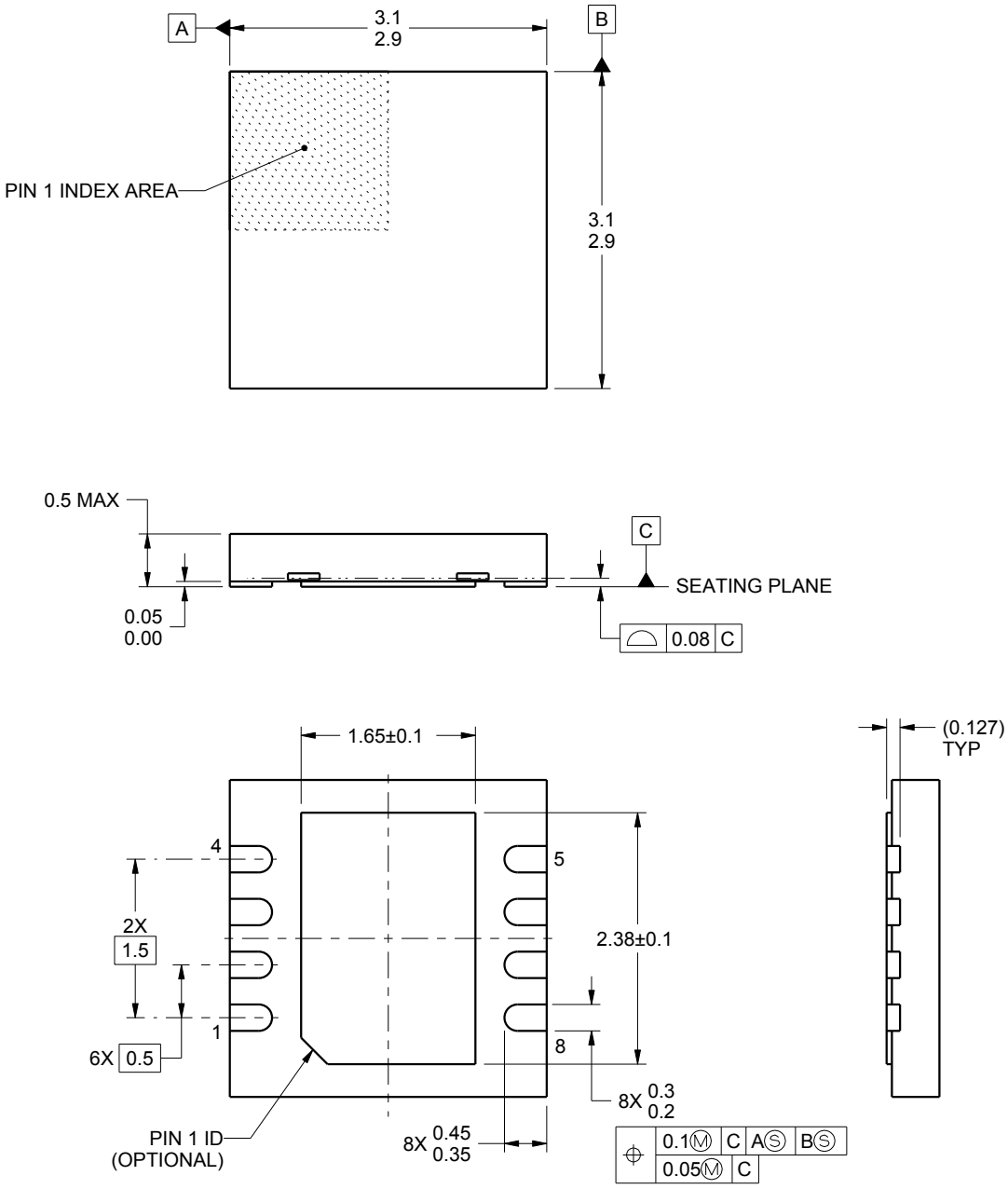
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DNX0008A

X1SON - 0.5 mm max height

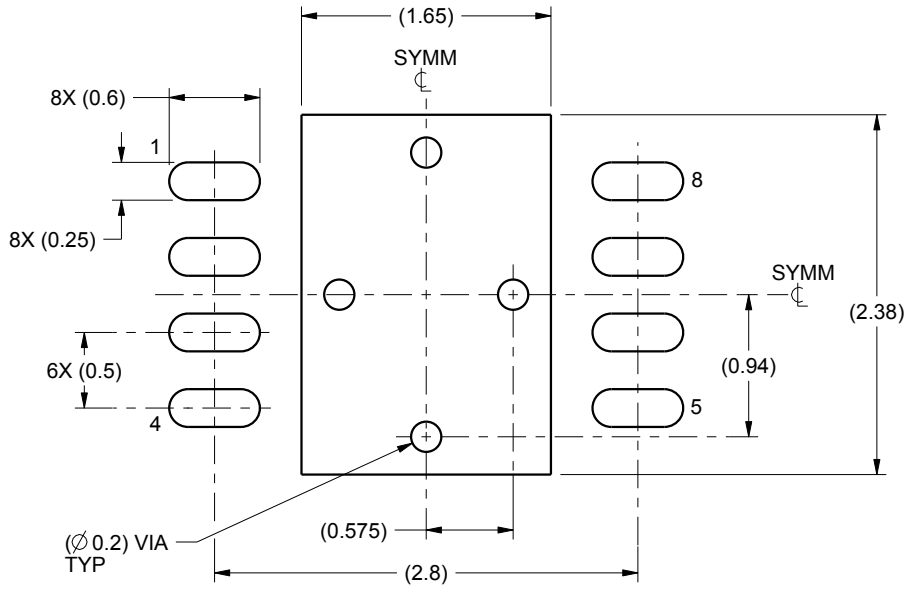
PLASTIC SMALL OUTLINE - NO LEAD



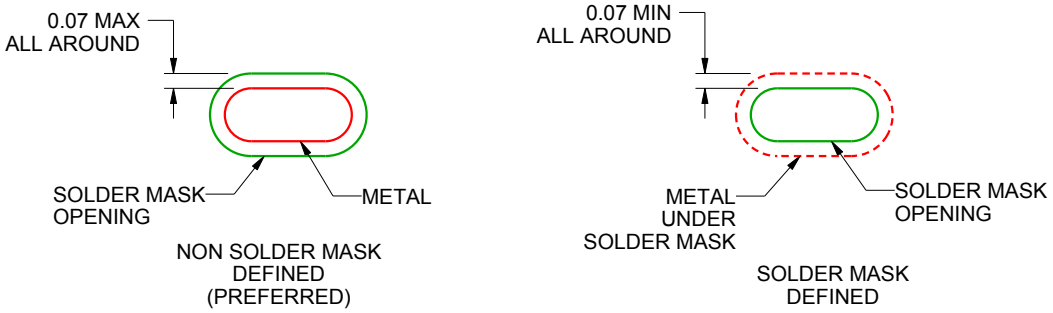
4221623/A 08/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

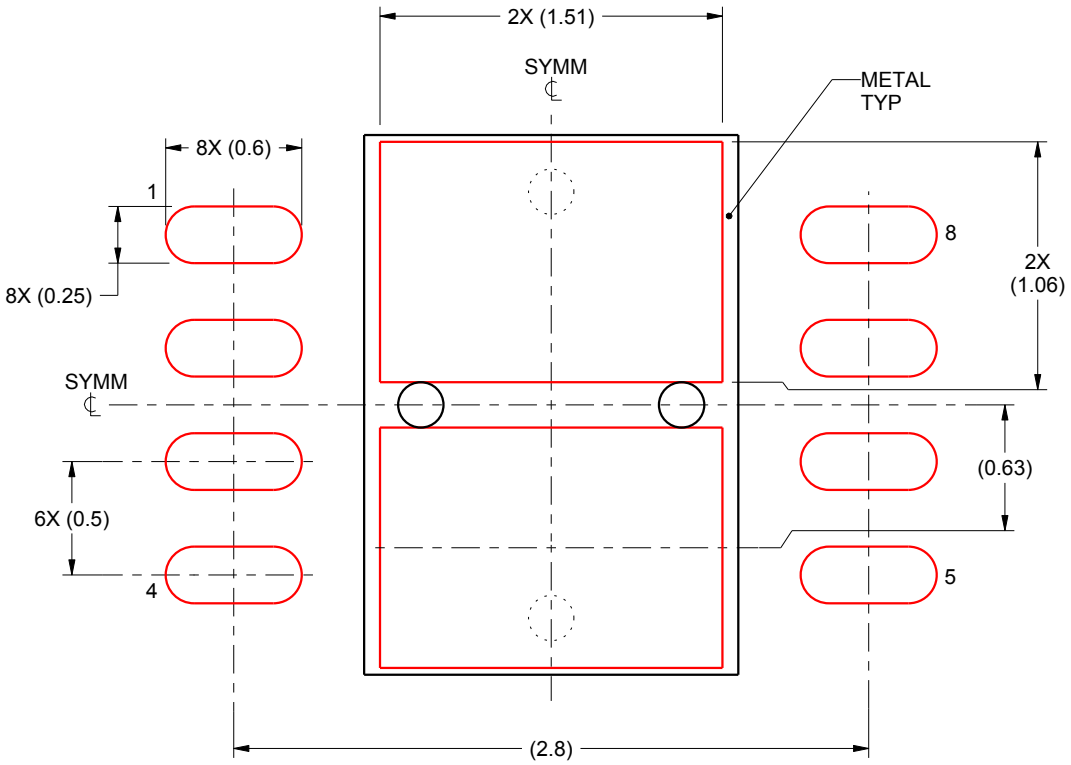


SOLDER MASK DETAILS

4221623/A 08/2014

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
82% PRINTED SOLDER COVERAGE BY AREA
SCALE:30X

4221623/A 08/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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