TWO-CHANNEL AUTOMOTIVE DIGITAL AMPLIFIER

Check for Samples: TAS5412-Q1

FEATURES

- **TAS5412-Q1 - Single-Ended Input**
- **2-Channel Digital Power Amplifier**
- **2 Analog Inputs, 2 BTL Power Outputs**
- **Typical Output Power per Channel at 10%**
  - **28 Watts/Ch, Into 4 Ω at 14.4 VDC**
  - **46 Watts/Ch, Into 2 Ω at 14.4 VDC**
  - **79 Watts/Ch, Into 4 Ω at 24 VDC**
  - **150 Watts Into 2 Ω at 24 VDC PBTL**
  - **90 Watts Into 1 Ω at 14.4 VDC PBTL**
- **THD+N < 0.02%, 1 kHz, 1 W Into 4 Ω**
- **Patented Pop- and Click-Reduction Technology**
- **Patented AM Interference Avoidance**
- **Patented Cycle-by-Cycle Current Limit**
- **75-dB PSRR**
- **Four-Address I^2C Serial Interface for Device Configuration and Control**
- **Channel Gains: 12 dB, 20 dB, 26 dB, 32 dB**
- **Load Diagnostic Functions:**
  - **Output Open and Shorted Load**
  - **Output-to-Power and -to-Ground Shorts**
  - **Patented Tweeter Detection**
- **Protection and Monitoring Functions:**
  - **Short-Circuit Protection**
  - **50-V Load-Dump Protection**
  - **Fortuitous Open-Ground and -Power Tolerant**
  - **Patented Output DC Level Detection While Music Is Playing**
  - **Overtemperature Protection**
  - **Over- and Undervoltage Protection**
  - **Clip Detection**
- **TAS5412-Q1 - 64-Pin QFP (PHD) PowerPAD™ Surface-Mount Package**
- **Pin Compatible With 4-Channel Devices**
- **Designed for Automotive EMC Requirements**
- **Will Be Qualified According to AEC-Q100**
- **ISO9000:2002 TS16949 Certified**
- **–40 to 105°C Ambient Temperature Range**

APPLICATIONS

- **Radio Head Units**
- **External Amplifiers**

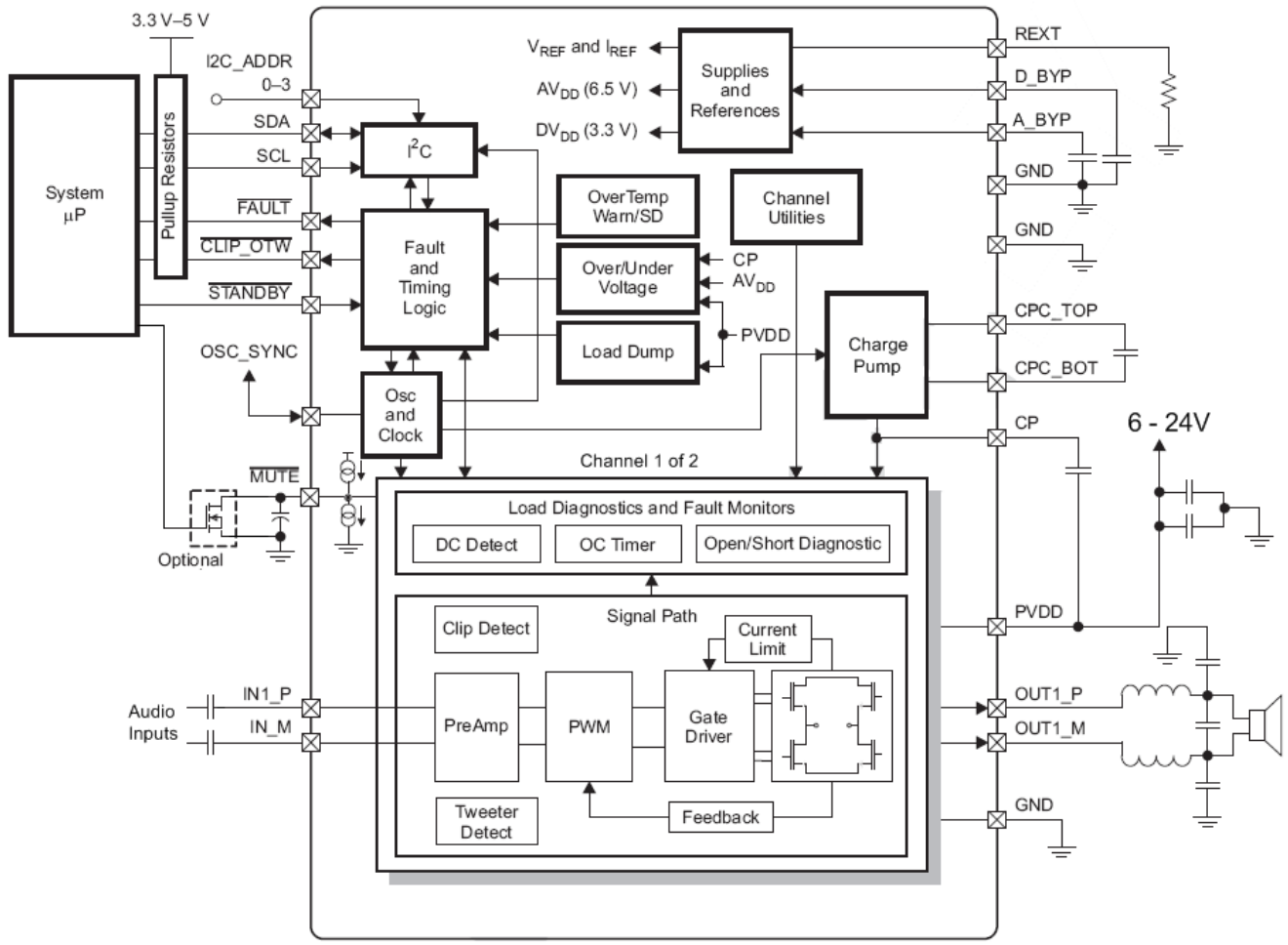
DESCRIPTION

The device is a two-channel digital audio amplifier designed for use in automotive head units and external amplifiers. It provides two channels at 28 W into 4 Ω at 10% THD+N from 14.4 V or 46 W into 2 Ω at 10% THD+N. The digital PWM topology provides dramatic improvements in efficiency over traditional linear amplifier solutions. This reduces the power dissipated by the amplifier by a factor of ten under typical music playback conditions. The device incorporates a patented PWM design that provides excellent power-supply rejection in the harsh electrical environment common in automotive applications. Applications attain high efficiency without the need for complicated power supply schemes. The design allows synchronization of multiple devices.

The device incorporates all the functionality needed to perform in the demanding OEM applications area, including load diagnostic functions for detecting and diagnosing misconnected outputs.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

TAS5412-Q1 FUNCTIONAL BLOCK DIAGRAM



PIN ASSIGNMENTS AND FUNCTIONS

The pin assignments are as follows:

TAS5412-Q1
PHD Package
(Top View)

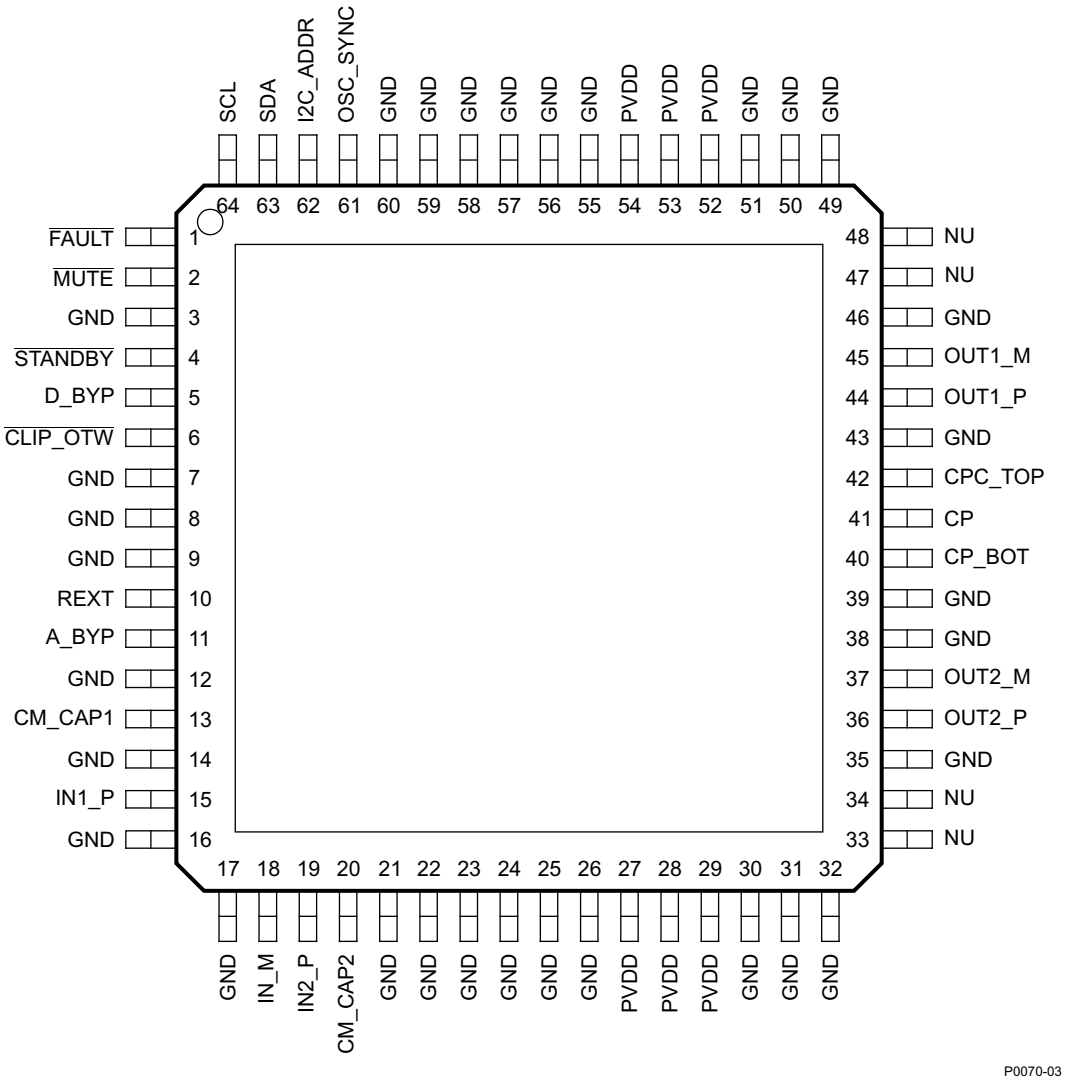


Table 1. TERMINAL FUNCTIONS

TERMINAL		TYPE	DESCRIPTION
NAME	NO.		
A_BYP	11	PBY	Bypass pin for the AVDD analog regulator
$\overline{\text{CLIP\_OTW}}$	6	DO	Reports clip detect, tweeter detection, and overtemperature warning with open-drain output
CM_CAP1	13	AI	Common mode capacitor
CM_CAP2	20	AI	Common mode capacitor
CP	41	CP	Top of main storage capacitor for charge pump
CPC_BOT	40	CP	Bottom of flying capacitor for charge pump
CPC_TOP	42	CP	Top of flying capacitor for charge pump
D_BYP	5	PBY	Bypass pin for DVDD regulator output
$\overline{\text{FAULT}}$	1	DO	Global fault output (open-drain): UV, OV, OTSD, OCSD, dc

Table 1. TERMINAL FUNCTIONS (continued)

TERMINAL		TYPE	DESCRIPTION
NAME	NO.		
GND	3, 7-9, 12,14, 16, 17, 21–26, 30–32, 35, 38, 39, 43, 49–51, 55–60	GND	Ground
I2C_ADDR	62	AI	I^2C address bit
IN1_P	15	AI	Non-inverting analog input for channel 1
IN2_P	19	AI	Non-inverting analog input for channel 2
IN_M	18	ARTN	Signal return for both analog channel inputs
$\overline{\text{MUTE}}$	2	DI	Gain-ramp control
NU	33, 34, 47, 48	NC	No connect, do not connect to ground
OSC_SYNC	61	DI, DO	Oscillator input from master or output to slave amplifiers
OUT1_M	45	PO	– polarity output for bridge 1
OUT1_P	44	PO	+ polarity output for bridge 1
OUT2_M	37	PO	– polarity output for bridge 2
OUT2_P	36	PO	+ polarity output for bridge 2
PVDD	27–29, 52–54	PWR	PVDD supply
REXT	10	AI	Precision resistor pin to set analog reference
SCL	64	DI	I^2C clock input from system I^2C master
SDA	63	DI, DO	I^2C data I/O for communication with system I^2C master
$\overline{\text{STANDBY}}$	4	DI	Active-low STANDBY pin. Standby (low), power up (high)

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

			VALUE	UNIT
PVDD	DC supply voltage range	Relative to GND	–0.3 to 30	V
$PVDD_{MAX}$	Pulsed supply-voltage range	t ≤ 400 ms exposure	–1 to 50	V
$PVDD_{RAMP}$	Supply-voltage ramp rate		15	V/ms
I_{PVDD}	Externally imposed dc supply current per PVDD or GND pin		±12	A
I_{PVDD_MAX}	Pulsed supply current per PVDD pin (one shot)	t < 100 ms	17	A
I_O	Maximum allowed dc current per output pin		±13.5	A
I_{O_MAX} (1)	Pulsed output current per output pin (single pulse)	t < 100 ms	±17	A
I_{IN_MAX}	Maximum current, all digital and analog input pins (2)	DC or pulsed	±1	mA
I_{MUTE_MAX}	Maximum current on $\overline{\text{MUTE}}$ pin	DC or pulsed	±20	mA
I_{IN_ODMAX}	Maximum sinking current for open-drain pins		7	mA
V_{LOGIC}	Input voltage range for logic pin relative to GND (SCL and SDA pins)		–0.3 to 6	V
V_{I2C_ADDR}	Input voltage range for I2C_ADDR pin relative to GND		–0.3 to 6	V
$V_{STANDBY}$	Input voltage range for $\overline{\text{STANDBY}}$ pin		–0.3 to 5.5	V
V_{OSC_SYNC}	Input voltage range for OSC_SYNC pin relative to GND		–0.3 to 3.6	V
$V_{AIN\_AC\_MAX\_5412}$	Maximum ac-coupled input voltage(2), analog input pins		1.9	Vrms
V_{GND}	Maximum voltage between GND pins		±0.3	V
T_J	Maximum operating junction temperature range		–55 to 150	°C
T_{stg}	Storage temperature range		–55 to 150	°C

(1) Pulsed-current ratings are maximum survivable currents externally applied to the TAS5412-Q1. Reverse-battery, fortuitous open-ground, and fortuitous open-supply fault conditions may result in high currents.
(2) See *Application Information* section for information on analog input voltage and ac coupling.

THERMAL CHARACTERISTICS

PARAMETER		VALUE (Typical)	UNIT
$R_{\theta JC}$	Junction-to-case (heat slug) thermal resistance	1.7	°C/W
	Exposed pad dimensions	8 × 8	mm

ELECTROSTATIC DISCHARGE (ESD)

PARAMETER	PINS	VALUE (Typical)	UNIT
Human-body model (HBM) AEC-Q100-002	ALL	3000	V
Charged-device model (CDM) AEC-Q100-011	Corner pins excluding SCL	750	
	All pins (including SCL) except CP and CP_TOP	600	
	CP and CP_TOP pins	400	
Machine model (MM) AEC-Q100-003	All	100	

RECOMMENDED OPERATING CONDITIONS (1)

			MIN	NOM	MAX	UNIT
$PVDD_{OP}$	DC supply voltage range relative to GND		6	14.4	24	V
$PVDD_{I2C}$	DC supply voltage range for I^2C reporting		5	14.4	26.5	V
V_{AIN_5412} (2)	Analog audio input signal level	AC-coupled input voltage	0		0.25–1 (3)	Vrms
T_A	Ambient temperature		–40		105	°C
T_J	Junction temperature	An adequate heat sink is required to keep T_J within specified range.	–40		115	°C
R_L	Nominal speaker load impedance		2	4		Ω
V_{PU}	Pullup voltage supply (for open-drain logic outputs)		3	3.3 or 5	5.5	V
R_{PU_EXT}	External pullup resistor on open-drain logic outputs	Resistor connected between open-drain logic output and V_{PU} supply	10	47	100	kΩ
R_{PU_I2C}	I^2C pullup resistance on SDA and SCL pins		1	4.7	10	kΩ
R_{I2C_ADD}	Total resistance of voltage divider for I^2C address slave 1 or slave 2, connected between D_BYP and GND pins		10		100	kΩ
R_{REXT}	External resistance on REXT pin	1% tolerance required	19.8	20	20.2	kΩ
C_{D_BYP}, C_{A_BYP}	External capacitance on D_BYP and A_BYP pins		10		120	nF
C_{OUT}	External capacitnace to GND on OUT_X pins			150	680	nF
C_{IN}	External capacitance to analog input pin in series with input signal			1		µF
C_{FLY}	Flying capacitor on charge pump		0.47	1	1.5	µF
C_P	Charge-pump capacitor	50 V needed for load dump	0.47	1	1.5	µF
C_{MUTE}	Capacitance on MUTE pin		100	330		nF
$C_{OSCSYNC\_MAX}$	Allowed loading capacitance on OSC_SYNC pin			75		pF

(1) The *Recommended Operating Conditions*table specifies only that the device is functional in the given range. See the *Electrical Characteristics*table for specified performance limits.
(2) Signal input for full unclipped output with gains of 32 dB, 26 dB, 20 dB, and 12 dB
(3) Maximum recommended input voltage is determined by the gain setting.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise noted): T_{Case}= 25°C, PVDD = 14.4 V, R_L= 4 Ω, f_S = 417 kHz, P_{out}= 1 W/ch, Rext = 20 kΩ, AES17 filter, master-mode operation (see application diagram)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERATING CURRENT						
I_{PVDD_IDLE}	PVDD idle current	Both channels in MUTE mode		125	175	mA
I_{PVDD_Hi-Z}		Both channels in Hi-Z mode		60		
I_{PVDD_STBY}	PVDD standby current	STANDBY mode, T_J = 85°C		2	12	µA
OUTPUT POWER						
P_{OUT}	Output power per channel	4 Ω, PVDD = 14.4 V, THD+N = 1%, 1 kHz, T_c= 75°C		23		W
		4 Ω, PVDD = 14.4 V, THD+N = 10%, 1 kHz, T_c= 75°C	25	28		
		4 Ω, PVDD = 24 V, THD+N = 1%, 1 kHz, T_c= 75°C		62		
		4 Ω, PVDD = 24 V, THD+N = 10%, 1 kHz, T_c= 75°C	63	79		
		2 Ω, PVDD = 14.4 V, THD+N = 1%, 1 kHz, T_c= 75°C		38		
		2 Ω, PVDD = 14.4 V, THD+N = 10%, 1 kHz, T_c= 75°C	40	50		
		PBTL 2-Ω operation, PVDD = 24 V, THD+N = 10%, 1 kHz, T_c= 75°C		150		
		PBTL 1-Ω operation, PVDD = 14.4 V, THD+N = 10%, 1 kHz, T_c= 75°C		90		
EFF_P	Power efficiency	2 channels operating, 23-W output power per ch, L = 10 µH, T_J = 85°C		90		%
AUDIO PERFORMANCE						
V_{NOISE}	Noise voltage at output	G = 26 dB, zero input, and A-weighting		60	100	µV
Crosstalk	Channel crosstalk	1 W, G = 26 dB, 1 kHz	60	75		dB
PSRR	Power-supply rejection ratio	G = 26 dB, PVDD = 14.4 Vdc + 1 Vrms, f = 1 kHz	60	75		dB
THD+N	Total harmonic distortion + noise	P = 1 W, G = 26 dB, f = 1 kHz, 0°C = T_J = 75°C		0.02%	0.1%	
f_S	Switching frequency	Switching frequency selectable for AM interference avoidance	336	357	378	kHz
			392	417	442	
			470	500	530	
R_{AIN}	Analog input resistance	Internal shunt resistance on each input pin	63	82	106	kΩ
V_{IN_CM}	Common-mode input voltage	AC-coupled common-mode input voltage (zero differential input)		1.3		Vrms
V_{CM_INT}	Internal common-mode input bias voltage	Internal bias applied to IN_M pin		3.37		V
G	Voltage gain (V_O / V_{IN})	Source impedance = 0 Ω, gain measurement taken at 1 W of power per channel	11	12	13	dB
			19	20	21	
			25	26	27	
			31	32	33	
G_{CH}	Channel-to-channel variation	Any gain commanded	–1	0	1	dB
PWM OUTPUT STAGE						
r_{DSon}	FET drain-to-source resistance	Not including bond-wire resistance, T_J= 25°C		75	95	mΩ
V_{O_OFFSET}	Output offset voltage	Zero input signal, dc offset reduction enabled, and G = 26 dB		±10	±50	mV
PVDD OVERVOLTAGE (OV) PROTECTION						
V_{OV}	PVDD overvoltage shutdown		24.6	26.4	28.2	V
PVDD UNDERVOLTAGE (UV) PROTECTION						
V_{UV_SET}	PVDD undervoltage shutdown		5	5.3	5.6	V
V_{UV_CLEAR}	Recovery voltage for PVDD UV		6.2	6.6	7.2	V
AVDD						
V_{A_BYP}	A_BYP pin voltage			6.5		V
$V_{A\_BYP\_UV\_SET}$	A_BYP UV voltage			3.5		V
$V_{A\_BYP\_UV\_CLEAR}$	Recovery voltage A_BYP UV			4.3		V
DVDD						
V_{D_BYP}	D_BYP pin voltage			3.3		V
POWER-ON RESET (POR)						

ELECTRICAL CHARACTERISTICS (continued)

Test conditions (unless otherwise noted): T_{Case}= 25°C, PVDD = 14.4 V, R_L= 4 Ω, f_S = 417 kHz, P_{out}= 1 W/ch, Rext = 20 kΩ, AES17 filter, master-mode operation (see application diagram)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{POR}	Maximum PVDD voltage for POR; I^2C active above this voltage				4	V
V_{POR_HY}	PVDD recovery hysteresis voltage for POR			0.1		V
REXT						
V_{REXT}	Rext pin voltage			1.27		V
CHARGE PUMP (CP)						
V_{CPUV_SET}	CP undervoltage			4.8		V
V_{CPUV_CLEAR}	Recovery voltage for CP UV			4.9		V
OVERTEMPERATURE (OT) PROTECTION						
T_{OTW1_CLEAR}	Junction temperature for overtemperature warning		96	112	128	°C
T_{OTW1_SET}/ T_{OTW2_CLEAR}			106	122	138	
T_{OTW2_SET}/ T_{OTW3_CLEAR}			116	132	148	
T_{OTW3_SET}/ T_{OTSD_CLEAR}			126	142	158	
T_{OTSD}	Junction temperature for overtemperature shutdown		136	152	168	
T_{FB}	Junction temperature for overtemperature foldback	Per channel	130	150	170	
CURRENT LIMITING PROTECTION						
I_{LIM}	Current limit (load current)	Level 1	5.5	7.3	9	A
		Level 2 (default)	10.6	12.7	15	
OVERCURRENT (OC) SHUTDOWN PROTECTION						
I_{MAX}	Maximum current (peak output current)	Level 1, any short to supply, ground, or other channels	7.8	9.8	12.2	A
		Level 2 (default)	11.9	14.8	17.7	
TWEETER DETECT						
I_{TH_TW}	Load-current threshold for tweeter detect		330	445	560	mA
I_{LIM_TW}	Load-current limit for tweeter detect			2.1		A
STANDBY MODE						
V_{IH_STBY}	$\overline{\text{STANDBY}}$ input voltage for logic-level high		2			V
V_{IL_STBY}	$\overline{\text{STANDBY}}$ input voltage for logic-level low				0.7	V
I_{STBY_PIN}	$\overline{\text{STANDBY}}$ pin current			0.1	0.2	µA
MUTE MODE						
G_{MUTE}	Output attenuation	$\overline{\text{MUTE}}$ pin ≤ 0.5 Vdc for 200 ms, or I^2C mute enabled		100		dB
DC DETECT						
$V_{TH\_DC\_TOL}$	DC-detect threshold tolerance			25%		
t_{DCD}	DC-detect step-response time for two channels				5.3	s
CLIP REPORT						
$V_{OH\_CLIP\_OTW}$	$\overline{\text{CLIP\_OTW}}$ pin output voltage for logic level high (open-drain logic output)	External 47-kΩ pullup resistor to 3 V–5.5 V	2.4			v
$V_{OL\_CLIP\_OTW}$	$\overline{\text{CLIP\_OTW}}$ pin output voltage for logic-level low (open-drain logic output)				0.5	V
$T_{DELAY\_CLIPDET}$	Signal delay when output clipping detected				20	µs
MODE PINS (DIAG, $\overline{\text{SOFT\_MUTE}}$, I^2C MODE)						
V_{OH}	Mode pin output voltage for logic-level high (open-drain logic output)		2		5.5	V
V_{OL}	Mode pin output voltage for logic-level low (open-drain logic output)		0		0.7	V
FAULT REPORT						

ELECTRICAL CHARACTERISTICS (continued)

Test conditions (unless otherwise noted): T_{Case}= 25°C, PVDD = 14.4 V, R_L= 4 Ω, f_S = 417 kHz, P_{out}= 1 W/ch, Rext = 20 kΩ, AES17 filter, master-mode operation (see application diagram)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH_FAULT}	$\overline{FAULT}$ pin output voltage for logic-level high (open-drain logic output)	External 47-kΩ pullup resistor to 3 V–5.5 V	2.4			V
V_{OL_FAULT}	$\overline{FAULT}$ pin output voltage for logic-level low (open-drain logic output)				0.5	
OPEN/SHORT DIAGNOSTICS						
R_{S2P}, R_{S2G}	Maximum resistance to detect a short from OUT pins to PVDD or ground				200	Ω
R_{OPEN_LOAD}	Minimum load resistance to detect open circuit	Including speaker wires	300	800	1300	Ω
$R_{SHORTED\_LOAD}$	Maximum load resistance to detect short circuit	Including speaker wires	0.5	1.0	1.5	Ω
CHIP SELECT						
t_{LATCH_CS}	Time delay to latch I^2C address after POR			300		µs
V_{CS}	Voltage on CS pin for address 0	Connect to GND	0%	0%	15%	V_{D_BYP}
	Voltage on CS pin for address 1	External resistors in series between D_BYP and GND as a voltage divider	25%	35%	45%	
	Voltage on CS pin for address 2		55%	65%	75%	
	Voltage on CS pin for address 3	Connect to D_BYP	85%	100%	100%	
I^2C						
t_{HOLD_I2C}	Power-on hold time before I^2C communication	$\overline{STANDBY}$ high		1		ms
f_{SCL}	SCL clock frequency				400	kHz
V_{IH_SCL}	SCL pin input voltage for logic-level high	R_{PU_I2C}= 5-kΩ pullup, supply voltage = 3.3 V or 5 V	2.1		5.5	V
V_{IL_SCL}	SCL pin input voltage for logic-level low		–0.5		1.1	V
V_{OH_SDA}	SDA pin output voltage for logic-level high	I^2C read, R_{I2C}= 5-kΩ pullup, supply voltage = 3.3 V or 5 V	2.4			V
V_{OL_SDA}	SDA pin output voltage for logic-level low	I^2C read, 3-mA sink current			0.4	V
V_{IH_SDA}	SDA pin input voltage for logic-level high	I^2C write, R_{I2C}= 5-kΩ pullup, supply voltage = 3.3 V or 5 V	2.1		5.5	V
V_{IL_SDA}	SDA pin input voltage for logic-level low	I^2C write, R_{I2C}= 5-kΩ pullup, supply voltage = 3.3 V or 5 V	–0.5		1.1	V
C_i	Capacitance for SCL and SDA pins				10	pF
OSCILLATOR						
$V_{OH\_OSCSYNC}$	OSC_SYNC pin output voltage for logic-level high	CS pin set to MASTER mode	2.4		3.6	V
$V_{OL\_OSCSYNC}$	OSC_SYNC pin output voltage for logic-level low				0.5	V
$V_{IH\_OSCSYNC}$	OSC_SYNC pin input voltage for logic-level high	CS pin set to SLAVE mode	2		3.6	V
$V_{IL\_OSCSYNC}$	OSC_SYNC pin input voltage for logic-level low				0.8	V
f_{OSC_SYNC}	OSC_SYNC pin clock frequency	CS pin set to MASTER mode, f_S= 500 kHz	3.76	4	4.24	MHz
		CS pin set to MASTER mode, f_S= 417 kHz	3.13	3.33	3.63	
		CS pin set to MASTER mode, f_S= 357 kHz	2.68	2.85	3	

TIMING REQUIREMENTS FOR I²C INTERFACE SIGNALS

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
t_r	Rise time for both SDA and SCL signals			300	ns
t_f	Fall time for both SDA and SCL signals			300	ns
$t_{w(H)}$	SCL pulse duration, high	0.6			µs
$t_{w(L)}$	SCL pulse duration, low	1.3			µs
t_{su2}	Setup time for START condition	0.6			µs
t_{h2}	START condition hold time after which first clock pulse is generated	0.6			µs
t_{su1}	Data setup time	100			ns
t_{h1}	Data hold time	0 (1)			ns
t_{su3}	Setup time for STOP condition	0.6			µs
C_B	Load capacitance for each bus line			400	pF

(1) A device must internally provide a hold time of at least 300 ns for the SDA signal to bridge the undefined region of the falling edge of SCL.

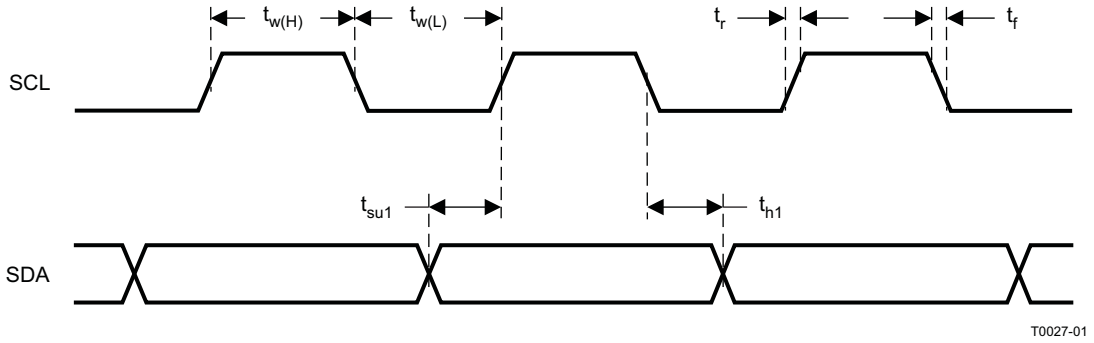


Figure 1. SCL and SDA Timing

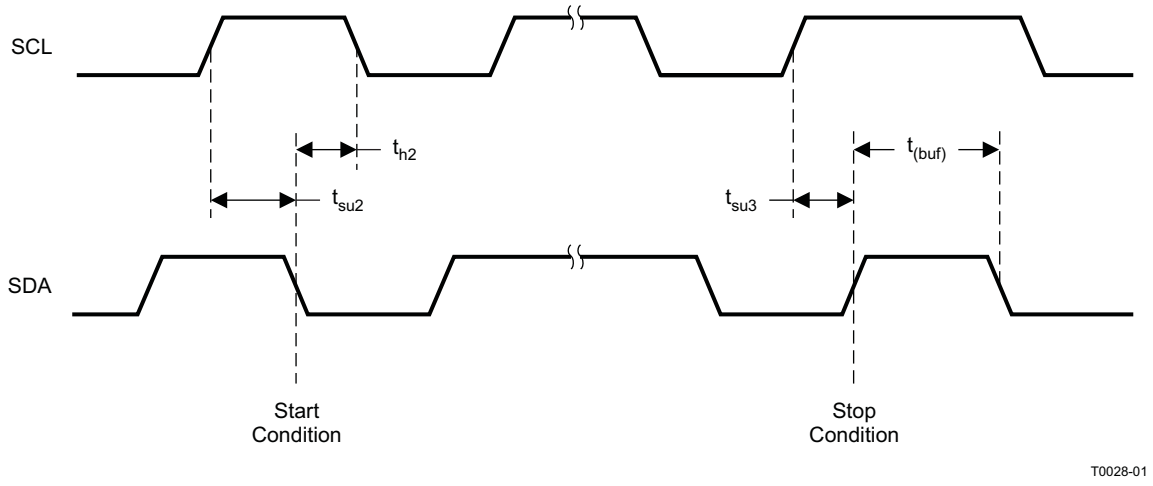


Figure 2. Timing for Start and Stop Conditions

TYPICAL CHARACTERISTICS

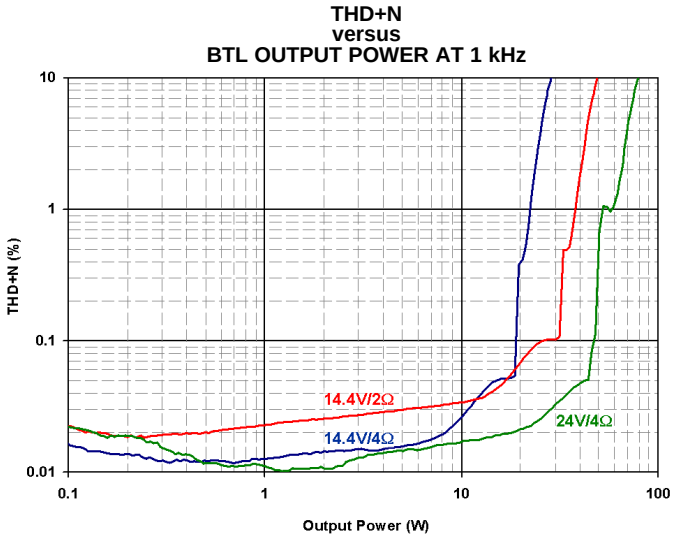


Figure 3.

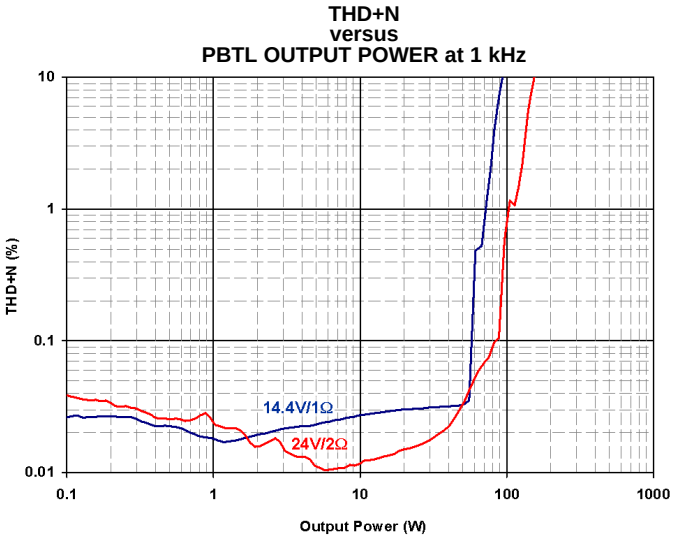


Figure 4.

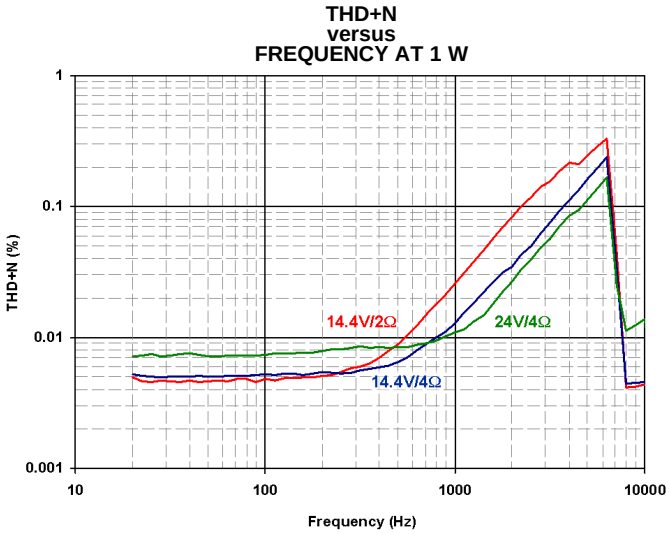


Figure 5.

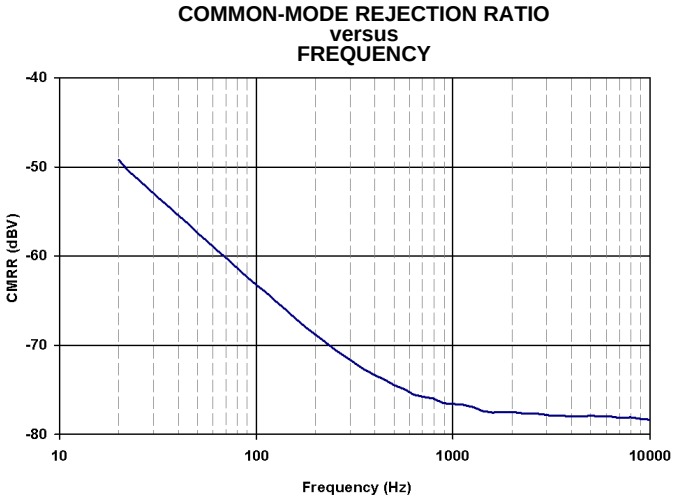


Figure 6.

TYPICAL CHARACTERISTICS (continued)

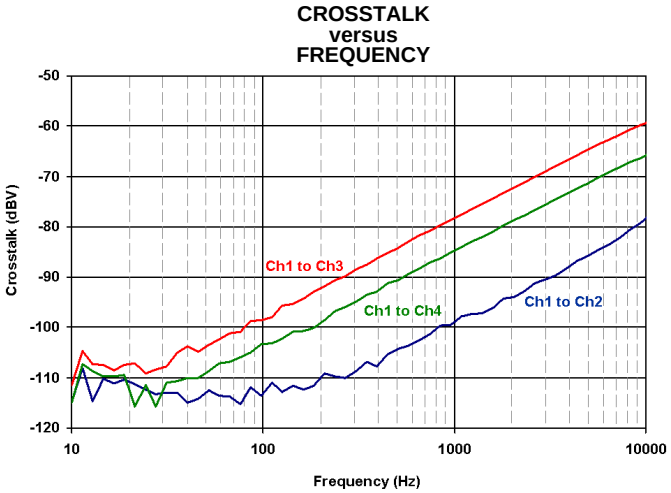


Figure 7.

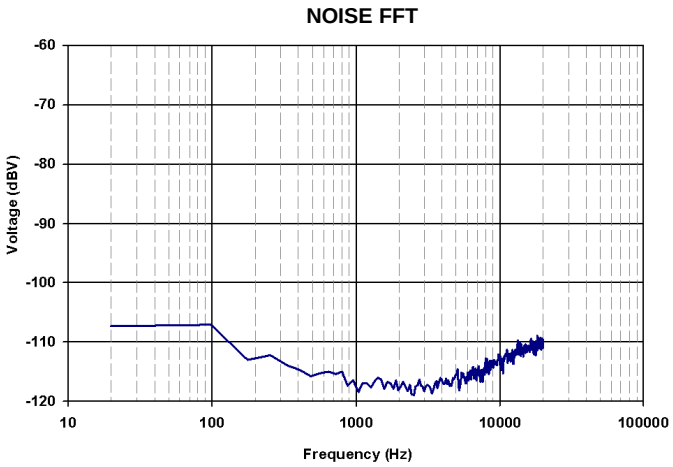


Figure 8.

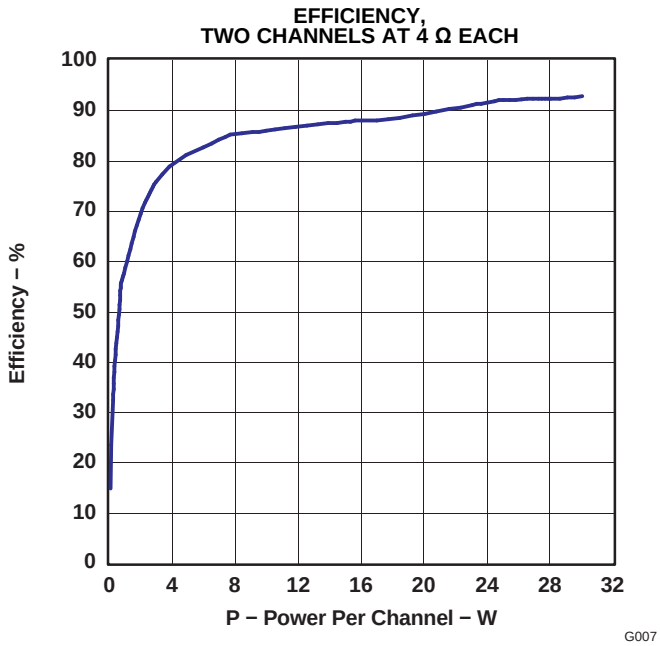


Figure 9.

DESCRIPTION OF OPERATION

OVERVIEW

The device is a two-channel analog-input audio amplifier for use in the automotive environment. The design uses an ultra-efficient class-D technology developed by Texas Instruments. This technology allows for reduced power consumption, reduced heat, and reduced peak currents in the electrical system. The device realizes an audio sound system design with smaller size and lower weight than traditional class-AB solutions.

The device has the following major blocks:

- Preamplifier
- PWM
- Gate drive
- Power FETs
- Diagnostics
- Protection
- Power supply
- I^2C serial communication bus

Preamplifier

The preamplifier is a high-input-impedance, low-noise, low-offset-voltage input stage with adjustable gain. The high input impedance allows the use of low-cost input capacitors while still achieving extended low-frequency response. A dedicated, internally regulated supply powers the preamplifier, giving excellent noise immunity and channel separation. Also included in the preamplifier are:

1. **Mute Pop-and-Click Control**—Application of a mute at the crest or trough of an audio input signal reshapes and amplifies the signal as a step. Listeners perceive such a step as a loud click. The TAS5412-Q1 avoids clicks by ramping the gain gradually on reception of a mute or play command. The start or stopping of switching in a class-D amplifier can cause another form of click and pop. The TAS5412-Q1 incorporates a patented method to reduce the pop energy during the switching start-up and shutdown sequences. Fault conditions require rapid protection response by the TAS5412-Q1, which does not have time to ramp the gain down in a pop-free manner. The device transitions into Hi-Z mode when an OV, UV, OC, OT, or dc fault is encountered. Also, activation of the $\overline{\text{STANDBY}}$ pin may not be pop-free.
2. **Gain Control**—The four gain settings are set in the preamplifier via I^2C control registers. Setting of the gain outside of the global feedback resistors of the TAS5412-Q1 thus allows for stability in the system at all gain settings with properly loaded conditions.

Pulse-Width Modulator (PWM)

The PWM converts the analog signal from the preamplifier into a switched signal of varying duty cycle. This is the critical stage that defines the class-D architecture. In the TAS5412-Q1, the modulator is an advanced design with high bandwidth, low noise, low distortion, excellent stability, and full 0–100% modulation capability. The patented PWM uses clipping recovery circuitry to eliminate the deep saturation characteristic of PWMs when the input signal exceeds the modulator waveform.

Gate Drive

The gate driver accepts the low-voltage PWM signal and level-shifts it to drive a high-current, full-bridge, power FET stage.

Power FETs

The BTL output for each channel comprises four rugged N-channel FETs, each of which is low r_{DSon} for high efficiency and maximum power transfer to the load. These FETs handle large voltage transients during load dump.

Load Diagnostics

The device incorporates load-diagnostic circuitry designed to help pinpoint the nature of output misconnections during installation. The diagnostics include functions for detecting and determining the status of output connections. The following diagnostics are supported:

- Short to GND
- Short to PVDD
- Short across load
- Open load
- Tweeter detection

Reporting the presence of any of the short or open conditions to the system is via I^2C register read. One can read the tweeter detect status from the CLIP_OTW pin when properly configured.

1. **Output Short and Open Diagnostics**—The device contains circuitry designed to detect shorts and open conditions on the outputs. One can only invoke the load diagnostic function when the output is in the Hi-Z mode. There are four phases of test during load diagnostics and two levels of test. In the full level, all channels must be in the Hi-Z state. The diagnostic tests all four phases on each channel, and both channels at the same time. When fewer than two channels are in Hi-Z, the reduced level of test is the only available option. In the reduced level, the only available tests are short to PVDD and short to GND. Load diagnostics can occur at power up before the amplifier is moved out of Hi-Z mode. If the amplifier is already in play mode, it must *Mute* and then *Hi-Z* to allow performing the load diagnostic. By performing the mute function, the normal pop- and click-free transitions occur before the diagnostics begin. The device performs the diagnostics as shown in Figure 10. Figure 11 shows the impedance ranges for the open-load and shorted-load diagnostics. Reading of the diagnostic results is from the diagnostic register for each channel via I^2C.

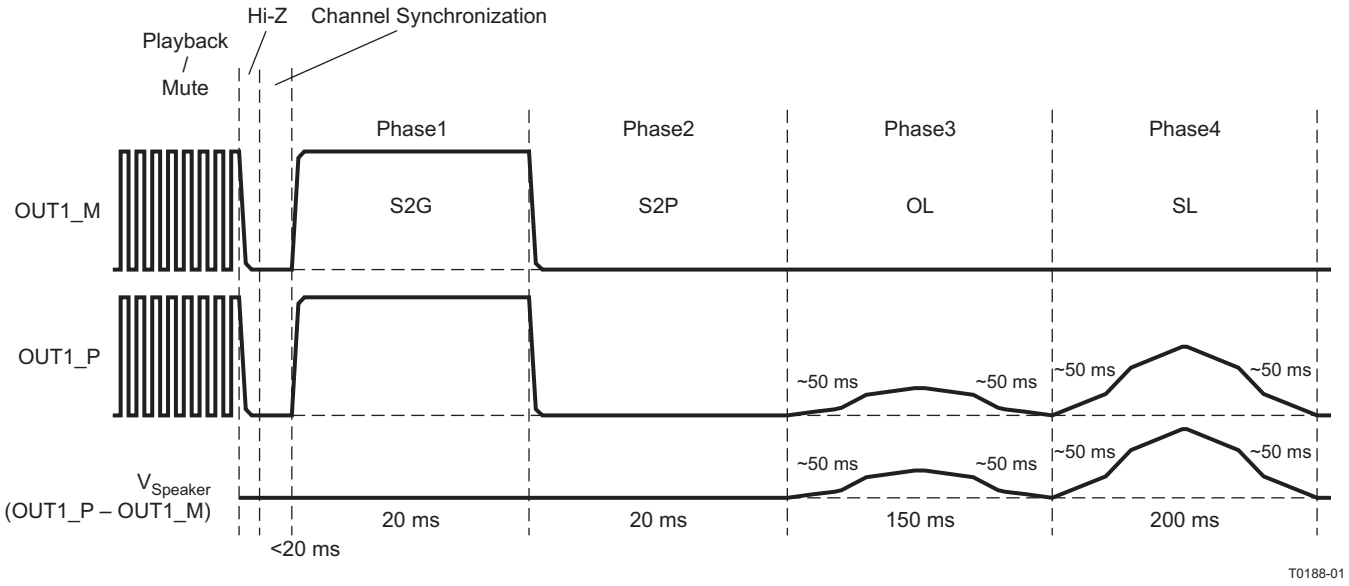


Figure 10. Load Diagnostics Sequence of Events

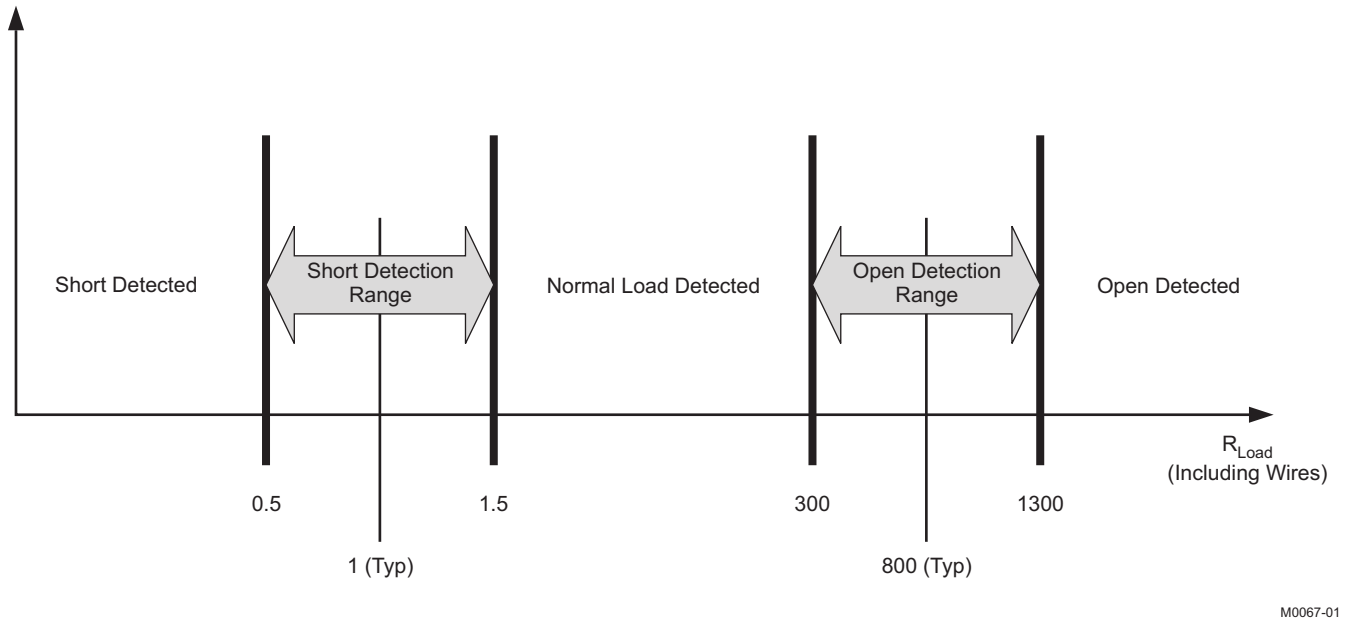


Figure 11. Open- and Shorted-Load Detection

2. **Tweeter Detection**—Tweeter detection is an alternate operating mode used to determine the proper connection of a frequency-dependent load (such as a speaker with a crossover). Invocation of tweeter detection is via I^2C, and both channels should be tested individually. Tweeter detection uses the average cycle-by-cycle current-limit circuit (see the *CBC* section) to measure the current delivered to the load. The proper implementation of this diagnostic function depends on the amplitude of a user-supplied test signal and on the impedance-versus-frequency curve of the acoustic load. The system (external to the device) must generate a signal to which the load responds. The user must calibrate the frequency and amplitude of this signal to result in a current draw that is greater than the tweeter detection threshold when the load under test is present, and less than the detection threshold if the load is not properly connected. The current level for the tweeter detection threshold, as well as the maximum current that can safely be delivered to a load when in tweeter-detection mode, is in the Electrical Characteristics section of the datasheet. The tweeter-detection results are available on the $\overline{\text{CLIP\_OTW}}$ pin during the application of the test signal. During tweeter-detection activation (when the tested load is present), pulses on the $\overline{\text{CLIP\_OTW}}$ pin begin to toggle. The pulses on the $\overline{\text{CLIP\_OTW}}$ pin report low whenever the current exceeds the detection threshold, and the pin remains low until the current no longer exceeds the threshold. The minimum low-pulse period that one can expect is equal to one period of the switching frequency. Having an input signal that increases the duration of detector activation (for example, increasing the amplitude of the input signal) increases the amount of time for which the $\overline{\text{CLIP\_OTW}}$ pin reports low.
NOTE: Because tweeter detection is an alternate *operating mode*, it is necessary to place the channels to be tested in Play mode (via register 0x0C) after activation of tweeter detection in order to commence the detection process. Additionally, the appropriate settings must be in register 0x0A, enabling the $\overline{\text{CLIP\_OTW}}$ to report the results of tweeter detection.

Protection and Monitoring

1. **Cycle-By-Cycle Current Limit (CBC)**—The CBC current-limiting circuit terminates each PWM pulse to limit the output-current flow when current exceeds the average current-limit (I_{LIM}) threshold. The overall effect on the audio in the case of a current overload is quite similar to a voltage-clipping event, where the device temporarily limits power at the peaks of the musical signal and normal operation continues without disruption on removal of the overload. The TAS5412-Q1 does not prematurely shut down in this condition. Both channels continue in play mode and pass signal.
2. **Overcurrent Shutdown (OCSD)**—Under severe short-circuit events, such as a short to PVDD or ground, the device uses a peak-current detector, and the affected channel shuts down in 200 µs to 390 µs if the conditions are severe enough. The shutdown speed depends on a number of factors, such as the impedance of the short circuit, supply voltage, and switching frequency. Only the shorted channels shut down in such a

scenario. The user may restart the affected channel via I²C. An OCSD event activates the fault pin, with the I²C fault register recording the affected channels. If the supply or ground short is strong enough to exceed the peak current threshold but not severe enough to trigger the OCSD, the peak current limiter prevents excess current from damaging the output FETs, and operation returns to normal after the short is removed.

3. **DC Detect**—This circuit detects a dc offset continuously during normal operation at the output of the amplifier. If the dc offset reaches the level defined in the I²C registers for the specified time period, the circuit triggers. By default, a dc detection event does not shut the output down. One can enable or disable the shutdown function via I²C. If enabled, the triggered channel shuts down, but the others remain playing, and the device asserts the FAULT pin. The I²C registers define the dc level.
4. **Clip Detect**—The clip-detect circuit alerts the user to the presence of a 100% duty-cycle PWM due to a clipped waveform. When this occurs, the device passes to the CLIP_OTW pin a signal that remains asserted until the 100% duty-cycle PWM signal is no longer present. Through I²C, one can change the CLIP_OTW signal to clip-only, OTW-only, or both. A fourth mode, used only during diagnostics, is the option to report detected tweeter-detection events on these pins (see the *Tweeter Detection* section). The microcontroller in the system can monitor the signal at the CLIP_OTW pin. The microcontroller configuration may be such as to reduce the volume on the channel in an active clipping-prevention circuit.
5. **Overtemperature Warning (OTW), Overtemperature Shutdown (OTSD), and Thermal Foldback**—The device asserts the CLIP_OTW pin when the die temperature reaches 125°C. The OTW has three temperature thresholds with a 10°C hysteresis. Indication of the thresholds is in I²C register 0x04 bits 5, 6, and 7. The device still functions until the temperature reaches the OTSD threshold, 155°C, at which time it places the outputs into Hi-Z mode and asserts the FAULT pin. I²C is still active in the event of an OTSD, which allows reading the registers for faults, but all audio ceases abruptly. The OTSD resets at 145°C, to allow the turning the TAS5412-Q1 back on through I²C. The OTW indication persists until the temperature drops below 115°C. All temperatures are nominal values. The thermal foldback decreases the channel gain.
6. **Undervoltage (UV) and Power-On Reset (POR)**—The undervoltage (UV) protection detects low voltages on PVDD, AVDD, and CP. In the event of an undervoltage, the device asserts the FAULT pin and updates the I²C register for the voltage which caused the event. Power-on-reset (POR) occurs when PVDD drops low enough. A POR event causes the I²C to go into a high-impedance state. After the device recovers from the POR event, re-initialization of the device via I²C is necessary.
7. **Overvoltage (OV) and Load Dump**—The OV protection detects high voltages on PVDD. If PVDD reaches the overvoltage threshold, the device asserts the FAULT pin and updates the I²C register. If the voltage increases beyond the load dump threshold of 29 Vdc, the device shuts down and must undergo a restart once the voltage returns to a safe value. After the device recovers from a load-dump event, the device requires re-initialization via I²C. The TAS5412-Q1 can withstand 50-V load-dump voltage spikes. Load Diagnostics shows the regions of operating voltage and the profile of the load-dump event.

Power Supply

A car battery that can have a large voltage swing most commonly provides the power for the device. PVDD is a filtered battery voltage, and is the supply for the output FETS and the low-side FET gate driver. A charge pump (CP) supply provides power to the high-side FET gate driver. The charge pump supplies the gate-drive voltages. AVDD, which comes from an internal linear regulator, powers the analog circuitry. This supply requires a 0.1-µF, 10-V external bypass capacitor at the A_BYP pin. TI recommends attaching no external components except the bypass capacitor to this pin. DVDD, which comes from an internal linear regulator, powers the digital circuitry. The D_BYP pin requires a 0.1-µF, 10-V external bypass capacitor. TI recommends that no external components except the bypass capacitor be attached to this pin.

The device can withstand fortuitous open-ground and -power conditions. Fortuitous open-ground usually occurs when a speaker wire is shorted to ground, allowing for a second ground path through the body diode in the output FETs. The uniqueness of the diagnostic capabilities allows debugging of the speakers and speaker wires, eliminating the need to remove the amplifier to diagnose the problem.

I²C Serial Communication Bus

The device communicates with the system processor via the I²C serial communication bus. It is an I²C slave-only device. The processor can poll the device via I²C to determine the operating status. Reporting of all fault conditions and detections is via I²C. The setting of numerous features and operating conditions is also via I²C.

The I²C bus allows control of the following configurations:

- Control the gain each channel independently. The gain settings are 12 dB, 20 dB, 26 dB, and 32 dB.

- Select AM non-interference switching frequency
- Configure the $\overline{\text{CLIP\_OTW}}$ pin
- Enable or disable the dc-detect function with selectable threshold
- Place channel in Hi-Z (switching stopped) mode (mute)
- Select tweeter detect, set detect threshold, and initiate function
- Initiate open- and shorted-load diagnostic
- Reset faults and return to normal switching operation from Hi-Z mode (unmute)

In addition to the standard SDA and SCL pins for the I^2C bus, the device includes a single pin that allows up to four devices to work together in a system with no additional hardware required for communication or synchronization. The I2C_ADDR pin sets the device in master or slave mode and selects the I^2C address for that device. Tie I2C_ADDR to DGND for master, to 1.2 Vdc for slave 1, to 2.4 Vdc for slave 2, and to D_BYP for slave 3. The OSC_SYNC pin synchronizes the internal clock oscillators and thereby avoids beat frequencies. Optional application of an external oscillator to this pin allows external control of the switching frequency.

Table 2. I2C_ADDR Pin Connection

DESCRIPTION	I2C_ADDR PIN CONNECTION	I^2C ADDRESS
Device 0 - OSC_SYNC clock master	To SGND pin	0xD8/D9
Device 1 - OSC_SYNC clock slave 1	35% DVDD (resistive voltage divider between D_BYP pin and SGND pin) (1)	0xDA/DB
Device 2 - OSC_SYNC clock slave 2	65% DVDD (resistive voltage divider between D_BYP pin and SGND pin) (1)	0xDC/DD
Device 3 - OSC_SYNC clock slave 3	To D_BYP pin	0xDE/DF

(1) R_{CS} with 5% or better tolerance is recommended.

I^2C Bus Protocol

The device has a bidirectional serial control interface that is compatible with the Inter IC (I^2C) bus protocol and supports 400-kbps data transfer rates for random and sequential write and read operations. This is a slave-only device that does not support a multimaster bus environment or wait-state insertion. Use the control interface to program the registers of the device and to read device status.

The I^2C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. Data transfer on the bus is serial, one bit at a time. The address and data transfers are in byte (8-bit) format with the most-significant bit (MSB) transferred first. In addition, the receiving device acknowledges each byte transferred on the bus with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data terminal (SDA) while the clock is HIGH to indicate start and stop conditions. A HIGH-to-LOW transition on SDA indicates a start, and a LOW-to-HIGH transition indicates a stop. Normal data bit transitions must occur within the low time of the clock period. Figure 12 shows these conditions. The master generates the 7-bit slave address and the read/write bit to open communication with another device and then wait for an acknowledge condition. The device holds SDA LOW during the acknowledge-clock period to indicate an acknowledgement. When this occurs, the master transmits the next byte of the sequence. Addressing of each device is by a unique 7-bit slave address plus read/write bit (1 byte). All compatible devices share the same signals via a bidirectional bus using a wired-AND connection. There must be an external pullup resistor for the SDA and SCL signals to set the HIGH level for the bus. There is no limit on the number of bytes comprising a transmission between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus.

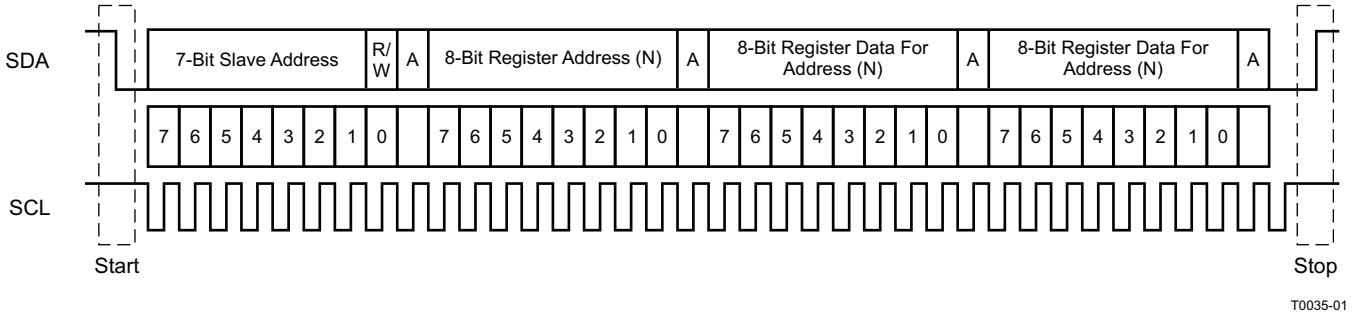


Figure 12. Typical I²C Sequence

Use the CS pin (pin 62) to program the device for one of four addresses. These four addresses are licensed I²C addresses and do not conflict with other licensed I²C audio devices. To communicate with the device, the I²C master uses addresses shown in Table 2. Read and write data transmissions can use single-byte or multiple-byte data transfers.

Random Write

As shown in Figure 13, a single-byte data-write transfer begins with the master device transmitting a start condition followed by the I²C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a write data transfer, the read/write bit is a 0. After receiving the correct I²C device address and the read/write bit, the device responds with an acknowledge bit. Next, the master transmits the address byte or bytes corresponding to the internal memory address being accessed. After receiving the address byte, the device again responds with an acknowledge bit. Next, the master device transmits the data byte to be written to the memory address being accessed. After receiving the data byte, the device again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data-write transfer.

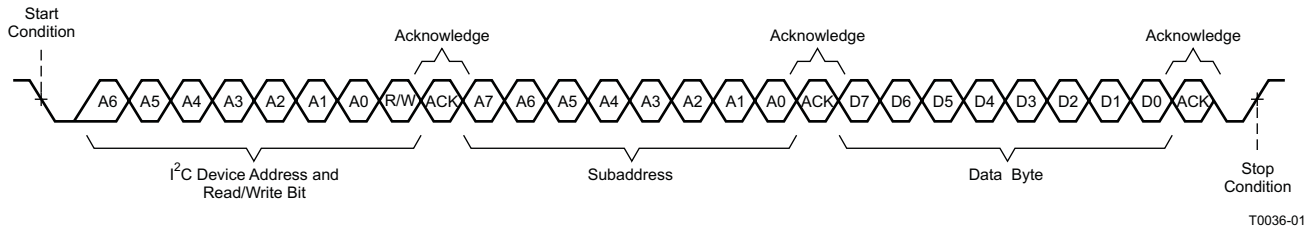


Figure 13. Random Write Transfer

Sequential Write

A sequential data-write transfer is identical to a single-byte data-write transfer except that the master transmits multiple data bytes to the device as shown in Figure 14. After receiving each data byte, the device responds with an acknowledge bit, and the I²C subaddress automatically increments by one.

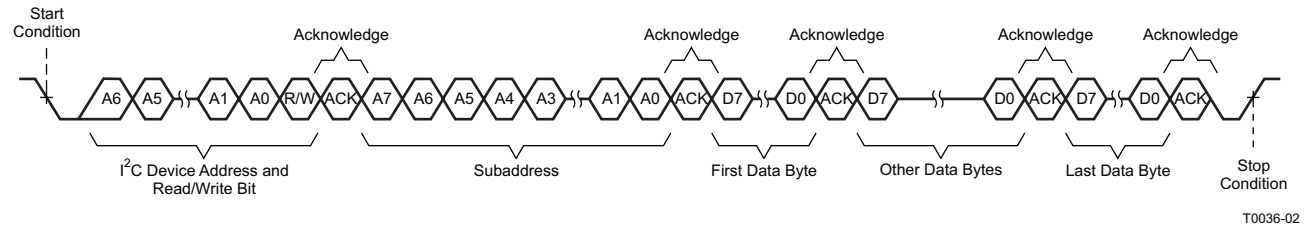


Figure 14. Sequential Write Transfer

A sequential data-write transfer is identical to a single-byte data-write transfer except that the master transmits multiple data bytes to the device as shown in Figure 14. After receiving each data byte, the device responds with an acknowledge bit, and the I^2C subaddress automatically increments by one.

Random Read

As shown in Figure 15, a single-byte data-read transfer begins with the master device transmitting a start condition followed by the I^2C device address and the read/write bit. The data-read transfer actually performs a write followed by a read. Initially, a write transfers the address byte or bytes of the internal memory address to be read. As a result, the read/write bit is a 0. After receiving the address and the read/write bit, the device responds with an acknowledge bit. In addition, after sending the internal memory address byte or bytes, the master device transmits another start condition followed by the device address and the read/write bit again. This time the read/write bit is a 1, indicating a read transfer. After receiving the address and the read/write bit, the device again responds with an acknowledge bit. Next, the device transmits the data byte from the memory address being read. After receiving the data byte, the master transmits a not-acknowledge followed by a stop condition to complete the single-byte data-read transfer.

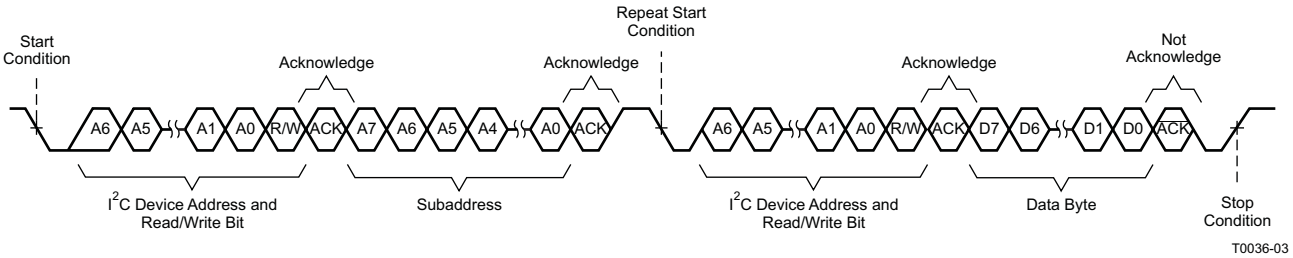


Figure 15. Random Read Transfer

Sequential Read

A sequential data-read transfer is identical to a single-byte data-read transfer except that the device transmits multiple data bytes to the master as shown in Figure 16. Except for the last data byte, the master responds with an acknowledge bit after receiving each data byte and automatically increments the I^2C subaddress by one.
Note: The fault registers do not have sequential read capabilities.

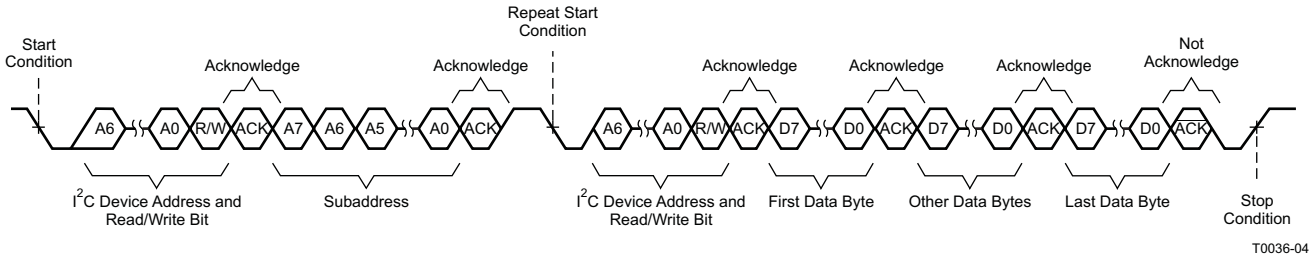


Figure 16. Sequential Read Transfer

A sequential data-write transfer is identical to a single-byte data-write transfer except that the master transmits multiple data bytes to the device as shown in Figure 14. After receiving each data byte, the device responds with an acknowledge bit, and the I^2C subaddress automatically increments by one.

Table 3. TAS5412-Q1 I^2C Addresses

DESCRIPTION		FIXED ADDRESS					SELECTABLE WITH ADDRESS PIN		READ/WRITE BIT	I^2C ADDRESS
		MSB	6	5	4	3	2	1	LSB	
0 – OSC MASTER	I^2C WRITE	1	1	0	1	1	0	0	0	0xD8
	I^2C READ	1	1	0	1	1	0	0	1	0xD9
1 – OSC SLAVE1	I^2C WRITE	1	1	0	1	1	0	1	0	0xDA
	I^2C READ	1	1	0	1	1	0	1	1	0xDB
2 – OSC SLAVE2	I^2C WRITE	1	1	0	1	1	1	0	0	0xDC
	I^2C READ	1	1	0	1	1	1	0	1	0xDD
3 – OSC SLAVE3	I^2C WRITE	1	1	0	1	1	1	1	0	0xDE
	I^2C READ	1	1	0	1	1	1	1	1	0xDF

Table 4. I^2C Address Register Definitions

ADDRESS	TYPE	REGISTER DESCRIPTION
0x00	Read	Latched fault register 1, global and channel fault
0x01	Read	Latched fault register 2, dc offset and overcurrent detect
0x02	Read	Latched diagnostic register 1, load diagnostics, channel 1
0x03	Read	Latched diagnostic register 2, load diagnostics, channel 2
0x04	Read	External status register 1, temperature and voltage detect
0x05	Read	External status register 2, Hi-Z and low-low state
0x06	Read	External status register 3, mute and play modes
0x07	Read	External status register 4, load diagnostics
0x08	Read, Write	External control register 1, channel gain select
0x09	Read, Write	Not used
0x0A	Read, Write	External control register 2, switching frequency and clip pin select
0x0B	Read, Write	External control register 3, load diagnostic, master mode select
0x0C	Read, Write	External control register 4, output state control
0x0D	Read, Write	External control register 5, output state control
0x0E	Read, Write	Not used
0x0F	Read, Write	Not used
0x10	Read, Write	External control register 6, dc detect threshold selection
0x13	Read	External status register 5, overtemperature shutdown and thermal foldback

Table 5. Fault Register 1 (0x00) Protection

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	0	0	No protection-created faults, default value
–	–	–	–	–	–	–	1	Overtemperature warning has occurred
–	–	–	–	–	–	1	–	DC offset has occurred in any channel
–	–	–	–	–	1	–	–	Overcurrent shutdown has occurred in any channel
–	–	–	–	1	–	–	–	Overtemperature shutdown has occurred
–	–	–	1	–	–	–	–	Charge-pump undervoltage has occurred
–	–	1	–	–	–	–	–	AVDD, analog voltage, undervoltage has occurred
–	1	–	–	–	–	–	–	PVDD undervoltage has occurred
1	–	–	–	–	–	–	–	PVDD overvoltage has occurred

Table 6. Fault Register 2 (0x01) Protection

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	0	0	No protection-created faults, default value
–	–	–	–	–	–	1	–	Ovecurrent shutdown channel 1 has occurred
–	–	–	–	–	1	–	–	Overcurrent shutdown channel 2 has occurred
–	–	1	–	–	–	–	–	DC offset channel 1 has occurred
–	1	–	–	–	–	–	–	DC offset channel 2 has occurred
X	–	–	X	X	–	–	X	Reserved

Table 7. Diagnostic Register 1 (0x02) Load Diagnostics

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	0	0	No load-diagnostic-created faults, default value
–	–	–	1	–	–	–	–	Output short to ground channel 1 has occurred
–	–	1	–	–	–	–	–	Output short to PVDD channel 1 has occurred
–	1	–	–	–	–	–	–	Shorted load channel 1 has occurred
1	–	–	–	–	–	–	–	Open load channel 1 has occurred
–	–	–	–	X	X	X	X	Reserved

Table 8. Diagnostic Register 2(0x03) Load Diagnostics

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	0	0	No load-diagnostic-created faults, default value
–	–	–	–	–	–	–	1	Output short to ground channel 2 has occurred
–	–	–	–	–	–	1	–	Output short to PVDD channel 2 has occurred
–	–	–	–	–	1	–	–	Shorted load channel 2 has occurred
–	–	–	–	1	–	–	–	Open load channel 2 has occurred
X	X	X	X	–	–	–	–	Reserved

Table 9. External Status Register 1 (0x04) Fault Detection

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	0	0	No protection-created faults are present, default value
–	–	–	–	–	–	–	1	PVDD overvoltage fault is present
–	–	–	–	–	–	1	–	PVDD undervoltage fault is present
–	–	–	–	–	1	–	–	AVDD, analog voltage fault is present
–	–	–	–	1	–	–	–	Charge-pump voltage fault is present
–	–	–	1	–	–	–	–	Overtemperature shutdown is present
–	–	1	–	–	–	–	–	Overtemperature warning
–	1	1	–	–	–	–	–	Overtemperature warning level 1
1	0	1	–	–	–	–	–	Overtemperature warning level 2
1	1	1	–	–	–	–	–	Overtemperature warning level 3

Table 10. External Status Register 2 (0x05) Output State of Individual Channels

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	1	1	0	Output is in Hi-Z mode, not in low-low mode (1), default value
–	–	–	–	–	–	0	–	Channel 1 Hi-Z mode (0 = not Hi-Z, 1 = Hi-Z)
–	–	–	–	–	0	–	–	Channel 2 Hi-Z mode (0 = not Hi-Z, 1 = Hi-Z)
–	–	1	–	–	–	–	–	Channel 1 low-low mode (0 = not low-low, 1 = low-low) (1)
–	1	–	–	–	–	–	–	Channel 2 low-low mode (0 = not low-low, 1 = low-low) (1)
X	–	–	X	X	–	–	X	Reserved

(1) *Low-low* is defined as both outputs actively pulled to ground.

Table 11. External Status Register 3 (0x06) Play and Mute Modes

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	0	0	Mute mode is disabled, play mode disabled, default value, (Hi-Z mode)
–	–	–	–	–	–	1	–	Channel 1 is in play mode.
–	–	–	–	–	1	–	–	Channel 2 is in play mode.
–	–	1	–	–	–	–	–	Channel 1 is in mute mode.
–	1	–	–	–	–	–	–	Channel 2 is in mute mode.
X	–	–	X	X	–	–	X	Reserved

Table 12. External Status Register 4 (0x07) Load Diagnostics

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	0	0	No channels are set in load diagnostics mode, default value
–	–	–	–	–	–	1	–	Channel 1 is in load diagnostics mode.
–	–	–	–	–	1	–	–	Channel 2 is in load diagnostics mode.
–	–	1	–	–	–	–	–	Channel 1 is in overtemperature foldback.
–	1	–	–	–	–	–	–	Channel 2 is in overtemperature foldback.
X	–	–	X	X	–	–	X	Reserved

Table 13. External Control Register 1 (0x08) Gain Select

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
1	0	1	0	1	0	1	0	Set gain for both channels to 26 dB, default value
–	–	–	–	0	0	–	–	Set channel 1 gain to 12 dB
–	–	–	–	0	1	–	–	Set channel 1 gain to 20 dB
–	–	–	–	1	1	–	–	Set channel 1 gain to 32 dB
–	–	0	0	–	–	–	–	Set channel 2 gain to 12 dB
–	–	0	1	–	–	–	–	Set channel 2 gain to 20 dB
–	–	1	1	–	–	–	–	Set channel 2 gain to 32 dB
X	X	–	–	–	–	X	X	Reserved

Table 14. External Control Register 2 (0x0A) Switching Frequency Select and Clip_OTW Configuration

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	1	1	0	1	Set f_S = 417 kHz, configure clip and OTW detection, 45° phase, disable hard stop
–	–	–	–	–	–	0	0	Set f_S = 500 kHz
–	–	–	–	–	–	1	0	Set f_S = 357 kHz
–	–	–	–	–	–	1	1	Invalid frequency selection (do not set)
–	–	–	–	0	0	–	–	Configure $\overline{\text{CLIP\_OTW}}$ pin for tweeter detect only
–	–	–	–	0	1	–	–	Configure $\overline{\text{CLIP\_OTW}}$ pin for clip detect only
–	–	–	–	1	0	–	–	Configure $\overline{\text{CLIP\_OTW}}$ pin for overtemperature warning only
–	–	–	1	–	–	–	–	Enable hard-stop mode
–	–	1	–	–	–	–	–	Set f_S to a 180° phase difference between adjacent channels
–	1	–	–	–	–	–	–	Send sync pulse from OSC_SYNC pin (device must be in master mode).
1	–	–	–	–	–	–	–	Report thermal foldback to the $\overline{\text{CLIP\_OTW}}$ pin.

Table 15. External Control Register 3 (0x0B) Load Diagnostics and Master-or-Slave Control

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	1	0	1	0	0	0	0	Disable load diagnostics, enable dc-detect SD, master mode
–	–	–	–	–	–	1	–	Enable channel 1, load diagnostics
–	–	–	–	–	1	–	–	Enable channel 2, load diagnostics

Table 15. External Control Register 3 (0x0B) Load Diagnostics and Master-or-Slave Control (continued)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
–	–	–	–	X	–	–	X	Reserved
–	–	–	0	–	–	–	–	Disable dc detect shutdown on all channels
–	–	1	–	–	–	–	–	Enable tweeter-detect mode
–	0	–	–	–	–	–	–	Enable slave mode (provide external oscillator)
1	–	–	–	–	–	–	–	Send clock, OSC_SYNC pin has clock output (valid only in master mode)

Table 16. External Control Register 4 (0x0C) Output Control

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	1	1	1	1	1	All channels, Hi-Z, mute, reset disabled
–	–	–	–	–	–	0	–	Set channel 1 to mute mode, non-Hi-Z
–	–	–	–	–	0	–	–	Set channel 2 to mute mode, non-Hi-Z
–	X	X	–	X	–	–	X	Reserved
–	–	–	0	–	–	–	–	Set non-Hi-Z channels to play mode, (unmute)
1	–	–	–	–	–	–	–	Reset device

Table 17. External Control Register 5 (0x0D) Output Control

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	0	0	Low-low state disabled, both channels
–	–	–	–	–	–	1	–	Set channel 1 to low-low state
–	–	–	–	–	1	–	–	Set channel 2 to low-low state
X	X	X	X	X	–	–	X	Reserved

Table 18. External Control Register 6 (0x10) DC Detect Threshold Selection

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	0	1	Default dc detect value (1.6 V)
–	–	–	–	–	–	0	0	Minimum dc detect value (0.8 V)
–	–	–	–	–	–	1	0	Maximum dc detect value (2.4 V) Note: a value of 11 is invalid
–	–	–	–	–	1	–	–	Enable enhanced-crosstalk mode
–	–	–	–	1	–	–	–	Add a 20-ms delay between load diagnostic phases
–	–	–	1	–	–	–	–	4× longer short-to-power (S2P) and short-to-ground (S2G) phases
1	–	–	–	–	–	–	–	Slower common mode (CM) ramp-down from mute mode
–	X	X	–	–	–	–	–	Reserved

Table 19. External Status Register 5 (0x13) Overtemperature and Thermal Foldback Status

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	0	0	Default overtemperature foldback status, no channel is in foldback
–	–	–	–	–	–	1	–	Channel 1 in thermal foldback
–	–	–	–	–	1	–	–	Channel 2 in thermal foldback
–	–	1	–	–	–	–	–	Channel 1 in overtemperature shutdown
–	1	–	–	–	–	–	–	Channel 2 in overtemperature shutdown
X	–	–	X	X	–	–	X	Reserved

Hardware Control Pins

The device has several hardware pins for real-time control and indication of device status.

$\overline{\text{FAULT}}$ pin: This active-low, open-drain output pin indicates the presence of a fault condition that requires the device to go automatically into the Hi-Z mode or standby mode. When asserting this pin high, the device is protecting itself and the system from potential damage. One can read the exact nature of the fault via I^2C, with the exception of faults that are the result of PVDD voltage excursions below POR. In this case, the device goes into standby mode and the I^2C bus is no longer operational. However, the fault indication remains, due to the fact that the $\overline{\text{FAULT}}$ pin is open-drain and active-high.

$\overline{\text{CLIP\_OTW}}$ pin: The function of this active-low pin, configured by the user, indicates one of the following conditions: overtemperature warning, the detection of clipping, or the logical OR of both of these conditions. Selection of the configuration is via I^2C. During tweeter-detect diagnostics, detection of a tweeter also results in assertion of this pin.

$\overline{\text{MUTE}}$ pin: This active-low pin is for hardware control of the mute-and-unmute function for all four channels. Capacitor CMUTE controls the time constant for the gain ramp needed to produce a pop- and click-free mute function. For pop- and click-free operation, implement the mute function through I^2C commands. The use of a hard mute with an external transistor does not ensure pop- and click-free operation; TI does not recommend such use unless there is a requirement for an emergency hard mute function in case of a loss of I^2C control. Do not share the CMUTE capacitor between more than one device.

$\overline{\text{STANDBY}}$ pin: Asserting this active-low pin puts the device into a complete shutdown, limiting the current draw to 2 µA, typical. Assertion typically occurs when the car ignition is in the off position. Another use of the pin is to shut down the device rapidly on violation of certain operating conditions. Pin assertion causes the loss of all I^2C register content and causes the I^2C bus to go into the high-impedance state.

EMI Considerations

Automotive-level EMI performance depends on both careful integrated-circuit design and good system-level design. Controlling sources of electromagnetic interference (EMI) is a major consideration in all aspects of the TAS5412-Q1 design.

The TAS5412-Q1 has minimal parasitic inductances due to the short leads on the PHD package. This dramatically reduces the EMI that results from current passing from the die to the system PCB. Each channel of the TAS5412-Q1 also operates at a different phase. The phase between channels is I^2C selectable to either 45° or 180°, to reduce EMI caused by high-current switching. The TAS5412-Q1 incorporates patent-pending circuitry that optimizes output transitions that cause EMI.

AM Radio EMI Reduction

To reduce interference in the AM radio band, the TAS5412-Q1 has the ability to change the switching frequency via I^2C commands. Table 20 lists the recommended frequencies. The fundamental frequency and its second harmonic straddle the AM radio band listed. This eliminates the tones that can be present due to the switching frequency being demodulated by the AM radio. To function properly, AM avoidance requires the use of a 20-kΩ, 1% tolerance Rext resistor.

Table 20. Recommended Switching Frequencies for AM Mode Operation

US		EUROPEAN	
AM FREQUENCY (kHz)	SWITCHING FREQUENCY (kHz)	AM FREQUENCY (kHz)	SWITCHING FREQUENCY (kHz)
		522-540	417
540–917	500	540–914	500
917–1125	417	914–1122	417
1125–1375	500	1122–1373	500
1375–1547	417	1373–1548	417
1547–1700	357	1548–1701	357

Operating States

the following tables depict the operating regions, or states, of the TAS5412-Q1.

Table 21. Operating States and Supplies

STATE NAME	OUTPUT FETS	CHARGE PUMP	OSCILLATOR	I^2C	AVDD and DVDD
STANDBY	Hi-Z, floating	Stopped	Stopped	Stopped	OFF
Hi-Z	Hi-Z, weak pulldown	Active	Active	Active	ON
Mute	Switching at 50%	Active	Active	Active	ON
Normal operation	Switching with audio	Active	Active	Active	ON

Table 22. Global Faults and Actions

FAULT OR EVENT	FAULT OR EVENT CATEGORY	MONITORING MODES	REPORTING METHOD	ACTION TYPE	ACTION RESULT	LATCHED/ SELF-CLEARING
POR	Voltage fault	All	$\overline{\text{FAULT}}$ pin	Hard mute (no ramp)	Standby	Self-clearing
Undervoltage		Hi-Z, mute, normal	I^2C + $\overline{\text{FAULT}}$ pin		Hi-Z	Latched
Overvoltage						
Overtemperature warning	Thermal warning	Hi-Z, mute, normal	I^2C + $\overline{\text{OTW}}$ pin	None	None	Self-clearing
Overtemperature shutdown	Thermal fault	Hi-Z, mute, normal	I^2C + $\overline{\text{FAULT}}$ pin	Hard mute (no ramp)	Standby	Latched

Table 23. Channel Faults and Actions

FAULT OR EVENT	FAULT OR EVENT CATEGORY	MONITORING MODES	REPORTING METHOD	ACTION TYPE	ACTION RESULT	LATCHED or SELF-CLEARING
Open/short diagnostic	Diagnostic	Hi-Z (I^2C activated)	I^2C	None	None	Latched
Output clipping	Warning	Mute or play	$\overline{\text{CLIP\_OTW}}$ pin	None	None	Self-clearing
CBC load current limit	Online protection			Current limit	Start OC timer	Self-clearing
OC fault	Output channel fault		I^2C + $\overline{\text{FAULT}}$ pin	Hard mute	Hi-Z	Latched
DC detect				Hard mute	Hi-Z	Latched
OT foldback	Warning		I^2C + $\overline{\text{OTW}}$ pin	Current limit	None	Self-clearing

Power Shutdown and Restart Sequence Control

The gain ramp of the filtered output signal and the updating of the I^2C registers correspond to the $\overline{\text{MUTE}}$ pin voltage during the ramping process. The value of the external capacitor on the $\overline{\text{MUTE}}$ pin dictates the length of time that the $\overline{\text{MUTE}}$ pin takes to complete its ramp.

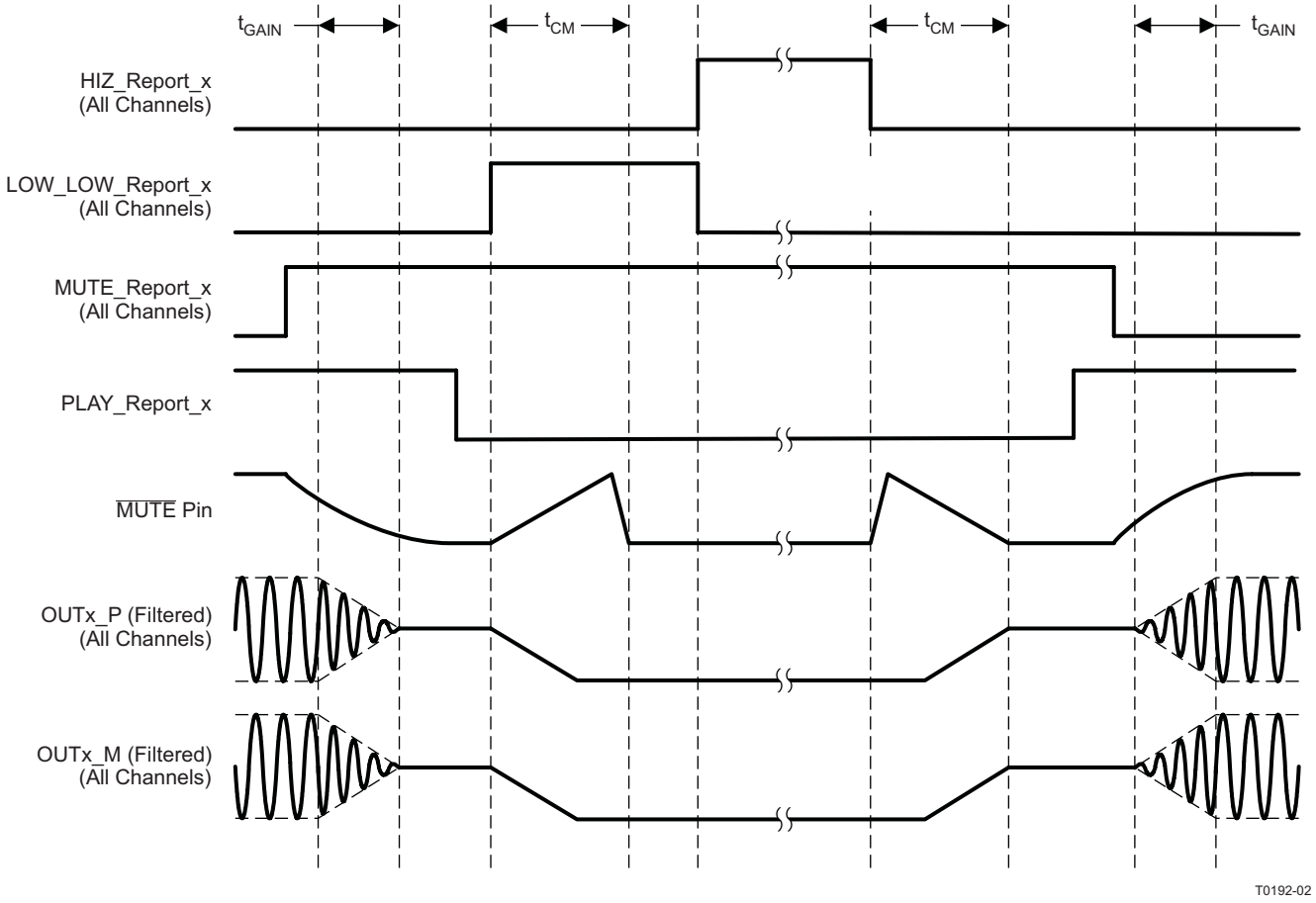


Figure 17. Click- and Pop-Free Shutdown and Restart Sequence Timing Diagram With Two Channels Sharing the Mute Pin

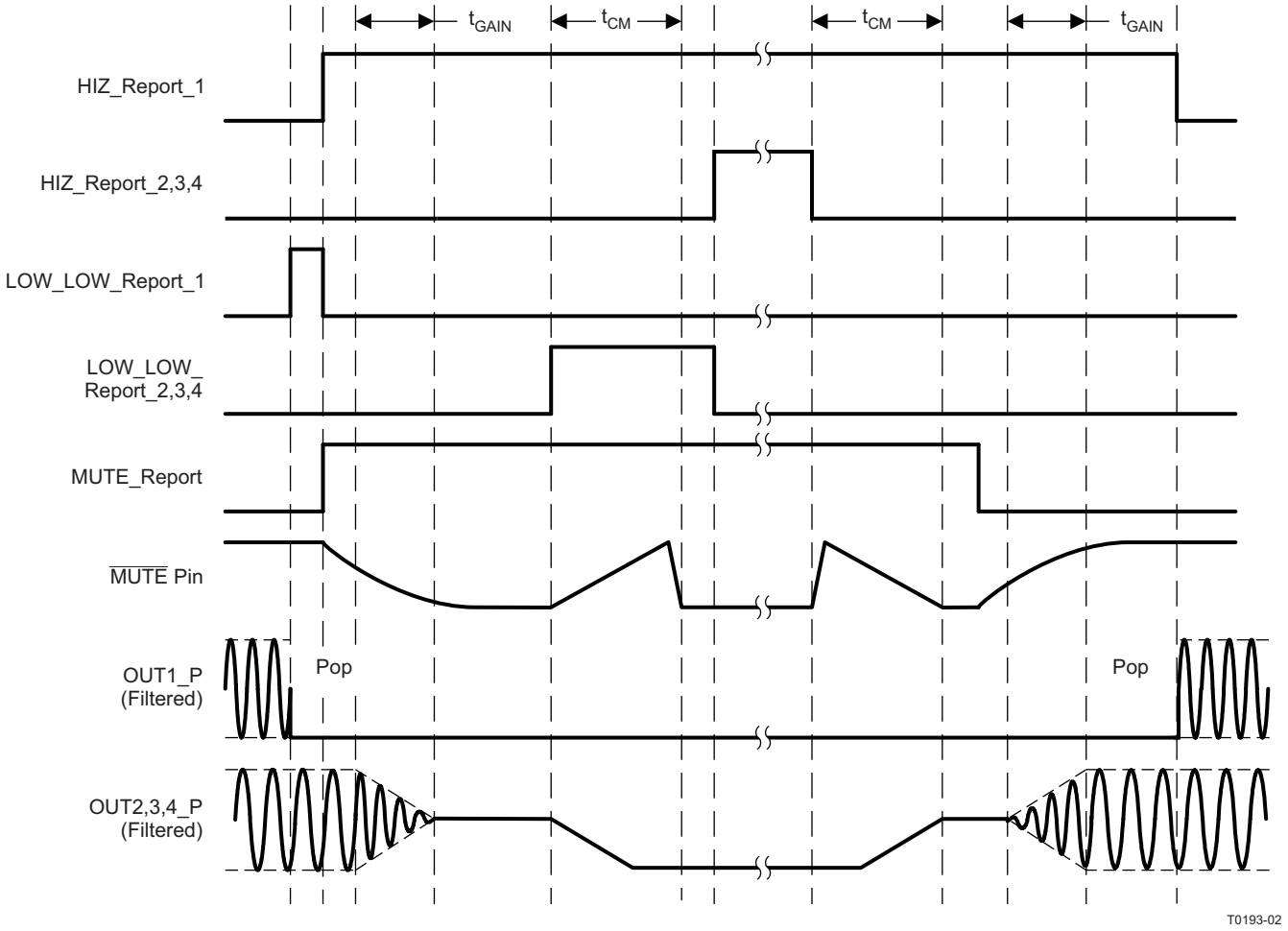


Figure 18. Individual Channel Shutdown and Restart Sequence Timing Diagram

Latched-Fault Shutdown and Restart Sequence Control

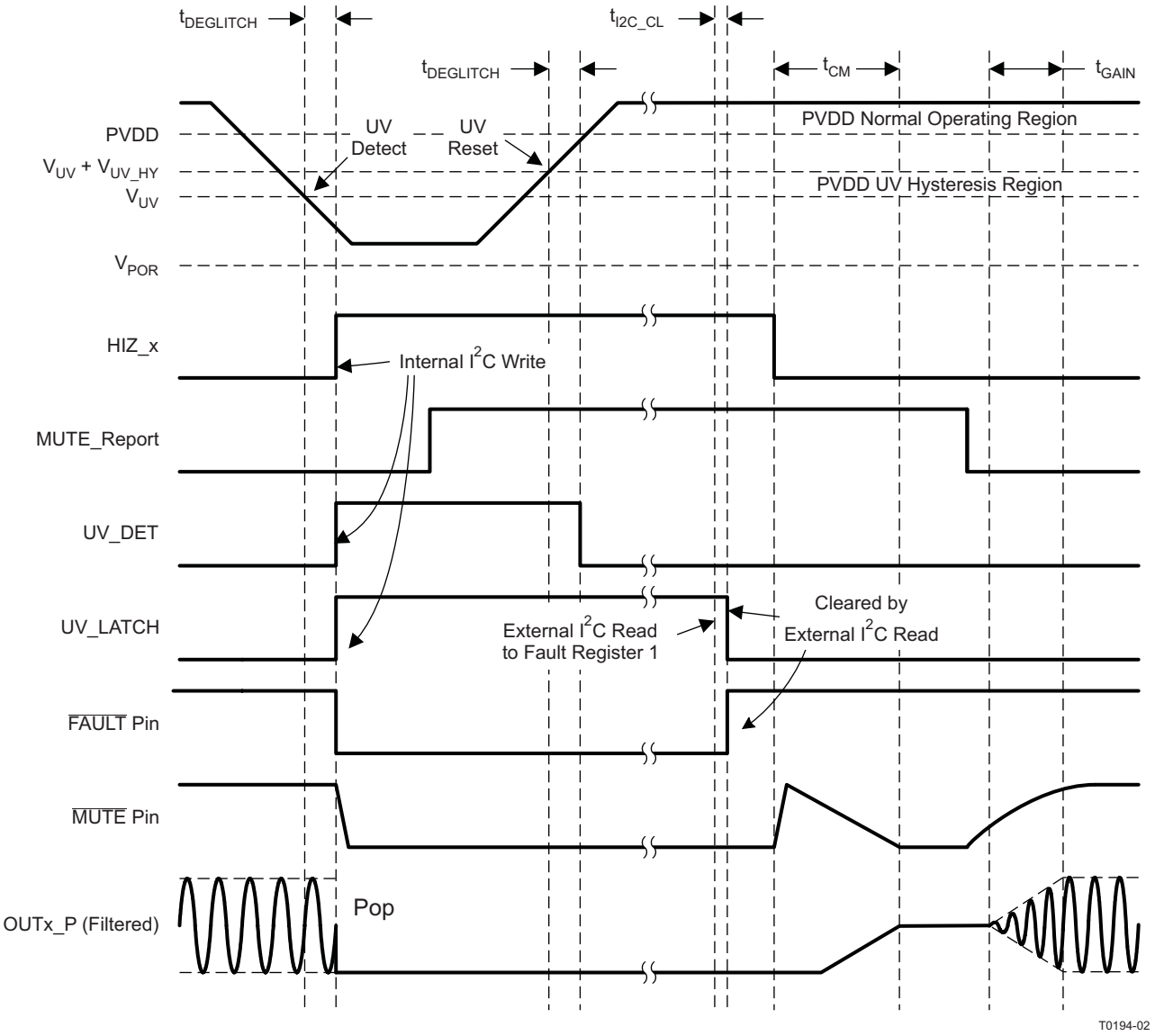


Figure 19. Latched Global-Fault Shutdown and Restart Timing Diagram (UV Shutdown and Recovery)

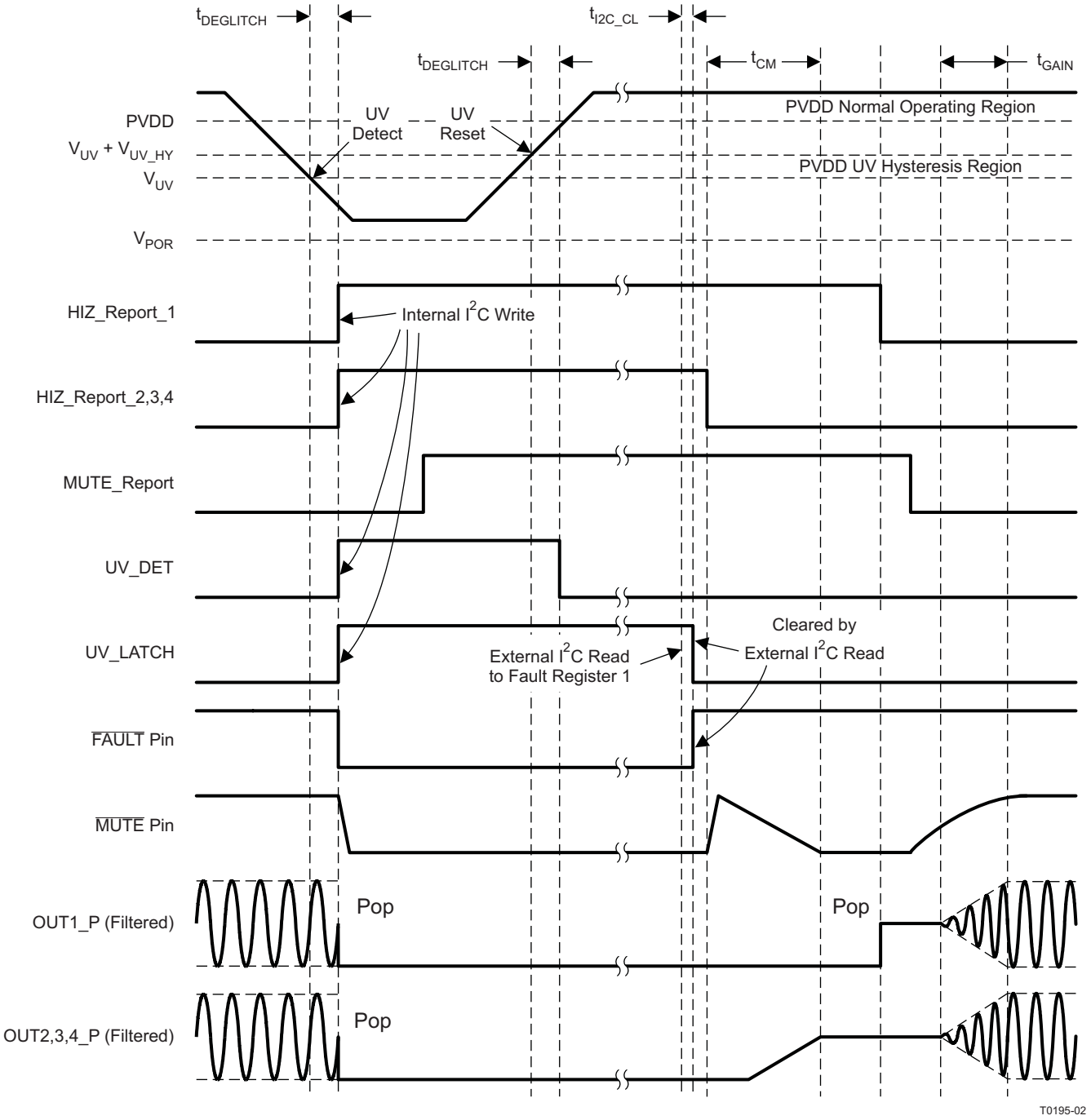


Figure 20. Latched Global-Fault Shutdown and Individual-Channel Restart Timing Diagram (UV Shutdown and Recovery)

APPLICATION INFORMATION

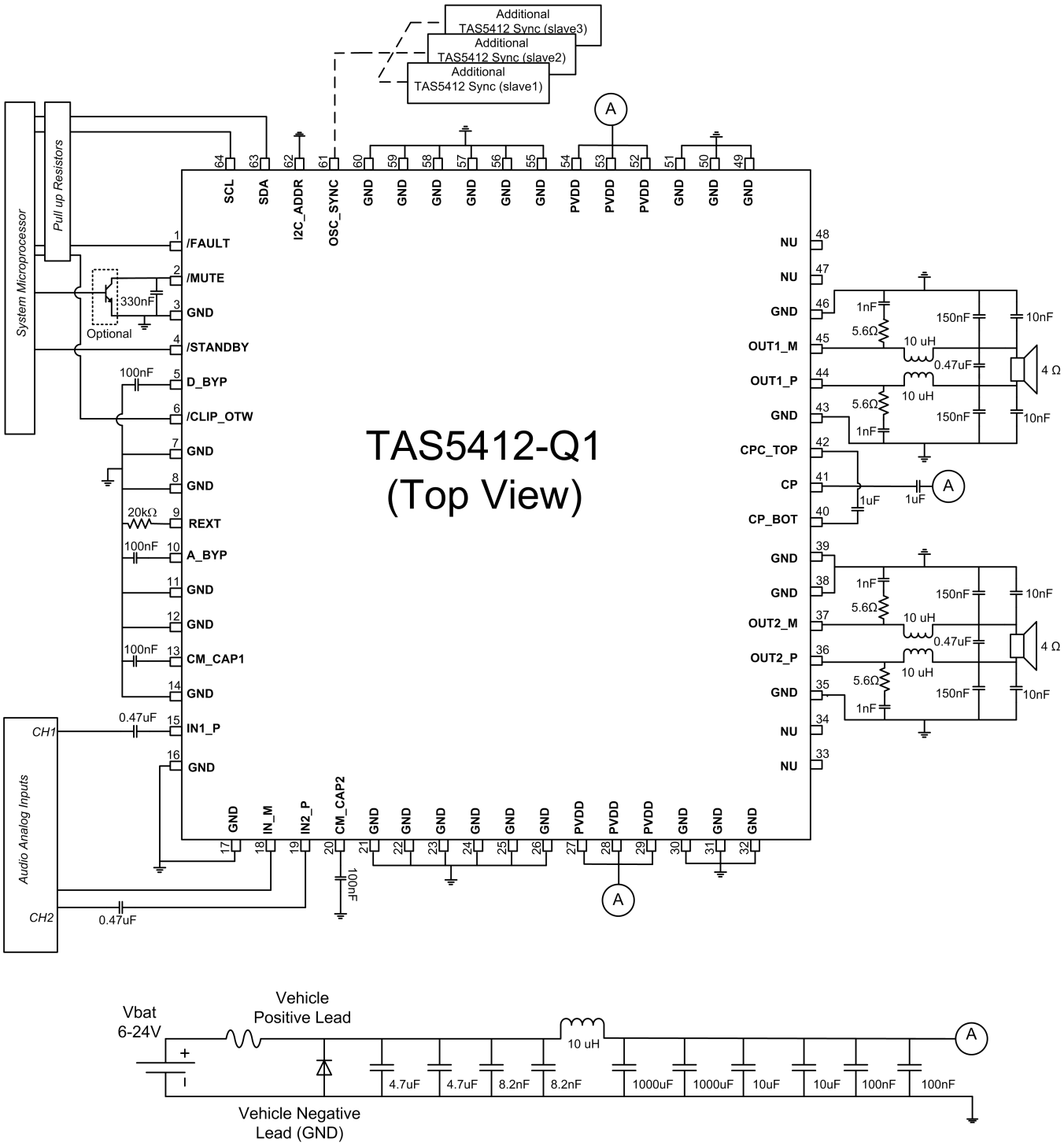


Figure 21. TAS5412-Q1 Typical Application Schematic

Parallel Operation (PBTL)

One can parallel the device outputs on the load side of the LC output filter. Parallel operation requires identical I^2C settings for any paralleled channels in order to have reliable system performance and evenly dissipated power on multiple channels. Having identical gain and current-limit settings can also prevent energy feeding back from one channel to the other. For smooth power up, power down, and mute operation, send the same control commands (such as mute, play, Hi-Z, etc.) to the paralleled channels at the same time. The device also supports load diagnostics for parallel connection. There is no support for paralleling on the device side of the LC output filter, and device failure can result.

Input Filter Design

For the TAS5412-Q1, the IN_M pin should have an impedance to GND that is equivalent to the parallel combination of the input impedances of all IN_P channels combined, including any source impedance from the previous stage in the system design. For example, if each of the two IN_P channels has a 1-µF dc blocking capacitor, 1 kΩ of series resistance due to an input RC filter, and 1 kΩ of source resistance from the DAC supplying the audio signal, the IN_M channel should have a 2-µF capacitor in series with a 1-kΩ resistor to GND (2 × 1 µF in parellel = 2 µF; 2 × 2 kΩ in parallel = 1 kΩ).

Demodulation Filter Design

High-current LDMOS transistors in an H-bridge configuration drive the amplifier outputs. These transistors are either off or on. The result is a square-wave output signal with a duty cycle that is proportional to the amplitude of the audio signal. TI recommends the use of a second-order LC filter to recover the audio signal. The main purpose of the demodulation filter is to attenuate the high-frequency components of the output signals that are out of the audio band. Design of the demodulation filter significantly affects the audio performance of the power amplifier. Therefore, to meet the device THD+N specification, carefully consider the selection of the inductors used in the output filter. The rule is that the inductance should remain stable within the range of peak current seen at maximum output power and deliver approximately 5 µH of inductance at 16 A. If this rule is observed, the device should not have distortion issues due to the output inductors. Another parameter to be considered is the idle-current loss in the inductor. This can be measured or specified as inductor dissipation (D). The target specification for dissipation is less than 0.05. If the dissipation factor is above this value, idle current increases. In general, 10-µH inductors suffice for most applications. The change in output load resistance slightly alters the frequency response of the amplifier; however, unless tight control of frequency response is necessary (better than 0.5 dB), it is not necessary to deviate from 10 µH.

Line-Driver Applications

In many automotive audio applications, the end user would like to use the same head unit to drive either a speaker (with several ohms of impedance) or an external amplifier (with several kilohms of impedance). The device is capable of supporting both applications. However, the output filter must be sized appropriately to handle the expected output load in either case (that is, one must populate different output-filter values to handle the two different cases).

Thermal Information

The thermally augmented package interfaces directly to a heat sink using a thermal interface compound (for example, Arctic Silver® Ceramique™ thermal compound.) The heat sink then absorbs heat from the IC and couples it to the local air. With proper thermal managerment this process can reach equilibrium and heat can be continually removed from the ICs. Because of the efficiency of the TAS5412-Q1, heat sinks can be smaller than those required for linear amplifiers of equivalent performance.

$R_{\theta JA}$is a system thermal resistance from junction to ambient air. As such, it is a system parameter with the following components:

- $R_{\theta JC}$ (the thermal resistance from junction to case, or in this case the heat slug)
- Thermal resistance of the thermal grease
- Heat-sink thermal resistance

One can calculate the thermal resistance of the thermal grease from the exposed heat slug area and the thermal grease manufacturer's area thermal resistance (expressed in °C-in^2/W or °C-mm^2/W). The area thermal resistance of the example thermal grease with a 0.001 inch (0.0254 mm) thick layer is about 0.007°C-in^2/W (4.52°C-mm^2/W). The approximate exposed heat slug size is as follows:

TAS5412-Q1, 64-pin PHD…….. 0.099 in^2(64 mm^2)

Dividing the example thermal grease area resistance by the area of the heat slug gives the actual resistance through the thermal grease for both parts:

TAS5412-Q1, 64-pin PHD…….. 0.07 °C/W

The thermal resistance of thermal pads is generally considerably higher than a thin layer of thermal grease. Because of its even-higher thermal resistance, do not use thermal tape at all. The heat sink vendor generally predicts heat-sink thermal resistance, modeled using a continuous-flow-dynamics (CFD) model, or measured.

Thus, for a single monaural channel in the IC, the system $R_{\theta JA}$= $R_{\theta JC}$+ thermal-grease resistance + heat-sink resistance.

The following table indicates modeled parameters for one TAS5412-Q1 IC on a heat sink. The junction temperature is set at 115°C in both cases, while delivering 20 Wrms per channel into 4-Ω loads with no clipping. Assume that the thermal grease is about 0.001 inches (0.0254 mm) thick.

Device	TAS5412-Q1, 64-Pin PHD
Ambient temperature	25°C
Power to load	20 W × 2
Power dissipation	1.90 W × 2
ΔT inside package	6.46°C
ΔT through thermal grease	0.27°C
Required heatsink thermal resistance	21.91°C/W
Junction temperature	115°C
System $R_{\theta JA}$	23.68°C/W
$R_{\theta JA}$ × power dissipation	90°C

Electrical Connection of Heat Slug and Heat Sink

Connect electrically to ground or leave floating any heat sink that connects to the heat slug of the device. Never connect the heat slug to any electrical node other than GND.

REVISION HISTORY

Changes from Revision Original (August 2013) to Revision A **Page**

- Changed data sheet from PRODUCT PREVIEW to PRODUCTION DATA 1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TAS5412TPHDRQ1	ACTIVE	HTQFP	PHD	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	TAS5412TQ1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

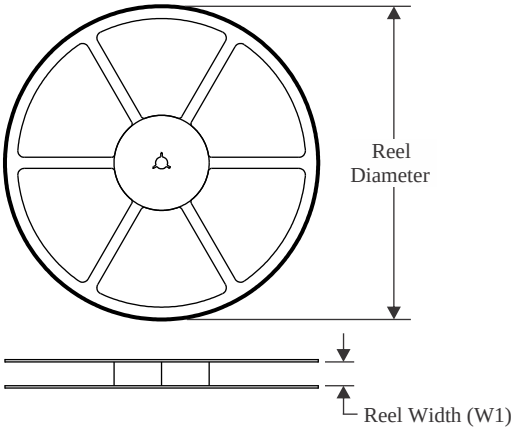
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

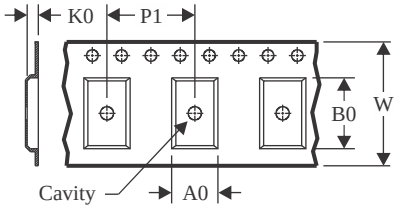
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

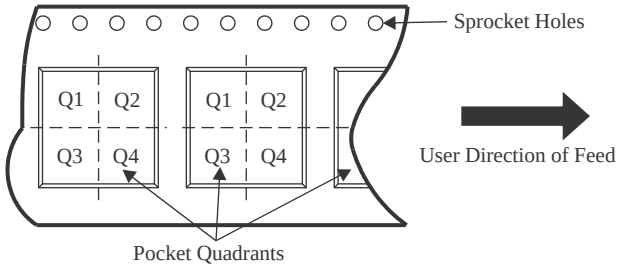


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

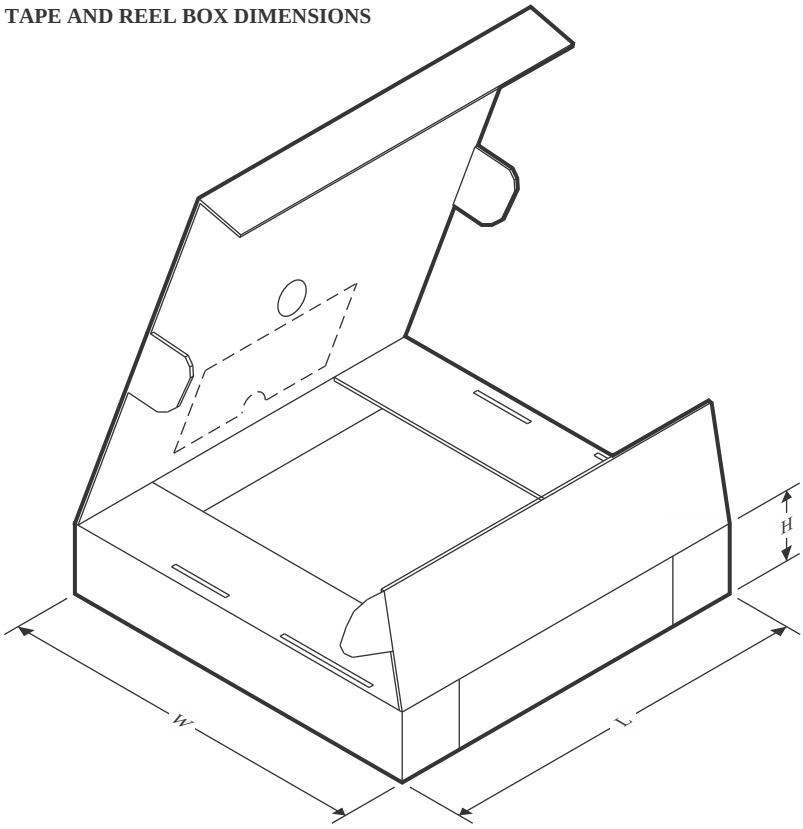
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS5412TPHDRQ1	HTQFP	PHD	64	1000	330.0	24.4	17.0	17.0	1.5	20.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS5412TPHDRQ1	HTQFP	PHD	64	1000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

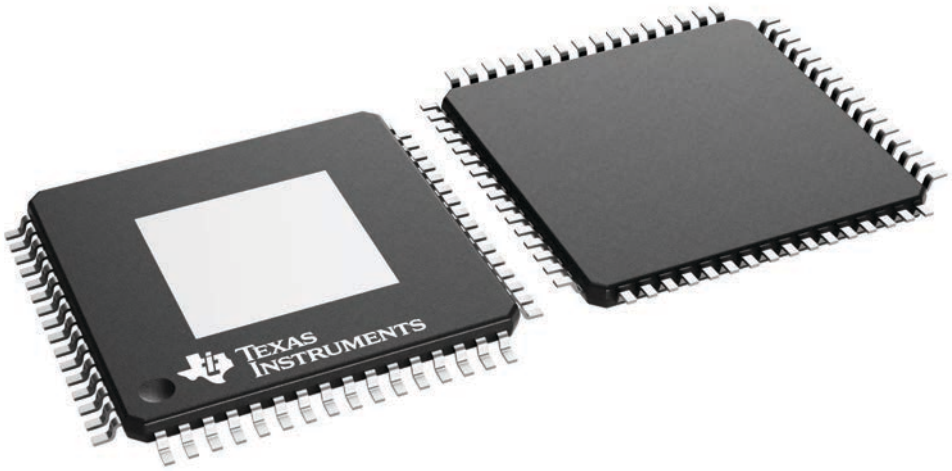
PHD 64

HTQFP - 1.2 mm max height

14 x 14, 0.8 mm pitch

PLASTIC QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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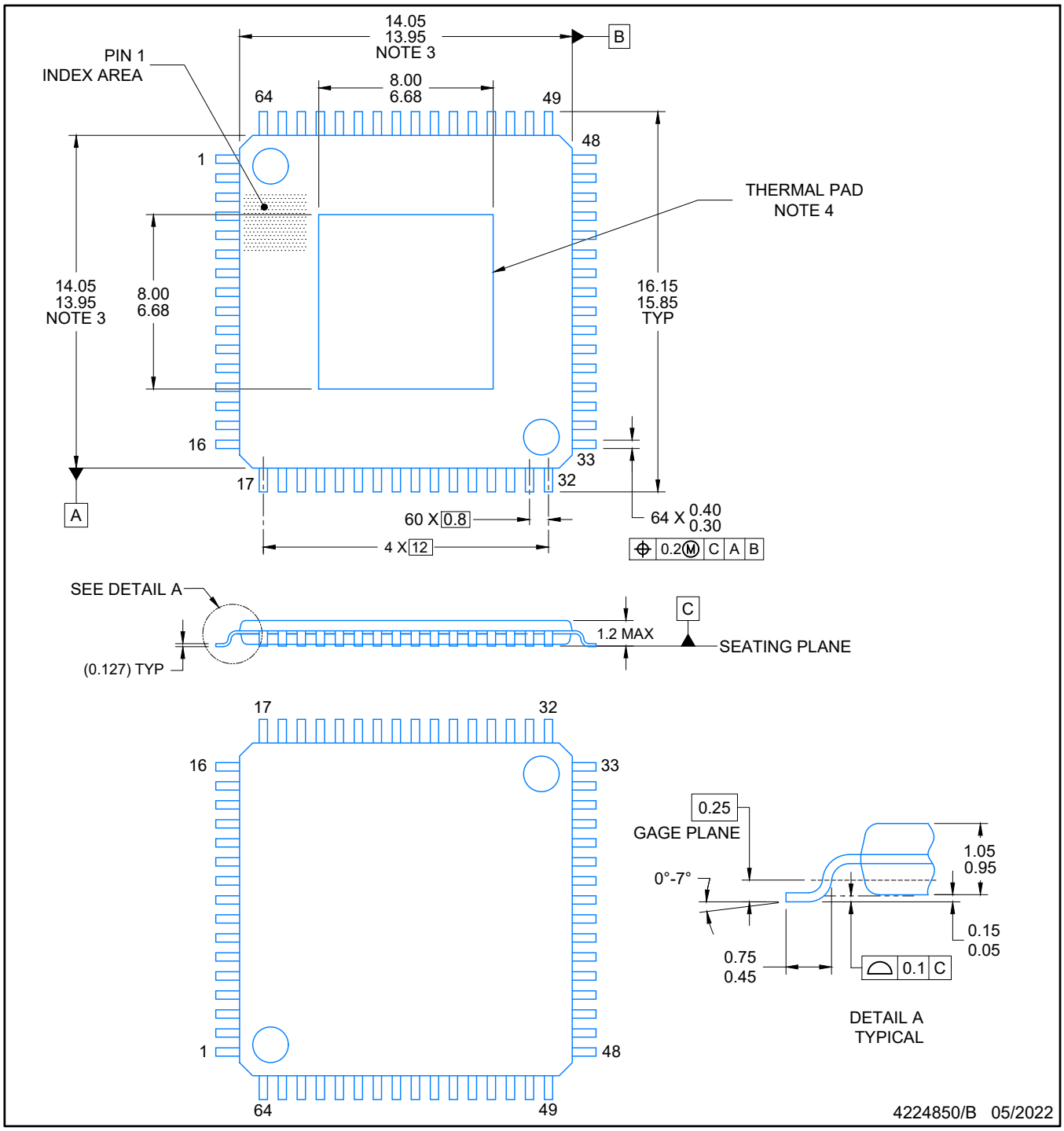
PACKAGE OUTLINE

PHD0064B

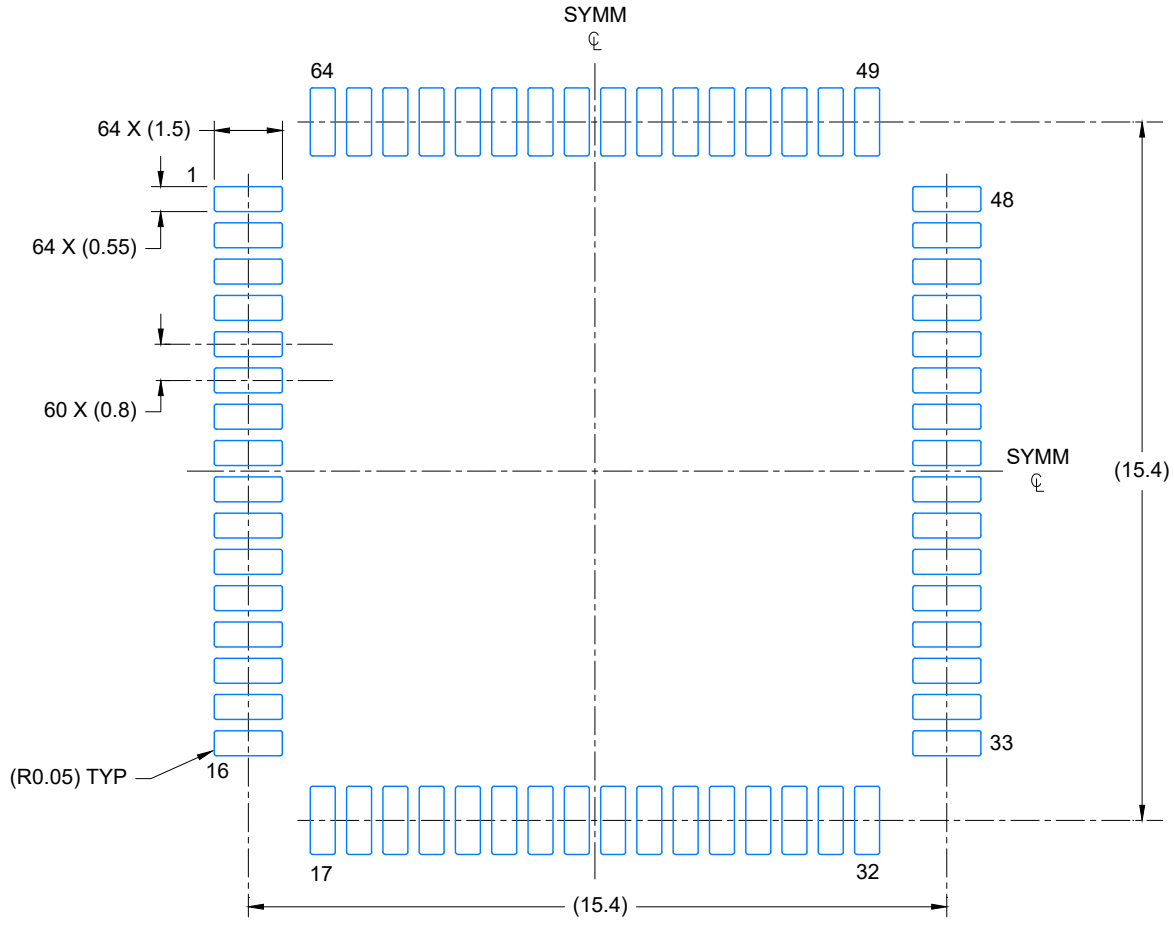
HTQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK

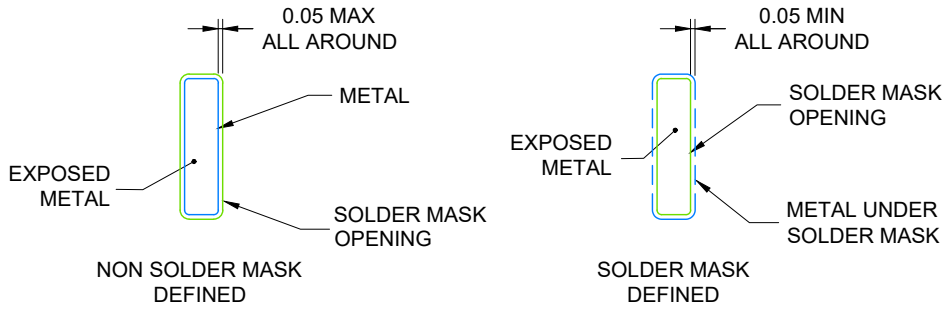


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. See technical brief. PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004) for information regarding recommended board layout.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 6X



SOLDER MASK DETAILS

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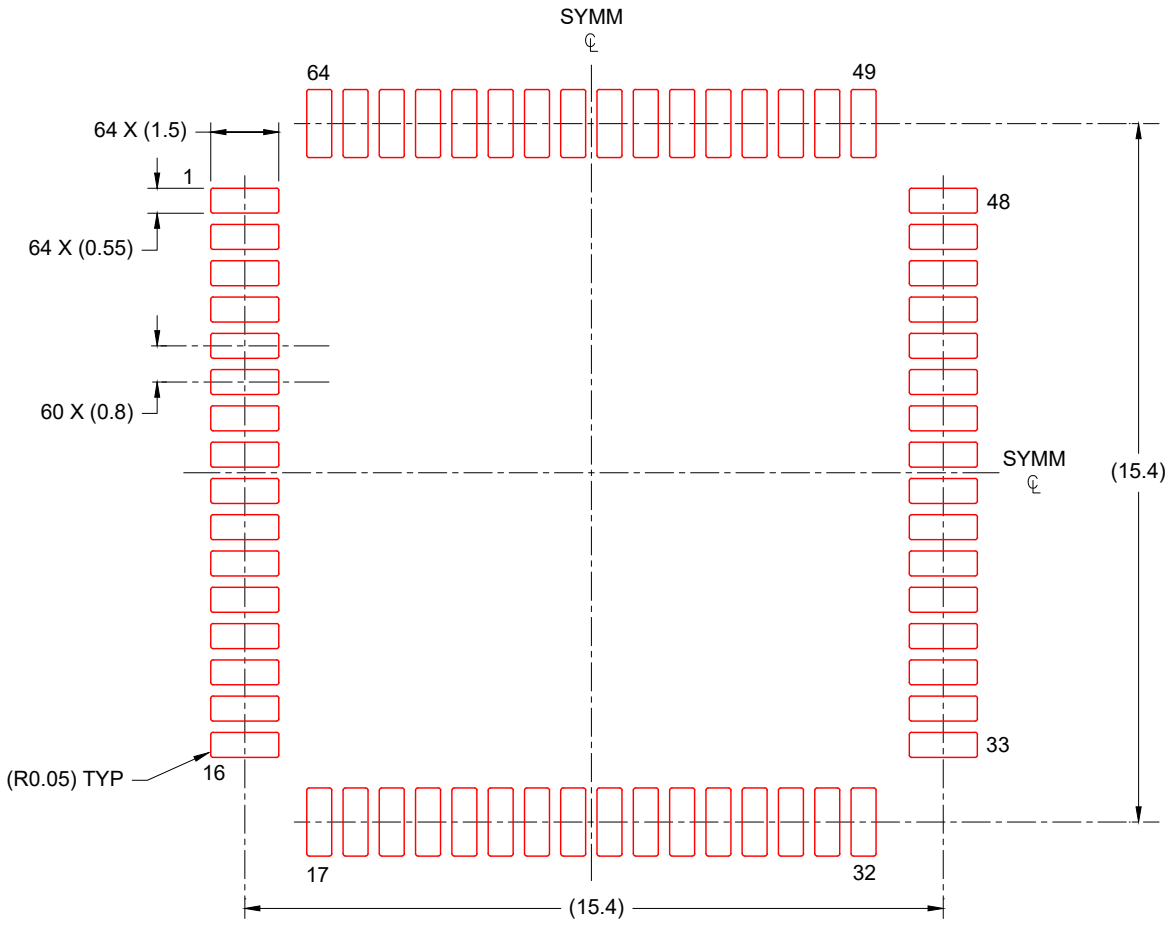
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
SCALE: 6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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