TUSB322I USB Type-C™ Configuration Channel Logic and Port Control with VCONN

1 Features

- USB Type-C™ Specification 1.1
- Backward Compatible with USB Type-C Specification 1.0
- Supports Up to 3 A of Current Advertisement and Detection
- Mode Configuration
  - Host Only – DFP/Source (I^2C Mode only)
  - Device Only – UFP/Sink (I^2C Mode only)
  - Dual Role Port – DRP
- Channel Configuration (CC)
  - Attach of USB Port Detection
  - Cable Orientation Detection
  - Role Detection
  - Type-C Current Mode (Default, Medium, High)+u
- V_{BUS} Detection
- I^2C or GPIO Control
- VCONN Support for Active Cables
- Cable Detection and Direction Control for External Switches
- Role Configuration Control through I^2C
- Supply Voltage: 4.5 V to 5.5 V
- Low Current Consumption
- Industrial Temperature Range of –40 to 85°C

2 Applications

- Host, Device, Dual Role Port Applications
- Mobile Phones
- Tablets and Notebooks
- USB Peripherals

3 Description

The TUSB322I device enables USB Type-C ports with the configuration channel (CC) logic required for Type-C ecosystems. The TUSB322I device uses the CC pins to determine port attach and detach, cable orientation, role detection, and port control for Type-C current mode. The TUSB322I device can be configured as a downstream facing port (DFP), upstream facing port (UFP), or a dual role port (DRP), making the TUSB322I device ideal for any application.

The TUSB322I device alternates configuration as a DFP or UFP according to the Type-C Specifications. The CC logic block monitors the CC1 and CC2 pins for pullup or pulldown resistances to determine when a USB port has been attached, the orientation of the cable, and the role detected. The CC logic detects the Type-C current mode as default, medium, or high depending on the role detected. V_{BUS} detection is implemented to determine a successful attach in UFP and DRP modes. The TUSB322I will supply VCONN when an active cable is detected.

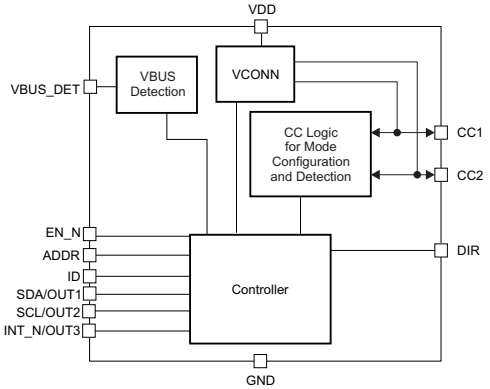
The device operates over a wide supply range and has low-power consumption. The TUSB322I device is available in industrial temperature ranges.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TUSB322I	X2QFN (12)	1.60 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



Sample Applications

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (September 2016) to Revision C — **Page**

- Changed R_{VBUS} values From: MIN = 891, TYP = 900, MAX = 909 KΩ To: MIN = 855, TYP = 887, MAX = 920 KΩ ... 6

Changes from Revision A (May 2016) to Revision B — **Page**

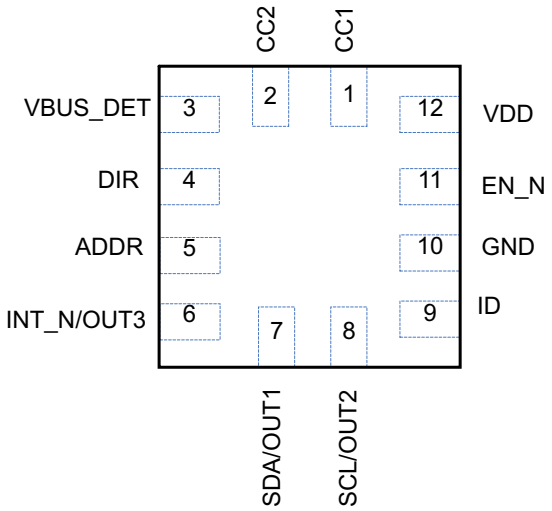
- Changed pins CC1 and CC2 values From: MIN = –0.3 MAX = V_{DD} + 0.3 To: MIN –0.3 MAX = 6 in the *Absolute Maximum Ratings* ... 4

Changes from Original (October 2015) to Revision A — **Page**

- Added Shutdown current consumption to *Electrical Characteristics* table. ... 5

5 Pin Configuration and Functions

RWB Package
12-Pin X2QFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CC1	1	I/O	Type-C configuration channel signal 1
CC2	2	I/O	Type-C configuration channel signal 2
VBUS_DET	3	I	5-V to 28-V V_{BUS} input voltage. V_{BUS} detection determines UFP attachment. One 900-kΩ external resistor required between system V_{BUS} and VBUS_DET pin.
DIR	4	O	DIR of plug. The open drain output indicates the detected plug orientation: Type-C plug position 2 (H); Type-C plug position 1 (L).
ADDR	5	I	Tri-level input pin to indicate I^2C address or GPIO mode: H - I^2C is enabled and I^2C 7-bit address is 0x67. NC - GPIO mode (I^2C is disabled) L - I^2C is enabled and I^2C 7-bit address is 0x47. ADDR pin should be pulled up to V_{DD} if high configuration is desired
INT_N/OUT3	6	O	The INT_N/OUT3 is a dual-function pin. When used as the INT_N, the pin is an open drain output in I^2C control mode and is an active low interrupt signal for indicating changes in I^2C registers. When used as OUT3, the pin is in audio accessory detect in GPIO mode: no detection (H), audio accessory connection detected (L).
SDA/OUT1	7	I/O	The SDA/OUT1 is a dual-function pin. When I^2C is enabled (ADDR pin is high or low), this pin is the I^2C communication data signal. When in GPIO mode (ADDR pin is NC), this pin is an open drain output for communicating Type-C current mode detect when the TUSB322I device is in UFP mode: default current mode detected (H); medium or high current mode detected (L).
SCL/OUT2	8	I/O	The SCL/OUT2 is a dual function pin. When I^2C is enabled (ADDR pin is high or low), this pin is the I^2C communication clock signal. When in GPIO mode (ADDR pin is NC), this pin is an open drain output for communicating Type-C current mode detect when the TUSB322I device is in UFP mode: default or medium current mode detected (H); high current mode detected (L).
ID	9	O	Open drain output; asserted low when the CC pins detect device attachment when port is a source (DFP), or dual-role (DRP) acting as source (DFP).
GND	10	G	Ground
EN_N	11	I	EN_N. Active low enable.
V_{DD}	12	P	Positive supply voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	V_{DD}	–0.3	6	V
Control pins	ADDR, ID, DIR, INT_N/OUT3, EN_N	–0.3	V_{DD} + 0.3	V
	CC1, CC2	–0.3	6	
	SDA/OUT1, SCL/OUT2	–0.3	V_{DD} + 0.3	
	VBUS_DET	–0.3	4	
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods can affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		4.5	5	5.5	V
V_{BUS}	System V_{BUS} voltage		4	5	28	V
VCONTROL	DC voltage range for control lines: ADDR, ID, DIR, INT_N/OUT3, SDA/OUT1, SCL/OUT2, EN_N, CC1, and CC2.		0		5.5	V
	DC voltage range for VBUSDET		0		4	V
VCONN	Supply for active cable (With V_{DD} at 5 V)		4.75		5.5	V
T_A	Operating free-air temperature	TUSB322I	–40	25	85	°C

6.4 Thermal Information

THERMAL METRIC(1)		TUSB322I RWB (X2QFN) 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	169.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	68.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	83.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	83.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and C Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Consumption						
$I_{SHUTDOWN\_UFP}$	Leakage current when VDD is supplied but the device is not enabled. (VDD = 5 V, EN_N = H)			0.04		µA
$I_{UNATTACHED\_UFP}$	Current consumption in unattached mode when port is unconnected and waiting for connection. (V_{DD} = 5 V, ADDR = NC, MODE_SELECT = 2'b01)			70		µA
I_{ACTIVE_UFP}	Current consumption in active mode. (V_{DD} = 5 V, ADDR = NC, MODE_SELECT = 2'b01)			70		µA
CC1 and CC2 Pins						
R_{CC_DB}	Pulldown resistor when in dead-battery mode.		4.1	5.1	6.1	kΩ
R_{CC_D}	Pulldown resistor when in UFP or DRP mode.		4.6	5.1	5.6	kΩ
$V_{UFP\_CC\_USB}$	Voltage level range for detecting a DFP attach when configured as a UFP and DFP is advertising default current source capability.		0.25		0.61	V
$V_{UFP\_CC\_MED}$	Voltage level range for detecting a DFP attach when configured as a UFP and DFP is advertising medium (1.5 A) current source capability.		0.7		1.16	V
$V_{UFP\_CC\_HIGH}$	Voltage level range for detecting a DFP attach when configured as a UFP and DFP is advertising high (3 A) current source capability.		1.31		2.04	V
$V_{TH\_DFP\_CC\_USB}$	Voltage threshold for detecting a UFP attach when configured as a DFP and advertising default current source capability.		1.51	1.6	1.64	V
$V_{TH\_DFP\_CC\_MED}$	Voltage threshold for detecting a UFP attach when configured as a DFP and advertising medium current (1.5 A) source capability.		1.51	1.6	1.64	V
$V_{TH\_DFP\_CC\_HIGH}$	Voltage threshold for detecting a UFP attach when configured as a DFP and advertising high current (3.0 A) source capability.		2.46	2.6	2.74	V
$V_{TH\_AC\_CC\_USB}$	Voltage threshold for detecting a active cable attach when configured as a DFP and advertising default current source.		0.15	0.2	0.25	V
$V_{TH\_AC\_CC\_MED}$	Voltage threshold for detecting a active cable attach when configured as a DFP and advertising medium current (1.5 A) source.		0.35	0.4	0.45	V
$V_{TH\_AC\_CC\_HIGH}$	Voltage threshold for detecting a active cable attach when configured as a DFP and advertising high current (3.0 A) source.		0.76	0.8	0.84	V
$I_{CC\_DEFAULT\_P}$	Default mode pullup current source when operating in DFP or DRP mode.		64	80	96	µA
$I_{CC\_MED\_P}$	Medium (1.5 A) mode pullup current source when operating in DFP or DRP mode.		166	180	194	µA
$I_{CC\_HIGH\_P}$	High (3 A) mode pullup current source when operating in DFP or DRP mode.(1)		304	330	356	µA
Control Pins: EN_N, ADDR, INT/OUT3, DIR, ID						
V_{IL}	Low-level control signal input voltage, (EN_N, ADDR)				0.4	V
V_{IM}	Mid-level control signal input voltage (ADDR)		0.28 × V_{DD}		0.56 × V_{DD}	V
V_{IH}	High-level control signal input voltage (EN_N, ADDR)		V_{DD} – 0.3		V_{DD}	V
I_{IH}	High-level input current		–20		20	µA
I_{IL}	Low-level input current		–10		10	µA
$I_{ID\_LEAKAGE}$	Current leakage on ID pin.	V_{DD} = 0 V; ID = 5 V			10	µA
R_{EN_N}	Internal pull-up resistance for EN_N.			1.1		MΩ
R_{pu}	Internal pullup resistance (ADDR)			588		kΩ
R_{pd}	Internal pulldown resistance (ADDR)			1.1		MΩ
V_{OL}	Low-level signal output voltage (open-drain) (INT_N/OUT3, ID)	I_{OL} = –1.6 mA			0.4	V

(1) V_{DD} must be 3.5 V or greater to advertise 3 A current.

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{p_ODext}	External pullup resistor on open drain IOs (INT_N/OUT3, ID)			200		kΩ
R_{p_TLext}	Tri-level input external pullup resistor (ADDR)			4.7		kΩ
I^2C - SDA/OUT1, SCL/OUT2 can operate from 1.8 or 3.3 V (±10%) when ADDR pin is low or high. (2)						
V_{DD_I2C}	Supply range for I^2C (SDA/OUT1, SCL/OUT2)		1.65	1.8	3.6	V
V_{IH}	High-level signal voltage		1.05			V
V_{IL}	Low-level signal voltage				0.4	V
V_{OL}	Low-level signal output voltage (open drain)	I_{OL} = –1.6 mA			0.4	V
VBUS_DET IO Pins (Connected to System V_{BUS} signal)						
V_{BUS_THR}	V_{BUS} threshold range		2.95	3.3	3.8	V
R_{VBUS}	External resistor between V_{BUS} and VBUS_DET pin		855	887	920	KΩ
R_{VBUS_PD}	Internal pulldown resistance for VBUS_DET			95		KΩ
DIR pin (Open Drain IO)						
V_{OL}	Low-level signal output voltage	I_{OL} = –1.6 mA			0.4	V
VCONN						
R_{ON}	On resistance of the VCONN power FET				1.25	Ω
V_{TOL}	Voltage tolerance on VCONN power FET				5.5	V
V_{PASS}	Voltage to pass through VCONN power FET				5.5	V
I_{VCONN}	VCONN current limit; VCONN is disconnected above the value		225	300	375	mA
C_{BULK}	Bulk capacitance on VCONN; placed on V_{DD} supply		10		200	uF

(2) When using 3.3 V for I^2C, customer must ensure V_{DD} is above 3.0 V at all times.

6.6 Timing Requirements

		MIN	NOM	MAX	UNIT
I^2C (SDA, SCL)					
$t_{SU:DAT}$	Data setup time	100			ns
$t_{HD;DAT}$	Data hold time	10			ns
$t_{SU:STA}$	Set-up time, SCL to start condition	0.6			µs
$t_{HD:STA}$	Hold time, (repeated) start condition to SCL	0.6			µs
$t_{SU:STO}$	Set up time for stop condition	0.6			µs
$t_{VD;DAT}$	Data valid time			0.9	µs
$t_{VD;ACK}$	Data valid acknowledge time			0.9	µs
t_{BUF}	Bus free time between a stop and start condition	1.3			µs
f_{SCL}	SCL clock frequency; I^2C mode for local I^2C control			400	kHz
t_r	Rise time of both SDA and SCL signals			300	ns
t_f	Fall time of both SDA and SCL signals			300	ns
C_{BUS_100KHZ}	Total capacitive load for each bus line when operating at ≤ 100 KHz			400	pF
C_{BUS_400KHZ}	Total capacitive load for each bus line when operating at 400 KHz.			100	pF

6.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{CCCB\_DEFAULT}$	Power on default of CC1 and CC2 voltage debounce time	DEBOUNCE register = 2'b00		168		ms
t_{VBUS_DB}	Debounce of VBUS_DET pin after valid V_{BUS_THR}			2		ms
$t_{DRP\_DUTY\_CYCLE}$	Power-on default of percentage of time DRP advertises DFP during a T_{DRP}	DRP_DUTY_CYCLE register = 2'b00		30%		
t_{DRP}	The period TUSB322I in DFP mode completes a DFP to UFP and back advertisement.		50	75	100	ms
t_{I2C_EN}	Time from EN_N low and V_{DD} active to I^2C access available				100	ms
t_{SOFT_RESET}	Soft reset duration		26	49	95	ms

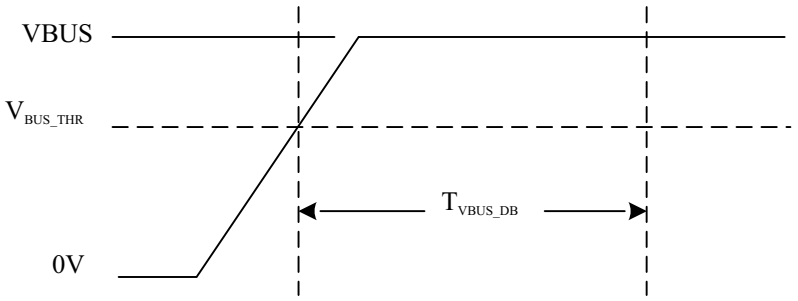


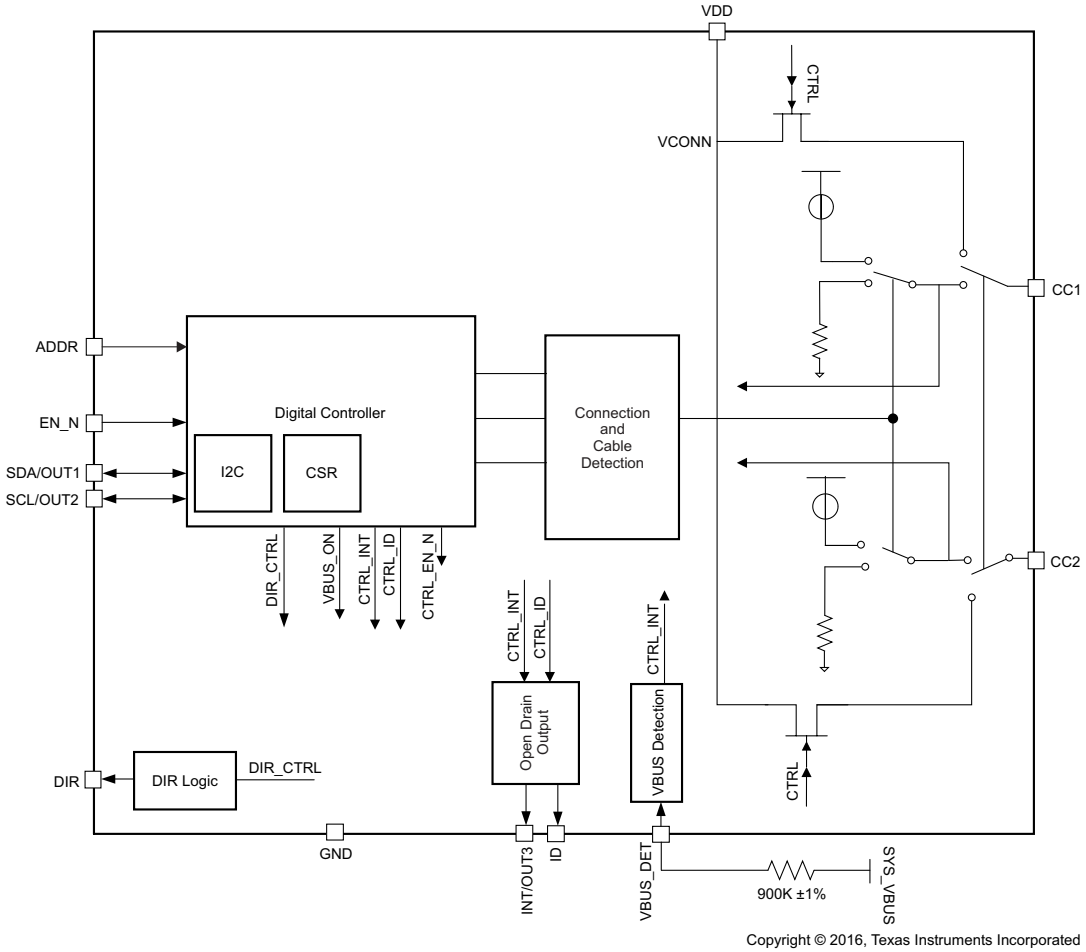
Figure 1. VBUS Detect and Debounce

7 Detailed Description

7.1 Overview

The USB Type-C ecosystem operates around a small form factor connector and cable that is flippable and reversible. Due to the nature of the connector, a scheme is required to determine the connector orientation. Additional schemes are required to determine when a USB port is attached and the acting role of the USB port (DFP, UFP, DRP), as well as to communicate Type-C current capabilities. These schemes are implemented over the CC pins according to the USB Type-C specifications. The TUSB322I device provides Configuration Channel (CC) logic for determining USB port attach and detach, role detection, cable orientation, and Type-C current mode. The TUSB322I device also contains several features such as VCONN sourcing, USB3.1 mux direction control, mode configuration, and low standby current, all of which make the TUSB322I device ideal for source or sinks in USB2.0 or USB3.1 applications.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Cables, Adapters, and Direct Connect Devices

Type-C Specification 1.1 defines several cables, plugs, and receptacles to be used to attach ports. The TUSB322I device supports all cables, receptacles, and plugs. The TUSB322I device does not support any USB feature which requires USB Power Delivery communications over CC lines, such as e-marking or alternate mode.

Feature Description (continued)

7.3.1.1 USB Type-C Receptacles and Plugs

Below is list of Type-C receptacles and plugs supported by the TUSB322I device:

- USB Type-C receptacle for USB2.0 and USB3.1 and full-featured platforms and devices
- USB full-featured Type-C plug
- USB2.0 Type-C plug

7.3.1.2 USB Type-C Cables

Below is a list of Type-C cables types supported by the TUSB322I device:

- USB full-featured Type-C cable with USB3.1 full-featured plug
- USB2.0 Type-C cable with USB2.0 plug
- Captive cable with either a USB full-featured plug or USB2.0 plug

7.3.1.3 Legacy Cables and Adapters

The TUSB322I device supports legacy cable adapters as defined by the Type-C Specification. The cable adapter must correspond to the mode configuration of the TUSB322I device.

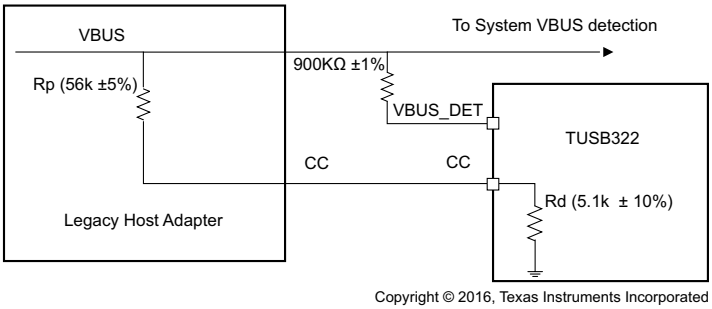


Figure 2. Legacy Adapter Implementation Circuit

7.3.1.4 Direct Connect Devices

The TUSB322I device supports the attaching and detaching of a direct-connect device.

7.3.1.5 Audio Adapters

Additionally, the TUSB322I device supports audio adapters for audio accessory mode, including:

- Passive Audio Adapter
- Charge Through Audio Adapter

7.3.2 Port Role Configuration

The TUSB322I default operation is dual-role port (DRP). The TUSB322I will always default to DRP operation anytime EN_N is asserted from high to low or I2C_SOFT_RESET bit is set. But the TUSB322I can be configured as DFP-only or UFP-only through changing the default state of the MODE_SELECT register. DFP-only and UFP-only mode is not available in GPIO mode. Table 1 lists the supported features in each mode:

Feature Description (continued)

Table 1. Supported Features for the TUSB322I Device by Mode

SUPPORTED FEATURES	DFP-Only	UFP-Only	DFP
Port attach and detach	Yes	Yes	Yes
Cable orientation (through I^2C)	Yes	Yes	Yes
Cable orientation through DIR pin	Yes	Yes	Yes
Current advertisement	Yes	—	Yes (DFP)
Current detection	—	Yes	Yes (UFP)
Accessory modes (audio and debug)	Yes	Yes	Yes
Active cable detection	Yes	—	Yes (DFP)
Try.SRC	—	—	Yes (DFP)
Try.SNK	—	—	Yes (UFP)
VCONN	Yes	—	Yes (DFP)
I^2C / GPIO	Yes	Yes	Yes
Legacy cables	Yes	Yes	Yes
V_{BUS} detection	—	Yes	Yes (UFP)

7.3.2.1 Downstream Facing Port (DFP) - Source

The TUSB322I device can be configured as a DFP-only device by changing the MODE_SELECT register default setting. In DFP mode, the TUSB322I device constantly presents Rps on both CC. In DFP mode, the TUSB322I device initially advertises default USB Type-C current. The Type-C current can be adjusted through I^2C if the system is required to increase the amount advertised. The TUSB322I device adjusts the Rps to match the desired Type-C current advertisement. As a DFP, the TUSB322I monitors the voltage level on CC pins looking for the Rd termination of a UFP. When a UFP is detected and TUSB322I is in the Attached.SRC state, the TUSB322I will supply VCONN on the CC pin that has Ra.

The following list describes the steps for enabling DFP-only.

1. Write a 1'b1 to DISABLE_TERM register (address 0x0A bit 0)

2. Write a 2'b10 to MODE_SELECT register (address 0x0A bits 5:4)

3. Write a 1'b0 to DISABLE_TERM register (address 0x0A bit 0)

When configured as a DFP, the TUSB322I can operate with older USB Type-C 1.0 devices except for a USB Type-C 1.0 DRP device. The TUSB322I cannot operate with a USB Type-C 1.0 DRP device. The limitation is a result of a backwards compatibility problem between USB Type-C 1.1 DFP and a USB Type-C 1.0 DRP.

7.3.2.2 Upstream Facing Port (UFP) - Sink

The TUSB322I device can be configured as a UFP-only by changing the MODE_SELECT register default setting. In UFP mode, the TUSB322I device constantly presents pulldown resistors (Rd) on both CC pins. The TUSB322I device monitors the CC pins for the voltage level corresponding to the Type-C mode current advertisement by the connected DFP. The TUSB322I device debounces the CC pins and wait for V_{BUS} detection before successfully attaching. As a UFP, the TUSB322I device detects and communicates the advertised current level of the DFP to the system through the I^2C CURRENT_MODE_DETECT register once in the Attached.SNK state.

Steps for enabling UFP-only:

1. Write a 1'b1 to DISABLE_TERM register (address 0x0A bit 0).

2. Write a 2'b01 to MODE_SELECT register (address 0x0A bits 5:4)

3. Write a 1'b0 to DISABLE_TERM register (address 0x0A bit 0).

7.3.2.3 Dual Role Port (DRP)

The TUSB322I default operation is a dual-role port controller. As a DRP, the TUSB322I can operate as a UFP (sink) or a DFP (source). In DFP mode, the TUSB322I toggles between presenting as a DFP (Rp on both CC pins) and presenting as a UFP (Rd on both CC pins).

When presenting as a DFP, the TUSB322I monitors the voltage level on the CC pins looking for the Rd termination of a UFP. When a UFP is detected and TUSB322I is in the Attached.SRC state, the TUSB322I will pull the ID pin low to indicate to the system the port is attached to a sink (UFP). Additionally, when a UFP is detected, the TUSB322I will supply VCONN on the unconnected CC pin if Ra is also detected. In DFP mode, the TUSB322I will initially advertise default USB Type-C current. The Type-C Current can be adjusted through I2C if the system wishes to increase the amount advertised. TUSB322I will adjust the Rps to match the desired Type-C Current advertisement. In GPIO mode, the TUSB322I will only advertise default Type C current.

When presenting as a UFP, the TUSB322I monitors the CC pins for the voltage level corresponding to the Type-C mode current advertisement by the connected DFP. The TUSB322I will debounce the CC pins and wait for VBUS detection before successfully attaching. As a UFP, the TUSB322I will detect and communicate the DFP's advertised current level to the system through the OUT1 and OUT2 GPIOs (if in GPIO mode) or through the I2C CURRENT_MODE_DETECT register once in the Attached.SNK state.

The TUSB322I supports two optional Type-C DRP features called Try.SRC and Try.SNK. Products supporting dual-role functionality can have a requirement to be a source (DFP) or a sink (UFP) when connected to another dual-role capable product. For example, a dual-role capable notebook can be used as a source when connected to a tablet, or a cell phone could be a sink when connected to a notebook or tablet. When standard DRP products (products which don't support either Try.SRC or Try.SNK) are connected together, the role (UFP or DFP) outcome is not predetermined. These two optional DRP features provide a means for dual-role capable products to connect to another dual-role capable product in the role desired. Try.SRC and Try.SNK are only available when TUSB322I is configured in I2C mode. When operating in GPIO mode, the TUSB322I will always operate as a standard DRP.

The Try.SRC feature of the TUSB322I device provides a means for a DRP product to connect as a DFP when connected to another DRP product that doesn't implement Try.SRC. When two products which implement Try.SRC are connected together, the role outcome of either UFP or DFP is the same as a standard DRP. Try.SRC is enabled by changing I2C register SOURCE_PREF to 2'b11. Once the register is changed to 2'b11, the TUSB322I will always attempt to connect as a DFP when attached to another DRP capable device.

7.3.3 Type-C Current Mode

When a valid cable detection and attach have been completed, the DFP has the option to advertise the level of Type-C current a UFP can sink. The default current advertisement for the TUSB322I device is 500 mA (for USB2.0) or 900 mA (for USB3.1). If a higher level of current is available, the I^2C registers can be written to provide medium current at 1.5 A or high current at 3 A. When the CURRENT_MODE_ADVERTISE register has been written to advertise higher than default current, the DFP adjusts the Rps for the specified current level. If a DFP advertises 3 A, it ensures that the V_{DD} of the TUSB322I device is 3.5 V or greater. Table 2 lists the Type-C current advertisements in GPIO an I^2C modes.

Table 2. Type-C Current Advertisement for GPIO and I^2C Modes

TYPE-C CURRENT		GPIO MODE (ADDR PIN IN NC)		I^2C MODE (ADDR PIN H, L)	
		UFP IN DRP MODE	DFP IN DRP MODE	UFP	DFP
Default	500 mA (USB2.0) 900 mA (USB3.1)	Current mode detected and output through OUT1 / OUT2	Only advertisement	Current mode detected and read through I^2C register	I^2C register default is 500 or 900 mA
Medium - 1.5 A			N/A		Advertisement selected through writing I^2C register
High - 3 A					

7.3.4 Accessory Support

The TUSB322I device supports audio and debug accessories in UFP, DFP mode and DRP mode. Audio and debug accessory support is provided through reading of I^2C registers. Audio accessory is also supported through GPIO mode with INT_N/OUT3 pin (audio accessory is detected when INT_N/OUT3 pin is low).

7.3.4.1 Audio Accessory

Audio accessory mode is supported through two types of adapters. First, the passive audio adapter can be used to convert the Type-C connector into an audio port. To effectively detect the passive audio adapter, the TUSB322I device must detect a resistance that is less than Ra on both of the CC pins.

Secondly, a charge through audio adapter can be used. The primary difference between a passive and charge through adapter is that the charge through adapter supplies 500 mA of current over VBUS. The charge through adapter contains a receptacle and a plug. The plug acts as a DFP and supplies V_{BUS} when the plug detects a connection.

When the TUSB322I device is configured in GPIO mode, OUT3 pin determines if an audio accessory is connected. When an audio accessory is detected, the OUT3 pin is pulled low.

7.3.4.2 Debug Accessory

Debug is an additional state supported by USB Type-C. The specification does not define a specific user scenario for this state, but the end user could use debug accessory mode to enter a test state for production specific to the application. Charge through debug accessory is not supported by TUSB322I when in DRP or UFP mode. The TUSB322I when configured as a DFP-only or as a DRP acting as a DFP will detect a debug accessory which presents Rd on both CC1 and CC2 pins. The TUSB322I will set ACCESSORY_CONNECTED register to 3'b110 to indicate a UFP debug accessory. The TUSB322I when configured as a UFP-only or as a DRP acting as a UFP will detect a debug accessory which presents Rp on both CC1 and CC2 pins. The TUSB322I will set ACCESSORY_CONNECTED register to 3b'111 to indicate a DFP debug accessory.

7.3.5 I^2C and GPIO Control

The TUSB322I device can be configured for I^2C communication or GPIO outputs using the ADDR pin. The ADDR pin is a tri-level control pin. When the ADDR pin is left floating (NC), the TUSB322I device is in GPIO output mode. When the ADDR pin is pulled high or pulled low, the TUSB322I device is in I^2C mode.

All outputs for the TUSB322I device are open drain configuration.

The OUT1 and OUT2 pins are used to output the Type-C current mode when in GPIO mode. Additionally, the OUT3 pin is used to communicate the audio accessory mode in GPIO mode. Table 3 lists the output pin settings. See for more information on the pins and their uses.

Table 3. Simplified Operation for OUT1 and OUT2

OUT1	OUT2	DESCRIPTION
H	H	Default current in unattached state
H	L	Default current in attached state
L	H	Medium current (1.5 A) in attached state
L	L	High current (3.0 A) in attached state

When operating in I^2C mode, the TUSB322I device uses the SCL and SDA lines for clock and data and the INT_N pin to communicate a change in I^2C registers, or an interrupt, to the system. The INT_N pin is pulled low when the TUSB322I device updates the registers with new information. The INT_N pin is open drain. The INTERRUPT_STATUS register will be set when the INT_N pin is pulled low. To clear the INTERRUPT_STATUS register, the end user writes to I^2C.

When operating in GPIO mode, the OUT3 pin is used in place of the INT_N pin to determine if an audio accessory is detected and attached. The OUT3 pin is pulled low when an audio accessory is detected.

NOTE

When using the 3.3-V supply for I^2C, the end user must ensure that the V_{DD} is 3 V and above. Otherwise the I^2C can back power the device.

7.3.6 V_{BUS} Detection

The TUSB322I device supports V_{BUS} detection according to the Type-C Specification. V_{BUS} detection is used to determine the attachment and detachment of a UFP and to determine the entering and exiting of accessary modes. V_{BUS} detection is also used to successfully resolve the role in DRP mode.

The system V_{BUS} voltage must be routed through a 900-kΩ resistor to the VBUS_DET pin on the TUSB322I device.

7.3.7 Cable Orientation and External MUX Control

The TUSB322I device has the ability to control an external/discrete MUX using the DIR pin. The TUSB322I detects the cable orientation by monitoring the voltage on the CC pins. When a voltage level within the proper threshold is detected on CC1, the DIR pin is pulled low. When a voltage level within the proper threshold is detected on CC2, the DIR is pulled high. The DIR pin is an open drain output. The I^2C communicates the cable orientation status for the TUSB322I device.

7.3.8 VCONN Support for Active Cables

The TUSB322I device supplies VCONN to active cables when configured in DFP mode or in DRP acting as a DFP mode. VCONN is provided only when the unconnected CC pin is terminated to a resistance, Ra, and after a UFP is detected and the Attached.SRC state is entered. When in DFP mode or in DRP acting as a DFP mode, a 5-V source must be connected to the VDD pin of the TUSB322I device after Attached.SRC. VCONN is supplied from VDD through a low resistance power FET out to the unconnected CC pin. VCONN is removed when a detach event is detected and the active cable is removed.

7.4 Device Functional Modes

The TUSB322I device has four functional modes. Table 4 lists these modes:

Table 4. USB Type-C States According to TUSB322I Functional Modes

MODES	GENERAL BEHAVIOR	MODE	STATES(1)
Unattached	USB port unattached. ID, PORT operational. I^2C on.	UFP-Only	Unattached.SNK
			AttachWait.SNK
		DRP	Toggle Unattached.SNK → Unattached.SRC
			AttachedWait.SRC or AttachedWait.SNK
		DFP-Only	Unattached.SRC
			AttachWait.SRC
Active	USB port attached. All GPIOs operational. I^2C on.	UFP-Only	Attached.SNK
			Audio Accessory
			Debug Accessory
		DRP	Attached.SNK
			Attached.SRC
			Audio accessory
			Debug accessory
		DFP-Only	Attached.SRC
			Audio accessory
			Debug accessory
Dead battery	No operation. V_{DD} not available.	DRP	Default device state to UFP/SNK with Rd.
Shutdown	No operation. V_{DD} available and EN_N pin high	DRP	Default device state to UFP/SNK with Rd.

(1) Required; not in sequential order.

7.4.1 Unattached Mode

Unattached mode is the primary mode of operation for the TUSB322I device, because a USB port can be unattached for a lengthy period of time. In unattached mode, V_{DD} is available, and all IOs and I^2C are operational. After the TUSB322I device is powered up, the part enters unattached mode until a successful attach has been determined. Initially, right after power up, the TUSB322I device comes up as an Unattached.SNK. The TUSB322I device toggles between the UFP and the DFP if configured as a DRP.

7.4.2 Active Mode

Active mode is defined as the port being attached. In active mode, all GPIOs are operational, and I^2C is read / write (R/W). When in active mode, the TUSB322I device communicates to the AP that the USB port is attached. This communication happens through the ID pin if TUSB322I is configured as a DFP or DRP connect as source. If TUSB322I is configured as a UFP or a DRP connected as a sink, the OUT1/OUT2 and INT_N/OUT3 pins are used. The TUSB322I device exits active mode under the following conditions:

- Cable unplug
- V_{BUS} removal if attached as a UFP
- Dead battery; system battery or supply is removed
- EN_N is floated or pulled high.

7.4.3 Shutdown Mode

Shutdown mode for TUSB322I is defined as follows:

- Supply voltage available and EN_N pin is high or floating.
- EN_N pin has internal pullup resistor
- The TUSB322I device is off, but still maintains the Rd on the CC pins.

7.4.4 Dead Battery Mode

During dead battery mode, V_{DD} is not available. CC pins always default to pulldown resistors in dead battery mode. Dead battery mode means:

- TUSB322I in UFP with 5.1 kΩ ± 20% Rd; cable connected and providing charge
- TUSB322I in UFP with 5.1 kΩ ± 20% Rd; nothing connected (application could be off or have a discharged battery)

NOTE

When V_{DD} is off, the TUSB322I non-failsafe pins (DIR, VBUS_DET, ADDR, OUT[3:1] pins) could back-drive the TUSB322I device if not handled properly. When necessary to pull these pins up, TI recommends pulling up DIR, ADDR, and INT_N/OUT3 to the device's V_{DD} supply. The VBUS_DET must be pulled up to V_{BUS} through a 900-kΩ resistor.

7.5 Programming

For further programmability, the TUSB322I device can be controlled using I²C. The TUSB322I device local I²C interface is available for reading/writing after T_{I2C_EN} when the device is powered up. The SCL and SDA terminals are used for I²C clock and I²C data respectively. If I²C is the preferred method of control, the ADDR pin must be set accordingly.

Table 5. TUSB322I I²C Addresses

TUSB322I I²C Target Address								
ADDR pin	**Bit 7 (MSB)**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0 (W/R)**
H	1	1	0	0	1	1	1	0/1
L	1	0	0	0	1	1	1	0/1

The following procedure should be followed to write to TUSB322I I²C registers:

1. The master initiates a write operation by generating a start condition (S), followed by the TUSB322I 7-bit address and a zero-value R/W bit to indicate a write cycle
2. The TUSB322I device acknowledges the address cycle
3. The master presents the sub-address (I²C register within the TUSB322I device) to be written, consisting of one byte of data, MSB-first
4. The TUSB322I device acknowledges the sub-address cycle
5. The master presents the first byte of data to be written to the I²C register
6. The TUSB322I device acknowledges the byte transfer
7. The master can continue presenting additional bytes of data to be written, with each byte transfer completing with an acknowledge from the TUSB322I device
8. The master terminates the write operation by generating a stop condition (P)

The following procedure should be followed to read the TUSB322I I²C registers:

1. The master initiates a read operation by generating a start condition (S), followed by the TUSB322I 7-bit address and a one-value R/W bit to indicate a read cycle
2. The TUSB322I device acknowledges the address cycle
3. The TUSB322I device transmits the contents of the memory registers MSB-first starting at register 00h or last read sub-address+1. If a write to the T I²C register occurred prior to the read, then the TUSB322I device starts at the sub-address specified in the write.
4. The TUSB322I device waits for either an acknowledge (ACK) or a not-acknowledge (NACK) from the master after each byte transfer; the I²C master acknowledges reception of each data byte transfer
5. If an ACK is received, the TUSB322I device transmits the next byte of data
6. The master terminates the read operation by generating a stop condition (P)

The following procedure should be followed for setting a starting sub-address for I²C reads:

1. The master initiates a write operation by generating a start condition (S), followed by the TUSB322I 7-bit address and a zero-value R/W bit to indicate a read cycle
2. The TUSB322I device acknowledges the address cycle
3. The master presents the sub-address (I²C register within the TUSB322I device) to be read, consisting of one byte of data, MSB-first
4. The TUSB322I device acknowledges the sub-address cycle
5. The master terminates the read operation by generating a stop condition (P)

NOTE

If no sub-addressing is included for the read procedure, then the reads start at register offset 00h and continue byte-by-byte through the registers until the I²C master terminates the read operation. If a I²C address write occurred prior to the read, then the reads start at the sub-address specified by the address write.

7.6 Register Maps

7.6.1 CSR Registers

Table 6. CSR Registers

Offset	Reset	Register Name	Section
0x07 through 0x00	[0x00, 0x54, 0x55, 0x53, 0x42, 0x33, 0x32, 0x32]	Device Identification	*Device Identification Register*
0x08	0x00	Connection Status	*Connection Status Register*
0x09	0x20	Connection Status and Control	*Connection Status and Control Register*
0x0A	0x00	General Control	*General Control Register*
0xA0	0x02	Device Revision	*Device Revision Register*

7.6.1.1 Device Identification Register (offset = 0x07 through 0x00) [reset = 0x00, 0x54, 0x55, 0x53, 0x42, 0x33, 0x32, 0x32]

Figure 3. Device Identification Register

7	6	5	4	3	2	1	0
DEVICE_ID							
R-0							

LEGEND: R = Read only; -*n* = value after reset

Table 7. Device Identification Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DEVICE_ID	R		For the TUSB322I device these fields return a string of ASCII characters returning TUSB322I Addresses 0x07 - 0x00 = {0x00, 0x54, 0x55, 0x53, 0x42, 0x33, 0x32, 0x32}

7.6.1.2 Connection Status Register (offset = 0x08) [reset = 0x00]

Figure 4. Connection Status Register

7	6	5	4	3	2	1	0
CURRENT_MODE_ADVERTISE		CURRENT_MODE_DETECT		ACCESSORY_CONNECTED			ACTIVE_CABLE_DETECTION
RW		RU		RU			RU

LEGEND: R/W = Read/Write; R/U = Read/Update

Table 8. Connection Status Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	CURRENT_MODE_ADVERTISE	R	2'b00	These bits are programmed by the application to raise the current advertisement from default. 00 – Default (500 mA / 900 mA) initial value at startup 01 – Mid (1.5 A) 10 – High (3 A) 11 – Reserved
5-4	CURRENT_MODE_DETECT	RU	2'b00	These bits are set when a UFP determines the Type-C Current mode. 00 – Default (value at start up) 01 – Medium 10 – Charge through accessory – 500 mA 11 – High

Table 8. Connection Status Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-1	ACCESSORY_CONNECTED	RU	2'b00	These bits are read by the application to determine if an accessory was attached. 000 – No accessory attached (default) 001 – Reserved 010 – Reserved 011 – Reserved 100 – Audio accessory 101 – Audio charged thru accessory 110 – Debug accessory when TUSB322I is connected as a DFP. 111 – Debug accessory when TUSB322I is connected as a UFP.
0	ACTIVE_CABLE_DETECTION	RU	1'b0	This flag indicates that an active cable has been plugged into the Type-C connector. When this field is set, an active cable is detected.

7.6.1.3 Connection Status and Control Register (offset = 0x09) [reset = 0x20]

Figure 5. Connection Status and Control Register

7	6	5	4	3	2	1	0
ATTACHED_STATE		CABLE_DIR	INTERRUPT_STATUS	VCONN_FAULT	DRP_DUTY_CYCLE		DISABLE_UFP_ACCESSORY
RU		RU	RCU	RCU	RW		RW

LEGEND: R/W = Read/Write; R/U = Read/Update; R/C/U = Read/Clear/Update

Table 9. Connection Status and Control Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	ATTACHED_STATE	RU	2'b00	This is an additional method to communicate attach other than the ID pin. These bits can be read by the application to determine what was attached. 00 – Not attached (default) 01 – Attached.SRC (DFP) 10 – Attached.SNK (UFP) 11 – Attached to an accessory
5	CABLE_DIR	RU	1'b1	Cable orientation. The application can read these bits for cable orientation information. 0 – CC1 1 – CC2 (default)
4	INTERRUPT_STATUS	RCU	1'b0	The INT pin is pulled low whenever a CSR changes. When a CSR change has occurred this bit should be held at 1 until the application clears it. 0 – Clear 1 – Interrupt (When INT_N is pulled low, this bit will be 1. This bit is 1 whenever any CSR are changed)
3	VCONN_FAULT	RCU	1'b0	VCONN_FAULT Bit is set whenever a VCONN over-current limit is triggered. 0 - No fault. (default) 1 - Interrupt (INT_N is asserted low)

Table 9. Connection Status and Control Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-1	DRP_DUTY_CYCLE	RW	2'b00	Percentage of time that a DRP advertises DFP during tDRP 00 – 30% (default) 01 – 40% 10 – 50% 11 – 60%
0	DISABLE_UFP_ACCESSORY	RW	1'b0	Setting this field will disable UFP accessory support. 0 – UFP accessory support enabled (Default) 1 – UFP accessory support disabled

7.6.1.4 General Control Register (offset = 0x0A) [reset = 0x00]

Figure 6. General Control Register

7	6	5	4	3	2	1	0
DEBOUNCE		MODE_SELECT		I^2C_SOFT_RESET	SOURCE_PREF		DISABLE_TERM
RW		RW		RSU	RW		RW

LEGEND: R/W = Read/Write; R/S/U = Read/Set/Update

Table 10. General Control Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	DEBOUNCE	RW	2'b00	The nominal amount of time the TUSB322I device debounces the voltages on the CC pins. 00 – 168ms (default) 01 – 118ms 10 – 134ms 11 – 152ms
5-4	MODE_SELECT	RW	2'b00	This register can be written to set the TUSB322I device mode operation. The ADDR pin must be set to I^2C mode. 00 – DRP mode (start from unattached.SNK) (default) 01 – UFP mode (unattached.SNK) 10 – DFP mode(unattached.SRC) 11 – DRP mode(start from unattached.SNK)
3	I^2C_SOFT_RESET	RSU	1'b0	This register resets the digital logic. The bit is self-clearing. A write of 1 starts the reset. The following registers can be affected after setting this bit: CURRENT_MODE_DETECT ACTIVE_CABLE_DETECTION ACCESSORY_CONNECTED ATTACHED_STATE CABLE_DIR
2-1	SOURCE_PREF	RW	2'b00	This field controls the TUSB322I behavior when configured as a DRP. 00 – Standard DRP (default) 01 – DRP will perform Try.SNK 10 – Reserved 11 – DRP will perform Try.SRC

Table 10. General Control Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	DISABLE_TERM	RW	1'b0	This field will disable the termination on CC pins and transition the CC state machine to the disabled state. 0 – Termination enabled according TUSB322I mode of operation (default) 1 – Termination disabled and state machine held in disable state.

7.6.1.5 Device Revision Register (offset = 0xA0) [reset = 0x02]

Figure 7. Device Revision Register

7	6	5	4	3	2	1	0
REVISION							
R							

LEGEND: R = Read only

Table 11. Device Revision Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	REVISION	R	'h02	Revision of TUSB322I. Defaults to 0x02.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TUSB322I device is a Type-C configuration channel logic and port controller. The TUSB322I device can detect when a Type-C device is attached, what type of device is attached, the orientation of the cable, and power capabilities (both detection and broadcast). The TUSB322I device can be used in a source application (DFP) or in a sink application (UFP).

8.2 Typical Application

Typical Application (continued)

8.2.1 DRP in I²C Mode

Figure 8 shows the TUSB322I device configured as a DRP in I²C mode.

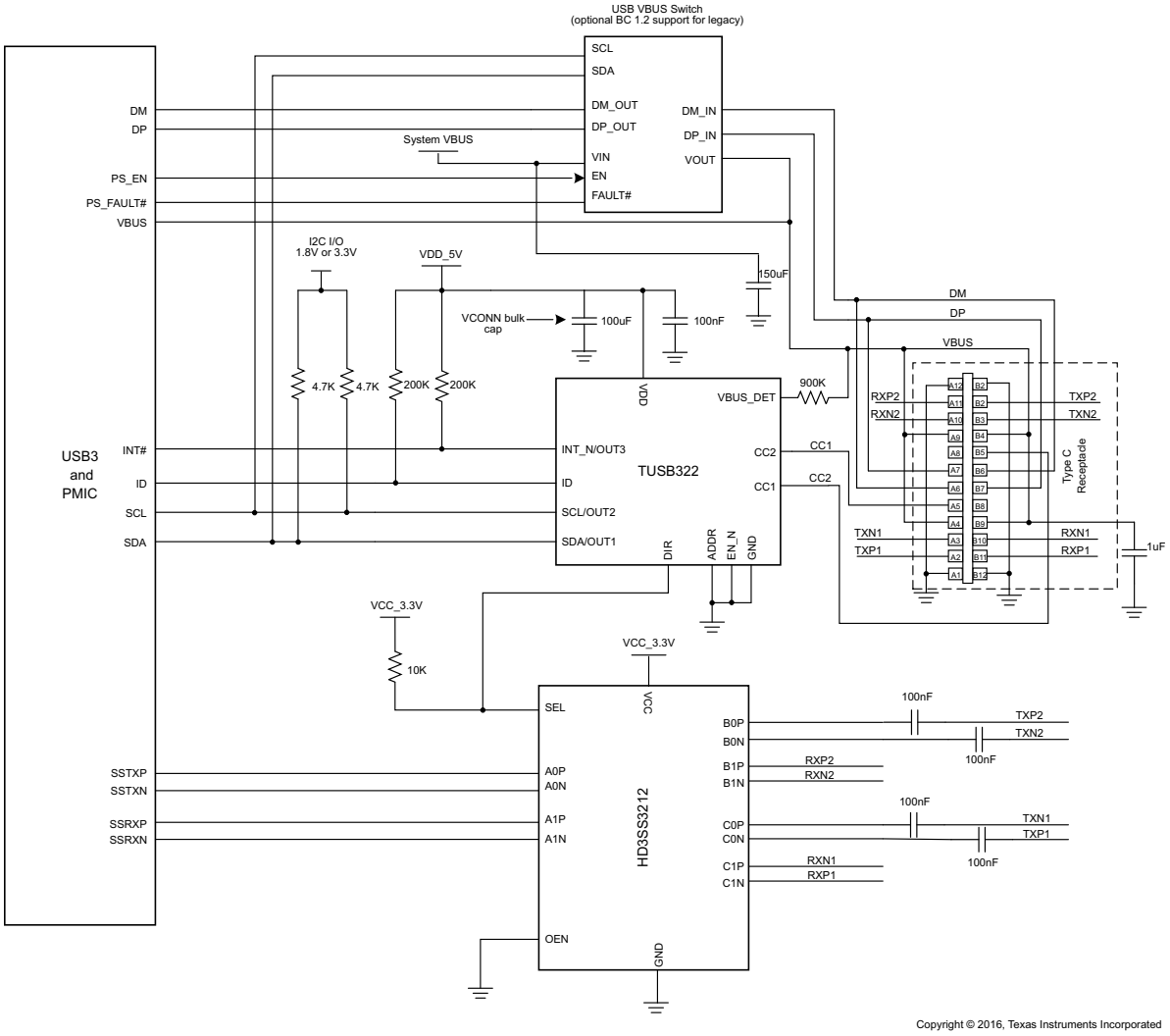


Figure 8. DRP in I²C Mode Schematic

8.2.1.1 Design Requirements

For the design example, use the parameters listed in Table 12.

Table 12. Design Requirements for DRP in I²C Mode

DESIGN PARAMETER	VALUE
V_{DD} (4.5 to 5.5 V)	5 V
Mode (I²C or GPIO)	I²C ADDR pin must be pulled down or pulled up
I²C address (0x67 or 0x47)	0x47 ADDR pin must be pulled low or tied to GND
Type-C port type (UFP, DFP, or DRP)	DRP MODE_SELECT register = 2'b00.
VCONN Support	Yes

8.2.1.2 Detailed Design Procedure

The TUSB322I device supports a V_{DD} in the range of 4.5 V to 5.5 V. In this particular use case, 5 V is connected to the V_{DD} pin. Because VCONN support is required for a DRP, the 5 V on V_{DD} meets the USB Type-C VCONN requirement of 4.75 V to 5.5 V. A 100-nF capacitor is placed near V_{DD}. Also, a 100-µF capacitor is used to meet the USB Type-C bulk capacitance requirement of 10 µF to 220 µF.

The TUSB322I device is placed into I^2C mode by either pulling the ADDR pin high or low. In this case, the ADDR pin is tied to GND which results in a I^2C address of 0x47. The SDA and SCL must be pulled up to either 1.8 V or 3.3 V. When pulled up to 3.3 V, the V_{DD} supply must be at least 3 V to keep from back-driving the I^2C interface.

The INT_N/OUT3 pin is used to notify the PMIC when a change in the TUSB322I I^2C registers occurs. This pin is an open drain output and requires an external pullup resistor. The pin should be pulled up to V_{DD} using a 200-kΩ resistor.

The ID pin is used to indicate when a connection has occurred if the TUSB322I device is a DFP while configured for DRP. An OTG USB controller can use this pin to determine when to operate as a USB Host or USB Device. When this pin is driven low, the OTG USB controller functions as a host and then enables V_{BUS}. The Type-C standard requires that a DFP not enable V_{BUS} until the V_{BUS} is in the Attached.SRC state. If the ID pin is not low but V_{BUS} is detected, then the OTG USB controller functions as a device. The ID pin is open drain output and requires an external pullup resistor. The ID pin should be pulled up to V_{DD} using a 200-kΩ resistor.

The DIR pin is used to control the mux for connecting the USB3 SS signals to the appropriate pins on the USB Type-C receptacle. In this particular case, a HD3SS3212 is used as the mux. To minimize crossing in routing the USB3 SS signals to the USB Type C connector, the connection of CC1 and CC2 to the TUSB322I is swapped. When swapping the CC1 and CC2 connection, the CABLE_DIR register will also be reversed (0 = CC2 and 1 = CC1).

The VBUS_DET pin must be connected through a 900-kΩ resistor to V_{BUS} on the Type-C that is connected. This large resistor is required to protect the TUSB322I device from large V_{BUS} voltage that is possible in present day systems. This resistor along with internal pulldown keeps the voltage observed by the TUSB322I device in the recommended range.

The USB2 specification requires the bulk capacitance on V_{BUS} based on UFP or DFP. When operating the TUSB322I device in a DRP mode, it alternates between UFP and DFP. If the TUSB322I device connects as a UFP, the large bulk capacitance must be removed.

Table 13. USB2 Bulk Capacitance Requirements

PORT CONFIGURATION	MIN	MAX	UNIT
Downstream facing port (DFP)	120		µF
Upstream facing port (UFP)	1	10	µF

8.2.1.3 Application Curves

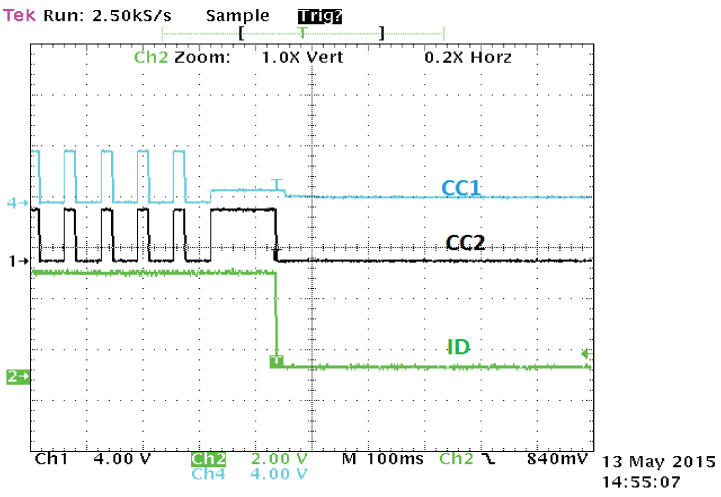


Figure 9. Application Curve for DRP in I^2C Mode

8.2.2 DFP in I²C Mode

Figure 10 shows the TUSB322I device configured as a DFP in I²C mode.

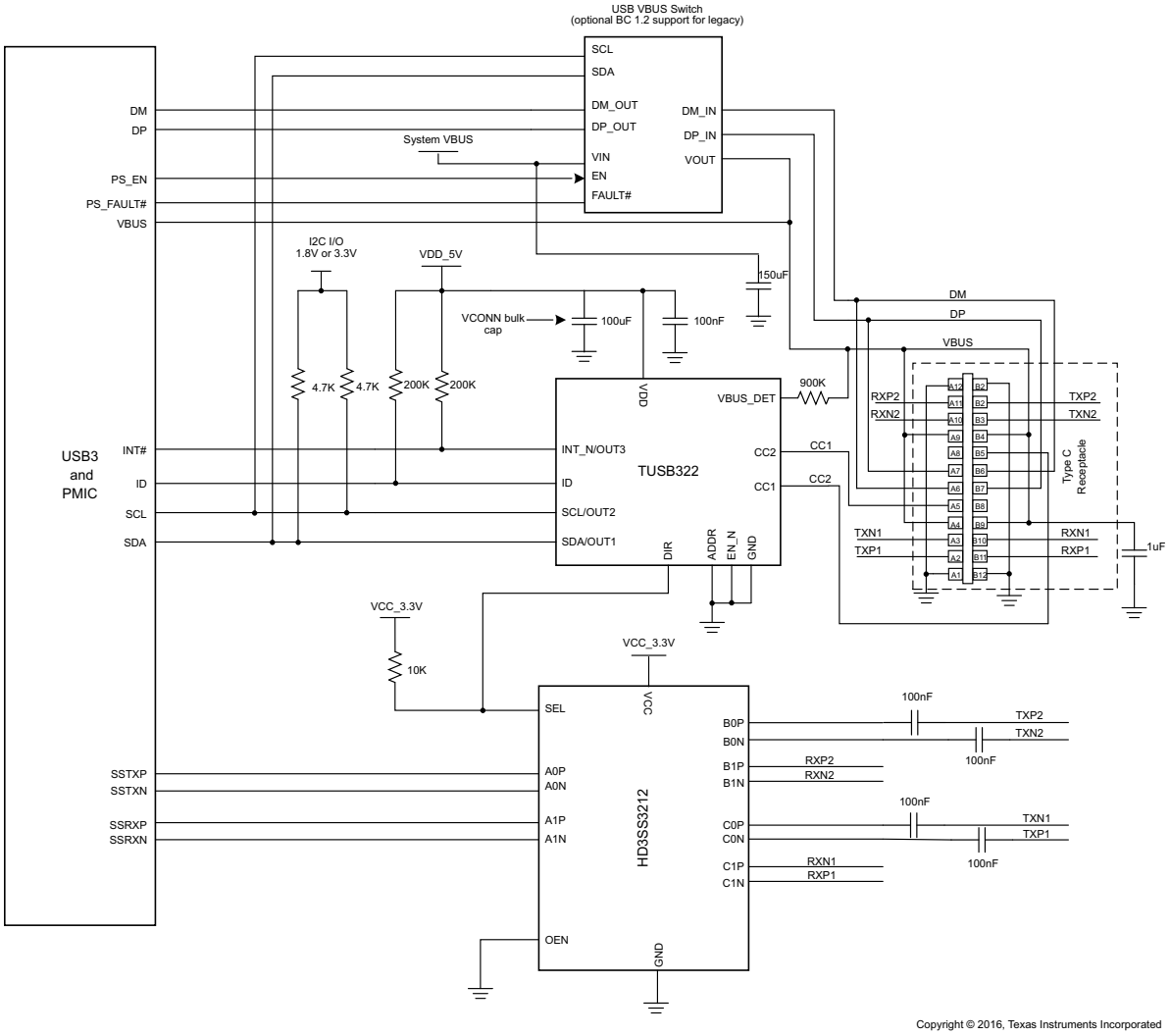


Figure 10. DFP in I²C Mode Schematic

8.2.2.1 Design Requirements

For the design example, use the parameters listed in Table 14:

Table 14. Design Requirements for DFP in I²C Mode

DESIGN PARAMETER	VALUE
V_{DD} (4.5 V to 5.5 V)	5 V
Mode (I²C or GPIO)	I²C ADDR pin must be pulled down or pulled up
I²C address (0x61 or 0x60)	0x47 ADDR pin must be pulled low or tied to GND
Type-C port type (UFP, DFP, or DRP)	DFP MODE_SELECT = 2'b10
VCONN Support	Yes

8.2.2.2 Detailed Design Procedure

The TUSB322I device supports a V_{DD} in the range of 4.5 V to 5.5 V. In this particular case, V_{DD} is set to 5 V. A 100-nF capacitor is placed near V_{DD}. Also, a 100-µF capacitor is used to meet the USB Type-C bulk capacitance requirement of 10 µF to 220 µF.

The TUSB322I device is placed into I^2C mode by either pulling the ADDR pin high or low. In this particular case, the ADDR pin is tied to GND which results in a I^2C address of 0x47. The SDA and SCL must be pulled up to either 1.8 V or 3.3 V. When pulled up to 3.3 V, the V_{DD} supply must be at least 3 V to keep from back-driving the I^2C interface.

The INT_N/OUT3 pin is used to notify the PMIC when a change in the TUSB322I I^2C registers occurs. This pin is an open drain output and requires an external pullup resistor. The pin should be pulled up to V_{DD} using a 200-kΩ resistor.

The DIR pin is used to control the mux for connecting the USB3 SS signals to the appropriate pins on the USB Type-C receptacle. In this particular case, a HD3SS3212 is used as the mux. To minimize crossing in routing the USB3 SS signals to the USB Type C connector, the connection of CC1 and CC2 to the TUSB322I is swapped. When swapping the CC1 and CC2 connection, the CABLE_DIR register will also be reversed (0 = CC2 and 1 = CC1).

The Type-C port mode is determined by the state of the MODE_SELECT register. When the MODE_SELECT register is 2'b10, the TUSB322I device is in DFP mode. The TUSB322I will exit the DFP mode if the MODE_SELECT register is changed, I2C_SOFT_RESET is set, or EN_N pin is transitioned from high to low.

The VBUS_DET pin must be connected through a 900-kΩ resistor to V_{BUS} on the Type-C that is connected. This large resistor is required to protect the TUSB322I device from large V_{BUS} voltage that is possible in present day systems. This resistor along with internal pulldown keeps the voltage observed by the TUSB322I device in the recommended range.

The USB2 specification requires the bulk capacitance on V_{BUS} based on UFP or DFP. When operating the TUSB322I device in a DFP mode, a bulk capacitance of at least 120 µF is required. In this particular case, a 150-µF capacitor was chosen.

8.2.2.3 Application Curves

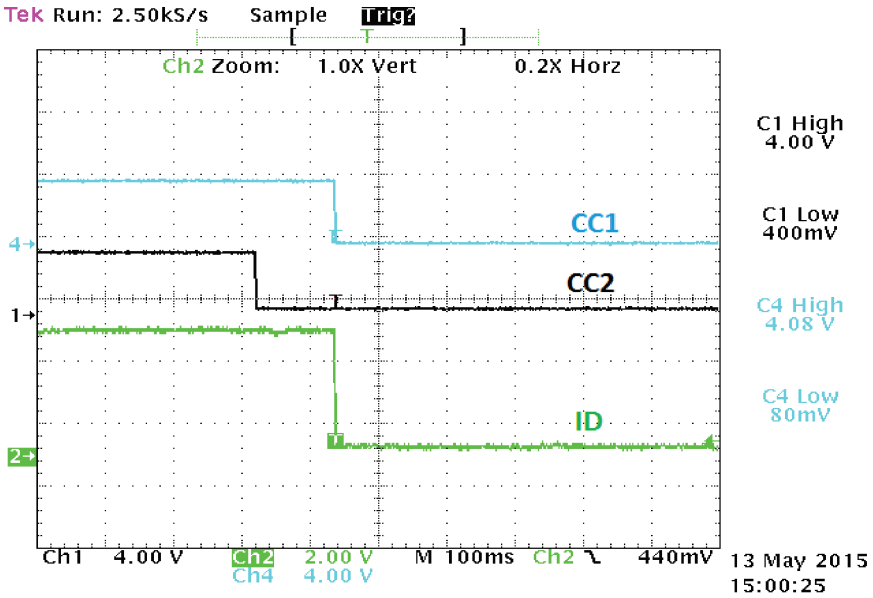


Figure 11. Application Curve for DFP in I^2C Mode

8.2.3 UFP in I²C Mode

Figure 12 shows the TUSB322I device configured as a UFP in I²C mode.

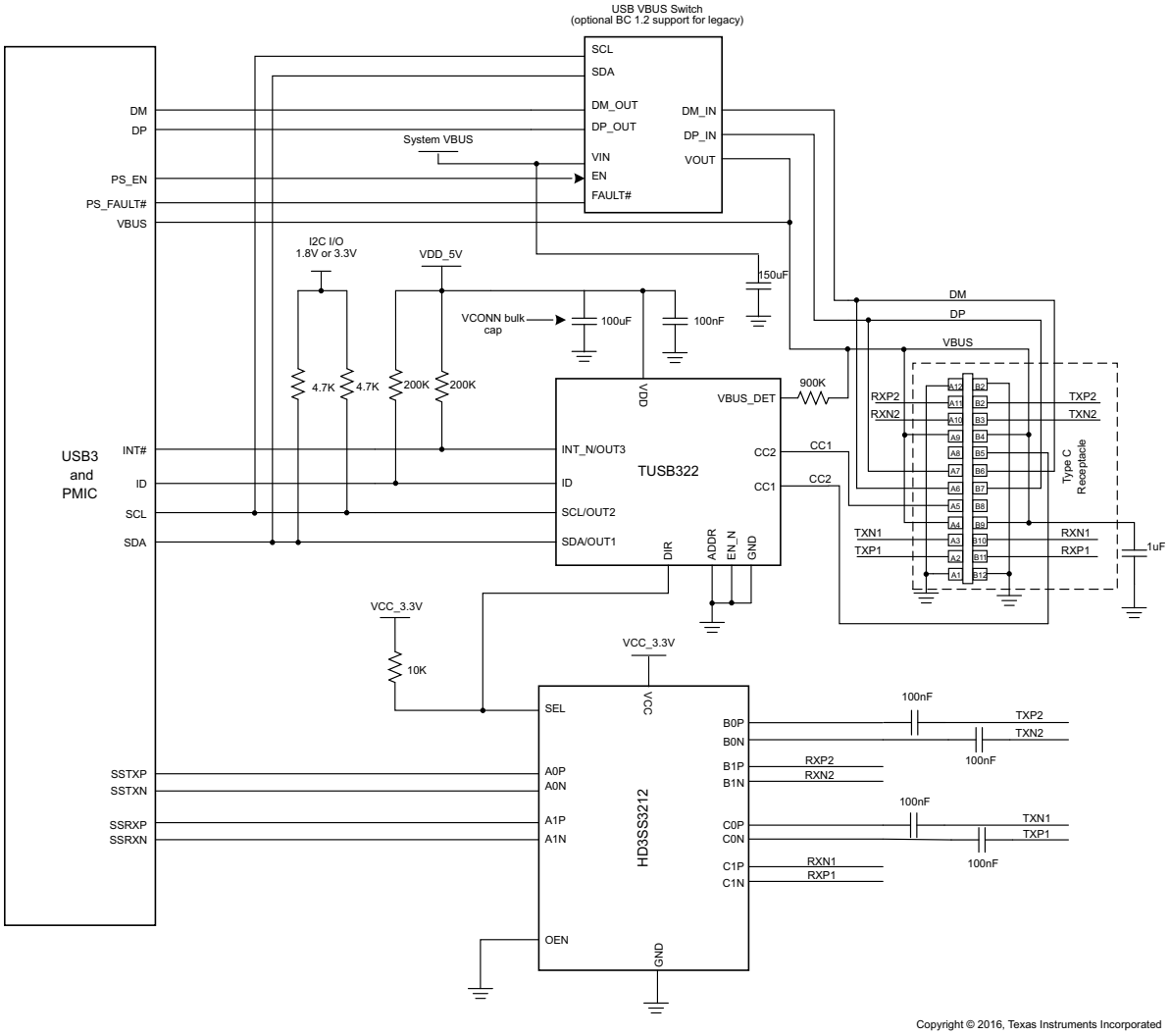


Figure 12. UFP in I²C Mode Schematic

8.2.3.1 Design Requirements

For the design example, use the parameters listed in Table 15:

Table 15. Design Requirements for UFP in I²C Mode

DESIGN PARAMETER	VALUE
V_{DD} (4.5 V to 5.5 V)	5 V
Mode (I²C or GPIO)	I²C ADDR pin must be pulled down or pulled up
I²C address (0x61 or 0x60)	0x47 ADDR pin must be pulled low or tied to GND
Type-C port type (UFP, DFP, or DRP)	UFP MODE_SELECT = 2'b01
VCONN Support	No

8.2.3.2 Detailed Design Procedure

The TUSB322I device supports a V_{DD} in the range of 4.5 V to 5.5 V. In this particular case, V_{DD} is set to 5 V. A 100-nF capacitor is placed near V_{DD}.

The TUSB322I device is placed into I^2C mode by either pulling the ADDR pin high or low. In this case, the ADDR pin is tied to GND which results in a I^2C address of 0x47. The SDA and SCL must be pulled up to either 1.8 V or 3.3 V. When pulled up to 3.3 V, the V_{DD} supply must be at least 3 V to keep from back-driving the I^2C interface.

The INT_N/OUT3 pin is used to notify the PMIC when a change in the TUSB322I I^2C registers occurs. This pin is an open drain output and requires an external pullup resistor. The pin should be pulled up to V_{DD} using a 200-kΩ resistor.

The DIR pin is used to control the mux for connecting the USB3 SS signals to the appropriate pins on the USB Type-C receptacle. In this particular case, a HD3SS3212 is used as the mux. To minimize crossing in routing the USB3 SS signals to the USB Type C connector, the connection of CC1 and CC2 to the TUSB322I is swapped. When swapping the CC1 and CC2 connection, the CABLE_DIR register will also be reversed (0 = CC2 and 1 = CC1).

The Type-C port mode is determined by the state of the MODE_SELECT register. When the MODE_SELECT register is 2'b01, the TUSB322I device is in UFP mode. The TUSB322I will exit the UFP mode if the MODE_SELECT register is changed, I2C_SOFT_RESET is set, or EN_N pin is transitioned from high to low.

The VBUS_DET pin must be connected through a 900-kΩ resistor to V_{BUS} on the Type-C that is connected. This large resistor is required to protect the TUSB322I device from large V_{BUS} voltage that is possible in present day systems. This resistor along with internal pulldown keeps the voltage observed by the TUSB322I device in the recommended range.

The USB2 specification requires the bulk capacitance on V_{BUS} based on UFP or DFP. When operating the TUSB322I device in a UFP mode, a bulk capacitance between 1 µF to 10 µF is required. In this particular case, a 1-µF capacitor was chosen.

8.2.3.3 Application Curves

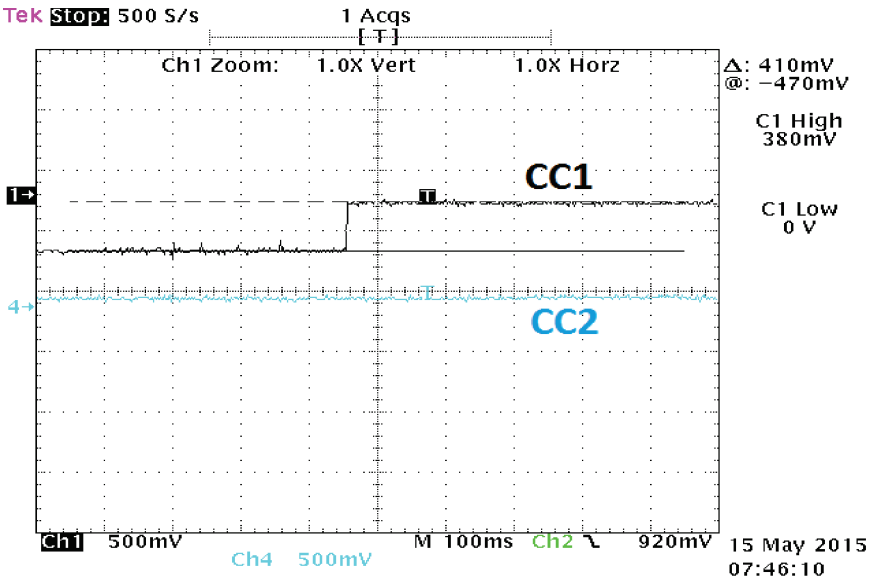


Figure 13. Application Curve for UFP in I^2C Mode

8.3 Initialization Set Up

The general power-up sequence for the TUSB322I device (EN_N tied to GND) is as follows:

1. System is powered off (device has no V_{DD}). The TUSB322I device is configured internally in UFP mode with Rds on CC pins (dead battery).
2. V_{DD} ramps – POR circuit.
3. I^2C supply ramps up.
4. The TUSB322I device enters unattached.SNK and functions as a DRP. If DRP is not the desired mode of operation, then software must change MODE_SELECT register to desired mode (UFP or DFP).
5. The TUSB322I device monitors the CC pins as a DFP and V_{BUS} for attach as a UFP.
6. The TUSB322I device enters active mode when attach has been successfully detected.

9 Power Supply Recommendations

The TUSB322I device has a wide power supply range from 4.5 to 5.5 V. The TUSB322I device can be run off of a system power such as a battery.

10 Layout

10.1 Layout Guidelines

1. An extra trace (or stub) is created when connecting between more than two points. A trace connecting pin A6 to pin B6 will create a stub because the trace also has to go to the USB Host. Ensure that:
   – A stub created by short on pin A6 (DP) and pin B6 (DP) at Type-C receptacle does not exceed 3.5 mm.
   – A stub created by short on pin A7 (DM) and pin B7 (DM) at Type-C receptacle does not exceed 3.5 mm.
2. A 100-nF capacitor should be placed as close as possible to the TUSB322I V_{DD} pin.

10.2 Layout Example

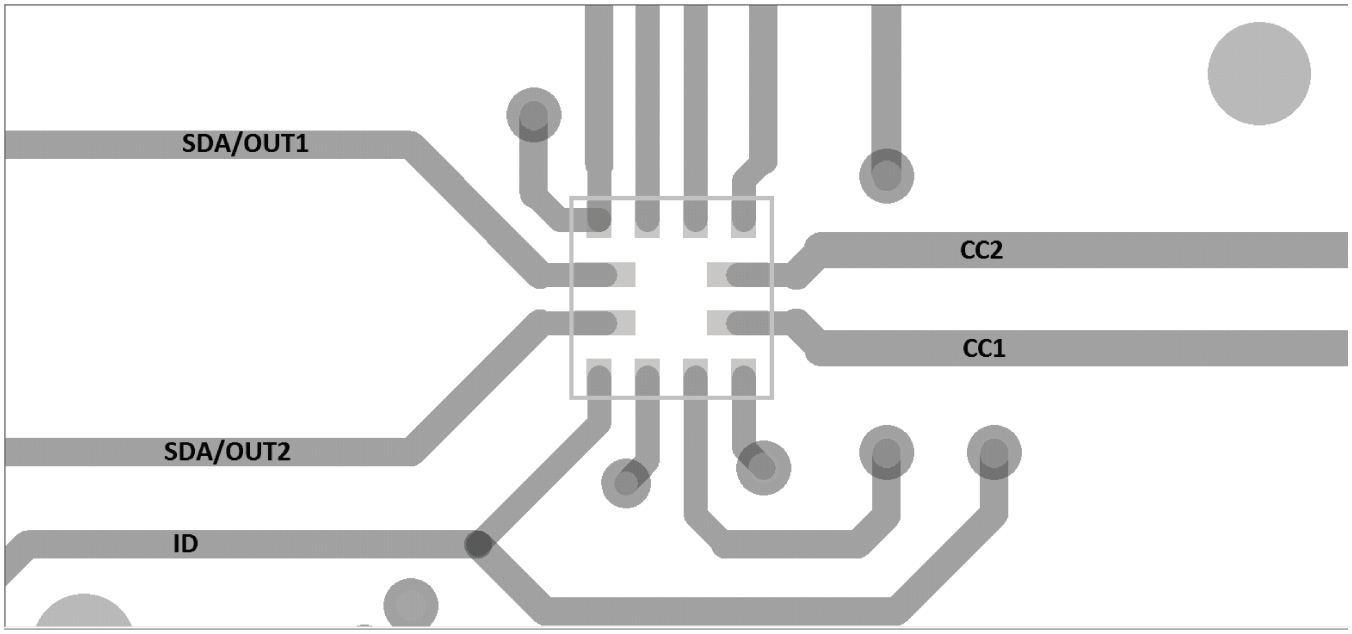


Figure 14. TUSB322I Layout

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *Semiconductor and C Package Thermal Metrics* application report, SPRA953

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
USB Type-C is a trademark of USB Implementers Forum.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TUSB322IRWBR	ACTIVE	X2QFN	RWB	12	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	72	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

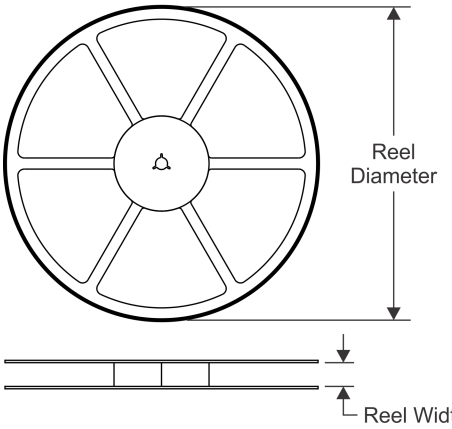
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

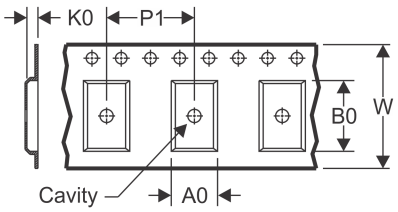
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

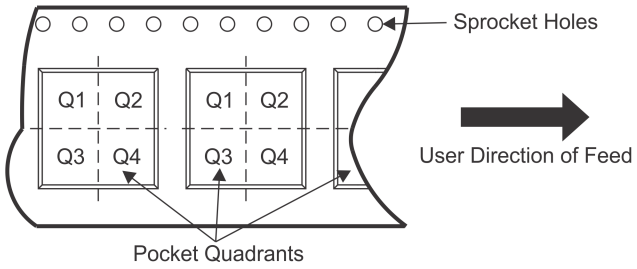


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

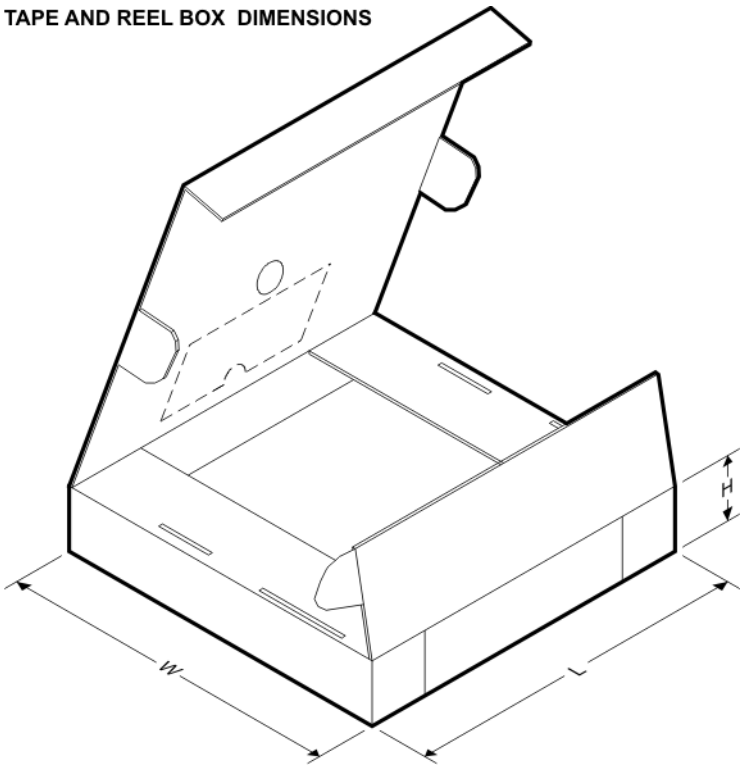
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TUSB322IRWBR	X2QFN	RWB	12	3000	180.0	8.4	1.8	1.8	0.61	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

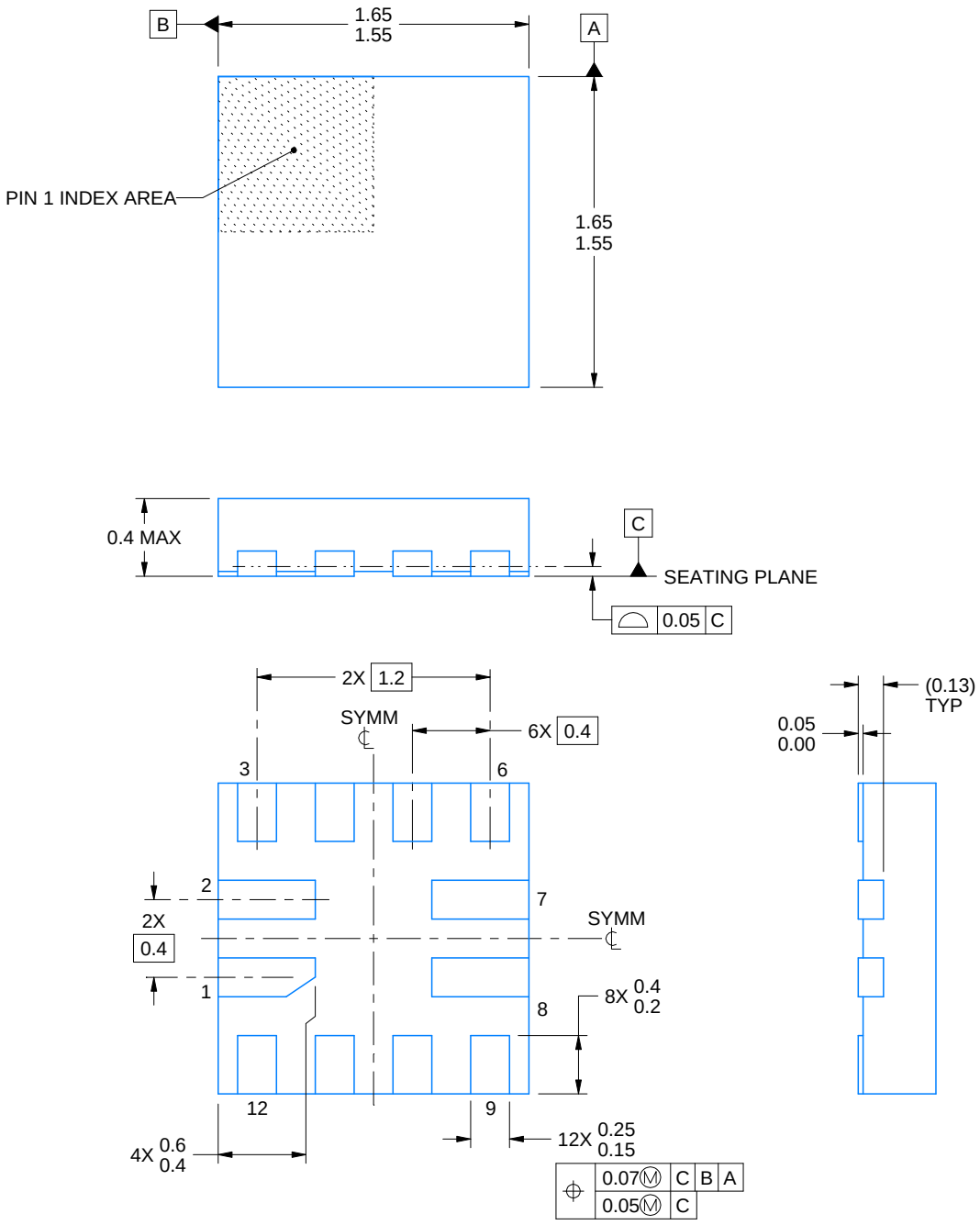
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TUSB322IRWBR	X2QFN	RWB	12	3000	213.0	191.0	35.0

PACKAGE OUTLINE

RWB0012A

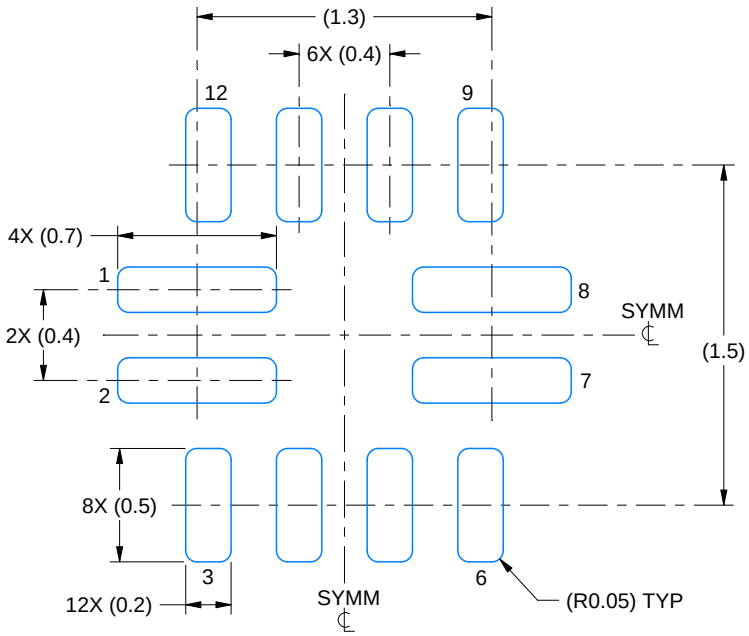
X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

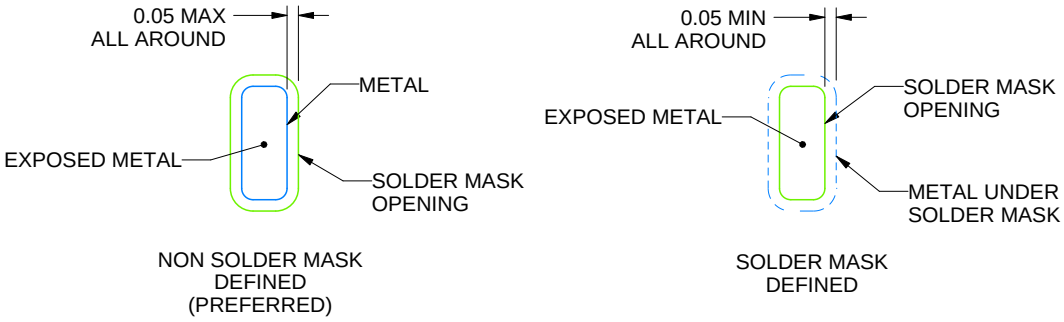


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



SOLDER MASK DETAILS

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NOTES: (continued)

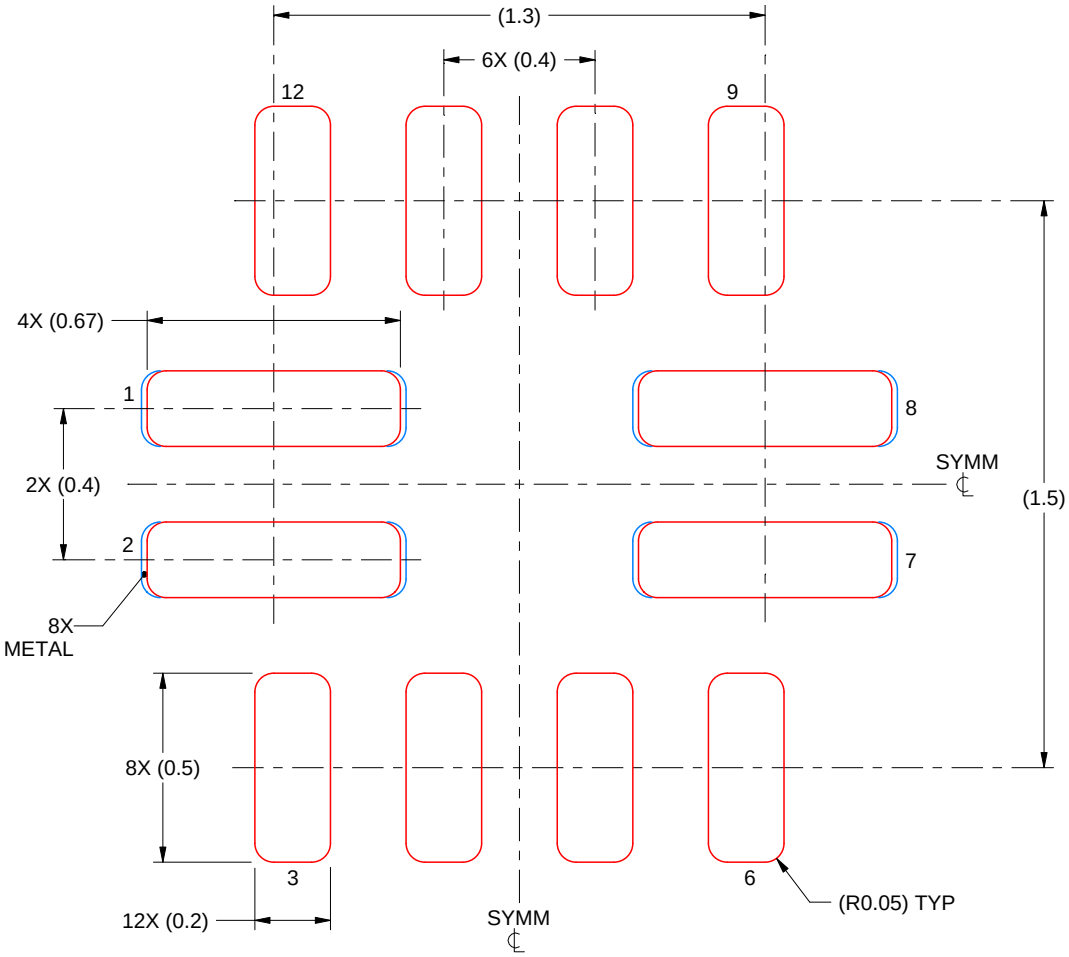
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

RWB0012A

X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

PADS 1,2,7 & 8
96% PRINTED SOLDER COVERAGE BY AREA
SCALE:50X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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