XTR111 Precision Voltage-to-Current Converter and Transmitter

1 Features

- Easy-to-design input/output ranges: 0mA–20mA, 4mA–20mA, 5mA–25mA or configurable voltage outputs
- Nonlinearity: 0.002%
- Low offset drift: 1µV/°C
- Accuracy: 0.015%
- Single-supply operation
- Wide supply range: 7V to 44V
- Output error flag ($\overline{\text{EF}}$)
- Output disable (OD)
- Adjustable voltage regulator: 3V to 15V
- Packages:
  - 10-pin HVSSOP
  - 10-pin VSON

2 Applications

- HVAC valve and actuator control
- Analog output module
- CPU (PLC controller)
- Flow transmitter

3 Description

The XTR111 is a precision voltage-to-current converter designed for the standard 0mA to 20mA or 4mA to 20mA analog signals, and sources up to 32mA. The ratio between input voltage and output current is set by a single resistor, R_{SET}. The circuit can also be modified for voltage-output operation.

An external P-MOSFET transistor provides high output resistance and a broad-compliance voltage range that extends from 2V less than the supply voltage, V_{VSP}, to voltages far less than ground.

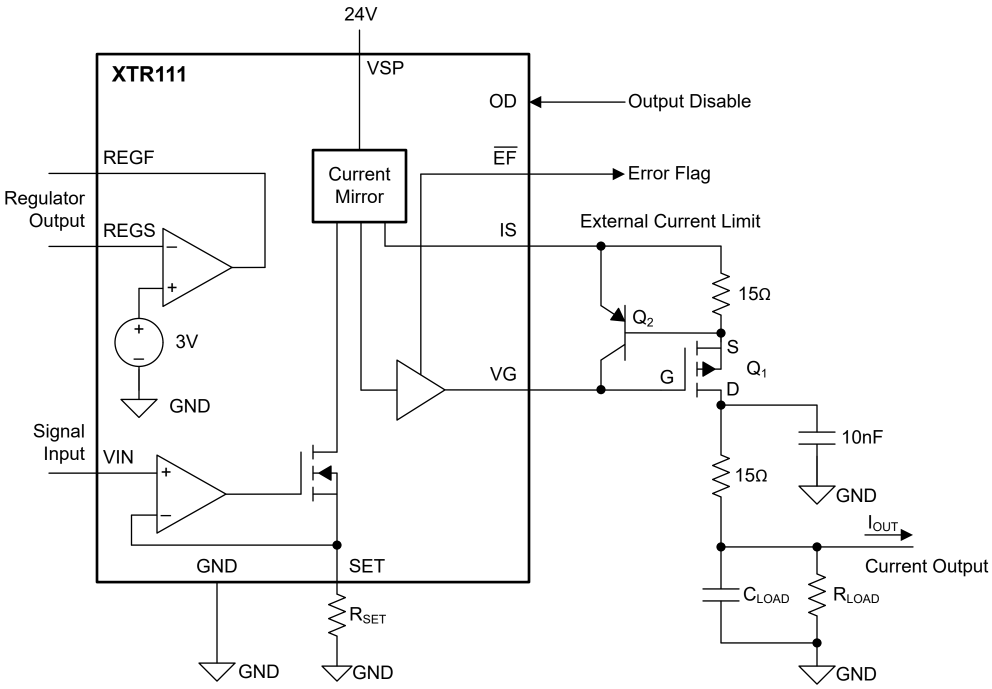
The adjustable 3V to 15V subregulator output provides the supply voltage for additional circuitry.

The XTR111 is available in 10-pin HVSSOP and VSON surface-mount packages.

Package Information

PART NUMBER	PACKAGE[1]	PACKAGE SIZE[2]
XTR111	DGQ (HVSSOP, 10)	3mm × 4.9mm
	DRC (VSON, 10)	3mm × 3mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Note: See Figure 6-5 for other current-limit configurations.

Voltage-to-Current Converter

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4 Pin Configurations and Functions

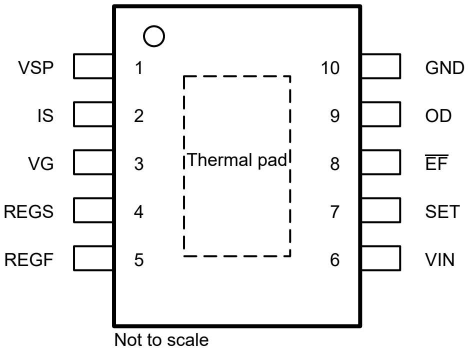


Figure 4-1. DGQ Package, 10-Pin HVSSOP (Top View)

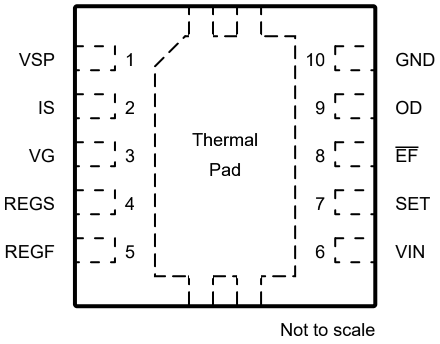


Figure 4-2. DRC Package, 10-Pin VSON (Top View)

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VSP	Power	Positive supply
2	IS	Output	Source connection
3	VG	Output	Gate drive
4	REGS	Input	Regulator sense
5	REGF	Output	Regulator force
6	VIN	Input	Input voltage
7	SET	Input	Transconductance set
8	$\overline{EF}$	Output	Error flag (active low)
9	OD	Input	Output disable (active high)
10	GND	Ground	Negative supply
Pad	Thermal pad	—	Connect exposed thermal pad to GND

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{VSP}	Power supply voltage			44	V
	Voltage at SET(2)		–0.5	14	V
	Voltage at IS(2)		$(V_{VSP}) - 5.5$	$(V_{VSP}) + 0.5$	V
	Voltage at REGS, REGF, VIN, OD, $\overline{EF}$		–0.5	$(V_{VSP}) + 0.5$	V
	Voltage at REGF, VG		–0.5	$(V_{VSP}) + 0.5$	V
	Current into VG, REGS, REGF, VIN, SET, $\overline{EF}$,and OD pins(2) (3)			±25	mA
	Current into IS pin		–50	25	mA
	Output short-circuit duration(4)	VG	Continuous to common and V_{VSP}		
		REGF	Continuous to common and V_{VSP}		
T_A	Operating temperature		–55	125	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Input pins are diode-clamped to the power-supply rails. Current limit input signals that swing more than 0.5V beyond the supply rails.
(3) See Section 6.3.1, Section 6.3.4, and Section 6.3.6 for information regarding safe voltage ranges and currents.
(4) See Section 7.1 regarding safe voltage ranges and currents.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{VSP}	Power supply voltage	8		40	V
V_{VIN}	Input voltage	0		12	V
T_A	Specified ambient temperature	–40		85	°C

5.4 Thermal Information

THERMAL METRIC(1)		XTR111		UNIT
		DGQ (HVSSOP)	DRC (VSON)	
		10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	57.7	53.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	83.8	57.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	29.3	26.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.2	1.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	29.2	26.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	14.6	9.8	°C/W

(1) For information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.5 Electrical Characteristics

at T_A = 25°C, V_{VSP} = 24V, R_{SET} = 2.0kΩ, REGF connected to REGS; OD = low, and external FET connected (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
TRANSMITTER							
	Transfer function				$I_{OUT} = 10 \times V_{VIN} / R_{SET}$		
I_{OUT}	Specified output current	Specified performance(1)		0.1		25	mA
		Derated performance(2)			0 to 32		mA
	Current limit for output current				41 ±9		mA
	Nonlinearity, I_{OUT}/I_{SET} (2) (3)	I_{OUT} = 0.1mA to 25mA			0.002	0.02	% of Span
		I_{OUT} = 0.1mA to 32mA			0.004		% of Span
I_{OS}	Offset current	I_{OUT} = 4mA(1)			0.002	0.02	% of Span
			T_A = –40°C to +85°C		0.0002	0.001	% of Span/°C
			8V to 40V supply		0.0001	0.005	% of Span/V
	Span Error, I_{OUT}/I_{SET} (2)	I_{OUT} = 0.1mA to 25mA			0.015	0.1	% of Span
			T_A = –40°C to +85°C (1) (2)		5		ppm/°C
			8V to 40V supply(1)		0.0001		% of Span/V
	Output resistance	From drain of Q_{EXT} (4)			> 1		GΩ
	Output leakage	OD = high			< 1		µA
	Input impedance (VIN)				2.4 || 30		GΩ || pF
I_B	Input bias current (VIN)				15	25	nA
V_{OS}	Input offset voltage(2)	V_{VIN} = 20mV			0.3	1.5	mV
			T_A = –40°C to +85°C		1.5		µV/°C
V_{VIN}	Input voltage(5)	T_A = –40°C to +85°C			0 to 12		V
	Noise, referred to input(2)	f = 0.1Hz to 10Hz, I_{OUT} = 4mA			2.5		$µV_{PP}$
	Dynamic response				See Section 6.3.2		
V-REGULATOR OUTPUT (REGF)							
	Voltage reference(6)	R_{LOAD} = 5kΩ		2.85	3.0	3.15	V
			T_A = –40°C to +85°C(6)		30		ppm/°C
			8V to 40V supply(6)		0.1		mV/V
	Bias current into REGS(6)				0.8		µA
	Load regulation	I_{REGF} = 0.6mA to 5mA			3	5	mV/mA
	Supply regulation(6)	R_{LOAD} = 5kΩ			0.01		mV/V
	Output current			5			mA
	Short-circuit output current				21		mA
DIGITAL INPUT (OD)							
V_{IL}	Low-level threshold	T_A = –40°C to +85°C				0.6	**V**
V_{IH}	High-level threshold	T_A = –40°C to +85°C		1.8			**V**
	Internal pullup current	V_{OD} < 5.5V			4		µA
DIGITAL OUTPUT ($\overline{EF}$)							
I_{OH}	Leakage current (open drain)				1		µA
V_{OL}	Low-level output voltage	I_{EF} = 2.2mA				0.8	V
I_{OL}	Low-level output current	V_{EF} = 400mV			2		mA
POWER SUPPLY							
I_Q	Quiescent current(6)	I_{OUT} = 0mA			450	550	µA

(1) Includes input amplifier, but excludes R_{SET} tolerance. Offset current is the deviation from the current ratio of I_{SET} to I_{IS} (output current).
(2) See also Section 5.6.
(3) Span is the change in output current resulting from a full-scale change in input voltage.
(4) Within compliance range limited by ($+V_{VSP}$ – 2V) + V_{DS} required for linear operation of Q_{EXT}.
(5) See also Section 7.1.1.
(6) See also Section 5.6.

5.6 Typical Characteristics

at T_A = 25°C and V_{VSP} = 24V (unless otherwise noted)

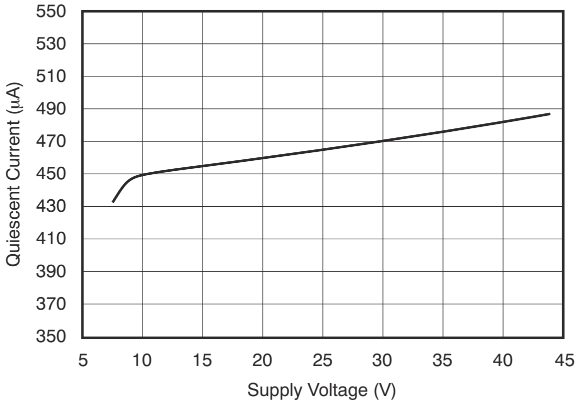


Figure 5-1. Quiescent Current vs Supply Voltage

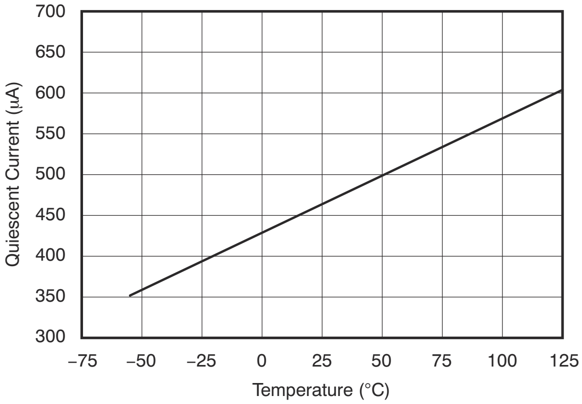


Figure 5-2. Quiescent Current vs Temperature

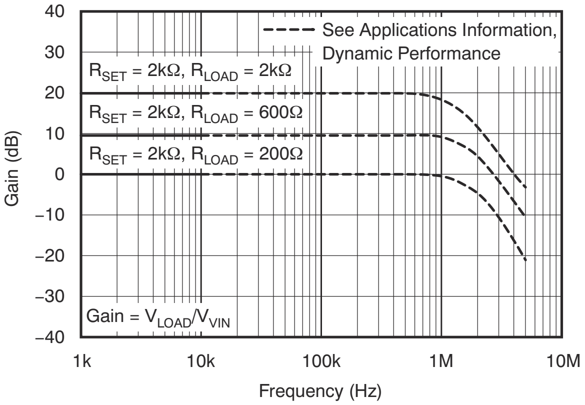


Figure 5-3. Gain vs Frequency

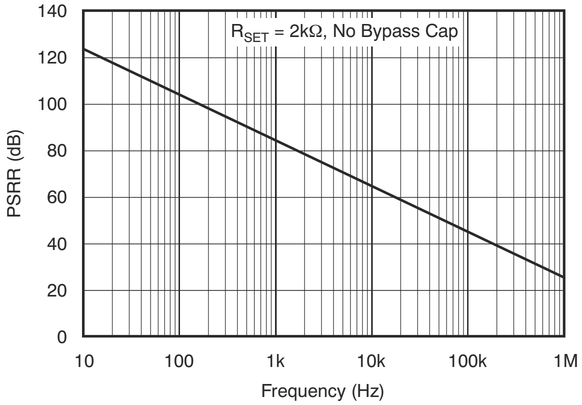


Figure 5-4. Power-Supply Rejection Ratio vs Frequency

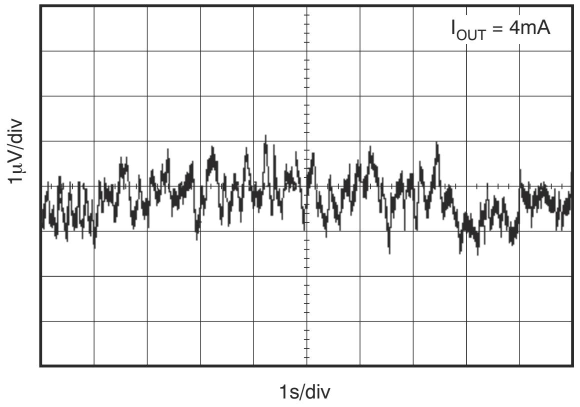


Figure 5-5. 0.1Hz to 10Hz Noise, RTI

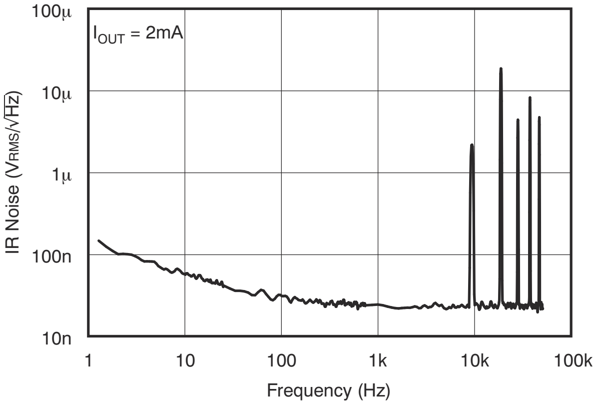


Figure 5-6. Input-Referred Noise Spectrum

5.6 Typical Characteristics (continued)

at T_A = 25°C and V_{VSP} = 24V (unless otherwise noted)

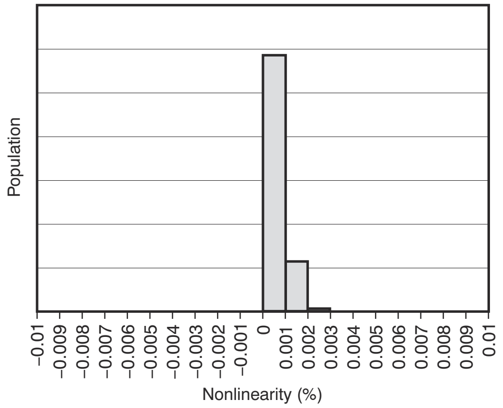


Figure 5-7. Nonlinearity Distribution

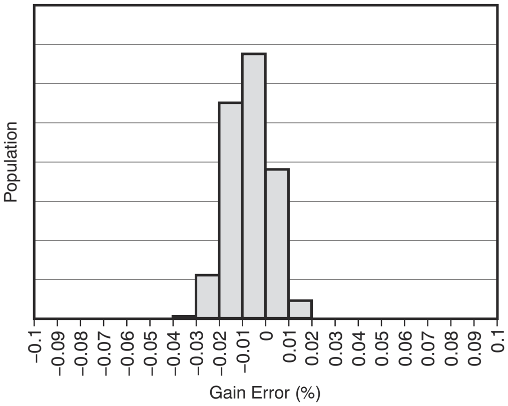


Figure 5-8. Gain Error Distribution

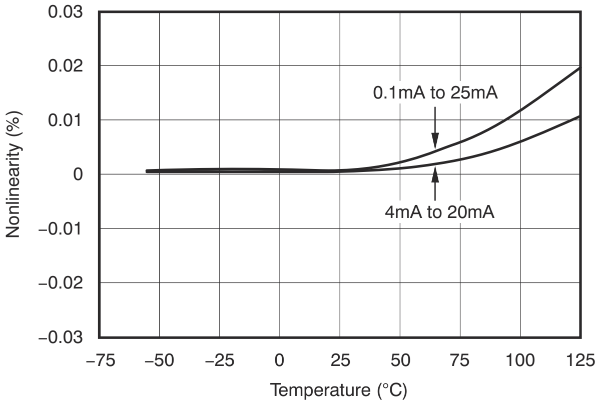
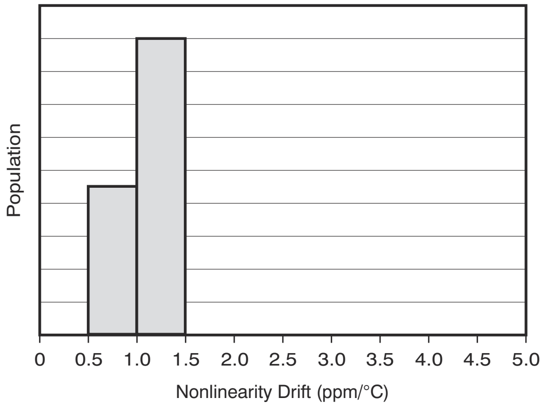


Figure 5-9. Nonlinearity vs Temperature



I_{OUT} = 0.1mA to 25mA, T_A = –55°C to +125°C

Figure 5-10. Nonlinearity Drift Distribution

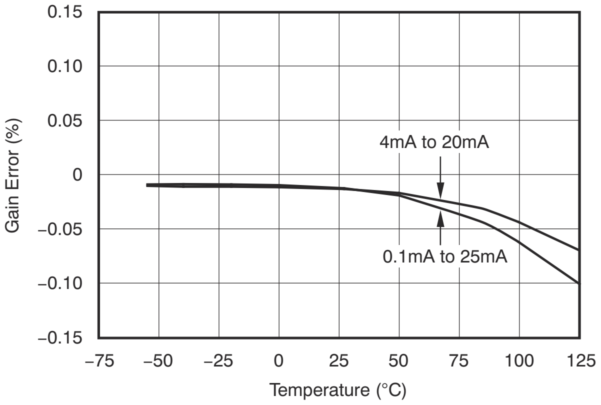
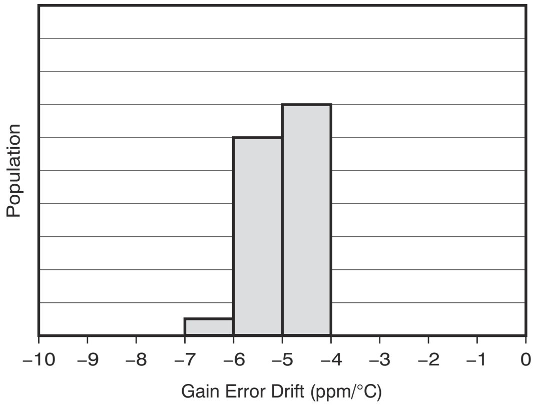


Figure 5-11. Gain Error vs Temperature

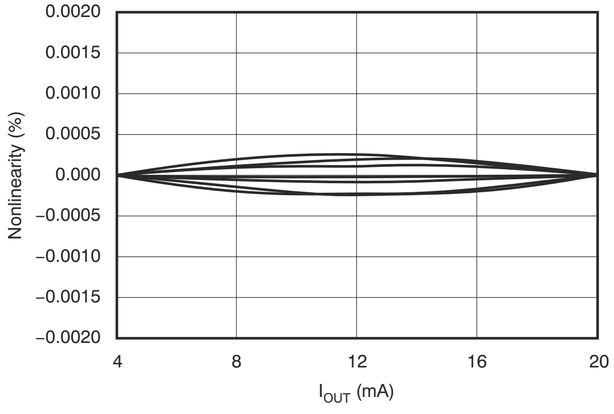


I_{OUT} = 0.1mA to 25mA, T_A = –55°C to +125°C

Figure 5-12. Gain-Error Drift Distribution

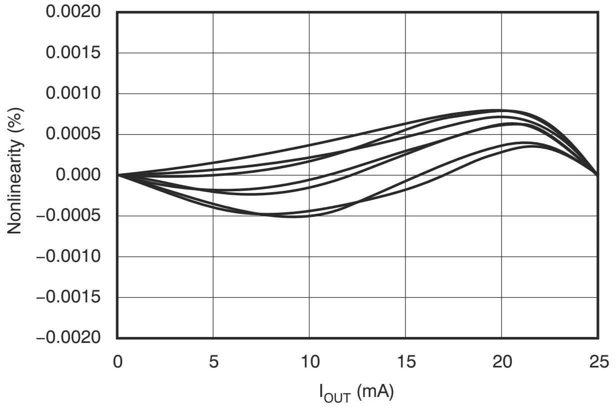
5.6 Typical Characteristics (continued)

at T_A = 25°C and V_{VSP} = 24V (unless otherwise noted)



2-point calibration at 4mA and 20mA

Figure 5-13. Typical Nonlinearity



2-point calibration at 0.1mA and 25mA

Figure 5-14. Typical Nonlinearity

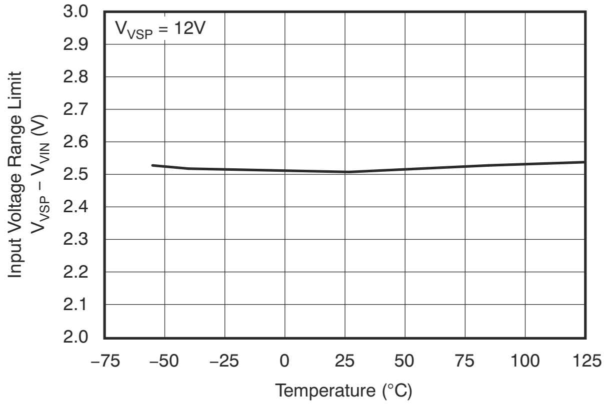


Figure 5-15. Input Voltage Range Limit to the Positive Supply vs Temperature

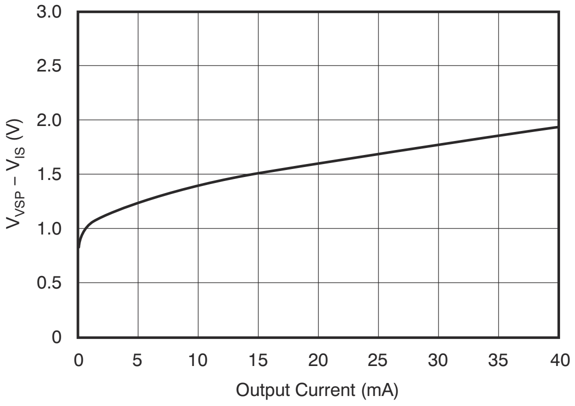


Figure 5-16. Source Connection Output Swing vs Output Current

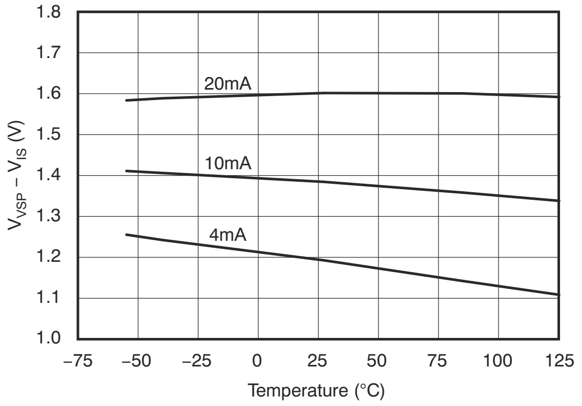


Figure 5-17. Source Connection Output Swing vs Temperature

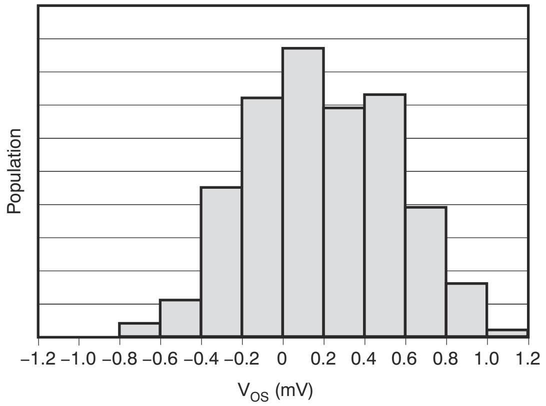


Figure 5-18. Input Offset Voltage Distribution

5.6 Typical Characteristics (continued)

at T_A = 25°C and V_{VSP} = 24V (unless otherwise noted)

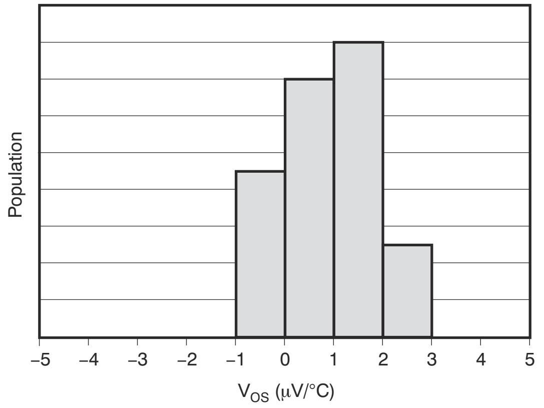


Figure 5-19. Input Offset Voltage Drift Distribution

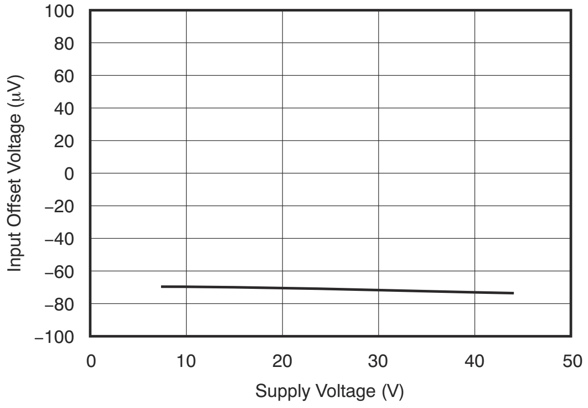


Figure 5-20. Input Offset Voltage vs Supply Voltage

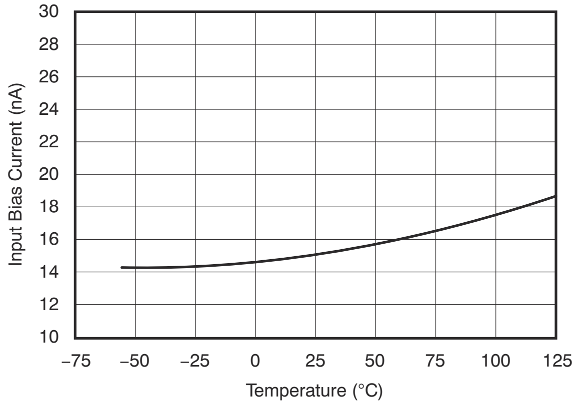


Figure 5-21. Amplifier Input Bias Current vs Temperature

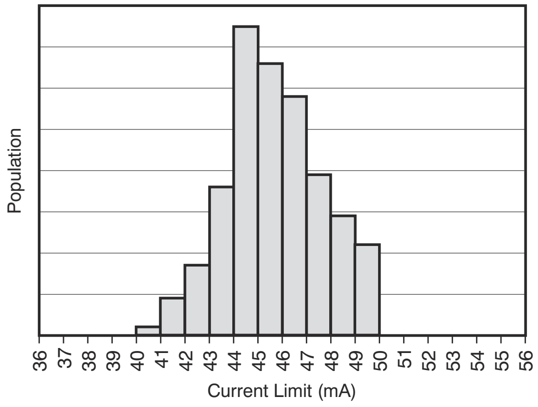


Figure 5-22. Output Current Limit Distribution

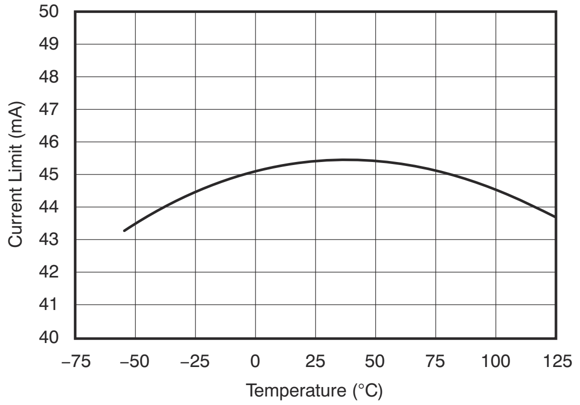


Figure 5-23. Output Current Limit vs Temperature

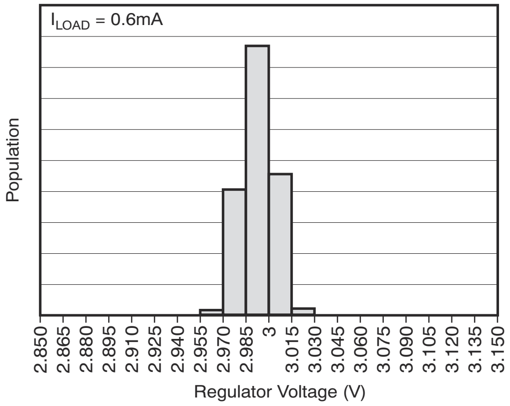


Figure 5-24. Regulator Voltage Distribution

5.6 Typical Characteristics (continued)

at T_A = 25°C and V_{VSP} = 24V (unless otherwise noted)

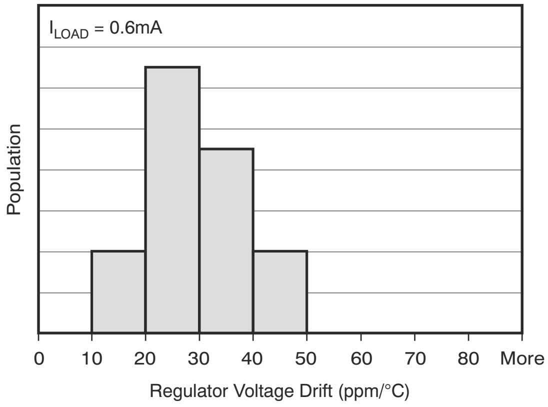


Figure 5-25. Regulator Voltage Drift Distribution

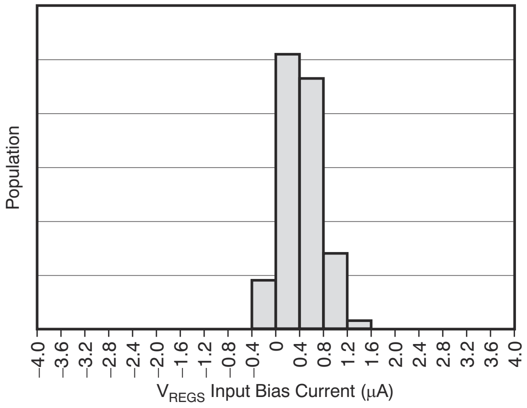


Figure 5-26. Regulator Input Bias Current Distribution (Current Into REGS Pin)

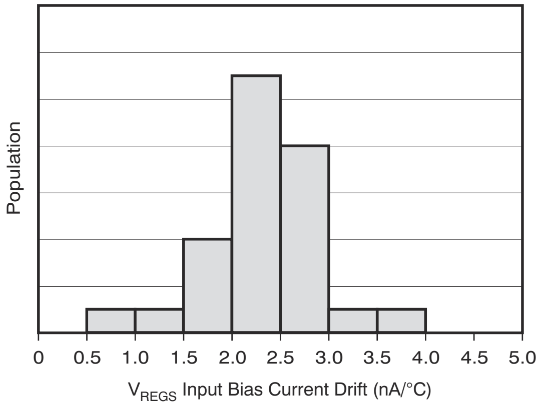


Figure 5-27. Regulator Input Bias Current Drift Distribution (Drift of Current into REGS Pin)

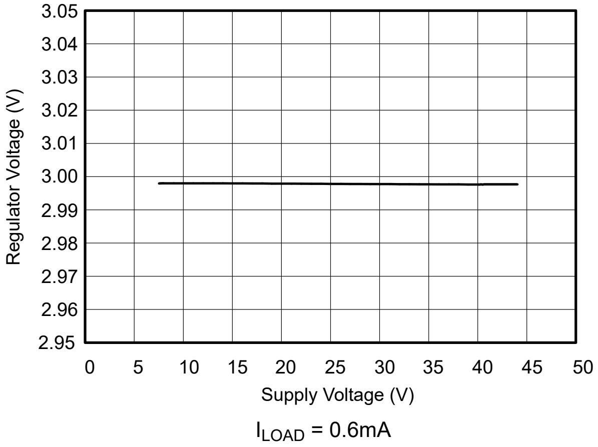


Figure 5-28. Regulator Voltage vs Supply Voltage

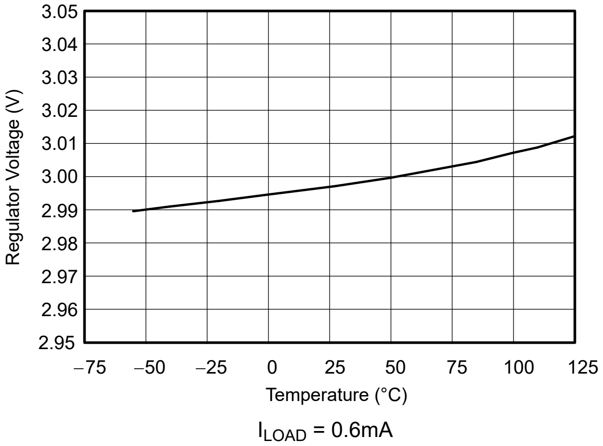
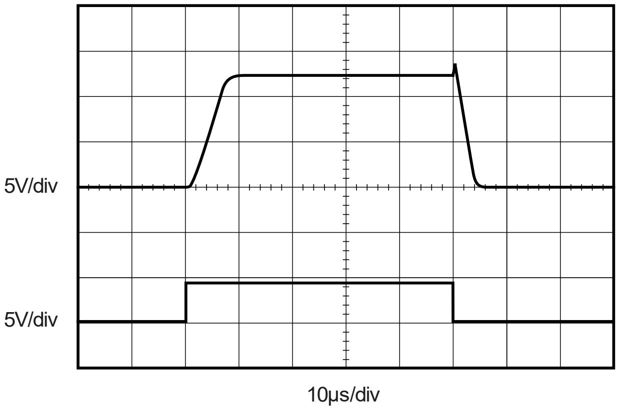


Figure 5-29. Regulator Voltage vs Temperature

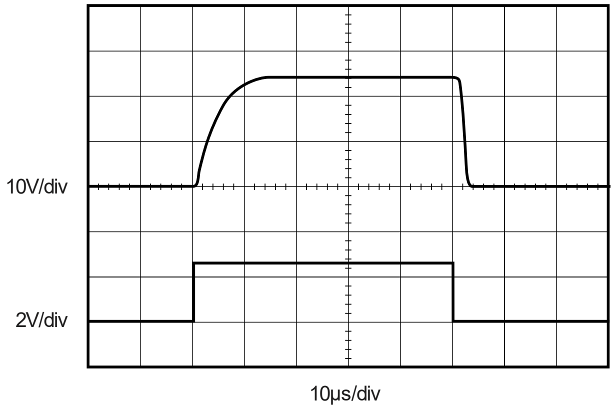


V_{FS} = 4V, R_{SET} = 2kΩ, R_{LD} = 600Ω,
C_{GATE} = 130pF, rising edge depends on C_{GATE} at VG pin

Figure 5-30. Step Response

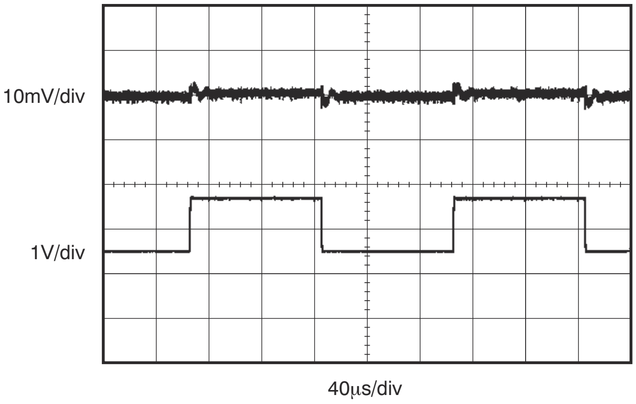
5.6 Typical Characteristics (continued)

at T_A = 25°C and V_{VSP} = 24V (unless otherwise noted)



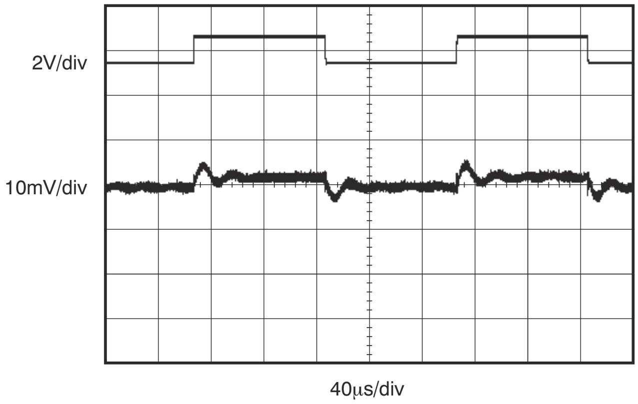
V_{FS} = 2.5V, R_{SET} = 1.25kΩ, R_{LD} = 600Ω,
C_{GATE} = 130pF, rising edge depends on C_{GATE} at VG pin

Figure 5-31. Step Response



V_{REG} gain = 1V, V_{REGF} = 3V, C_L = 470nF,
I_{LOAD} = 3mA ±0.3mA

Figure 5-32. Regulator Load Transient



V_{REG} gain = 4V, V_{REGF} = 12V, C_L = 470nF,
I_{LOAD} = 3mA ±0.3mA

Figure 5-33. Regulator Load Transient

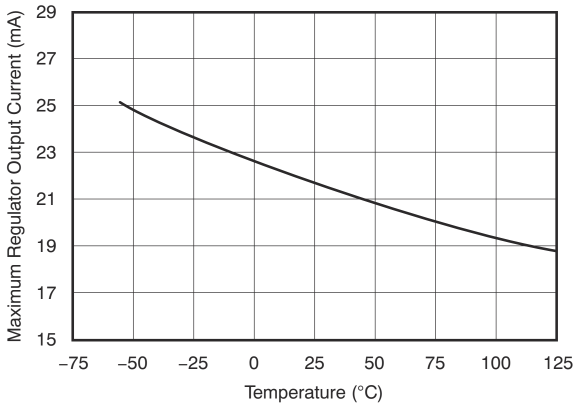


Figure 5-34. Maximum Regulator Current vs Temperature

6 Detailed Description

6.1 Overview

The XTR111 is a voltage-controlled current source capable of delivering currents from 0mA to 32mA. The primary intent of the XTR111 is to source the commonly-used industrial current ranges of 0mA to 20mA or 4mA to 20mA. The performance is specified for a supply voltage of up to 40V. The maximum supply voltage is 44V. The voltage-to-current ratio is defined by an external resistor, R_{SET}; therefore, the input voltage range can be freely set in accordance with application requirements. The output current is cascoded by an external P-channel MOSFET transistor for large voltage compliance extending below ground, and for easy power dissipation. This arrangement provides excellent suppression of typical interference signals from the industrial environment because of the extremely high output impedance and wide voltage compliance.

An error detection circuit activates a logic output (error flag pin, $\overline{EF}$) in case the output current cannot correctly flow. The $\overline{EF}$ pin indicates a wire break, high load resistor, or loss of headroom for the current output to the positive supply. The output disable (OD) pin provided can be used during power-on, multiplexing, and other conditions where the output presents no current. The OD pin has an internal pullup that causes the XTR111 to come up in output disable mode unless the OD pin is tied low.

The onboard voltage regulator can be adjusted from 3V to 15V and delivers up to 5mA load current. The voltage regulator is intended to supply signal conditioning and sensor excitation in 3-wire sensor systems. Voltages greater than 3V can be set by a resistive divider.

Figure 6-1 shows the basic connections. Input voltage V_{VIN} reappears across R_{SET} and controls 1/10 of the output current. The I-Mirror has a precise current gain of 10. This configuration has a transfer function of:

$$I_{OUT} = 10 \times \left(\frac{V_{VIN}}{R_{SET}}\right) \quad (1)$$

Set the voltage regulator output to a range of 3V to 12V by selecting R_1 and R_2 using the following equation:

$$V_{REGF} = 3V \times \frac{(R_1 + R_2)}{R_2} \quad (2)$$

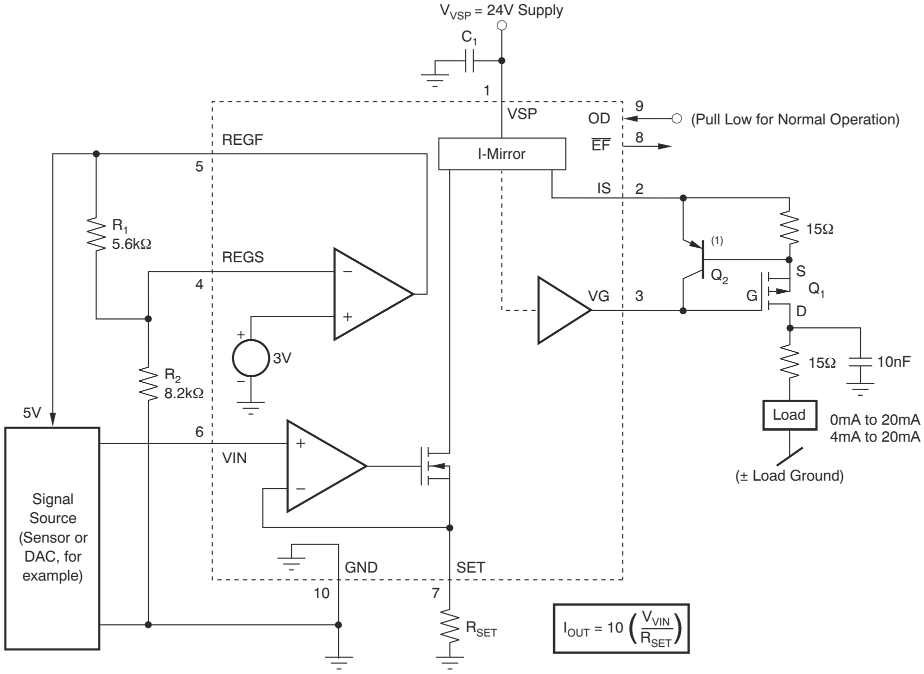
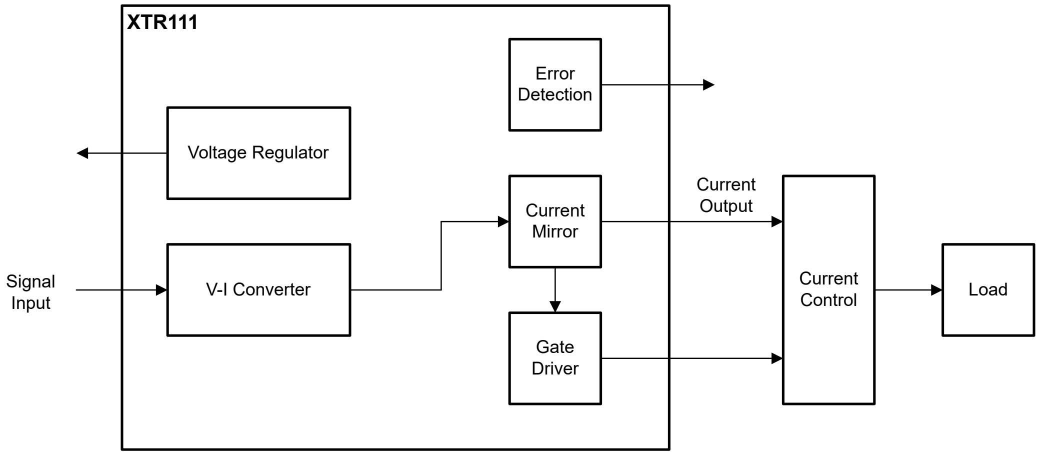


Figure 6-1. Basic Connection for 0mA to 20mA Related to a 0V-to-5V Signal Input With the Voltage Regulator Set to a 5V Output

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Explanation of Pin Functions

VIN: This input is a conventional, noninverting, high-impedance input of the internal operational amplifier (OPA). The internal circuitry is protected by clamp diodes to supplies. An additional clamp connected to approximately 18V protects internal circuitry. Place a small resistor in series with the input to limit the current into the protection if voltage can be present without the XTR111 being powered. Consider a resistor value equal to R_{SET} for bias current cancellation.

SET: The total resistance connected between this pin and VIN reference sets the transconductance. Additional series resistance can degrade accuracy and drift. The voltage on this pin must not exceed 14V because this pin is not protected to voltages greater than this level.

IS: This output pin is connected to the transistor source of the external FET. The accuracy of the output current to IS is achieved by dynamic error correction in the current mirror. Keep this pin within 6.5V the positive supply. An internal clamp is provided to protect the circuit; however, the internal clamp must be externally current-limited to less than 50mA.

VG: The gate drive for the external FET is protected against shorts to the supply and GND. The circuit is clamped to stay within 18V of the positive supply. Protect the external FET if the FET gate has the potential to exceed specified ratings.

REGF: The output of the regulator buffer can source up to 5mA of current, but has very limited sinking capability; less than 50µA. The maximum short-circuit current is in the range of 15mA to 25mA, changing over temperature.

REGS: This pin is the sense input of the voltage regulator and is referenced to an internal 3V reference circuit. The input bias current can be up to 2µA. Avoid capacitive loading of REGS that can compromise the loop stability of the voltage regulator.

VSP: The supply voltage of up to a maximum of 44V allows operation in harsh industrial environment and provides headroom for easy protection against overvoltage. Use a large enough bypass capacitor (> 100nF) and eventually a damping inductor or a small resistor (5Ω) to decouple the XTR111 supply from the noise typically found on the 24V supplies.

$\overline{\text{EF}}$: The active-low error flag (logic output) is intended for use with an external pullup resistor to logic-high for reliable operation when this output is used. However, this pin has a weak internal pullup resistor to 5V; leave unconnected if not used.

OD: This control input has a 4µA internal pullup resistor disabling the output. A pulldown resistor or short to GND is required to activate the output. Control OD to reduce output glitches during power on and power off. This logic input controls the output. If not used, connect this pin to GND. The regulator is not affected by OD.

6.3.2 Dynamic Performance

The rise time of the output current is dominated by the gate capacitance of the external FET.

The accuracy of the current mirror relies on the dynamic matching of multiple individual current sources. Settling to full resolution can require a complete cycle lasting around 100µs. Figure 6-2 shows an example of the ripple generated from the individual current source values that average to the specified accuracy over the full cycle.

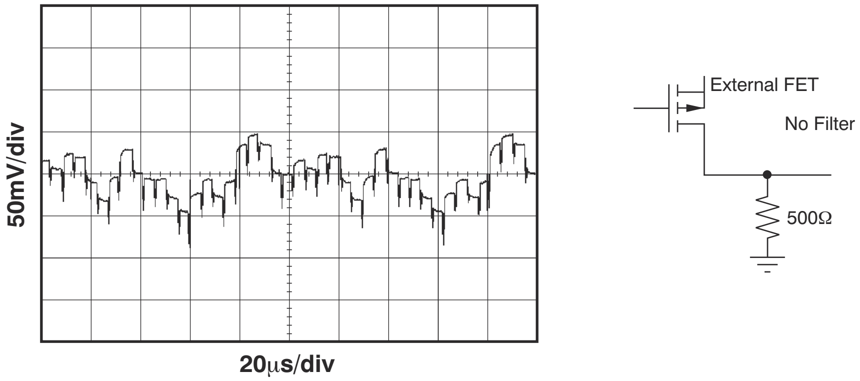


Figure 6-2. Output Noise Without Filter Into 500Ω

The output glitch magnitude depends on the mismatch of the internal current sources. The output glitch magnitude is approximately proportional to the output current level and scales directly with the load resistor value. The output glitch magnitude differs slightly from device to device. Figure 6-3 and Figure 6-4 show the effects of filtering the output.

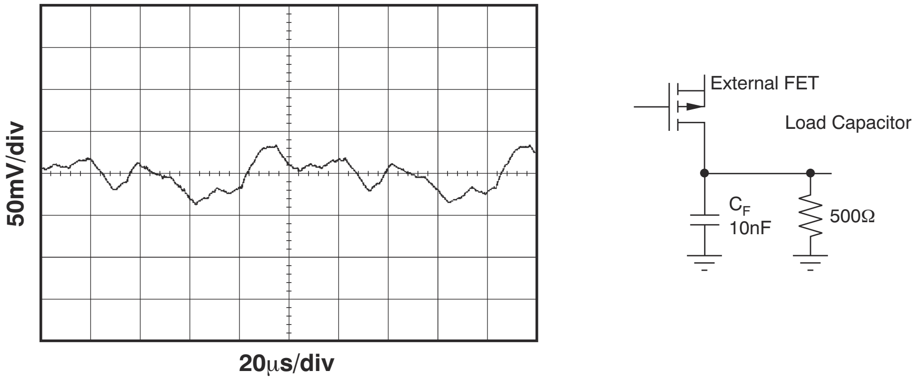
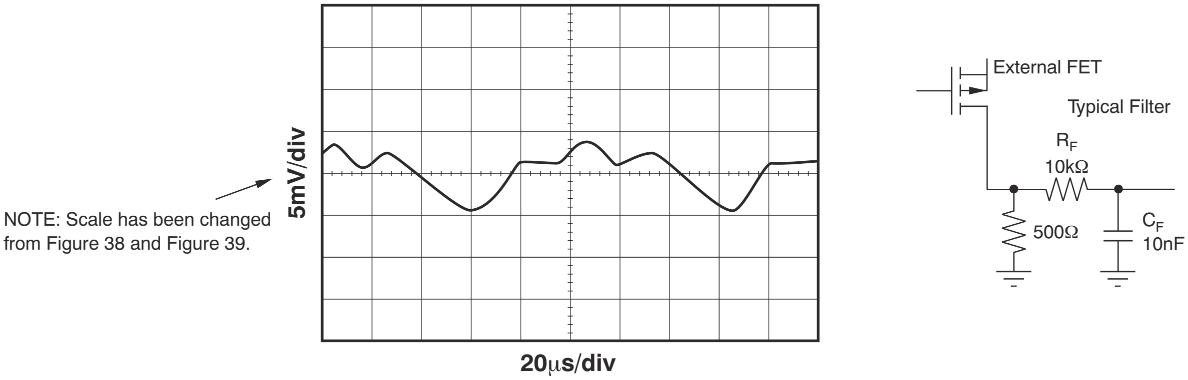


Figure 6-3. Output With 10nF Parallel to 500Ω



NOTE: Scale has been changed from Figure 38 and Figure 39.

Figure 6-4. Output With Additional Filter

6.3.3 External Current Limit

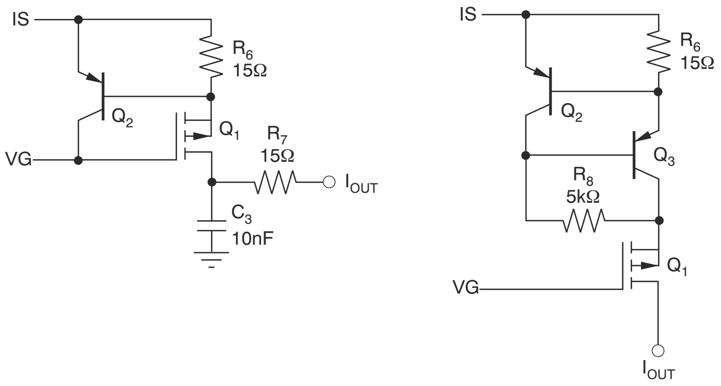
The XTR111 does not provide an internal current limit in case the external FET is forced to a low-impedance state. The internal current source controls the current, but a high current from IS to GND forces an internal voltage clamp between VSP and IS to turn on. This clamp results in a low-resistance path, and the current is only limited by the load impedance and the current capability of the external FET.

CAUTION

A high current can destroy the device. With the current loop interrupted (the load disconnected), the external MOSFET is fully turned on with a large gate-to-source voltage stored in the gate capacitance. The moment the loop is closed (the load connected), current flows into the load. However, for the first few microseconds, the MOSFET is still turned on, and depending on the load impedance, destructive current can flow. Use an external current limit to help protect the XTR111 from this condition.

Figure 6-5a shows an example of a current-limit circuit. Limit the current to 50mA. The 15Ω resistor (R_6) limits the current to approximately 37mA (33mA when hot). Select a PNP transistor that allows a peak current of several hundred milliamperes. Power dissipation is not usually critical because the peak current duration is only a few microseconds. However, observe the leakage current through the transistor from IS to VG. The addition of this current limiting transistor and R_6 still require time to discharge the gate of the external MOSFET. R_7 and C_3 are added for this reason, as well as to limit the steepness of external distortion pulses. Additional EMI and overvoltage protection can be required depending on the application.

Figure 6-5b is a universal and basic current-limiter circuit, using PNP or NPN transistors that can be connected in the source (IS to S) or in the drain output (in series with the current path). This circuit does not contribute to leakage currents. Consider adding an output filter like R_7 and C_3 in this limiter circuit.



a) Gate-Controlled Current Limit

b) Serial Current Limit

Figure 6-5. External Current Limit Circuits

6.3.4 External MOSFET

The XTR111 delivers the precise output current to the IS pin. The voltage at this pin is normally 1.4V less than V_{VSP}.

This output requires an external transistor (Q_{EXT}) that forms a cascode for the current output. The transistor must be rated for the maximum possible voltage on V_{OUT} and must dissipate the power generated by the current and the voltage across the transistor.

The gate drive (VG) can drive from close to the positive supply rail to 16V less than the positive supply voltage (V_{VSP}). Most modern MOSFETs accept a maximum V_{GS} of 20V. A protection clamp is only required if a large drain gate capacitance can pulse the gate beyond the rating of the MOSFET. Pulling the OD pin high disables the gate driver and closes a switch connecting an internal 3kΩ resistor from the VSP pin to the VG pin. This resistor discharges the gate of the external FET and closes the channel; see also Figure 6-6.

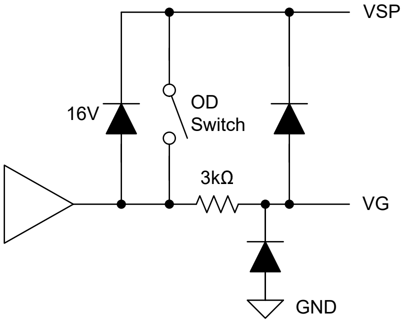


Figure 6-6. Equivalent Circuit for Gate Drive and Disable Switch

Table 6-1 lists some example devices in SO-compatible packages, but other devices can be used as well. Avoid external capacitance from IS. This capacitance can be compensated by adding additional capacitance from VG to IS; however, this compensation can slow down the output.

Table 6-1. P-Channel MOSFET (Examples)

MANUFACTURER(1)	PART NO.	BREAKDOWN VDS	PACKAGE	C-GATE
Infineon	BSP170P	–60V	SOT-223	328pF
ON Semiconductor	NTF2955	–60V	SOT-223	492pF
Supertex Inc.	TP2510	–100V	TO-243AA	80pF

(1) Data from published product data sheet; not ensured.

Select a drain-to-source breakdown voltage high enough for the application. Surge voltage protection can be required for negative overvoltages. For positive overvoltages, use a clamp diode to the 24V supply to help protect the FET from reversing.

6.3.5 Output Error Flag and Disable Input

The XTR111 has additional internal circuitry that detects an error in the output current. In case the controlled output current cannot flow as a result of a wire break, high load resistance, or the output voltage level approaching the positive supply, error flag $\overline{\text{EF}}$ (an open drain logic output), pulls low. When used, this digital output requires an external pullup resistor to logic high (the internal pullup resistor current is 2μA).

The output disable (OD) pin is a logic input with approximately 4μA of current through the internal pullup resistor to 5V. The XTR111 powers up with the output disabled until the OD pin is pulled low. A logic high disables the output to zero output current. This method can be used for calibration, power-on and power-off glitch reduction, and for output multiplexing with other outputs connected to the same pin.

Powering on while the output is disabled (OD = high) cannot fully suppress output glitching. While the supply voltage passes through the range of 3V to 4V, internal circuits turn on. Additional capacitance between the VG and IS pins can suppress the glitch. The smallest glitch energy appears with the OD pin left open; for practical use, however, this pin can be driven high through a 10kΩ resistor before the 24V supply is applied, if logic voltage is available earlier. Alternatively, an open-drain driver can control this pin using the internal pullup current. Pulling up to the internal regulator tends to increase the energy because of the delay of the regulator-voltage increase, again depending on the supply voltage rise time for the first few volts.

6.3.6 Voltage Regulator

The externally adjustable voltage regulator provides up to 5mA of current and offers drive (REGF) and sense (REGS) to allow external setting of the output voltage. Figure 6-7 shows the voltage regulator basic connections. The sense input (REGS) is referenced to 3.0V representing the lowest adjustable voltage level. An external resistor divider sets V_{REGF}.

$$V_{REGF} = V_{REGS} \times \frac{(R_1 + R_2)}{R_2} \tag{3}$$

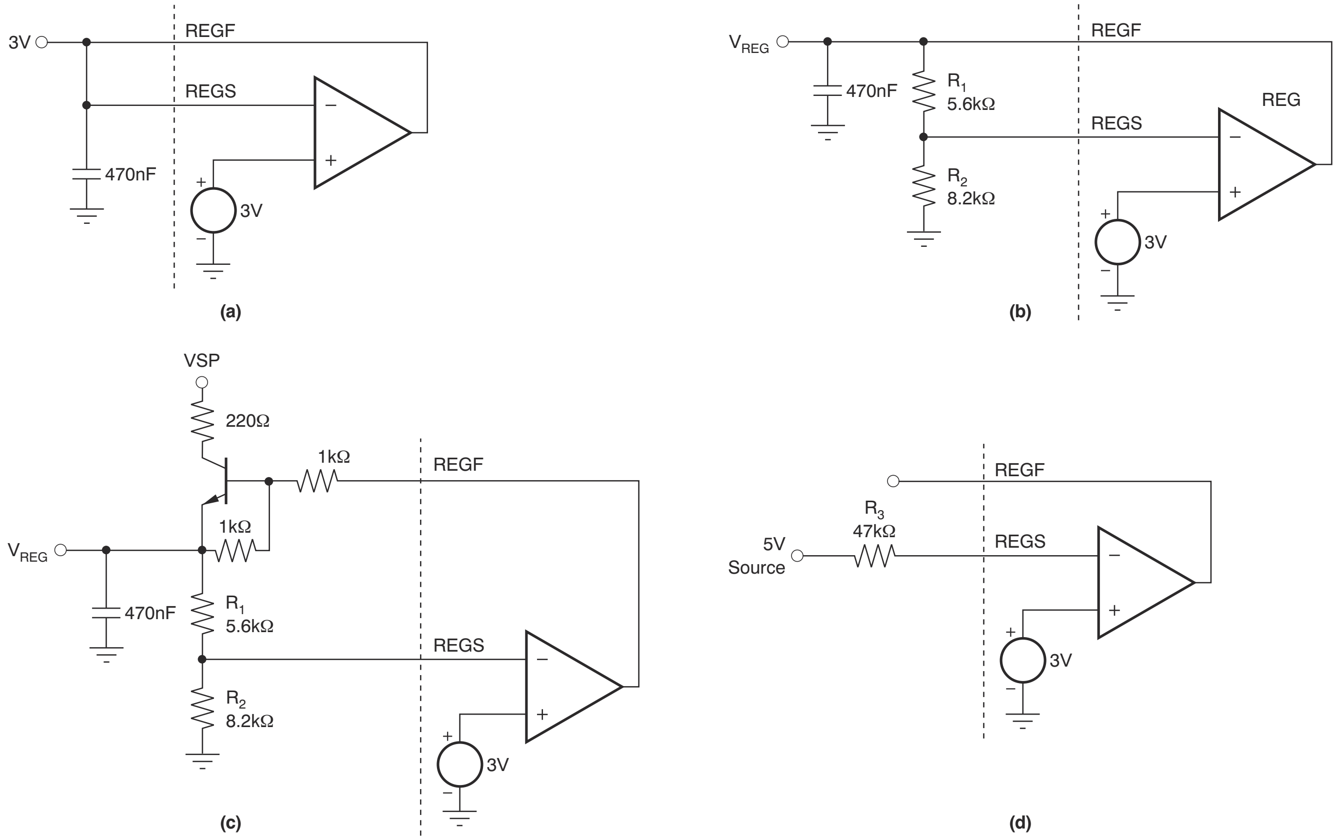


Figure 6-7. Basic Connections of the Voltage Regulator

Table 6-2 provides example values for the regulator adjustment resistors.

Table 6-2. Example Resistor Values for Setting the Regulator Voltage

V_{REGF}	R_1	R_2
3V	0kΩ	—
3.3V	3.3kΩ	33kΩ
5V	5.6kΩ	8.2kΩ
12.4V	27kΩ	8.6kΩ

The voltage at REGF is limited by the supply voltage. If the supply voltage drops close to the set voltage, the driver output saturates and follows the supply with a voltage drop of less than 1V (depending on load current and temperature).

For good stability and transient response, use a load capacitance of 470nF or greater. The bias current into the sense input (REGS) is typically less than 1μA. Consider the bias current when selecting high resistance values for the voltage setting because the bias current lowers the voltage and produces additional temperature dependence.

The REGF output cannot sink current. In case of supply-voltage loss, the output is protected against the discharge currents from load capacitors by internal protection diodes; the peak current must not exceed 25mA.

If the voltage regulator output is not used, connect REGF to REGS (3V mode) loaded with a 2.2nF capacitor. Alternatively, overdrive the loop pulling REGS high; Figure 6-7d shows this method.

6.3.7 Level Shift of 0V Input and Transconductance Trim

The XTR111 offers low offset voltage error at the input, which normally does not require cancellation. If the signal source cannot deliver 0V in a single-supply circuit, add a resistor from the SET pin to a positive reference voltage or the regulator output to shift the zero level for the input (V_{IN}) to a positive voltage. Therefore, the signal source can drive this value within a positive voltage range. The example in Figure 6-8 shows a 100mV (102.04mV) offset generated to the signal input. The larger this offset, however, the more influence of drift and inaccuracy is seen in the output signal. The voltage at SET must not be larger than 12V for linear operation.

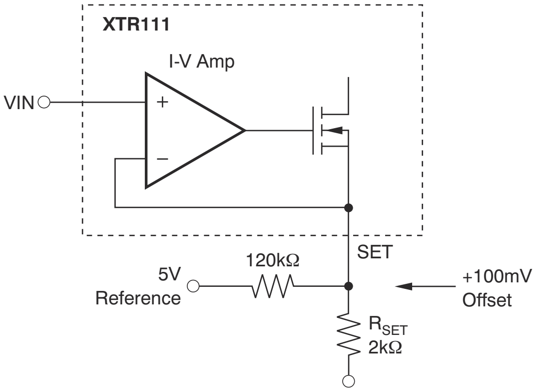


Figure 6-8. Input Voltage Level Shift for a 0mA Output Current

Transconductance (the input voltage to output current ratio) is set by R_{SET}. The desired resistor value can be found by choosing a combination of two resistors.

6.4 Device Functional Modes

The device has one mode of operation that applies when operated within the *Recommended Operating Conditions*.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Input Voltage

The input voltage range for a given output current span is set by R_{SET} according to the transfer function. Select a precise and low-drift resistor for best performance because resistor drift directly converts into drift of the output current. Careful layout must also minimize any series resistance with R_{SET} and the VIN reference point.

The input voltage is referred to the grounding point of R_{SET}. Therefore, this point must not be distorted from other currents. Assuming a 5V full-scale input signal for a 20mA output current, R_{SET} is 2.5kΩ. A resistance uncertainty of just 2.5Ω already degrades the accuracy to below 0.1%.

The linear input voltage range extends from 0V to 12V, or 2.3V less than the positive supply voltage (whichever is smaller). The lowest rated supply voltage accommodates an input voltage range of up to 5V. Potential clipping is not detected by an error signal; therefore, safe design guard banding is recommended.

Do not drive the input negative (referred to GND) greater than 300mV. Higher negative voltages turn on the internal protection diodes. Insert a resistor in series with the input if negative signals can occur eventually during power on or power off, or during other transient conditions. Select a resistor value that limits the possible current to 0.3mA. Higher currents are nondestructive (see Absolute Maximum Ratings), but can produce output current glitches unless in disable mode.

More protection against negative input signals is provided using a standard diode and a 2.2kΩ resistor, as shown in Figure 7-1.

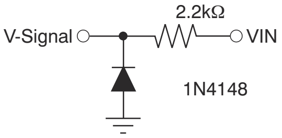


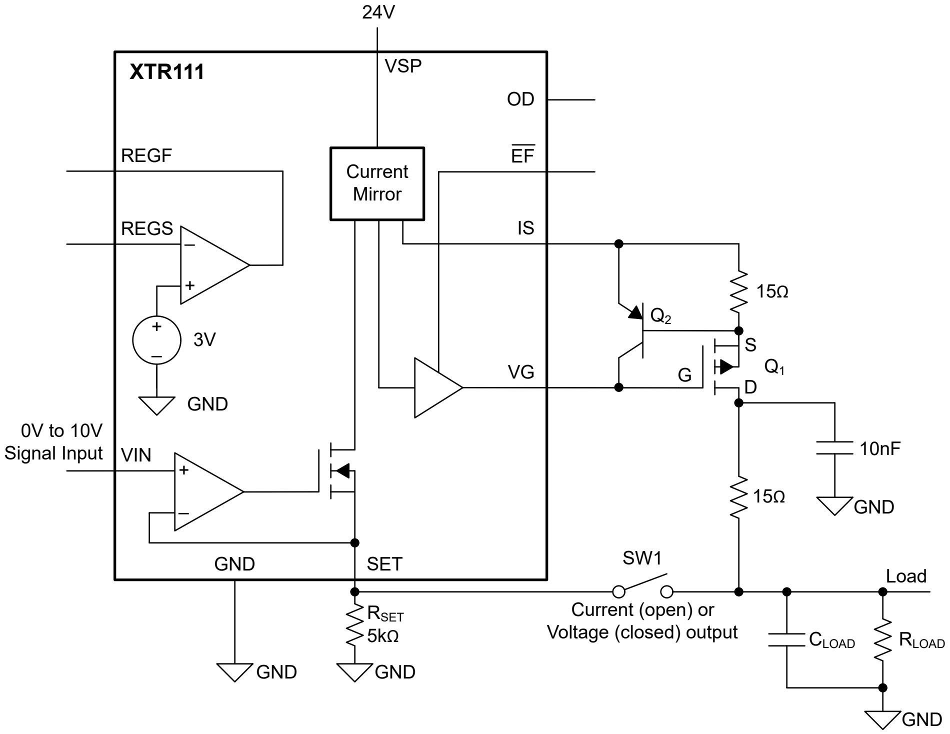
Figure 7-1. Enhanced Protection Against Negative Overload of V_{IN}

7.1.2 Error Flag Delay

In the event of a wire break or similar output fault, the current through the IS pin fails to satisfy the intended transfer function defined in Equation 1. The gate voltage VG falls as the XTR111 control loop attempts to correct for the discrepancy, eventually railing out. This condition is detected by the XTR111, causing the error flag to be asserted. Testing of the error flag functionality using the XTR111-2EVM suggests a typical delay of 650-700µs before $\overline{EF}$ goes low after a wire break event. As the load current (measured prior to the wire break) increases, this assertion delay decreases slightly, due to the lower initial VG voltage. The effective output capacitance, including both parasitic and intentional capacitance, acts to slow the fall of the output pin voltage and delays the assertion of the error flag. Furthermore, any parasitic capacitance on the $\overline{EF}$ pin forms an RC time constant with the external pullup resistance, increasing the fall time of the $\overline{EF}$ pin.

7.1.3 Voltage Output Configuration

The XTR111 can be configured in either current or voltage output mode. To use the XTR111 in voltage output mode, the load must be connected directly to the SET pin. The following example shows the use of a switch that can allow for selecting current or voltage output.



Note: When output is disabled and SW1 is closed, the SET pin can generate an error signal.

Figure 7-2. 0V-to-10V or 0mA-to-20mA Output Selected by Jumper SW1

7.1.4 4mA-to-20mA Output

The XTR111 does not provide internal circuits to generate 4mA with 0V input signal. Figure 7-3 shows that the most common way to shift the input signal is a two-resistor network connected to a voltage reference and the signal source. This arrangement allows easy adjustment for overrange and underrange conditions. The example assumes a 5V reference (V_{REF}) that equals the full-scale signal voltage and a signal span of 0V to 5V for 4mA-to-20mA (I_{MIN} to I_{MAX}) output.

The voltage regulator output or a more precise reference can be used as V_{REF}. Observe the potential drift added by the drift of the resistors and the voltage reference.

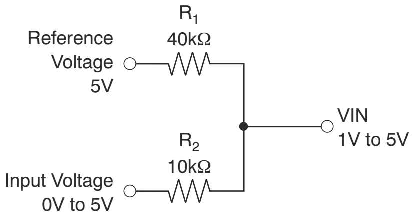


Figure 7-3. Resistive Divider for I_{MIN}-to-I_{MAX} Output (4mA to 20mA) With 0V to V_{FS} Signal Source

7.2 Typical Applications

7.2.1 0mA–20mA Voltage-to-Current Converter

A common application of the XTR111 is converting the voltage output of a DAC to a current for transmission in a current loop. The circuit shown in Figure 7-4 can be used to convert an input voltage of 0V to 5V from a DAC to an output current between 0mA and 20mA. The DAC is powered using the XTR111 voltage regulator configured to 5V.

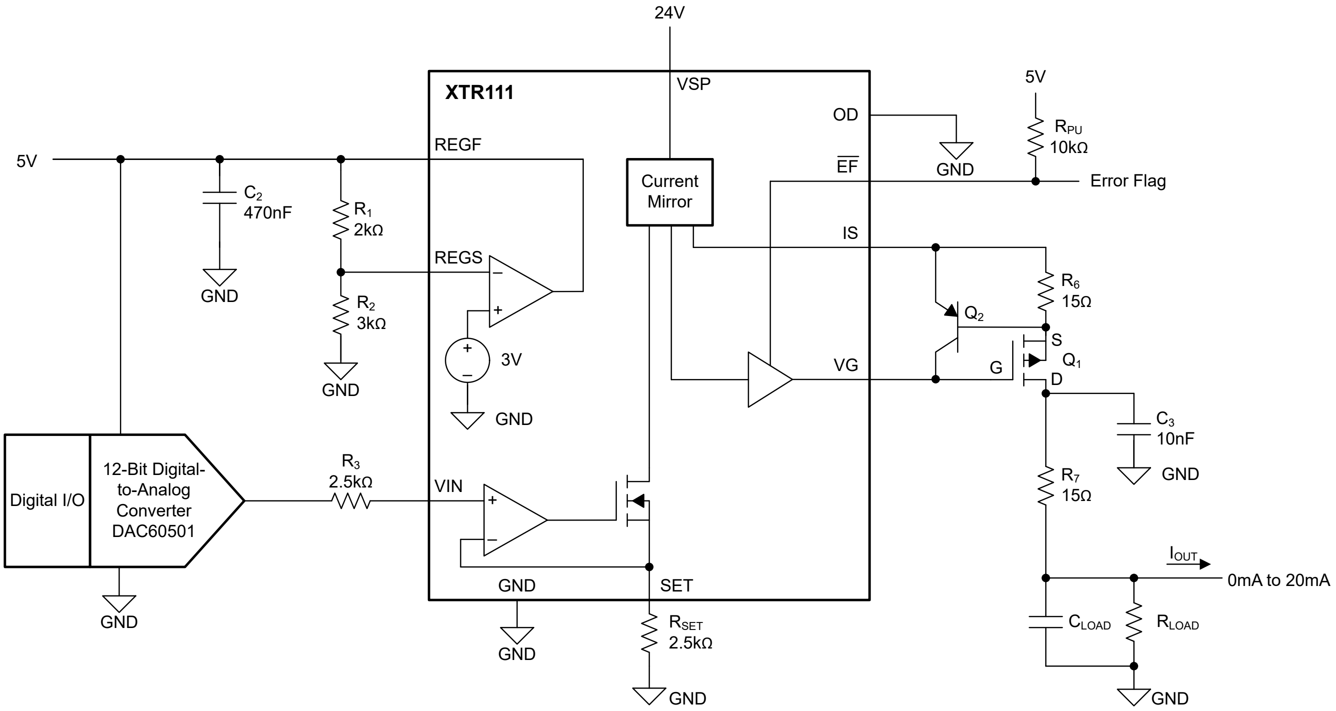


Figure 7-4. Current Using a 0V to 5V Input From the DAC60501, a 12-Bit Digital-to-Analog Converter

7.2.1.1 Design Requirements

In this example application, the supply voltage is 24V, and the DAC60501 was chosen. See Section 6.3.2 and Section 6.3.4 for additional design guidelines on external component selection. The design requirements for this application are listed in the following table:

Table 7-1. Design Parameters

PARAMETER	VALUE
Supply voltage (VSP)	24V
DAC supply voltage	5V
DAC output voltage range	0V to 5V
XTR111 output current range	0mA to 20mA

7.2.1.2 Detailed Design Procedure

The DAC60501 was selected because the DAC has 12-bit resolution, can be powered using a 5V supply, and has a 0-5V output range with a 5V supply. The DAC7551 can be used in place of the DAC60501 if desired. Pin 1 of the XTR111 is connected to the +24V supply rail, and instead of using a separate 5V supply line for the DAC, this application uses the voltage regulator built in to the XTR111 configured for 5V using R_1 and R_2. In this case, R_1 is 2kΩ and R_2 is 3kΩ, resulting in a V_{REGF} of 5V. To improve the stability of the voltage regulator, C_2 needs to be 470nF or larger. In this application, a 470nF capacitor was selected. For more details on configuring the voltage regulator, see Section 6.3.6.

The error flag logic output (EF) is not used in this application and can be left unconnected. To keep the output of the XTR111 enabled, the output disable pin (OD) needs to be connected to GND. For additional information on the output disable and output error flag pins, see Section 6.3.5.

For a 5V full-scale input signal corresponding to an output current of 20mA, R_{SET} was set to 2.5kΩ.

To create the external current limit, the Infineon BSP170P and Onsemi MMBT2907A were chosen as the external transistors. For additional examples of P-Channel MOSFETs, see Table 6-1. To limit the current output of the IS pin, R_6 was set to 15Ω. R_7 and C_3 were added for additional output filtering. For more information on the external current limit and selecting external transistors, see Section 6.3.3.

7.2.1.3 Application Curve

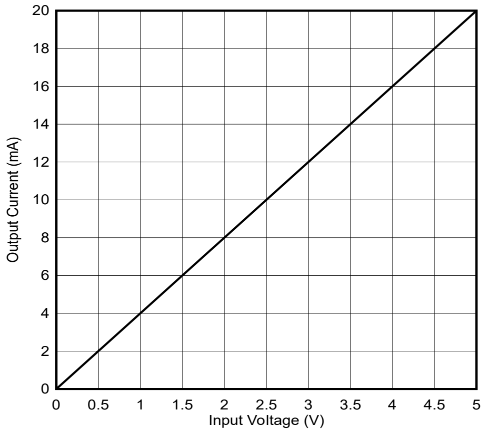
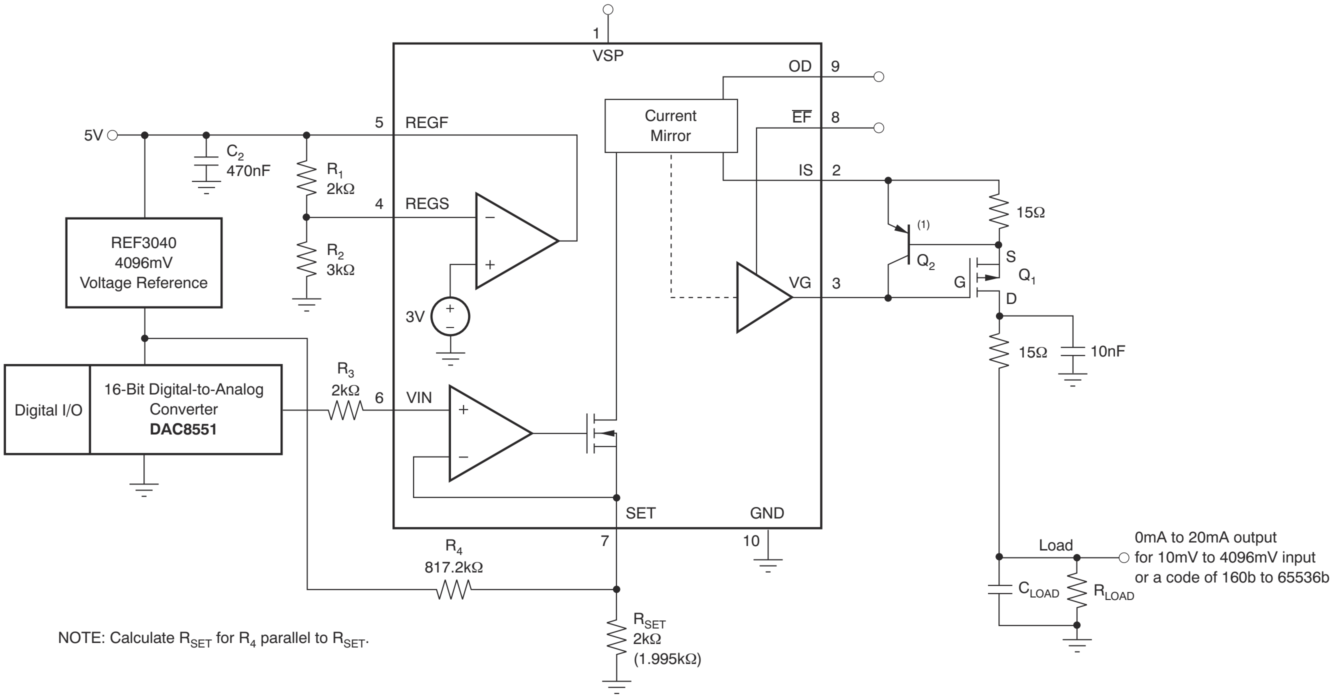


Figure 7-5. Output Current vs Input Voltage

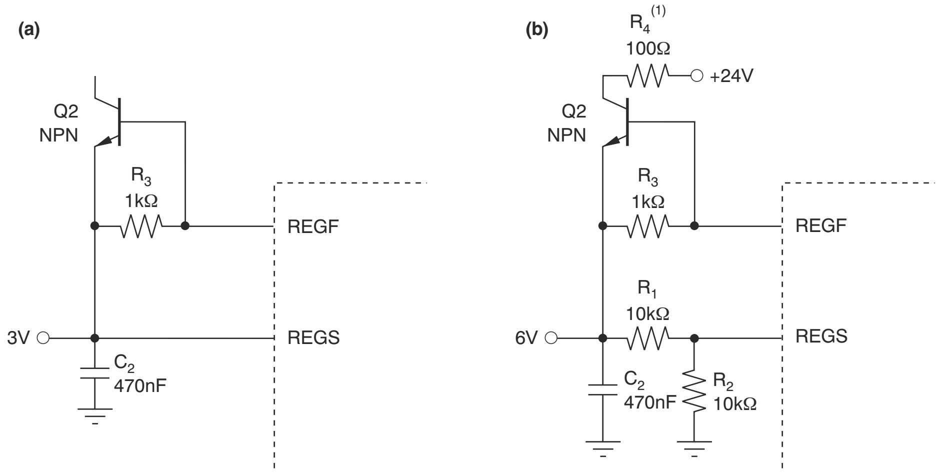
7.2.2 Additional Applications



NOTE: Calculate R_{SET} for R_4 parallel to R_{SET}.

Note: Input offset shifted by 10mV using R4 for zero adjustment range.

Figure 7-6. Precision Current Output With a 16-Bit DAC Voltage Input



NOTE: (1) Resistor R_4 can be calculated to protect Q_2 from over current in fault conditions.

Figure 7-7. Voltage Regulator Current Boost Using a Standard NPN Transistor

7.3 Power Supply Recommendations

The XTR111 requires a voltage supply within 8V to 40V. Adequate power-supply bypassing is required to protect associated circuitry. Use a large enough bypass capacitor (> 100nF), and place the bypass capacitor as close as possible to the device to decouple the XTR111 from noise typically found on 24V supplies.

7.4 Layout

7.4.1 Layout Guidelines

Solder the leadframe die pad to a thermal pad on the PCB. Figure 7-8 shows an example layout. Refinements to this layout can be required based on assembly process requirements. Mechanical drawings located at the end of this data sheet list the physical dimensions for the package and pad. The five holes in the landing pattern are optional, and are intended for use with thermal vias that connect the leadframe die pad to the heat-sink area on the printed circuit board (PCB).

Soldering the exposed pad significantly improves board-level reliability during temperature cycling, key push, package shear, and similar board-level tests. Even with applications that have low power dissipation, the exposed pad must be soldered to the PCB to provide structural integrity and long-term reliability.

7.4.1.1 Package and Heat Dissipation

The external FET transistor, used for the external current limit (see Section 6.3.3), is the most significant source of heat. The power dissipated by the external FET is a direct function of the maximum power supply voltage and maximum current output range supported in the application. Select a FET transistor that supports the maximum drain to source voltage and maximum power required; see also Section 6.3.4. Refer to the FET manufacturer for information on component placement requirements and heat sink selection.

The XTR111 only generates heat from the supply voltage with the quiescent current, the internal signal current that is 1/10 of the output current, and the current and internal voltage drop of the regulator.

The exposed thermal pad on the bottom of the XTR111 package allows excellent heat dissipation of the device into the printed circuit board (PCB).

7.4.1.2 Thermal Pad Guidelines

The thermal pad must be connected to the same voltage potential as the device GND pin.

Packages with an exposed thermal pad are specifically designed to provide excellent power dissipation, but board layout greatly influences overall heat dissipation. The thermal resistance from junction-to-ambient (T_{JA}) is specified for the packages with the exposed thermal pad soldered to a normalized PCB, as described in the *PowerPAD™ Thermally-Enhanced Package* application report. See also the EIA/JEDEC Specifications JESD51-0 to 7, the *QFN and SON PCB Attachment* application report, and the *Quad Flatpack No-Lead Logic Packages* application report. These documents are available for download at www.ti.com.

Note

All thermal models have an accuracy variation of 20%.

Component population, layout of traces, layers, and air flow strongly influence heat dissipation. Test worst-case load conditions in the real environment to maintain proper thermal conditions. Minimize thermal stress for proper long-term operation with a junction temperature much less than the absolute maximum rating.

7.4.2 Layout Example

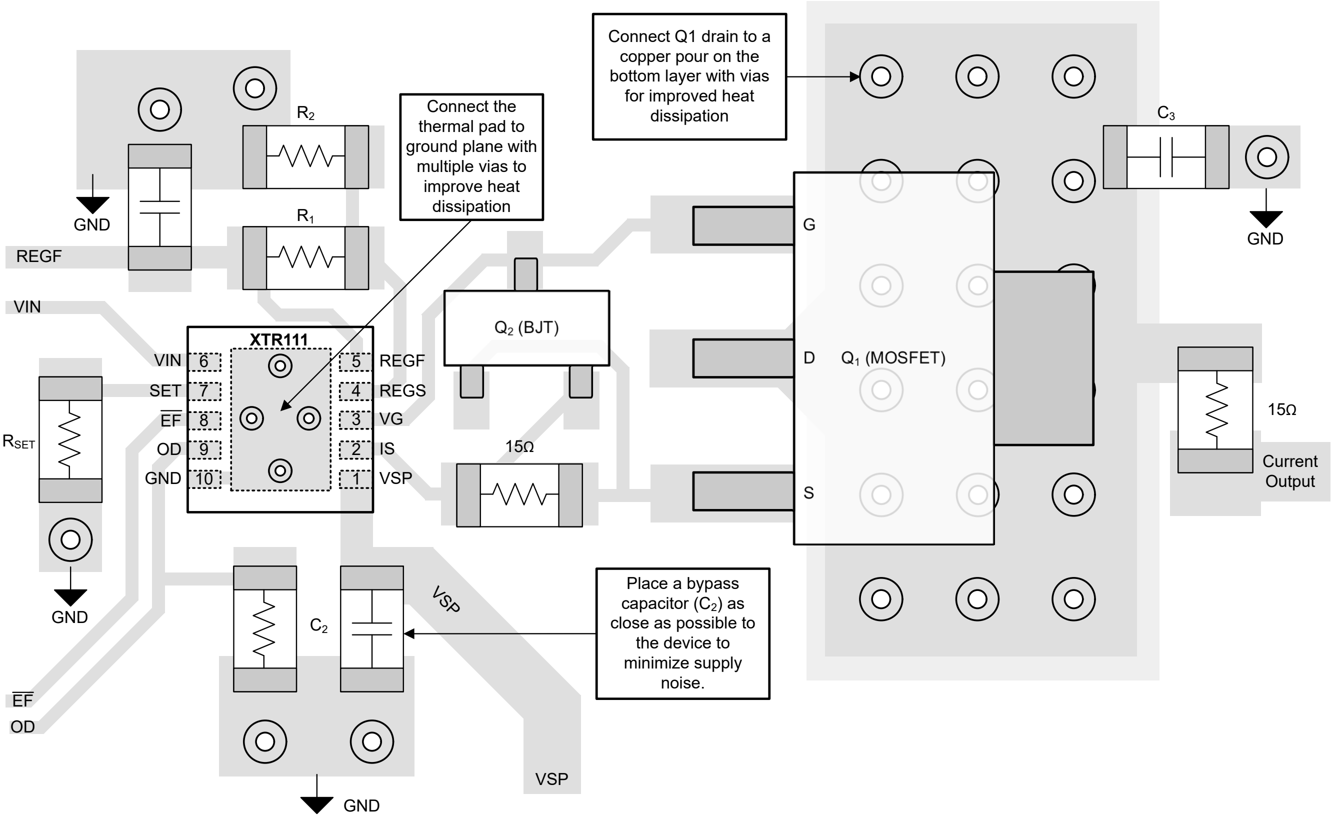


Figure 7-8. Layout Example

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Device Support

8.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *XTR111 Evaluation Module* user's guide
- Texas Instruments, *XTR111 Functional Safety FIT Rate, FMD and Pin FMA* functional safety information
- Texas Instruments, *How to Select Amplifiers for Pressure Transmitter Applications* application brief
- Texas Instruments, *Single-Channel, Isolated, 3-Wire Current Loop Transmitter* reference design with the XTR111
- Texas Instruments, *Special Function Amplifiers* Precision Labs video series on Current Loop Transmitters

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.5 Trademarks

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8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (June 2011) to Revision D (October 2024) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document................. 1
- Added the *Specifications*, *ESD Ratings*, *Recommended Operating Conditions*, *Thermal Information*, *Detailed Description*, *Overview*, *Functional Block Diagram*, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Typical Applications*, *Power Supply Recommendations*, *Layout*, *Layout Example*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections.......................1
- Changed maximum output current from 36mA to 32mA in *Description*.. 1
- Moved maximum current specification for IS from table note to table row.. 4
- Added charged device model (CDM) ESD specification of ±1000V to *ESD Ratings*.. 4
- Changed Specified output current (derated performance) maximum from 36mA to 32mA in *Electrical Characteristics* 5
- Changed Current limit for output current from 42 ±6mA to 41 ±9mA in *Electrical Characteristics* 5
- Changed Nonlinearity, I_{OUT}/I_{SET} test condition from "0.1mA to 36mA" to "0.1mA to 32mA" in *Electrical Characteristics* 5
- Deleted redundant specified and operating temperature, specified and operating voltage, and package thermal impedance from *Electrical Characteristics*... 5
- Changed maximum current specification from 36mA to 32mA in *Overview*...12
- Updated Table 6-1, *P-Channel MOSFET (Examples)* 15
- Added *Error Flag Delay* section to *Application Information* 19
- Changed from DAC7551 to DAC60501...21
- Added *Power Supply Recommendations* 24
- Added additional guidance on heat dissipation in *Package and Heat Dissipation* 24

Changes from Revision B (June, 2010) to Revision C (June, 2011) **Page**

- Updated wiring error in Figure 46, *Current Using a 0V to 5V Input From the DAC7551, a 12-Bit Digital-to-Analog Converter* 23

Changes from Revision A (August 2007) to Revision B (June 2010) **Page**

- Updated to fix errors in Figure 6-5 15

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
XTR111AIDGQR	ACTIVE	HVSSOP	DGQ	10	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CCM	Samples
XTR111AIDGQT	ACTIVE	HVSSOP	DGQ	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CCM	Samples
XTR111AIDRCR	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BSV	Samples
XTR111AIDRCT	ACTIVE	VSON	DRC	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BSV	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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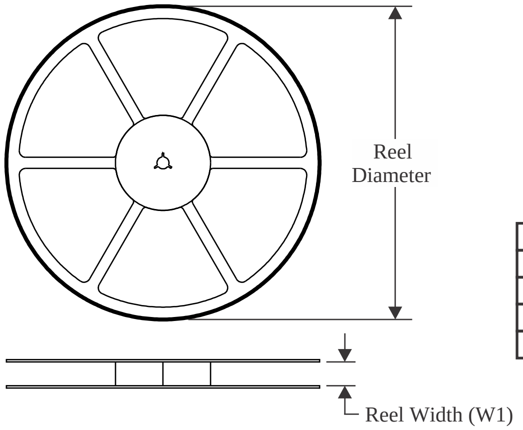
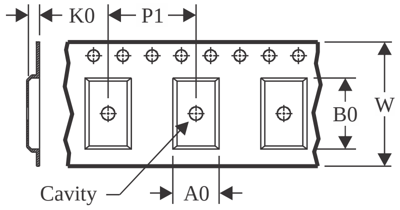
TAPE AND REEL INFORMATION

REEL DIMENSIONS

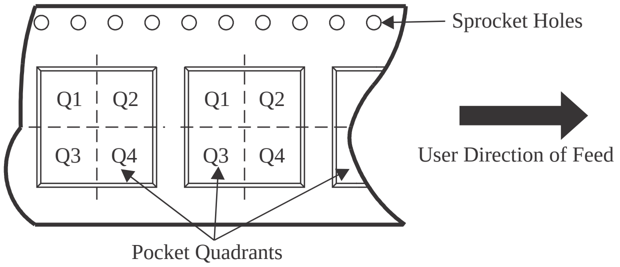


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

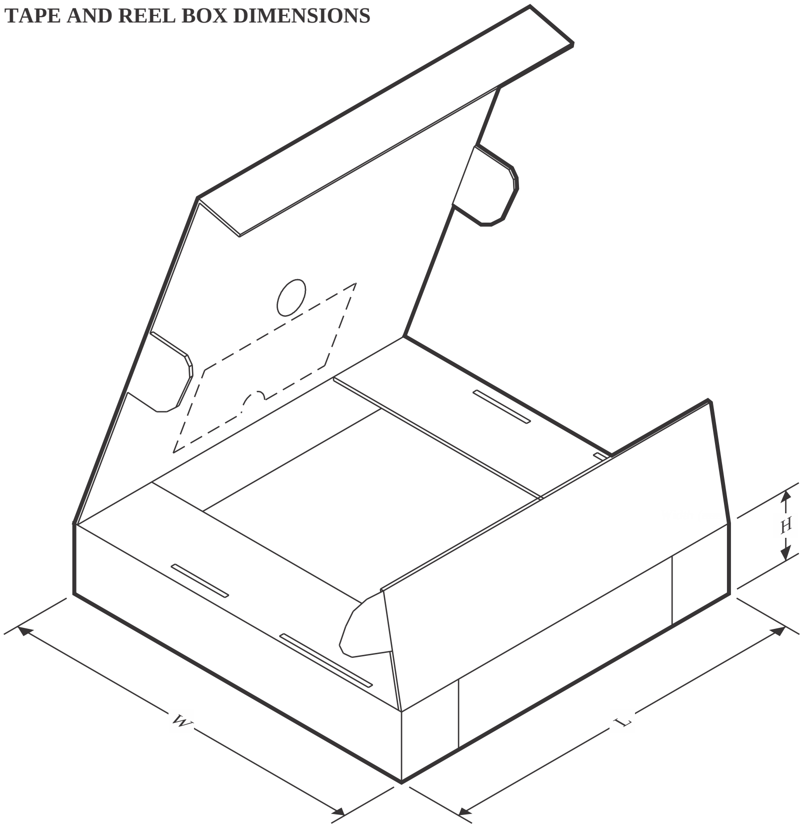
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
XTR111AIDGQR	HVSSOP	DGQ	10	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
XTR111AIDGQT	HVSSOP	DGQ	10	250	180.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
XTR111AIDRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
XTR111AIDRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
XTR111AIDGQR	HVSSOP	DGQ	10	2500	367.0	367.0	38.0
XTR111AIDGQT	HVSSOP	DGQ	10	250	213.0	191.0	35.0
XTR111AIDRCR	VSON	DRC	10	3000	356.0	356.0	35.0
XTR111AIDRCT	VSON	DRC	10	250	210.0	185.0	35.0

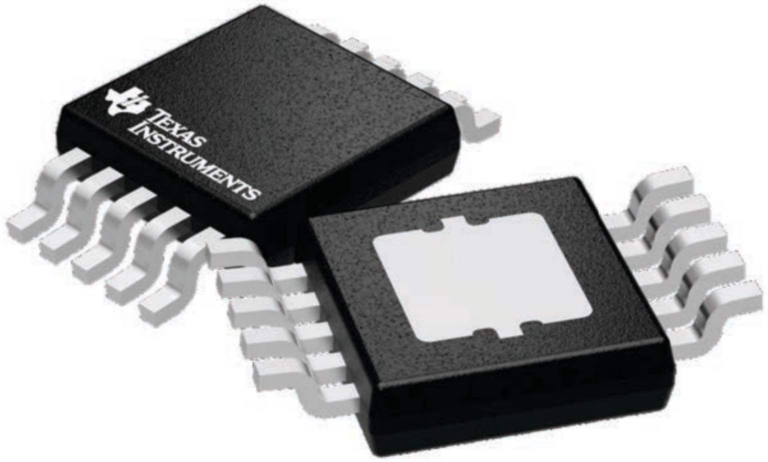
GENERIC PACKAGE VIEW

DGQ 10

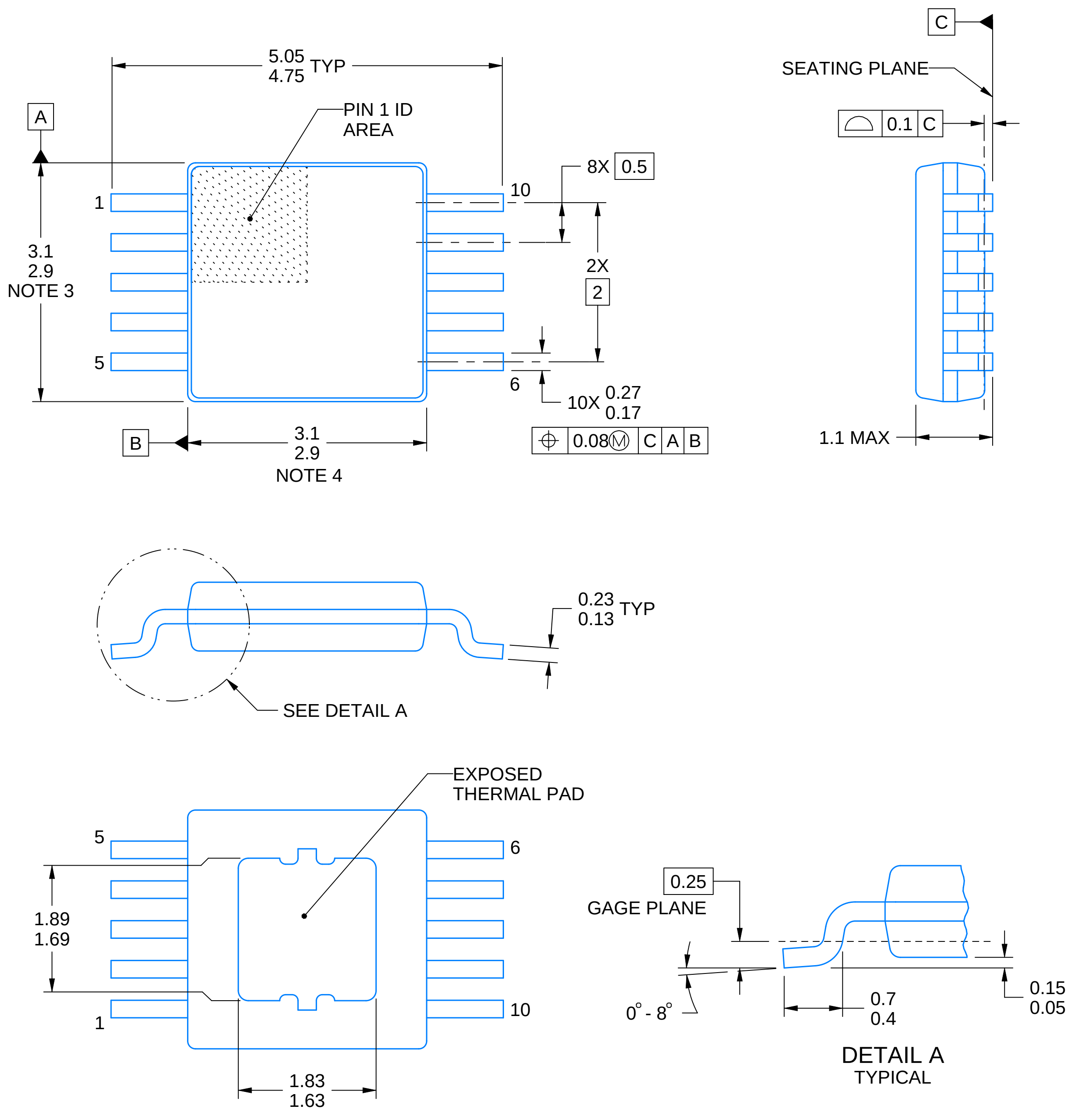
PowerPAD™ HVSSOP - 1.1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

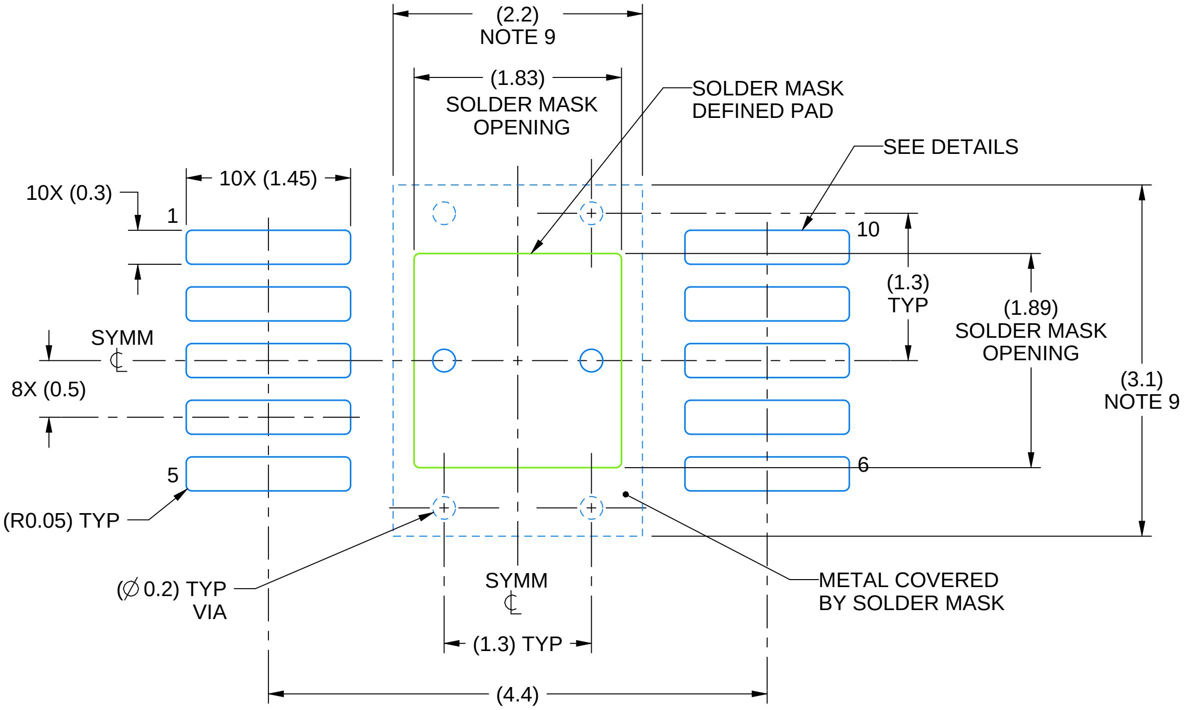


4218842/B 04/2024

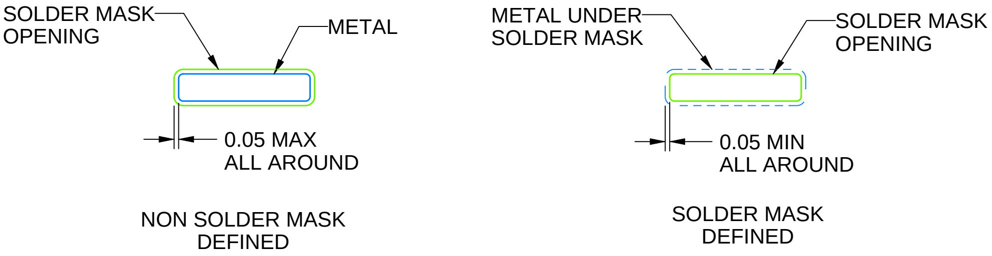
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA-T.



LAND PATTERN EXAMPLE
SCALE:15X

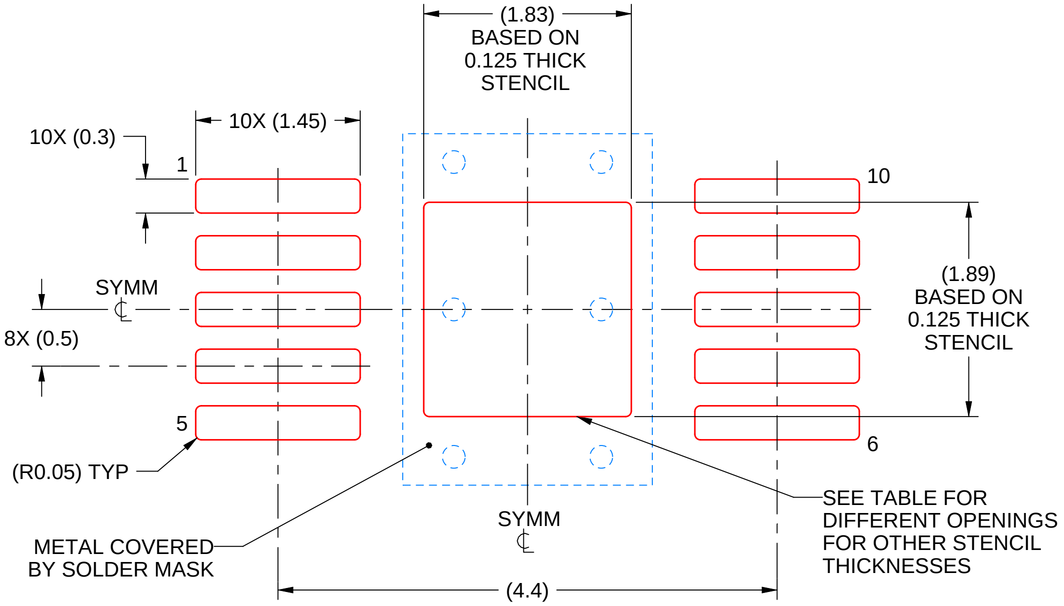


SOLDER MASK DETAILS

4218842/B 04/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.05 X 2.11
0.125	1.83 X 1.89 (SHOWN)
0.150	1.67 X 1.73
0.175	1.55 X 1.60

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

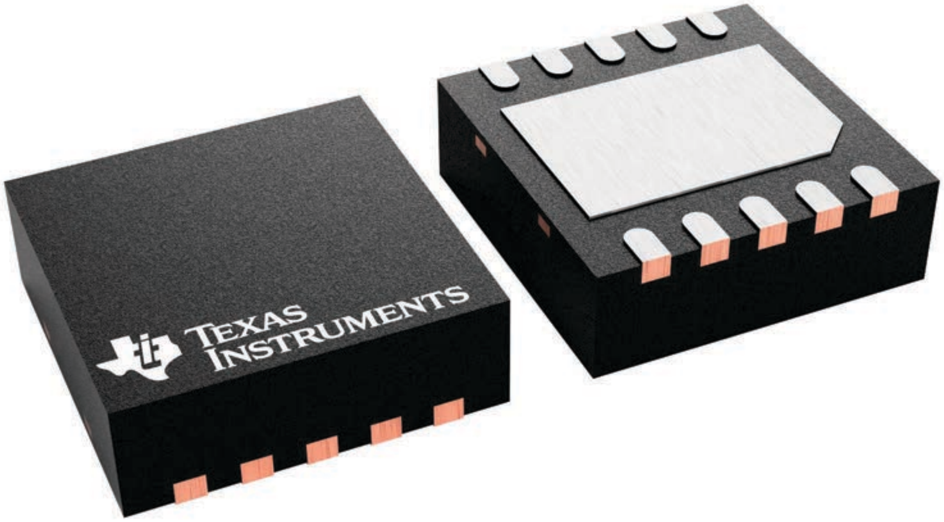
DRC 10

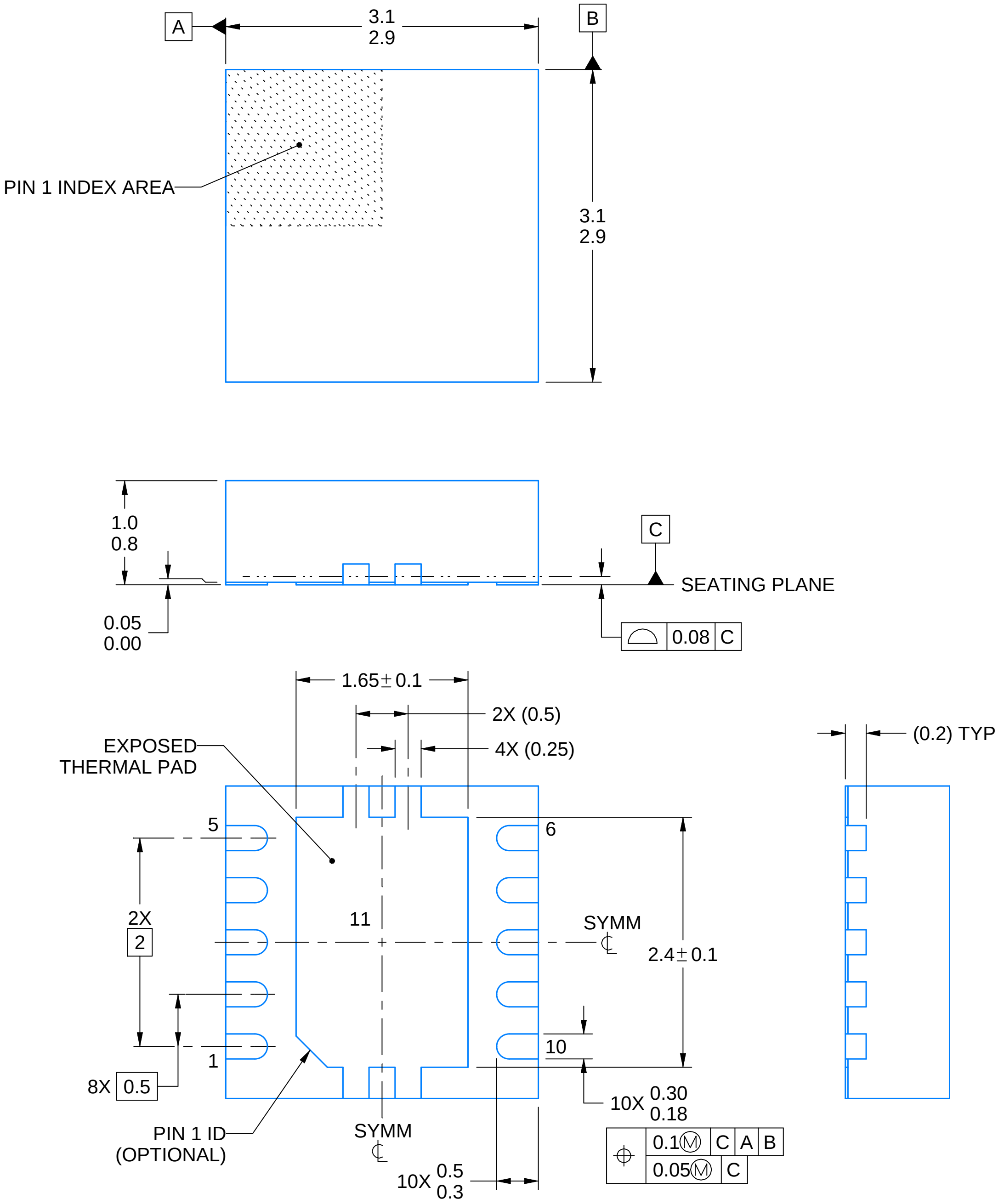
VSON - 1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

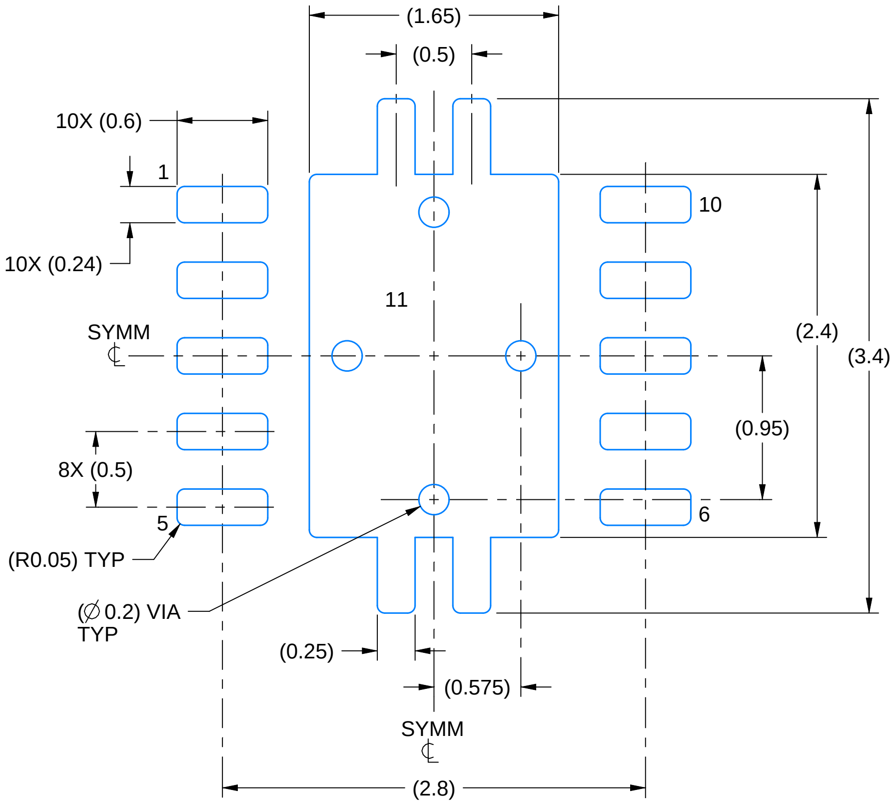




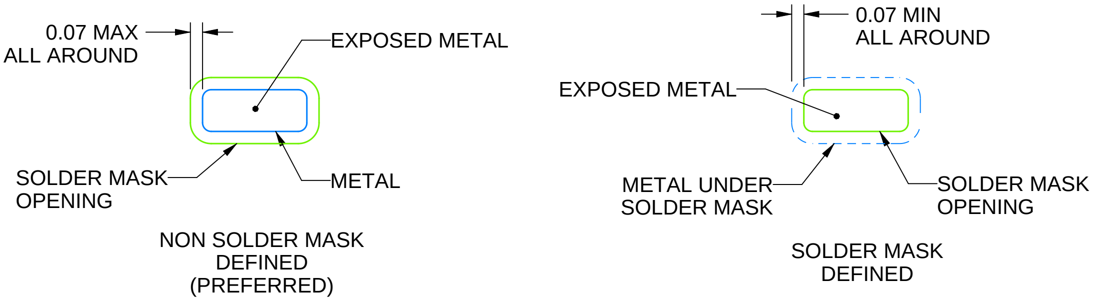
4218878/B 07/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

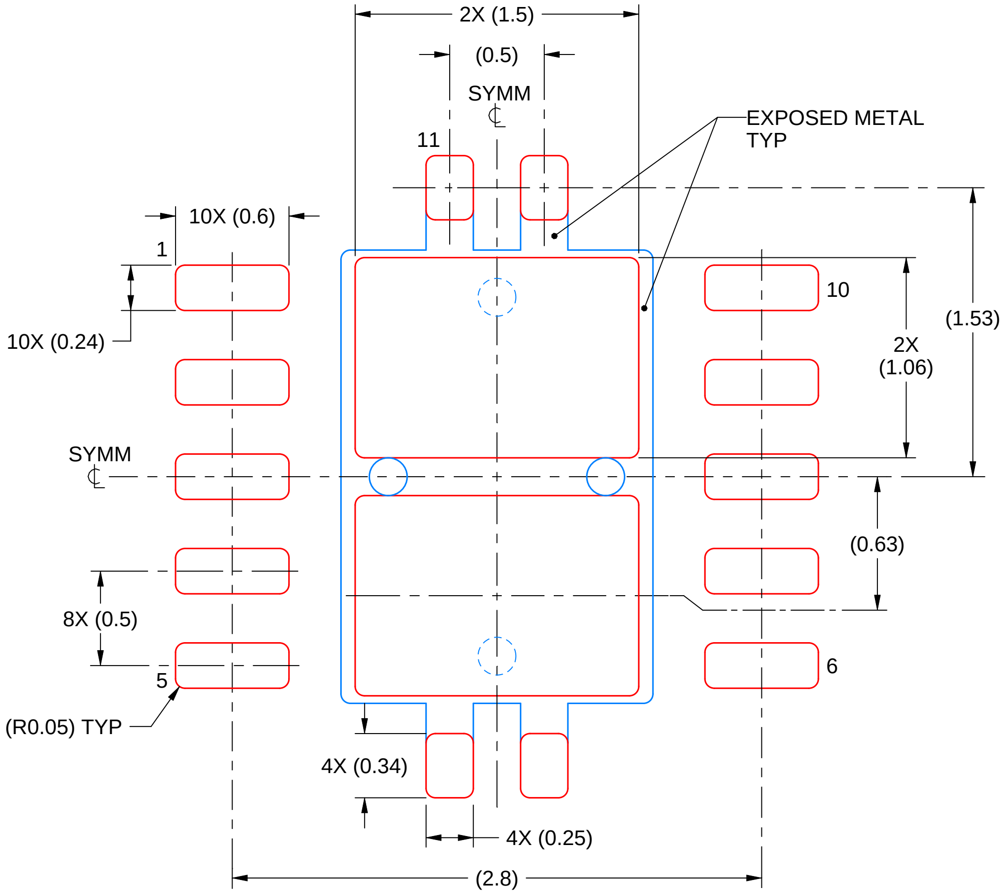


SOLDER MASK DETAILS

4218878/B 07/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218878/B 07/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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